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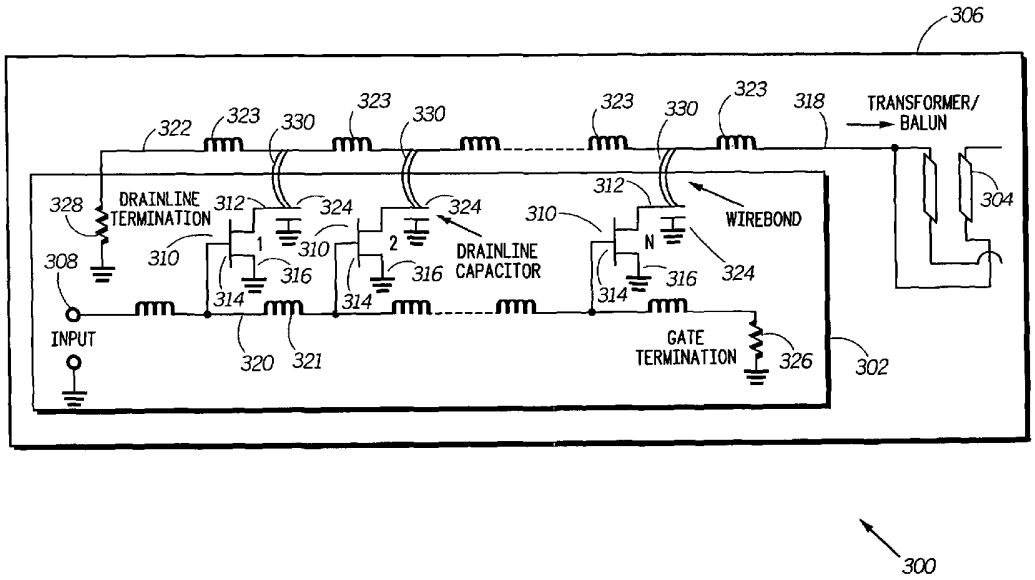
(54) **Title:** HYBRID STRUCTURE FOR DISTRIBUTED POWER AMPLIFIERS




(57) **Abstract:** A hybrid low voltage distributed power amplifier structure (300) provides improved efficiency by forming drain transmission line inductors (323) on a substrate (306) while the rest of the amplifier is built in IC form (302). A wirebond interconnection (330) is made between the IC s drainline capacitors (324) and the substrate s drainline inductors (323) which are a higher impedance point in the circuit. As a result, the wirebond inductance becomes negligible and has little or no impact on the power amplifier's performance.

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*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

# HYBRID STRUCTURE FOR DISTRIBUTED POWER AMPLIFIERS

## FIELD OF THE INVENTION

This invention relates generally to power amplifiers and more specifically to hybrid structures for distributed power amplifiers.

## BACKGROUND OF THE INVENTION

Low voltage power amplifiers are used in a variety of applications including radio and cellular handsets as well as wireless broadband applications to name a few. The term hybrid structure typically refers to passive circuit elements formed on non-semiconductor substrates combined with semiconductors. Hybrid structures are often used in the design of low voltage distributed power amplifier (PA) circuits because of the low cost properties of the structure. FIG. 1 shows a schematic 100 of a distributed power amplifier 102 integrated as a single chip coupled to balun/transformer 104 on a ceramic substrate 106. The substrate 106 is typically formed using Low Temperature Cofired Ceramics Technology (LTCC). The distributed power amplifier 102 includes an input 108, a plurality of transistors 110, here shown as field effect transistors (FETs) each having drain 112, gate 114 and source 116, and an output 118. Amplifier 102 further includes gate transmission line 120 having gateline inductors 121 as well as drain transmission line 122 having drainline inductors 123, along with drainline capacitors 124, and termination resistors 126, 128.

Traditionally, the distributed power amplifier 102 has been built with both the gate transmission line 120 and the drain transmission line 122 integrated on the power amplifier IC chip 102. The connection to the rest of the circuit is accomplished with wirebonds 130 at the output 118 of the power amplifier chip 102. For a low voltage power amplifier, the output 118 of the PA 102 is a low impedance point (3 to 4 ohm). Thus, the wirebond inductance significantly degrades the performance of the amplifier 102 since the inductive reactance of the wirebonds 130 is a large percentage of the total load impedance.

FIG. 2 shows a graph 200 of gain (dB) 202, output power (Pout, dBm) 204 and power-added efficiency (PAE%) 206 versus frequency (GHz). Graph 200 is based on a simulation for a five-cell PHEMT (Pseudomorphic High Electron Mobility)

transistor, drain-tapered, distributed amplifier with 1 watt output power with the wirebonds 130 connecting the IC 102 and the LTCC substrate 106 as shown in FIG. 1. Power amplifier efficiency is a design parameter of considerable interest, and circuit designers are constantly seeking ways of improving the efficiency which in turn translates into longer battery life for portable products.

Accordingly, it would be desirable to have a power amplifier structure that is less susceptible to the wirebonds so as to have less impact on impedance and thereby provide improved efficiency.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIG. 1 is a schematic diagram of a power amplifier in accordance with the prior art;

FIG. 2 is a graph of gain and output power and power-added efficiency versus frequency in accordance with the prior art;

FIG. 3 is a schematic diagram of a power amplifier in accordance with the present invention; and

FIG. 4 is a graph of gain and output power and power-added efficiency versus frequency in accordance with the present invention.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

## DETAILED DESCRIPTION OF THE DRAWINGS

FIG. 3 shows a schematic 300 for a distributed power amplifier 302 formed in accordance with the present invention, the power amplifier being coupled to a load, such as a transformer/balun 304. In accordance with the present invention, drain transmission line inductors 323 and output 318 are built in the ceramic substrate 306, and the rest of the amplifier 302 is built in IC form. Thus, the IC portion of power

amplifier 302 includes an input 308, a plurality of transistors 310, here shown as FETs each having drain 312, gate 314 and source 316. The IC portion of amplifier 302 further includes gate transmission line 320, gate transmission line inductors 321, drainline capacitors 324, and termination resistors 326, 328.

In accordance with the present invention, wirebond interconnection 330 is made between the drainline capacitors 324 and drainline inductors 323, which is a higher impedance point in the circuit. By moving the wirebond interconnection point to a higher impedance point in the circuit, the wirebond inductance will not introduce performance degradation typically caused by dynamic load errors. As a result, the wirebond inductance becomes negligible and has little or no impact on the power amplifier's performance.

FIG. 4 is a graph of gain (dB), output power (Pout, dBm) and power-added efficiency (PAE%) versus frequency (GHz) achieved for a hybrid structure formed in accordance with the present invention. The same parameters were used in the simulation of FIG. 4 as that in FIG. 2 except that the drainline transmission inductors were integrated onto the substrate 306 and wirebonded out from the PA to the inductive points. FIG. 4 shows significant performance improvement of the power amplifier compared to FIG. 3 over the entire frequency band.

Low voltage power amplifiers formed in accordance with the present invention can be used in a variety of products including, but not limited to, software definable radios, cellular handsets, and wireless broadband applications.

While shown as an FET configuration, one skilled in the art appreciates that the hybrid integration of the power amplifier extends to a variety of transistor types, including bipolar transistors in which the base transmission line remains part of the amplifier IC and the inductors of the collector transmission line is integrated into the substrate. While the hybrid structure has been described as preferably using a ceramic substrate, other substrate materials found in amplifier designs, such as organic substrates used in high density interconnect (HDI) can also be used.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification

and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

We claim:

# CLAIMS

1. A distributed power amplifier structure, comprising:

a substrate;

power amplifier circuitry including a plurality of transistors having transmission line inductors coupled thereto; and

transmission line inductors formed on the substrate and coupled to the transistors of the IC through wirebonds.

2. A distributed power amplifier structure, comprising:

a ceramic substrate;

an integrated circuit (IC) on the ceramic substrate, the IC including:

a plurality of transistors each having a drain, gate, and source, the source being coupled to ground, the gate being coupled to a series of gateline transmission inductors;

a series of drainline transmission inductors formed on the ceramic;

a drainline capacitor coupled to the drain of each transistor; and

a wirebond interconnection between each drainline transmission inductor on the ceramic and each drainline capacitor on the IC.

3. The distributed power amplifier structure of claim 2, further comprising:

an input on the IC; and

an output taken from the series of drainline transmission inductors, the output coupled to a load.

4. The distributed power amplifier of claim 2, wherein the power amplifier is used in a software definable radio.

5. The distributed power amplifier of claim 2, wherein the power amplifier is used in a cellular handset.

6. The distributed power amplifier of claim 2, wherein the power amplifier is used in a wireless broadband application.

7. The distributed power amplifier of claim 3, wherein the load comprises a balun/transformer integrated on the ceramic substrate.

8. The distributed power amplifier of claim 2, wherein the transistor is an Field Effect Transistor (FET).

9. A distributed power amplifier structure, comprising:

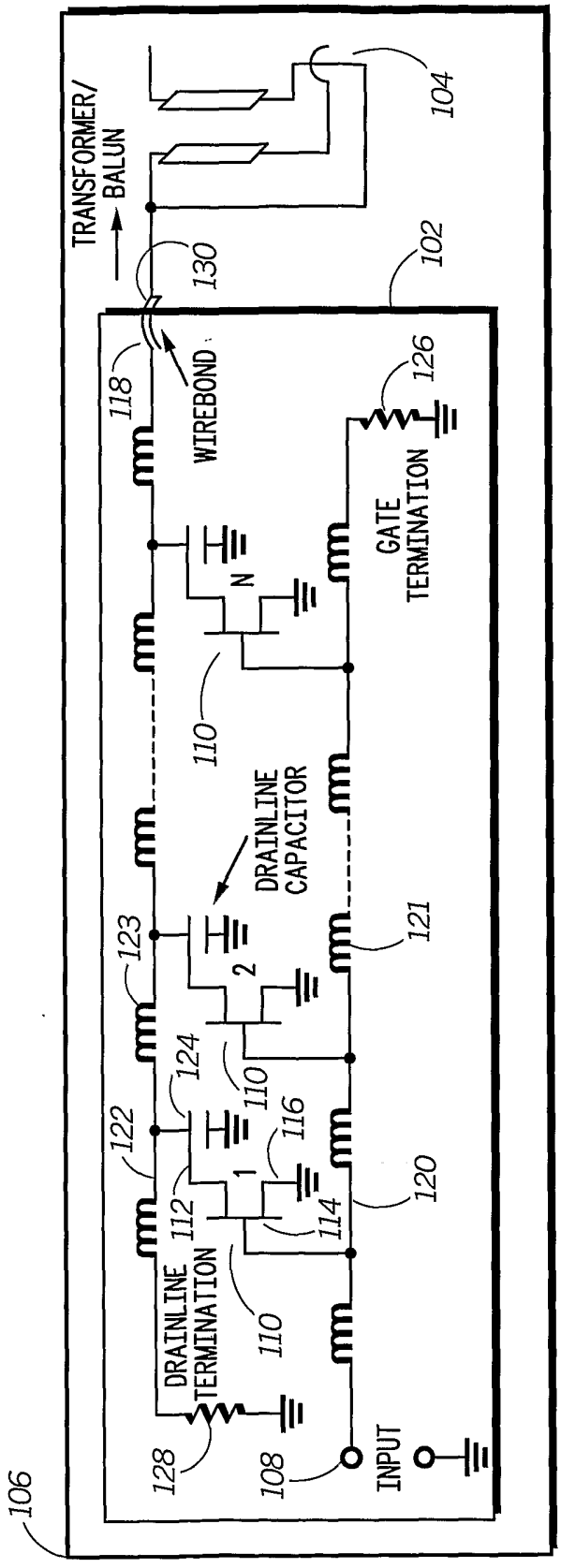
a substrate;

an integrated circuit (IC) formed over the substrate, the IC including a first portion of a distributed power amplifier circuit including transistors and a first set of transmission line inductors coupled to the transistors; and

a second set of transmission line inductors formed on the ceramic substrate and coupled to the transistors of the IC through wirebond interconnects.

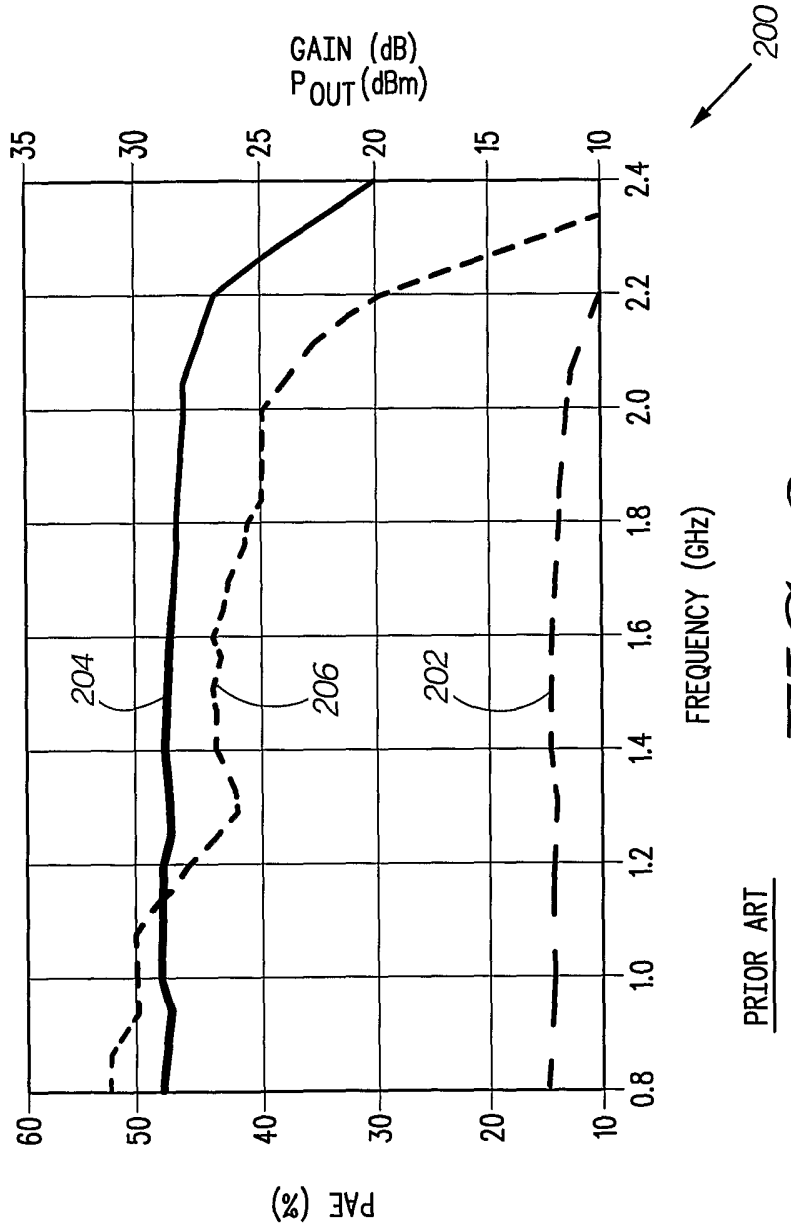
10. The distributed power amplifier structure of claim 9, wherein the substrate is ceramic.

11. The distributed power amplifier structure of claim 9, wherein the transistors are at least one of P-channel Field Effect Transistors (FETs), N-channel Field Effect Transistors (FETs) and bipolar transistors.



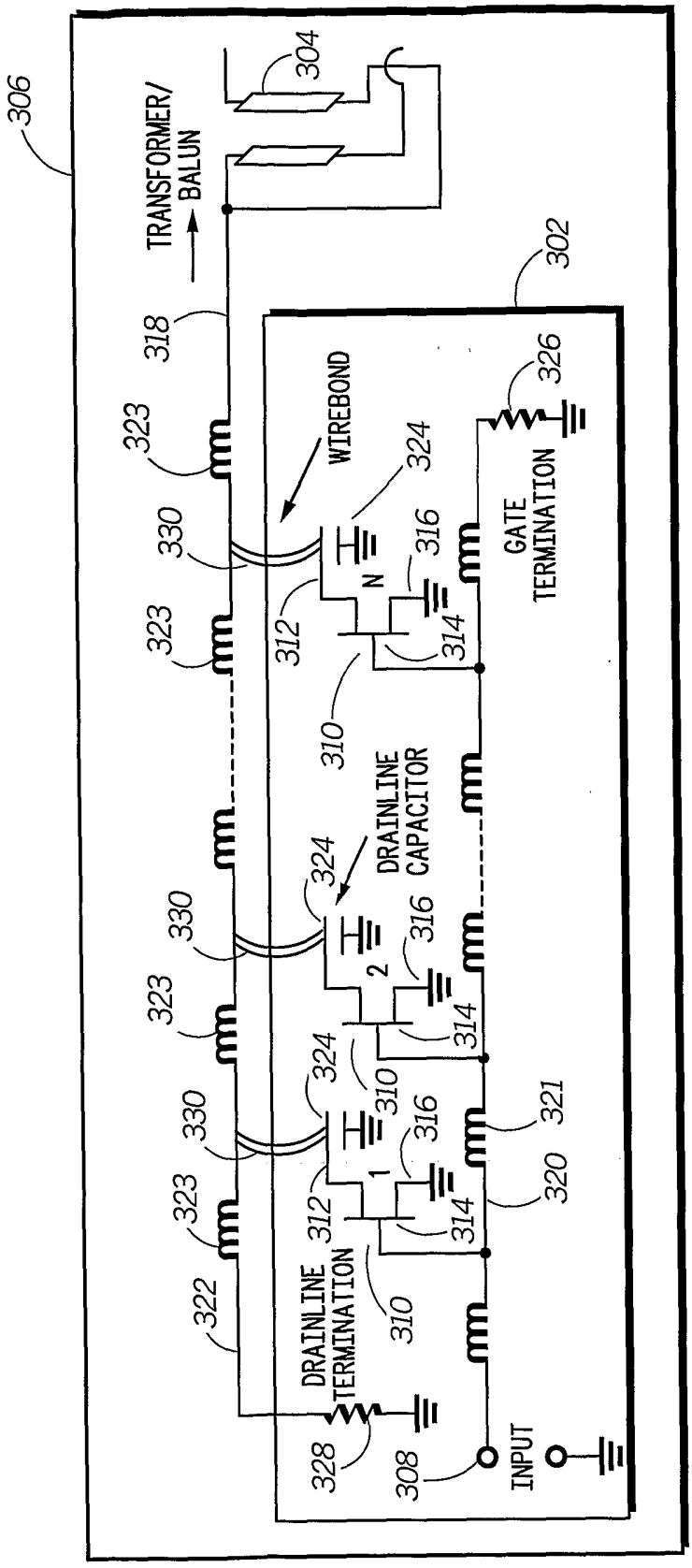

PRIOR ART

FIG. 1




PRIOR ART

FIG. 2


306
304
TRANSFORMER/
BALUN
318
302
323
WIREBOND
324
326
330
316
GATE
TERMINATION
N
312
314
310
DRAINLINE
CAPACITOR
2
1
321
320
322
DRAINLINE
TERMINATION
328
308
INPUT

300

FIG. 3

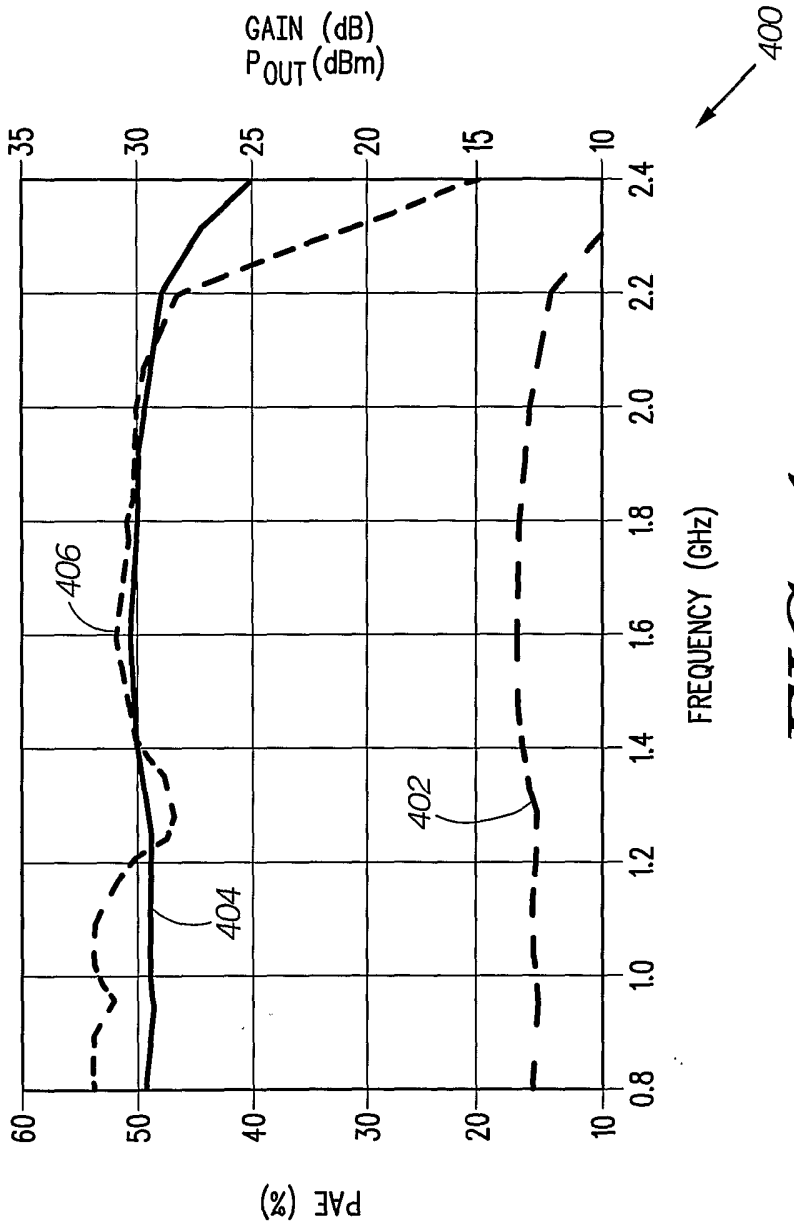

GAIN (dB)
$P_{OUT}$ (dBm)
400
35
30
25
20
15
10
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
FREQUENCY (GHz)
406
402
404
60
50
40
30
20
10
PAE (%)

FIG. 4

# INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/22571

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03F3/60 H01L23/66

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03F H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | D'AGOSTINO S ET AL: "A 0.5-12 GHz hybrid matrix distributed amplifier using commercially available FETs" MICROWAVE SYMPOSIUM DIGEST, 1991., IEEE MTT-S INTERNATIONAL BOSTON, MA, USA 10-14 JUNE 1991, NEW YORK, NY, USA,IEEE, US, 10 June 1991 (1991-06-10), pages 289-292, XP010037635 ISBN: 0-87942-591-1 the whole document --- | 1 |
| X | BROUZES H ET AL: "A 1 to 40 GHz MESFET hybrid distributed amplifier" IEEE MTT-S DIGEST, 13 June 1989 (1989-06-13), pages 849-852, XP010085710 the whole document --- | 1-6,8-11 |
| | -/-- | |

[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 21 October 2003 | 28/10/2003 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016 | Agerbaek, T |

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# INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/22571

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication,where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | BIRAN Y: "2 - 22 Ghz Low Noise Distributed Amplifier Design" JOURNAL: UNKNOWN, 7 March 1989 (1989-03-07), pages 1-4, XP010300543 the whole document --- | 1 |
| X | US 4 446 445 A (APEL THOMAS R) 1 May 1984 (1984-05-01) abstract; figures 1,2 ----- | 1-11 |

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

# INTERNATIONAL SEARCH REPORT

[redacted]formation on patent family members

International Application No
PCT/US 03/22571

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 4446445 A | 01-05-1984 | NONE | |