(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
5 October 2017 (05.10.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/171935 A1

(51) International Patent Classification:
H01L 21/04 (2006.01) *H01L 21/311* (2006.01)
H01L 21/3213 (2006.01) *H01L 23/522* (2006.01)
H01L 21/768 (2006.01)

(21) International Application Number:
PCT/US2016/059951

(22) International Filing Date:
1 November 2016 (01.11.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
15/088,557 1 April 2016 (01.04.2016) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to the identity of the inventor (Rule 4.17(i))*

Published:

— *with international search report (Art. 21(3))*

(54) Title: HYDROGEN BARRIERS IN A COPPER INTERCONNECT PROCESS

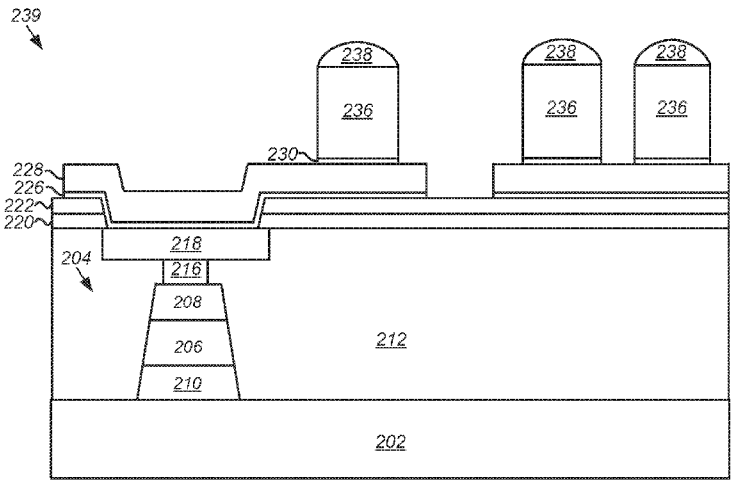

FIG. 2K

(57) Abstract: A microelectronic system including hydrogen barriers and copper pillars for wafer level packaging and method of fabricating the same are provided. Generally, the method includes: forming an insulating hydrogen barrier over a surface of a first substrate; exposing at least a portion of an electrical contact to a component in the first substrate by removing a portion of the insulating hydrogen barrier, the component including a material susceptible to degradation by hydrogen; forming a conducting hydrogen barrier over at least the exposed portion of the electrical contact; and forming a copper pillar over the conducting hydrogen barrier. In one embodiment, the material susceptible to degradation is lead zirconate titanate (PZT) and the microelectronic systems device is a ferroelectric random access memory including a ferroelectric capacitor with a PZT ferroelectric layer. Other embodiments are also disclosed.

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Hydrogen Barriers In A Copper Interconnect Process

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is an International Application of U.S. Application Number 15/088,557, filed on April 1, 2016, which claims the benefit of priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application Ser. No. 62/255,211, filed November 13, 2015, all of which are incorporated by reference herein in their entirety.

TECHNICAL FIELD

[0002] The present disclosure relates generally to microelectronic system packaging, and more particularly, to a copper interconnect process to enable a face-to-face and wafer-level-chip-scale packaging and to a microelectronic system including hydrogen barriers and copper interconnects.

BACKGROUND

[0003] Wafer-level-chip-scale packaging (WLCSP) is a type of package for integrated circuits (ICs) or Micro-Electromechanical System (MEMS), having an area that no greater than 120% of the area of the chip or die it contains, and is generally surface mountable. Face-to-Face (F2F) packaging is a type of WLCSP in which multiple dies or chips of a microelectronic system are vertically stacked and electrically coupled within a single package reducing a size or footprint of the package. F2F packages utilize copper (CU) pillar or bumps and redistribution layers (RDL) to interconnect bond pads formed on exposed facing surfaces of the chips. CU pillars allow a finer pitch, reduce the probability of CU pillars bridging, and decrease the capacitance load for the circuits, as compared to flip-chip technology using solder bumps, thereby allowing the

microelectronic system to operate at higher frequencies. MCM are particular advantageous for integrally packaging chips including circuits or components fabricated using incompatible technologies. For example, F2F packaging can be used where a first chip or substrate including logic circuits or a processor, typically fabricated using complementary metal-oxide-semiconductor (CMOS) technology, is electrically coupled to and integrally packaged with a second chip including an IC, such as a memory, or a MEMS fabricated using processes incompatible with CMOS technology.

[0004] Problems with conventional F2F packaging utilizing CU pillar and/or RDLs include diffusion of hydrogen through conductive and non-conductive layers surrounding a component in the IC or MEMS including a material susceptible to degradation by hydrogen. For example, a ferroelectric random access memory (F-RAM) including a ferroelectric capacitor with a lead zirconate titanate (PZT) ferroelectric layer or a MEMS with a piezoelectric layer including PZT. It has been observed that PZT is exposed to hydrogen, particular at elevated temperatures, the electrical properties of a PZT layer are severely degraded. Generally, there are two ways in which hydrogen is introduced to F2F packaged components. The first is during standard processing techniques used to form the CU pillars and RDL, or other interconnects which typically require hydrogen species at elevated process temperatures. The second is from hydrogen generated within the chip itself. For example, water adsorbed within permeable layer of the chip structure can react with metals causing dissociation of the water releasing hydrogen.

[0005] Thus, there is a need for a F2F package and packaging method that minimizes hydrogen penetration into ICs or MEMS including a material susceptible to

degradation by hydrogen during the packaging process. It is further desirable that structure of the F2F package minimizes penetration into ICs or MEMS of hydrogen generated within the chip itself.

SUMMARY

[0006] A microelectronic system including copper pillars and hydrogen barriers to minimize hydrogen penetration into a component incorporating a material that renders the component susceptible to degradation by hydrogen during forming the copper pillars is provided. The component is formed in a first substrate, and the microelectronic system further includes an insulating hydrogen barrier over a surface of the first substrate, the insulating hydrogen barrier having an opening exposing at least a portion of an electrical contact to the component, and a conducting hydrogen barrier over at least the exposed portion of the electrical contact. The copper pillar is formed over a top surface of the conducting hydrogen barrier and electrically coupled to the component through the conducting hydrogen barrier and the electrical contact. The material that renders the component susceptible to degradation can include lead zirconate titanate (PZT). In one embodiment, the microelectronic system can include a Micro-Electromechanical Systems (MEMS) device including PZT. In another embodiment, the microelectronic system can include a ferroelectric random access memory (F-RAM), and the component includes a ferroelectric capacitor incorporating a PZT ferroelectric layer.

[0007] In one embodiment, a method of fabricating the microelectronic system includes forming an insulating hydrogen barrier over a surface of a first substrate, and exposing at least a portion of an electrical contact to a component in the first substrate by

removing a portion of the insulating hydrogen barrier. The component includes a material that renders the component susceptible to degradation by hydrogen. A conducting hydrogen barrier is then formed over the exposed portion of the electrical contact and at least a portion of the insulating hydrogen barrier. A copper pillar is formed over the conducting hydrogen barrier, while the insulating hydrogen barrier and the conducting hydrogen barrier minimizes hydrogen penetration into the material of the component.

[0008] In one embodiment, the method further includes patterning the conducting hydrogen barrier to form a redistribution layer (RDL) prior to forming the copper pillar on the RDL over the insulating hydrogen barrier.

[0009] In another embodiment, the method further includes forming a copper (CU) RDL on the conducting hydrogen barrier and patterning the CU RDL and conducting hydrogen barrier prior to forming the copper pillar over a portion of the CU RDL over the insulating hydrogen barrier, while the insulating hydrogen barrier and the conducting hydrogen barrier minimizes hydrogen penetration into the material susceptible to degradation during forming the CU RDL.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Embodiments of the present invention will be understood more fully from the detailed description that follows and from the accompanying drawings and the appended claims provided below, where:

[0011] FIGs. 1A and 1B are a flowchart illustrating an embodiment of a method for packaging a microelectronic system in a face-to-face package including copper pillars and a copper redistribution layer according to an embodiment of the present disclosure;

[0012] FIGs. 2A-2L are block diagrams illustrating cross-sectional views of a portion of the microelectronic system formed by the method of the flowchart of FIGs. 1A and 1B;

[0013] FIG. 3 is a block diagram illustrating a cross-sectional view of a portion of the microelectronic system according to another embodiment of the method of the present disclosure; and

[0014] FIG.4 is a block diagram illustrating cross-sectional views of a portion of the microelectronic system including a Micro-Electromechanical System (MEMS) formed by the method of the flowchart of FIGs. 1A and 1B.

DETAILED DESCRIPTION

[0015] Embodiments of face-to-face (F2F) packages including copper pillars and redistribution layers and methods of fabricating the same to minimize hydrogen penetration into a material susceptible to degradation by hydrogen are described herein with reference to figures. However, particular embodiments may be practiced without one or more of these specific details, or in combination with other known methods, materials, and apparatuses. In the following description, numerous specific details are set forth, such as specific materials, dimensions and processes parameters etc. to provide a thorough understanding of the present invention. In other instances, well-known semiconductor design and fabrication techniques have not been described in particular detail to avoid unnecessarily obscuring the present invention. Reference throughout this specification to "an embodiment" means that a particular feature, structure, material, or characteristic described in connection with the embodiment is included in at least one

embodiment of the invention. Thus, the appearances of the phrase "in an embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the invention. Furthermore, the particular features, structures, materials, or characteristics may be combined in any suitable manner in one or more embodiments.

[0016] The terms "over," "under," "between," and "on" as used herein refer to a relative position of one layer with respect to other layers. As such, for example, one layer deposited or disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer deposited or disposed between layers may be directly in contact with the layers or may have one or more intervening layers. In contrast, a first layer "on" a second layer is in contact with that second layer. Additionally, the relative position of one layer with respect to other layers is provided assuming operations deposit, modify and remove films relative to a starting substrate without consideration of the absolute orientation of the substrate.

[0017] Embodiments of a F2F packaging method to minimize hydrogen penetration into a material susceptible to degradation by hydrogen will now be described in detail with reference to FIGS. 1A and 1B, FIGs. 2A-2K and FIG. 3. FIGS. 1A and 1B are a flowchart illustrating an embodiment of a method for packaging a microelectronic system in a F2F package including CU pillars and a CU RDL. FIGs. 2A-2K are block diagrams illustrating cross-sectional views of a portion of the microelectronic system formed by the method of the flowchart of FIGs. 1A and 1B. FIG. 3 is a block diagram illustrating a cross-sectional view of a portion of the microelectronic system prepared for packaging according to another embodiment of the method of the present disclosure.

[0018] Referring to FIG. 1A and FIG. 2A, the process begins with forming a

component of a microelectronic system on or in a first substrate **202** or chip (step **102**). In the embodiment shown in FIG 2A, the microelectronic system is or includes a ferroelectric random access memory (F-RAM), and the component is a ferroelectric capacitor **204** incorporating a material susceptible to degradation by hydrogen. The ferroelectric capacitor **204** includes a ferroelectric material **206** between an upper electrode **208** and a lower electrode **210** covered by or embedded in a dielectric layer **212**. In addition to the ferroelectric capacitor **204** each cell in the F-RAM further includes a number of transistors (not shown) electrically coupled to the lower electrode **210** through a metallization layer **214** and to the upper electrode **208** through a vertical contact or via **216** extending through the dielectric layer **212** and an electrical contact **218** formed from a second metallization layer. Optionally, the ferroelectric capacitor **204** can further include conductive oxygen (O_2) barriers between the lower electrode **210** and metallization layer **214** and between the top electrode **208** via **216**, and sidewall encapsulation layers between the ferroelectric capacitor and dielectric layer **212**.

[0019] The ferroelectric capacitor **204**, dielectric layer **212**, metallization layer **214**, via **216** and electrical contact **218** are formed using a standard deposition and photolithographic process flows. The upper electrode **208** and lower electrode **210** can include one or more layers of iridium or iridium oxide having a thickness of from about 0.05 to about 0.20 μm, and are deposited or formed using chemical vapor deposition (CVD), atomic layer deposition (ALD) or physical vapor deposition (PVD). The metallization layer **214**, via **216** and electrical contact **218** can be or include aluminum, titanium, tungsten or alloys or mixtures thereof, and can be deposited by PVD, such as sputtering, evaporation, or electroless plating to a thickness of from about 1000 to about

5000 Å. Dielectric layer **212** can include one or more layers of an undoped oxide, such as ferroelectric oxide (FEO) or silicon-dioxide (SiO_2), a nitride, such as silicon nitride (Si_xN_y), a silicon-oxynitride ($SixO_yN_z$) or phosphosilicate glass (PSG) deposited by CVD to a thickness of from about ____ to about ____ microns (μ).

[0020] The ferroelectric material **206** generally includes a material such as lead zirconate titanate (PZT) Pb $[Zr_xTi_{1-x}]O_3$, which is susceptible to degradation by hydrogen and is deposited to a thickness of from about 0.04 to about 0.10 μm, using CVD, ALD or PVD. Data is stored in the ferroelectric capacitor by applying an external electric field across a ferroelectric material, which causes dipoles in the ferroelectric material to align with the field direction. After the electric field is removed data is stored in the cell using a remnant polarization of the ferroelectric material. As hydrogen penetrates or diffuses into the ferroelectric material, the oxide of the PZT undergoes reduction. Electrically this is observed as a decrease in the "remnant polarization", or charge that remains once the applied voltage is removed.

[0021] Next, as indicated in step **104** of FIG. 1A, the surfaces of the electrical contact **218** and dielectric layer **212** are planarized, for example, using a chemical mechanical polishing (CMP) process.

[0022] Referring to FIGs. 1A and 2B an insulating hydrogen barrier **220** is then formed over and/or directly on the planarized surfaces of the electrical contact **218** and dielectric layer **212** (step **106**). The insulating hydrogen barrier **220** can be or include one or more layers of aluminum oxide (Al_2O_3) having a thickness of from about ___ to about ___ Å or a silicon oxynitride (SiON) having a thickness of from about ___ Å to about ___ Å, and deposited by CVD or ALD.

[0023] In some embodiments, such as that shown in FIG. 2B, a passivation layer **222** is formed on the insulating hydrogen barrier **220** (step **108**). The passivation layer **222** can be or include one or more layers of dielectric material, such as silicate glass (USG), silicon nitride, silicon oxide, polymer, polyimides or combinations thereof. In one embodiment, the passivation layer **222** includes _____ having a thickness of from about ___ to about ___ Å deposited by CVD or ALD. **[Ali, 1) can the passivation layer be omitted in some embodiments or is it absolutely necessary for the device to work? 2) What is the material and thickness of the passivation layer and how is it deposited? Also, does either or both of the passivation layer or insulating hydrogen barrier need to be planarized after deposition?]**

[0024] Next, referring to FIGs. 1A and 2C a first opening **224** is formed in the insulating hydrogen barrier **220**, and passivation layer **222** if present, exposing at least a portion of the electrical contact **218** (step **110**). First opening **224** can be etched using standard photolithographic and dry or wet etching techniques. For example, a patterned photoresist layer (not shown) can be formed on the passivation layer **222**, and where the passivation layer includes _____ and the insulating hydrogen barrier **220** includes Al_2O_3, both layers can be etched in a wet etch process using a buffered oxide etch (BOE), a hydrofluoric (HF) wet etch, a pad etch, or any other similar hydrofluoric-based wet etching chemistry. Alternatively, the etch can be accomplished in a dry or plasma process using a mixture of a _____ based gas, such as _____, and _____ or _____. **[Ali, please provide some details of the etch process. Is wet or dry? Can both layers be etched in a single process?]**

[0025] Referring to FIGs. 1A and 2D a conducting hydrogen barrier **226** is

formed over at least the exposed portion of the electrical contact **218** (step **112**). Generally, the conducting hydrogen barrier is formed over at least a portion of the passivation layer **222** and insulating hydrogen barrier **220**, and in some embodiments, such as that shown, the conducting hydrogen barrier **226** is formed over and directly on substantially an entire surface of the passivation layer **222**. The conducting hydrogen barrier **226** can be or include one or more layers of titanium-aluminum-nitride (TiAlN) or aluminum titanium nitride (AlTiN) having a thickness of from about ___ Å to about ___ Å, and deposited by CVD or ALD. Alternatively, the conducting hydrogen barrier **226** can include one or more layers of titanium nitride (TiN), titanium oxynitride (TiON), titanium aluminum oxynitride (TiAlON) or aluminum (Al) having a thickness of from about ___ Å to about ___ Å, and deposited by CVD or ALD.

[0026] In some embodiments, such as that shown in FIG. 2E, a separate, dedicated redistribution layer (RDL) **228** is formed over the conducting hydrogen barrier **226** (step **114**). The RDL **228** serves to redistribute or relocate subsequently formed pads or pillars that are electrically coupled to the contact **218** away from a location directly over the contact. The RDL **228** can be or include one or more layers of conductive material, such as a metal or metal alloy. In one embodiment, the RDL **228** includes copper (Cu) having a thickness of from about ___ to about ___ Å deposited by plasma assisted CVD (PACVD). In one embodiment a capacitively coupled radio frequency (RF) hydrogen plasma including a copper precursor, such as hexafluoroacetylacetonate ($Cu(HFA)_2$), is used to form on a surface of the substrate via a reaction between the precursor adsorbed in the conducting hydrogen barrier **226** and atomic hydrogen. **[Ali, is this correct?]**

[0027] As noted above, the ferroelectric material **206** generally includes a material such PZT, which is susceptible to degradation by hydrogen. In conventional copper deposition processes hydrogen can diffuse into the PZT through the RDL and/or a conventional passivation, the contact **218**, via **216** and upper electrode **208**. In the method of the present disclosure the insulating hydrogen barrier **220** and the conducting hydrogen barrier **226** isolate the contact 218 from the hydrogen used or generated in the PACVD process, minimizing or substantially eliminating hydrogen penetration into the ferroelectric material **206** of the ferroelectric capacitor **204** during the forming of a Cu RDL **228**.

[0028] Generally, the RDL **228** is formed directly on the conducting hydrogen barrier **226** overlying the contact **218**, and over at least a portion of conducting hydrogen barrier overlying the passivation layer **222** and insulating hydrogen barrier **220**. In some embodiments, such as that shown, the RDL **228** is formed directly on substantially an entire surface of the conducting hydrogen barrier **226** overlying the passivation layer **222** and insulating hydrogen barrier **220**.

[0029] Next, in some embodiments, such as that shown in FIG. 2F, under bump metallization (UBM) **230** is formed over the conducting hydrogen barrier **226** and RDL **228** (step **114**). The UBM **230** can be or include one or more layers of a metal or metal alloy selected to serve as an adhesion or glue layer, a diffusion barrier and/or a seed layer. Generally, the UBM **230** is formed of titanium, tantalum, titanium nitride, tantalum nitride by PVD. In one embodiment, the UBM **230** can includes _____ having a thickness of from about ___ to about ___ Å deposited directly on the RDL **228** by sputtering, evaporation, or electroless plating.

[0030] Next, referring to FIGs. 1A and 2G the UBM **230**, RDL **228** and conducting hydrogen barrier **226** are patterned (step **116**). The UBM **230**, RDL **228** and conducting hydrogen barrier **226** can be patterned using standard photolithographic and dry or wet etching techniques. For example, a patterned photoresist layer (not shown) can be formed on the UBM **230**, and where UBM includes _____, RDL **228** includes copper, and the conducting hydrogen barrier **226** includes TiAlN, all of the layers can be etched in a wet etch process using a solution including an acid, such as nitric, acetic or sulfuric acid, and an oxidizing agent, such as hydrogen peroxide, permanganate, ferric ion, bromine or chromium. **[Ali, please provide some details of the etch process. Is wet or dry? Can all three layers be etched in a single process?]**

[0031] Referring to FIGs. 1B and 2H a photoresist (PR) coating **232** is deposited over the patterned UBM **230**, RDL **228** and conducting hydrogen barrier **226** and patterned using standard photolithographic techniques to form second openings **234** therein (step **118**).

[0032] Next, referring to FIGs. 1B and 2I copper (Cu) bumps or pillars **236** are formed in the second openings **234** on the UBM **230** exposed therein, and solder caps **238** formed on the pillars (step **120**). The Cu pillars **236** can be deposited to a thickness or height above the UBM **230** of from about ___ to about ___ μ by PACVD using a hydrogen plasma as described above with respect to the Cu RDL **228**. The insulating hydrogen barrier **220** and the conducting hydrogen barrier **226** minimizes or substantially eliminates hydrogen penetration into the ferroelectric material **206** of the ferroelectric capacitor **204** during the forming of the copper pillars **236**. The solder caps **238** can include tin, silver, lead, Cu, zinc, indium, gold, bismuth, antimony or alloys thereof, and

are be deposited directly on the Cu pillars **236** to a thickness of from about ___ to about ___ Å by a electroless plating process.

[0033] Referring to FIGs. 1B and 2J the patterned PR coating **232** is removed or stripped using standard photolithographic techniques, and exposed portions of the UBM **230**, not underlying the copper pillars **236** removed (step **122**). As with the step of patterning the UBM **230**, step **116**, described above, the exposed portions of the UBM can be removed in a wet etch process using a solution including an acid, such as nitric, acetic or sulfuric acid, and an oxidizing agent, such as hydrogen peroxide, permanganate, ferric ion, bromine or chromium. **[Ali, is this correct?]**

[0034] Next, referring to FIGs. 1B and 2K the first substrate **202** is singulated or diced to form individual die or chips, and solder caps **238** are softened or melted in a reflow soldering process in preparation for a face-to-face attachment to a companion-die or second substrate (step **124**). Generally, as shown in FIG. 2K each of the individual die or chips include one or more components of the microelectronic system, such as the ferroelectric capacitor **204**, and one or more Cu pillars **236** through which the die can be physically attached and electrically coupled to the companion-die or second substrate (not shown in this figure). **[Ali, is this correct?]**

[0035] Finally, referring to FIGs. 1B and 2L the singulated or diced first substrate **202** is physically attached and electrically coupled to the companion-die or second substrate **240** through the molten solder caps **238** to form a WLCSP or F2F package **242** as shown in FIG. 2L (step **126**). Referring to FIG. 2L the second substrate **240** includes first pads **244** on a top or facing surface to which the Cu pillars **236** are bonded and through which a number of other components, such as ICs **246**, formed on the second

substrate can be electrically coupled to components of the microelectronic system on the first substrate **202**. Additionally, the second substrate **240** can further include second pads **248** on a lower or opposing surface electrically coupled to the first pads **244** and/or ICs **246** formed in or on the second substrate by means of a number of through silicon vias (TSVs) **250**. The first and second substrates **202** and **240** can be encapsulated in a dielectric or plastic molding compound **252** and physically attached and/or electrically coupled to an external circuit via a number of a ball grid array **254** on the second substrate, or a backplane to which the second substrate is attached, to form a flat, no-lead package, such as a Quad Flat-pack No-lead (QFN) package.

[0036] Alternatively, in another embodiment (not shown) the F2F package **242** is an open cavity type package in which the first and second substrates **202** and **240** are positioned in an open cavity and enclosed by plastic, ceramic, glass or metal sidewalls attached to the second substrate, or a backplane and top wall or lid joining the sidewalls. Additionally, the second substrate 240 can be attached or wire bonded to a lead frame through which the first and second substrates **202** and **240** can be electrically coupled to an external circuit.

[0037] In yet another alternative embodiment, shown in FIG. 3, the conducting hydrogen barrier **226a** includes a material and a thickness selected to serve as a redistribution layer (RDL) to redistribute or relocate subsequently formed pads or pillars that are electrically coupled to the contact **218** away from a location directly over the contact. The RDL/conducting hydrogen barrier **226a** can include a single layer of titanium-aluminum-nitride (TiAlN), aluminum titanium nitride (AlTiN), titanium nitride (TiN), titanium oxynitride (TiON), titanium aluminum oxynitride (TiAlON) or aluminum

(Al) having a thickness of from about ___ Å to about ___ Å, and can be deposited by CVD or ALD. In one version of this embodiment the RDL/conducting hydrogen barrier **226a** can include a single layer of TiAlN or AlTiN having a thickness of from about ___ μ to about ___ μ deposited by CVD. It will be understood that this embodiment is advantageous in that it eliminates the need for a separate deposition and etch steps for a dedicated RDL **228**, and can further minimize hydrogen penetration into the ferroelectric material **206** of the ferroelectric capacitor **204** during processing by eliminating a Cu RDL **228**.

[0038] Finally, in another alternative embodiment, the microelectronic system is or can include a Micro-Electromechanical System (MEMS) having a component including a piezoelectric material susceptible to hydrogen degradation. Exemplary MEMS can include microphones, motion or position sensors, such as gyroscopes, accelerometers, and magnetometers, light modulators, resonators, transducers, and actuators or pumps, such as those used in inkjet print heads. An embodiment of a microelectronic system including a motion/positon sensing MEMS **256** having a component and including a piezoelectric material **258**, such as PZT, is shown in FIG. 4.

[0039] Referring to FIG. 4, in addition to the piezoelectric material **258** the MEMS includes an upper electrode **260** and a lower electrode **262** coupled to the piezoelectric material, and a test mass **266** formed on the upper electrode over the piezoelectric material, all enclosed in a cavity **264** formed in the dielectric layer **212**. The upper electrode **260** also serves as a spring for the test mass **266**. In operation, acceleration of the MEMS **256** exerts a force on the piezoelectric material **258**, which can be detected and measured by a change in the electrostatic force or voltage generated by

the piezoelectric material across the upper electrode **260** and lower electrode **262**. [**Ali, we should include an exemplary figure of a MEMS for which the packaging method, i.e., insulating and conducting H2 barrier can be used in order to not limit our claims to F-RAM. I have prepared a drawing of an accelerometer, but I am not certain that the figure or description is accurate or adequate. Could you correct the figure and description OR provide me with a rough diagram of such a MEMS for which the method of the invention can be used. Note, in the event you choose to do later please make certain the MEMS can be covered by a thick ILD and the H2 barriers could be formed over it.**]

[0040] Thus, embodiments of ferroelectric random access memories including a copper interconnect process to enable F2F and WLCSP packaging and to a microelectronic system including hydrogen barriers and copper interconnects have been described. Although the present disclosure has been described with reference to specific exemplary embodiments, it will be evident that various modifications and changes may be made to these embodiments without departing from the broader spirit and scope of the disclosure. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

[0041] The Abstract of the Disclosure is provided to comply with 37 C.F.R. §1.72(b), requiring an abstract that will allow the reader to quickly ascertain the nature of one or more embodiments of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. In addition, in the foregoing Detailed Description, it can be seen that various features are grouped together in a single embodiment for the purpose of streamlining the

disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed embodiments require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

IN THE CLAIMS

WHAT IS CLAIMED IS:

1. A method of fabricating a microelectronic system, the method comprising:

forming an insulating hydrogen barrier over a surface of a first substrate;

exposing at least a portion of an electrical contact to a component in the first substrate by removing a portion of the insulating hydrogen barrier, the component comprising lead zirconate titanate (PZT) and susceptible to degradation by hydrogen;

forming a conducting hydrogen barrier over at least the exposed portion of the electrical contact; and

forming a copper pillar over the conducting hydrogen barrier.

2. The method of claim 1 further comprising forming a passivation layer on the insulating hydrogen barrier prior to forming the conducting hydrogen barrier, and wherein exposing at least a portion of an electrical contact comprises removing a portion of the passivation layer.

3. The method of claim 1 further comprising forming an under bump metallization (UBM) layer over the conducting hydrogen barrier prior to forming the copper pillar, and wherein the copper pillar is formed on the UBM layer.

4. The method of claim 3 wherein forming the conducting hydrogen barrier comprises forming the conducting hydrogen barrier over at least a portion of the insulating hydrogen barrier, and further comprising patterning the conducting hydrogen

barrier to form a redistribution layer (RDL) prior to forming the copper pillar on the RDL over the insulating hydrogen barrier.

5. The method of claim 3 wherein forming the conducting hydrogen barrier comprises forming the conducting hydrogen barrier over at least a portion of the insulating hydrogen barrier, and further comprising forming a redistribution layer (RDL) on the conducting hydrogen barrier and patterning the RDL and conducting hydrogen barrier prior to forming the copper pillar over a portion of the RDL over the insulating hydrogen barrier.

6. The method of claim 5 wherein the RDL comprises copper (CU).

7. The method of claim 3 wherein the insulating hydrogen barrier comprises aluminum oxide (AL_2O_3) and the conducting hydrogen barrier comprises titanium-aluminum-nitride (TiAlN) or aluminum titanium nitride (AlTiN).

8. The method of claim 1 wherein the microelectronic system comprises a Micro-Electromechanical Systems (MEMS) device including the component comprising PZT.

9. The method of claim 1 wherein the microelectronic system comprises a ferroelectric random access memory and the component comprises a ferroelectric capacitor including a ferroelectric layer comprising PZT.

10. The method of claim 1 further comprising bonding and electrically connecting the first substrate to a second substrate through the copper pillars and enclosing the first substrate and the second substrate to form a face-to-face (F2F) package.

11. A method comprising:

forming an insulating hydrogen barrier over a surface of a first substrate;

exposing at least a portion of an electrical contact to a component in the first substrate by removing a portion of the insulating hydrogen barrier, the component including a material susceptible to degradation by hydrogen;

forming a conducting hydrogen barrier over the exposed portion of the electrical contact and at least a portion of the insulating hydrogen barrier; and

forming a copper pillar over the conducting hydrogen barrier, wherein the insulating hydrogen barrier and the conducting hydrogen barrier minimizes hydrogen penetration into the material susceptible to degradation during forming the copper pillar.

12. The method of claim 11 further comprising forming a copper (CU) redistribution layer (RDL) on the conducting hydrogen barrier and patterning the CU RDL and conducting hydrogen barrier prior to forming the copper pillar over a portion of the CU RDL over the insulating hydrogen barrier, wherein the insulating hydrogen barrier and the conducting hydrogen barrier minimizes hydrogen penetration into the material susceptible to degradation during forming the CU RDL.

13. A microelectronic system comprising:

a component in a first substrate, the component comprising lead zirconate titanate (PZT) and susceptible to degradation by hydrogen;

an insulating hydrogen barrier over a surface of the first substrate, the insulating hydrogen barrier comprising an opening exposing at least a portion of an electrical contact to the component;

a conducting hydrogen barrier over at least the exposed portion of the electrical contact; and

a copper pillar over a top surface of the conducting hydrogen barrier.

14. The microelectronic system of claim 13 further comprising an under bump metallization (UBM) formed over the conducting hydrogen barrier, and wherein the copper pillar is formed on the UBM.

15. The microelectronic system of claim 14 wherein the conducting hydrogen barrier extends over at least a portion of the insulating hydrogen barrier and is patterned to form a redistribution layer (RDL), and wherein the copper pillar is formed over the RDL and the insulating hydrogen barrier.

16. The microelectronic system of claim 16 wherein the conducting hydrogen barrier extends over at least a portion of the insulating hydrogen barrier, further comprising a redistribution layer (RDL) on the conducting hydrogen barrier, and wherein the copper pillar is formed over the RDL and the insulating hydrogen barrier.

17. The microelectronic system of claim 14 wherein the insulating hydrogen barrier comprises aluminum oxide (AL_2O_3) and the conducting hydrogen barrier comprises titanium-aluminum-nitride (TiAlN) or aluminum titanium nitride (AlTiN).

18. The microelectronic system of claim 13 wherein the microelectronic system comprises a Micro-Electromechanical Systems (MEMS) device including the component comprising PZT.

19. The microelectronic system of claim 13 wherein the microelectronic system comprises a ferroelectric random access memory and the component comprises a ferroelectric capacitor including a ferroelectric layer comprising PZT.

20. The microelectronic system of claim 13 further comprising a second substrate bonded and electrically connected to the first substrate through the copper pillars and enclosed in a face-to-face (F2F) package.

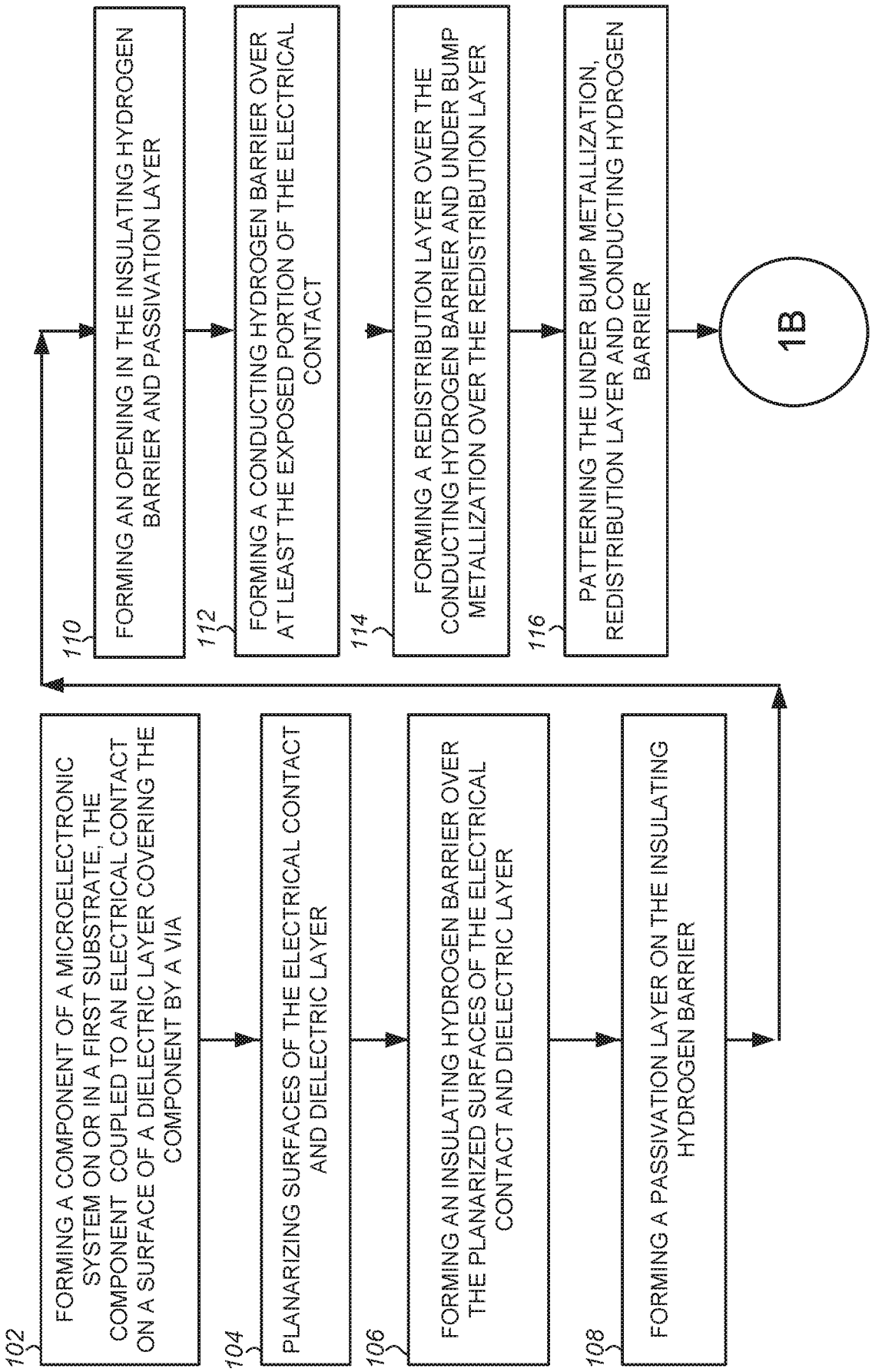
102
FORMING A COMPONENT OF A MICROELECTRONIC SYSTEM ON OR IN A FIRST SUBSTRATE, THE COMPONENT COUPLED TO AN ELECTRICAL CONTACT ON A SURFACE OF A DIELECTRIC LAYER COVERING THE COMPONENT BY A VIA
104
PLANARIZING SURFACES OF THE ELECTRICAL CONTACT AND DIELECTRIC LAYER
106
FORMING AN INSULATING HYDROGEN BARRIER OVER THE PLANARIZED SURFACES OF THE ELECTRICAL CONTACT AND DIELECTRIC LAYER
108
FORMING A PASSIVATION LAYER ON THE INSULATING HYDROGEN BARRIER
110
FORMING AN OPENING IN THE INSULATING HYDROGEN BARRIER AND PASSIVATION LAYER
112
FORMING A CONDUCTING HYDROGEN BARRIER OVER AT LEAST THE EXPOSED PORTION OF THE ELECTRICAL CONTACT
114
FORMING A REDISTRIBUTION LAYER OVER THE CONDUCTING HYDROGEN BARRIER AND UNDER BUMP METALLIZATION OVER THE REDISTRIBUTION LAYER
116
PATTERNING THE UNDER BUMP METALLIZATION, REDISTRIBUTION LAYER AND CONDUCTING HYDROGEN BARRIER
1B

FIG. 1A

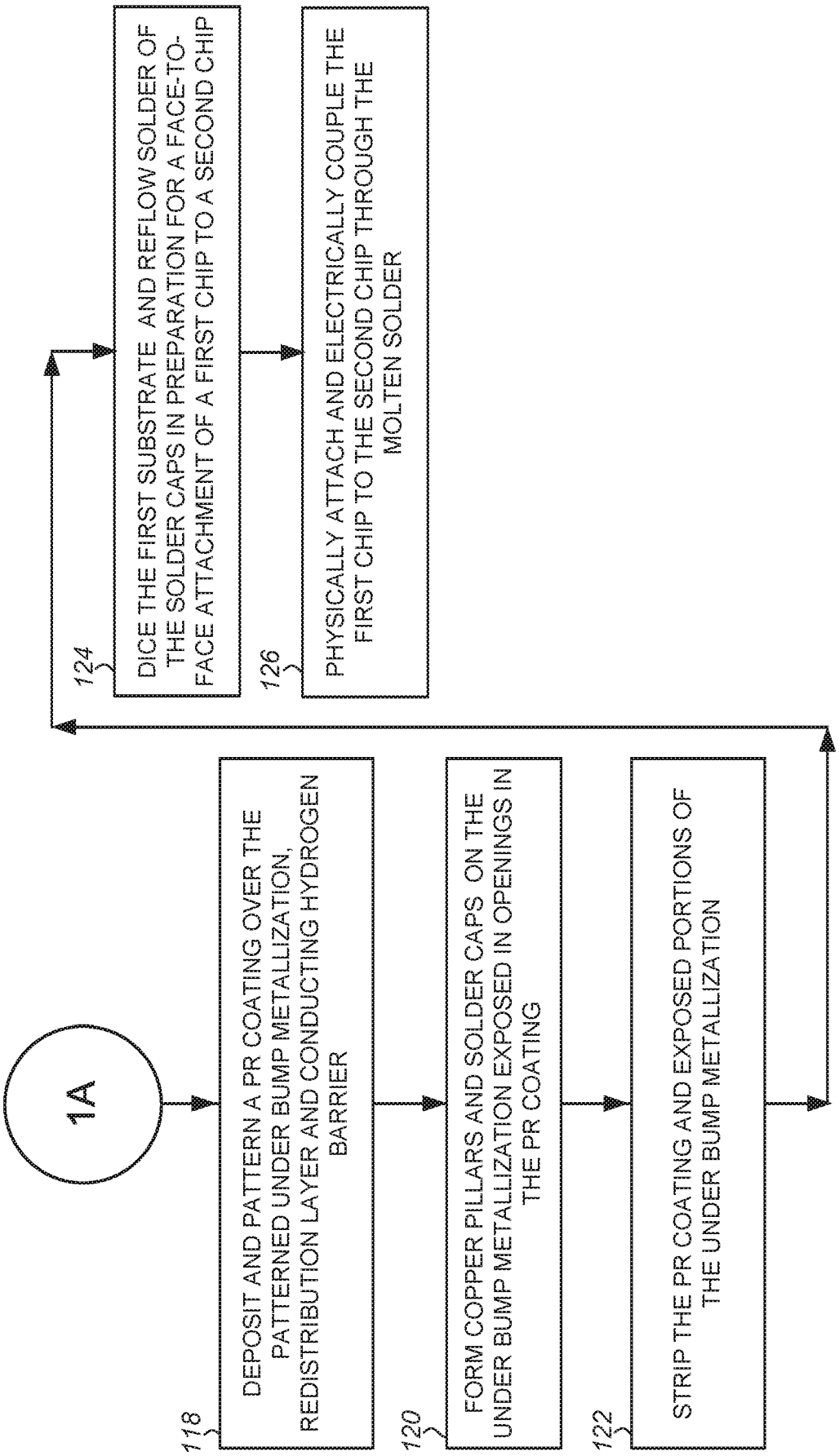
1A
118
DEPOSIT AND PATTERN A PR COATING OVER THE PATTERNED UNDER BUMP METALLIZATION, REDISTRIBUTION LAYER AND CONDUCTING HYDROGEN BARRIER
120
FORM COPPER PILLARS AND SOLDER CAPS ON THE UNDER BUMP METALLIZATION EXPOSED IN OPENINGS IN THE PR COATING
122
STRIP THE PR COATING AND EXPOSED PORTIONS OF THE UNDER BUMP METALLIZATION
124
DICE THE FIRST SUBSTRATE AND REFLOW SOLDER OF THE SOLDER CAPS IN PREPARATION FOR A FACE-TO-FACE ATTACHMENT OF A FIRST CHIP TO A SECOND CHIP
126
PHYSICALLY ATTACH AND ELECTRICALLY COUPLE THE FIRST CHIP TO THE SECOND CHIP THROUGH THE MOLTEN SOLDER

FIG. 1B

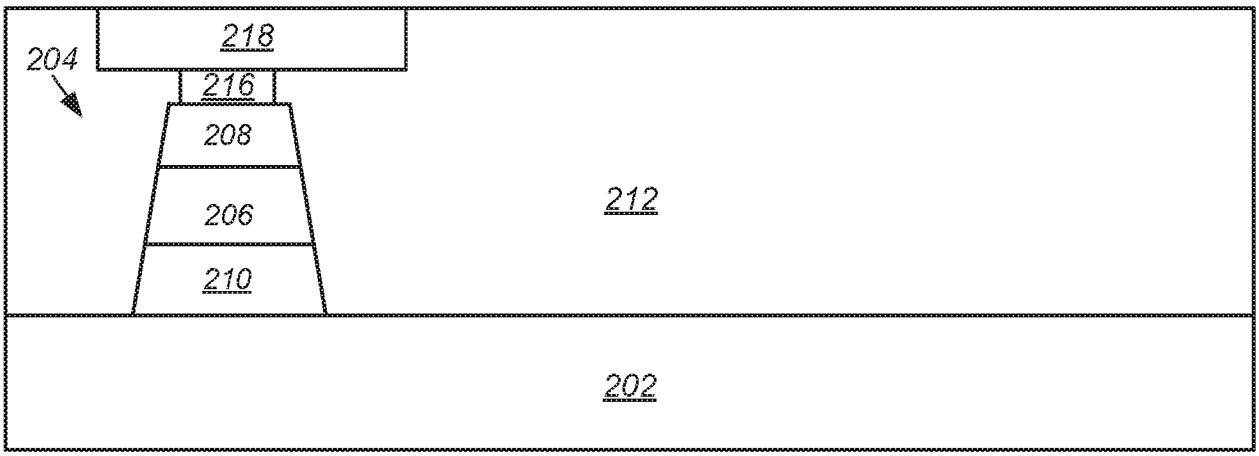

FIG. 2A

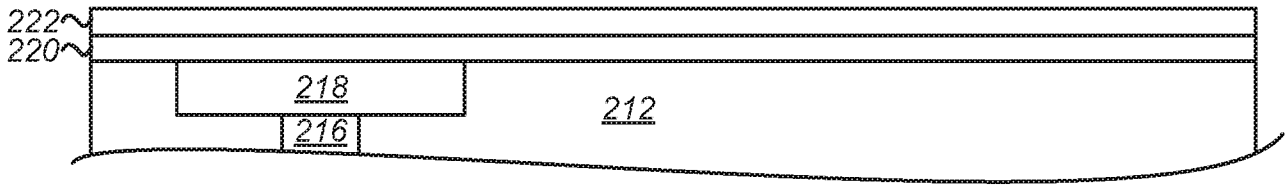

FIG. 2B

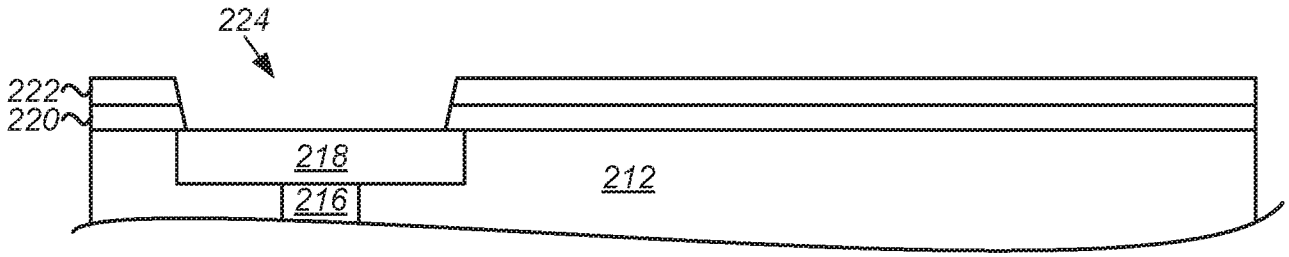

FIG. 2C

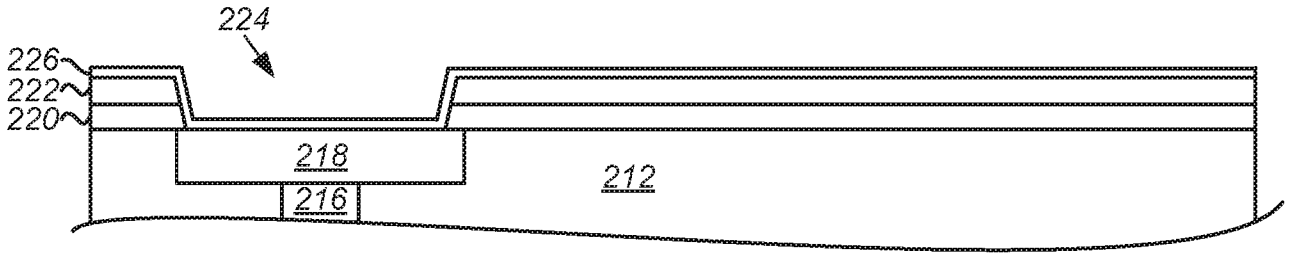

FIG. 2D

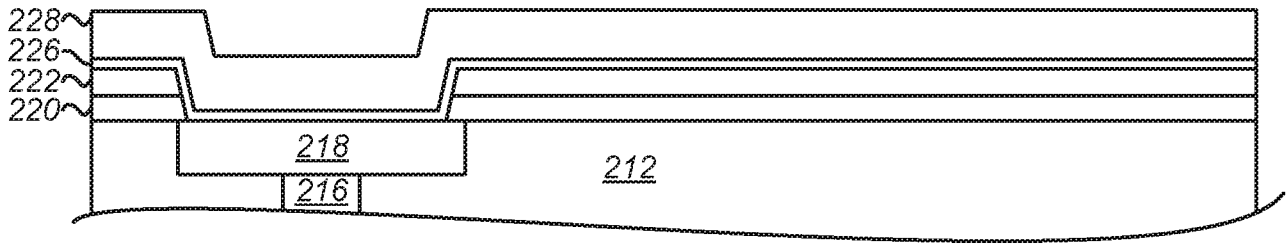

FIG. 2E

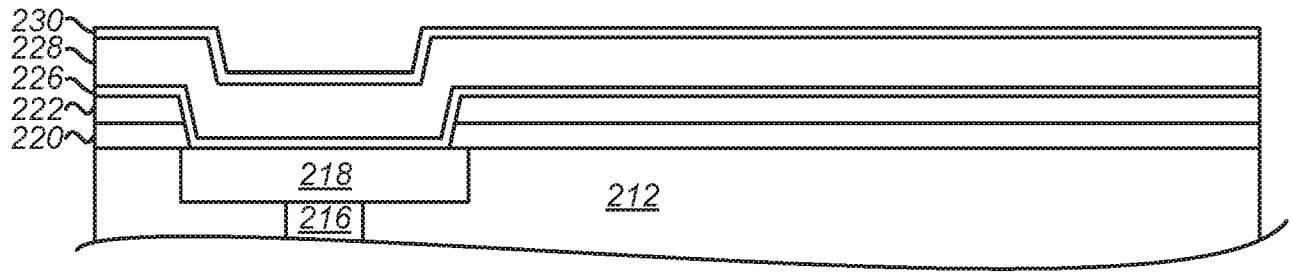

FIG. 2F

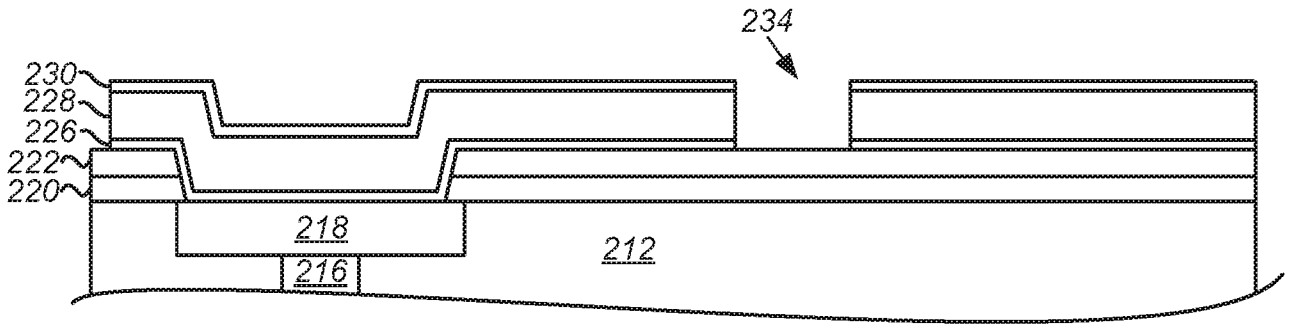
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FIG. 2G

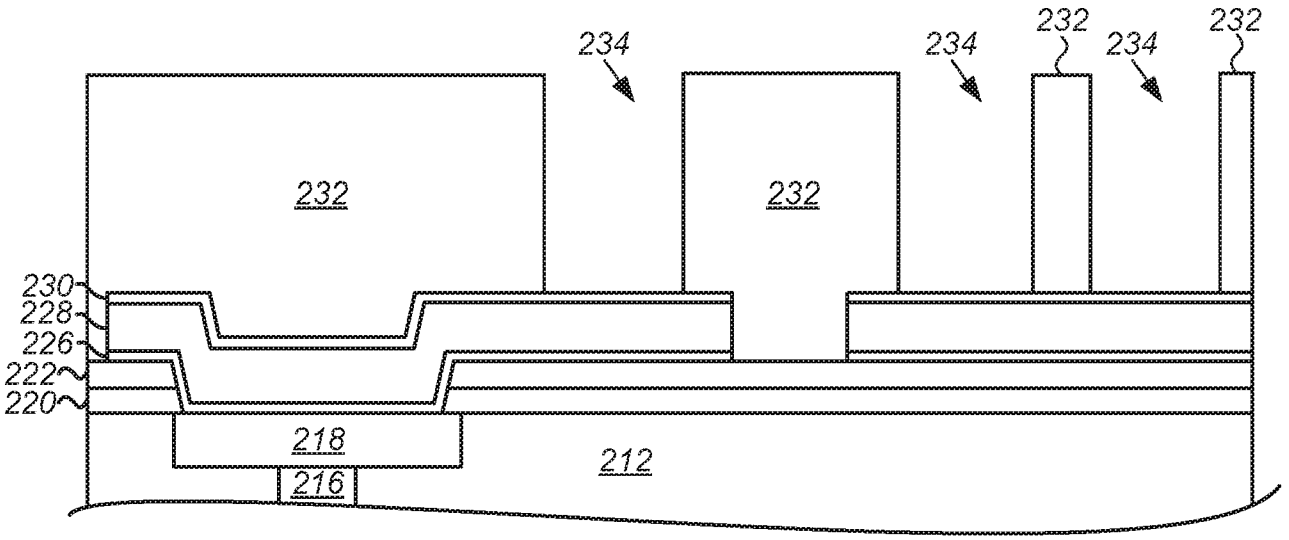
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FIG. 2H

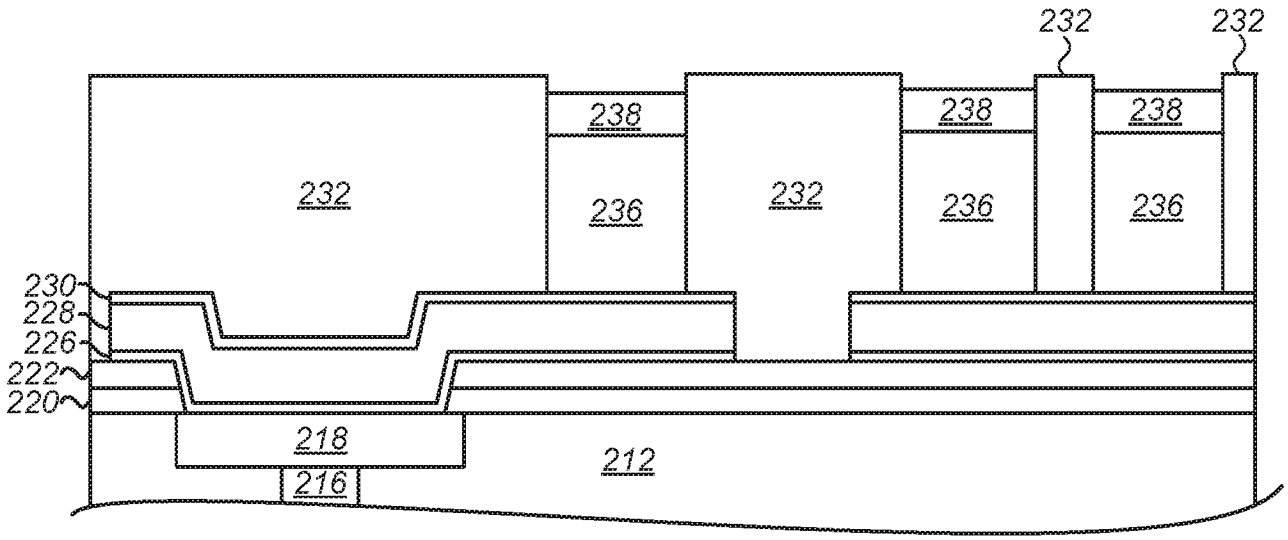
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FIG. 2I

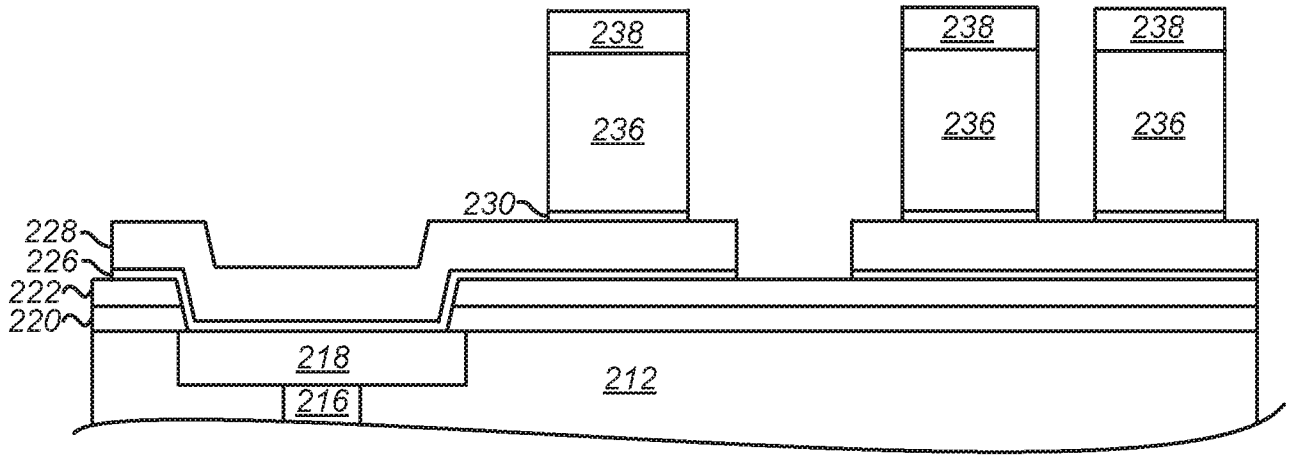
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FIG. 2J

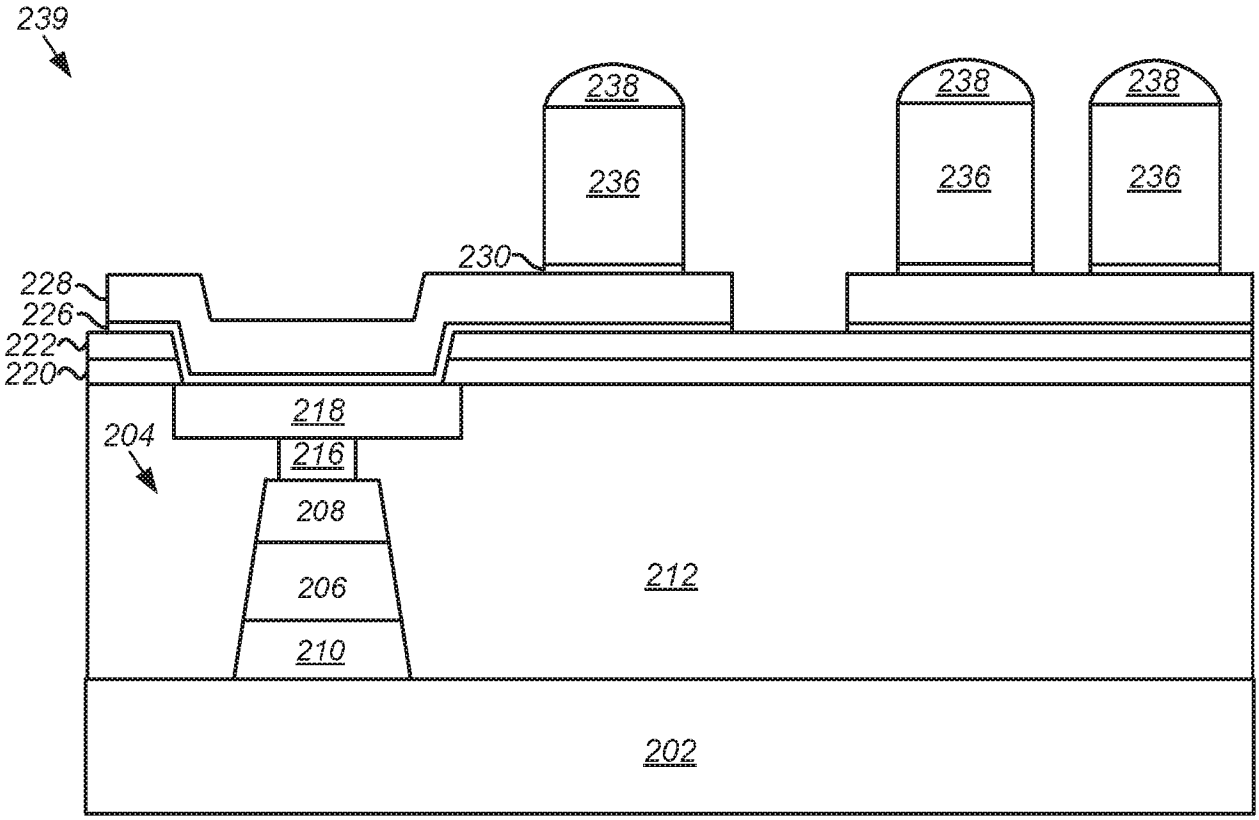
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FIG. 2K

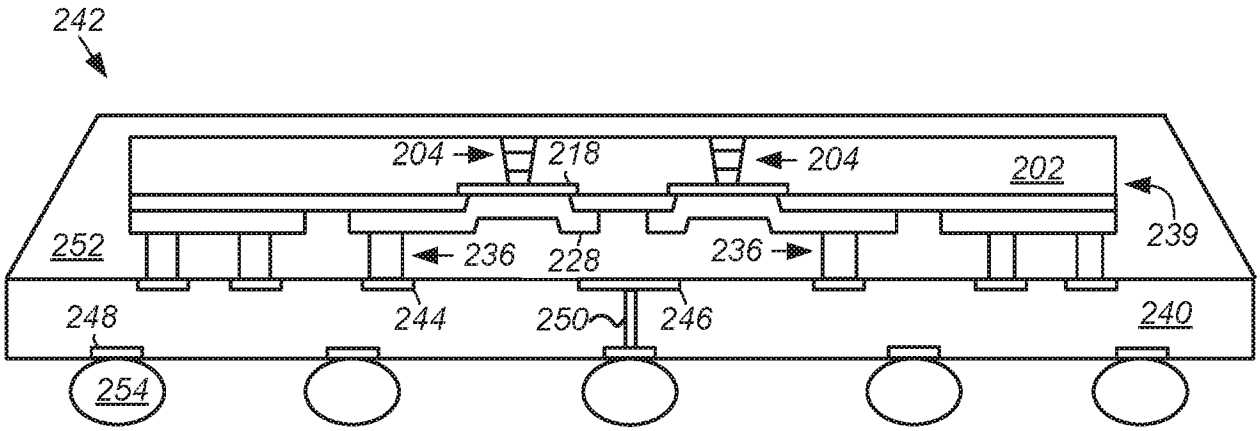
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FIG. 2L

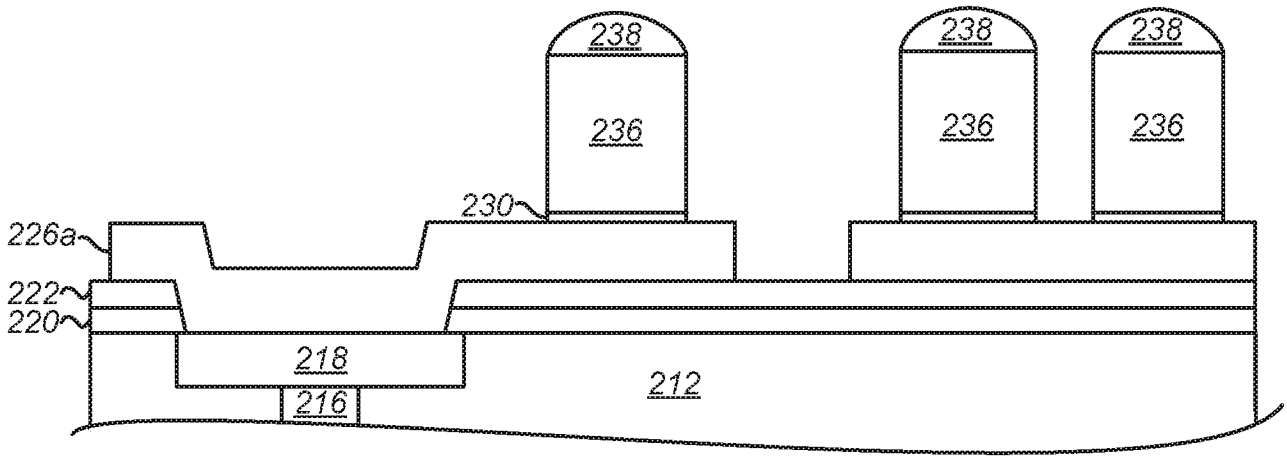
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FIG. 3

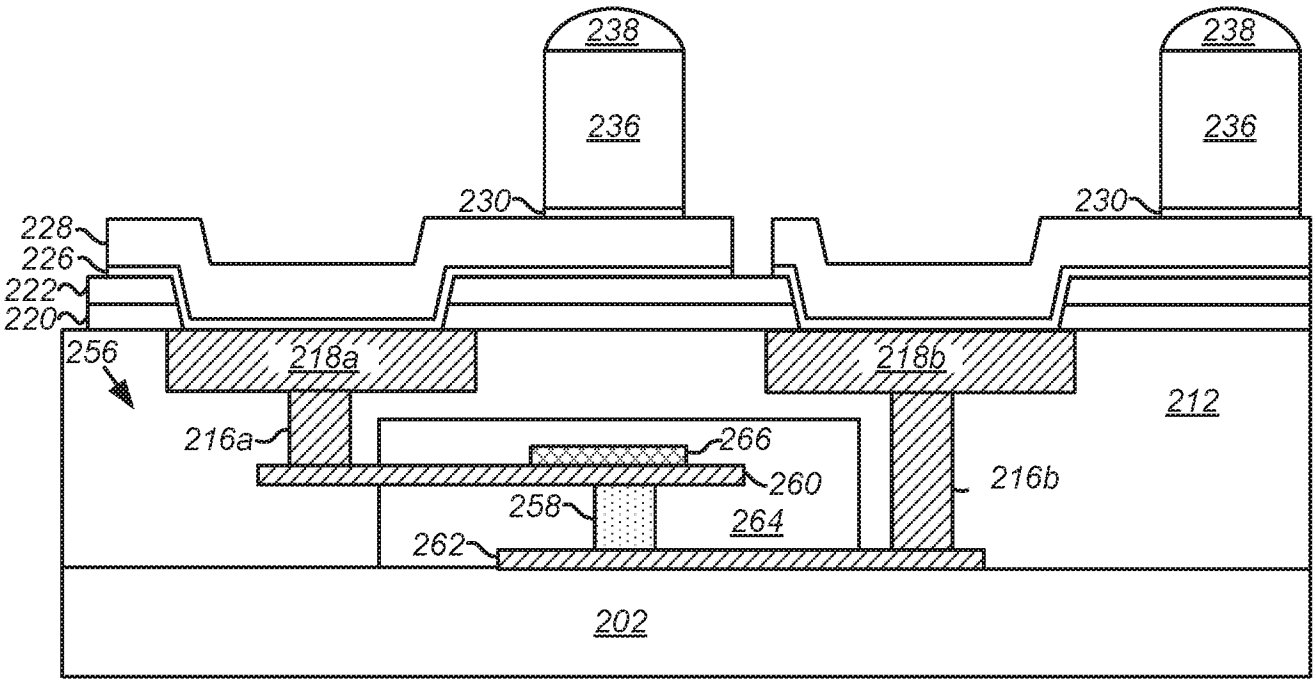
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FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 16/59951

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 21/04, H01L 21/3213, H01L 21/768, H01L 21/311, H01L 23/522 (2016.01)

CPC - H01L 21/04, H01L 21/3213, H01L 21/768, H01L 21/311, H01L 23/522, H01L 41/1876, H01L 2225/1058

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8)- H01L 21/04, H01L 21/3213, H01L 21/768, H01L 21/311, H01L 23/522 (2016.01);
CPC- H01L 21/04, H01L 21/3213, H01L 21/768, H01L 21/311, H01L 23/522, H01L 41/1876, H01L 2225/1058

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC- 257/735-776, 257/E21.589, 257/E21.59-E21.597, 257/29.2, 438/598-687;
Patents and NPL (classification, keyword; search terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Pub West (US EP JP WO), Pat Base (AU BE BR CA CH CN DE DK EP ES FI FR GB IN JP KR SE TH TW US WO), Google Patent, Google Scholar, Google Web, FPO; search terms: semiconductor, wafer, microelectronic, circuit, capacitor, copper, Cu, pillar, bump, pad, barrier, hydrogen, conducting, lead, zirconate, titanate, PZT, metallization, redistribute...

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012/0129335 A1 (IKUMO et al.) 24 May 2012 (24.05.2012), Figs. 3B, 4B, 19B, 36B, para [0010]-[0012], [0067], [0072]-[0074], [0078], [0085], [0093], [0109], [0125], [0134], [0140], [0141], [0148], [0188], [0193]-[0196]	1-20
Y	US 2014/0370673 A1 (ZELNER et al.) 18 December 2014 (18.12.2014), Figs. 4-6; para [0009], [0049], [0050], [0054], [0057], [0058], [0059], [0061], [0071]	1-20
Y	US 2008/0237866 A1 (WANG) 02 October 2008 (02.10.2008), Fig. 5E; para [0014], [0029], [0041], [0047], [0061]-[0063]	2
Y	US 2014/0134950 A1 (LEEDY) 15 May 2014 (15.05.2014), para [0071], [0074], [0076], [0081], [0084], [0093], [0121], [0498], [0727]	8-10, 18-20
Y	US 2015/0054129 A1 (SAIGOH et al.) 26 February 2015 (26.02.2015), para [0014]-[0070]	1-20
Y	US 2012/0064712 A1 (LEI et al.) 15 March 2012 (15.03.2012), para [0004]-[0022]	1-20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 January 2017	30 JAN 2017
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774