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(54) Title: POLY FUSE ROM WITH MOS DEVICE BASED CELL STRUCTURE AND THE METHOD FOR READ AND WRITE THEREFORE

(57) Abstract: A one-time programmable (OTP) structure is implemented using a self-aligned silicided (SALICIDE) poly-silicon fuse. In an example embodiment, the OTP structure is laid out as a fuse element having a first terminal and a second terminal. A switching transistor having a drain, source, and a gate surrounds the fuse element. The drain is coupled to the second terminal of the fuse element surrounds the fuse element. The gate surrounds the drain. The source surrounds the gate. To build transistor with sufficient drive capability for programming the fuse element, the geometry of the gate is laid out in a serpentine or an equivalent pattern increase the effective W/L. A feature of this layout is that OTP cells may be abutted to one-another to form an array. Metallization is arranged so that row lines connect to the first terminal of the fuse element and column lines connect to the gate of the switching transistor. The arrangement enables the placing of read and write circuits at opposite sides of the array. All of the gates in a column may be read simultaneously while providing write current to program one fuse at a time.

Poly Fuse ROM with MOS Device Based Cell Structure and the Method for Read and Write Therefore

RELATED APPLICATIONS

This application is a continuation-in-part of application Serial Number 09/368,400 titled COMPARATORS, MEMORY DEVICES, COMPARISON METHODS, AND MEMORY READING METHODS, filed August 4, 1999. This application is also related to application Serial Number 09/519,940 titled COMPARATORS, MEMORY DEVICES, COMPARISON METHODS, AND MEMORY READING METHODS, filed March 7, 2000 as a divisional application of 09/368,400. Both applications are herein incorporated by reference in their entirety.

FIELD OF INVENTION

The present invention is generally directed to the memory devices. In particular, the present invention relates to a method of programming a one-time programmable array implemented with silicided poly-silicon fuses.

BACKGROUND OF INVENTION

Many devices that may be taken for granted in modern electronics, would not exist without semiconductor memory. Memories may be classified as volatile and non-volatile. Volatile memory requires that power be maintained on the circuit to preserve the memory's contents. Such volatile memory includes DRAM (dynamic random access memory). Non-volatile memory includes ROM (read-only memory), EEPROM (electrically erasable ROM), and NVRAM (non-volatile RAM). Such memory retains its stored information even after the power supply is removed.

Of particular importance, is ROM. ROM is useful where an electronic device must repeatedly have access to the same set of instructions. For example, the built-in operating system (BIOS) of a personal computer is reused during booting-up of the system. Semiconductor ROM is typically an array of memory cells that may be programmed by the user. Depending upon the type, the memory array may be programmed a multiple of times or is one-time-only programmable (OTP).

The OTP ROM is an array of memory cells having fuse or anti-fuse fusible links. Fuse links are opened (i.e., by "blowing" open the fuses) by the application of a programming current. The opened fuse link has an impedance much greater than that of one not programmed. In contrast to a fuse link, an anti-fuse, when programmed has an impedance much less than that of one not programmed. An anti-fuse link is closed by initiating a deliberate electromigration of a conductive material bridging the gap between the anti-fuse link's two terminals. Consequently, in either fuse link type, programmed cells are in a logic state opposite that of non-programmed cells.

In an example fuse array, the programming voltage and current is about 30 volts and 100mA, respectively. This is significantly higher than the normal power supply voltage, V_{dd} which usually ranges from 1.5v to 5.5v in MOS circuits. Having such a programming voltage/current requirement poses significant challenges to designing, testing, and using the OTP array. For example, a tester and software may have special requirements to generate and test for the high voltage programming. The design itself may require charge pump schemes to step up the power supply voltage to provide programming signals. These workarounds increase the cost of design and test.

Accordingly, a need exists for an OTP array that requires programming voltages and currents not significantly higher than V_{dd}. Such an array would reduce design and testing cost.

SUMMARY OF INVENTION

The present invention is exemplified in a number of implementations, one of which is summarized below. A one-time programmable memory has a fuse element coupled to a large switching transistor. The large switching transistor is integral to the programming of the fuse element. As laid out, a programmable memory cell comprises a fuse element having a first terminal and a second terminal and a switching transistor having a drain, source, and a gate. The drain of the switching transistor is couple to the second terminal of the fuse element, it surrounds the fuse element. The gate surrounds the drain which in turn, is surrounded by the source. In an example embodiment, the gate is laid out in a serpentine pattern. The physical layout builds an electrical equivalent of a large switching transistor.

In another embodiment, an integrated circuit comprises at least one row line and at least one column along first and second directions, respectively. A semiconductor array of at least one programmable memory cell is arranged in rows and columns. Each programmable memory is accessible in response to levels established on selected ones of the

row and column lines. The programmable memory cell comprises a fuse element having a first terminal and a second terminal and a switching transistor having a drain, source, and a gate. The drain of the switching transistor surrounds the fuse element; the gate surrounds the drain; and the source surrounds the gate. Coupled to the first terminal of the fuse element is the row line. The second terminal of the fuse element is coupled to the drain of the switching transistor. Coupled to the gate of the switching transistor is the column line. A feature of this embodiment is that the switching transistor may be either N-MOS or P-MOS or BiCMOS. Another additional feature is the fuse element may be either a fuse or an anti-fuse.

The above summary of the present invention is not intended to represent each disclosed embodiment, or every aspect, of the present invention. Other aspects and example embodiments are provided in the figures and the detailed description that follows.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIG. 1 illustrates a fuse cell as applied to the present invention;

FIG. 2A depicts in layout the circuit of FIG. 1 having the poly-silicon, first metal, and contact points of the present invention;

FIG. 2B depicts the layout of FIG. 2A showing the additional second and third metal layers;

FIG. 2C depicts FIG. 2B having the inter-level contacts (vias) showing the fuse cell and its relation to placement in an array;

FIG. 3 depicts the architecture of the fuse array with Read and Write Circuits according to an embodiment of the present invention;

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and will herein be described in detail.

DETAILED DESCRIPTION

The present invention has been found to be useful and advantageous in connection with providing more reliable OTP (one time programmable structure) by using a salicided (self-aligned silicided) poly-silicon fuse structure array fabricated by a sub-micron CMOS process. However, the invention is not so limited

The OTP salicided poly-silicon fuse array is based on a building cell that includes a salicided poly-silicon fuse and a MOS switch. The two terminal fuse link has one terminal connected to an x-axis (row node) and the other terminal connected to the drain of a wide N-MOS device (switch). The N-MOS device's other two terminals, the source and gate are connected to ground and y-axis (column), respectively. The cells are grouped together to form an array of fuses. An example of a suitable OTP silicided poly-silicon fuse link may be found in U.S. Patent No. 5,854,510 of Sur et al. titled, "Low Power Programmable Fuse Structures." An example of suitable OTP anti-fuse link may be found in U.S. Patent No. 5,899,707 of Sanchez et al. titled, "Method for Making Doped Anti-fuse Structures." Additionally, another example of a suitable OTP anti-fuse may also be found in U.S. Patent No. 6,016,001 of Sanchez et al. titled, "Metal to Amorphous Silicon to Metal Anti-Fuse Structure." Other examples of OTP anti-fuse structures are discussed in U.S. Patent No. 5,821,558 of Han et al. titled, "Anti-Fuse Structures." and U.S. Patent No. 5,783,467 of Han et al. titled, "Method of Making Anti-Fuse Structures Using Implantation of Both Neutral and Dopant Species." These patents cited are each incorporated by reference, herein.

Refer to FIG. 1. The fuse cell 100 has a fuse link 130 coupled to the drain 130a of the N-MOS transistor 140 and to row 120 at 120a. The gate of the N-MOS transistor 140 is coupled to the column 110 at 110a. The source of the N-MOS transistor is coupled to ground at 140c.

Multiples of the fuse cell 100 are grouped to form an array. Each row of the array is connected to a wide P-MOS switch whose gate is coupled to the row decoder and whose source is coupled to a single write current source. A write is accomplished by selecting one row and one column that creates a path for the write current to blow a single fuse.

Each row of the array is connected to a small P-MOS device that mirrors a small read current. The read current is switched on during read mode with an N-MOS switch. During the read mode, one column of cells is selected and the read current biases each fuse in the column. Each of the resulting voltage drops across each fuse is then compared to a single reference voltage generated by a reference fuse. The reference fuse has a known impedance, a multiple of the impedance of an unblown fuse. In one example embodiment according to the present invention, the reference fuse has twice the impedance of an unblown fuse. An example method of programming a silicided poly-silicon fuse may be found in U.S. Patent No. 5,976,943 of Manley et al, titled, "Method for Bi-Layer Programmable Resistor," incorporated by reference, herein. Additionally, an example

method of programming anti-fuse structures may be found in U.S. Patent No. 5,753,540 of Wu et al, titled, "Apparatus and Method for Programming Anti-fuse Structures," also incorporated by reference, herein.

The fuse structure, according to the present invention has a cell design in which the fuse link is surrounded by a switching element. In one example, the switching element is a wide N-MOS transistor. Other switching elements may be used such as a wide P-MOS transistor or BiCMOS-based transistor. The specific application and process technology determine the suitable device chosen.

Refer to FIG. 2A. In an example embodiment according to the present invention the circuit of FIG. 1, has a layout 300 of the fuse 320b having a first terminal 320a and a second terminal 320c. The fuse is surrounded by a wide (in the range of about 80 to about 150um) N-MOS switching element that is made by using a serpentine structure 330b for the poly-silicon gate. The example circuit is built on a three-layer metal technology. However, the invention may be implemented in higher-order metal technology. The wide N-MOS device is needed to carry a relatively large write current. The first terminal 320a of fuse 320b is connected to a row line. The second terminal 320c of the fuse 320b is coupled to the drain 330a of the wide N-MOS device. The gate 330b is connected in the array to a column at 310a and 310b. The multiple connections protect against voltage-drops. The source 330c (shown in FIG. 2A as covered with a first metal layer) of the N-MOS transistor surrounds the serpentine gate 330b; the serpentine gate 330b, in turn surrounds the drain 330a. Contacts (not illustrated) in active device areas enable bonding of the first metal layer to the drain 330a and the source 330c. In subsequent metal layers, the interconnects between them are referred to as "vias."

Refer to FIG. 2B. Multiple metal layers connect the fuse 130 and wide N-MOS device 140 building the circuit as depicted in FIG. 1. In this example, a first metal layer 330c' connects the source 330c. This makes it easy to abut cells together in an array fashion since all N-MOS sources are connected to ground (V_{SS}). A horizontal second metal layer 320a' connects the first fuse terminal 320a to the row line of the array. The second fuse terminal 320c connects to the drain 330a of transistor 300. The gate 330b is connected to a third metal layer at the column connection 310d. The gate 330b through a contact follows a path to a first metal 310b (inter-layer interconnect as shown in FIG. 2C). From the first metal 310b the path continues to second metal 310b' through a via. From second metal 310b' to a third metal 310d through a second via, the path is complete to column connection 310d. In placing the fuse cell 300 in an array, the column 310d (that connects the gate 330b) and

row320a' (that connects the first fuse terminal 320a) readily abuts to the corresponding row and column of another fuse cell. Likewise, the source 330c of the N-MOS switching transistor connects to ground (V_{SS}) through a third metal layer 330c'.

Refer to FIG. 2C. The fuse cell element's three metal layers are connected at the appropriate locations to construct the circuit of FIG. 1. Inter-level connections, contacts and vias provide electrical connection, where desired, for different metal layers. For example, one or more vias 320a'' connects the first terminal 320a of fuse 320b to second metal 320a. The first terminal 320a of fuse 320b has a first metal contacting the poly silicon. (Not illustrated). Similarly, the source 330c is connected to a second metal layer 320c' through one or more vias 330c. One or more vias 310d' connects a third metal layer 310d to second metal layer 310b' through the first metal 310b and 310a that are coupled to the serpentine gate 330b. In using multiple layers of metal, the fuse cell 300 has inherent security features. The fuse element 330 may be covered with second metal and third metal to make optical identification of blown fuses difficult

Refer to FIG. 3. Having laid out the fuse cell, it may be arrayed. The circuit 200 employs the fuse cell 100 of FIG. 1 of the afore-mentioned layout of FIGS. 2A – 2C. The fuse cell 240 is laid out in an array 230. The write circuit 210 and read circuit 205areceive signals from the digital control block 230. The digital control block 230 enables the user to select and program a fuse from the array by addressing the appropriate location. Input 220 receives signals from the digital control block 230. The array is set to either read or write from signals received by input at 225. After programming, the digital control block enables the user to read a whole column at a time. The layout of the fuse cell element enables the mapping of write and read location with the same address. For example, in a 1024 cell array, a particular fuse cell is selected using a 10-bit address.

To verify the programming, the programmed fuse 240 is compared with an un-blown reference fuse 205b with a comparator circuit, which may be a sense amplifier 235. The reference fuse, which may be selectable, is 4x, 6x, 8x, or10x the physical size or resistance of the fuse link in a memory cell. There is also an externally adjustable read biasing current source (100μA to 500μA). Usually the reference fuse and the reading current are pre-selected. However, for test purposes, both of these options in conjunction with the write option allow a method in determining the appropriate read setting for a particular process technology.

While the present invention has been described with reference to several particular example embodiments, those skilled in the art will recognize that many changes

may be made thereto without departing from the spirit and scope of the present invention, which is set forth in the following claims.

CLAIMS:

1. A programmable semiconductor device (300) comprising:

a fuse element (320b) having a first terminal (320a) and a second terminal (320c);

a switching transistor having a first region (330a), second region (330b), and a third region (330c), wherein the first region of the switching transistor is coupled to the second terminal of the fuse element, the first region surrounding the fuse element, the third region surrounding the first region and the second region surrounding the third region.

2. The device of claim 1 wherein, the third region (330c) surrounding the first region (330a) is laid out in a serpentine pattern.

3. The device of claim 1 wherein, the switching transistor is a MOS-based

4. The device of claim 3,

wherein, the first region is a drain;

wherein, the second region is a source; and

wherein the third region is a gate.

5. The device of claim 3,

wherein, the first region is a source;

wherein, the second region is a drain; and

wherein the third region is a gate.

6. The device of claim 4 wherein, the switching transistor is selected from one of the following: N-MOS, P-MOS, BiCMOS.

7. The device of claim 5 wherein, the switching transistor is selected from one of the following: N-MOS, P-MOS, BiCMOS.

8. The device of claim 1 wherein, the fuse element is poly-silicon having a salicided layer thereon.

9. The device of claim 8 wherein,

the fuse element further comprises a structure having a low power programming threshold, comprising:

a substrate having a field oxide region;

a poly-silicon strip lying over the field oxide region and including an increased dopant concentration region; and

a silicided metallization layer having first and second regions lying over the poly-silicon strip, the first region has a first thickness, and the second region has a second thickness that is less than the first thickness and is positioned substantially over the increased dopant concentration region of the poly-silicon strip;

wherein the fuse element is programmable by breaking the second region.

10. The device of claim 5 wherein, the fuse element is an anti-fuse.

11. An integrated circuit (200), comprising:

at least one row line along a first direction;

at least one column line along a second direction; and

a semiconductor array (230) of at least one programmable memory cell (240) arranged in rows and columns, with each programmable memory cell to be accessed in response to levels (230) established on selected ones of the row and column lines, wherein the programmable memory cell comprises,

a fuse element (130; 240) having a first terminal (120a) and a second terminal (130a) ; and

a switching transistor (140) having a drain (130a), source (140c), and a gate (110a), wherein the drain of the switching transistor is coupled to the second terminal of the fuse element, the drain surrounding the fuse element, the gate surrounding the drain and the source surrounding the gate, wherein the first terminal of the fuse element is coupled to the row line and the gate is coupled to the column line.

12. The integrated circuit of claim 11 wherein,

the fuse element further comprises a structure having a low power programming threshold, comprising:

a substrate having a field oxide region;

a poly-silicon strip lying over the field oxide region and including an increased dopant concentration region; and

a silicided metallization layer having first and second regions lying over the poly-silicon strip, the first region has a first thickness, and the second region has a second thickness that is less than the first thickness and is positioned substantially over the increased dopant concentration region of the poly-silicon strip;

wherein the fuse element can be programmed by breaking the second region.

13. The integrated circuit of claim 11 wherein the switching transistor is MOS-based.

14. The integrated circuit of claim 11 wherein, the fuse element is an anti-fuse structure.

15. The integrated circuit of claim 11 wherein,
the switching transistor is selected from one of the following: N-MOS, P-MOS, BiCMOS.

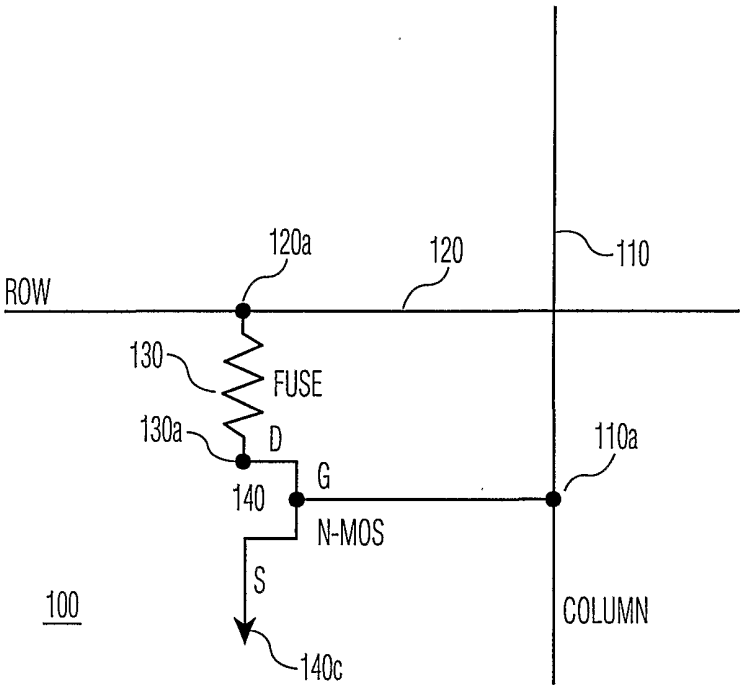

120a
120
110
ROW
130
FUSE
130a
D
110a
G
140
N-MOS
S
100
COLUMN
140c

FIG. 1

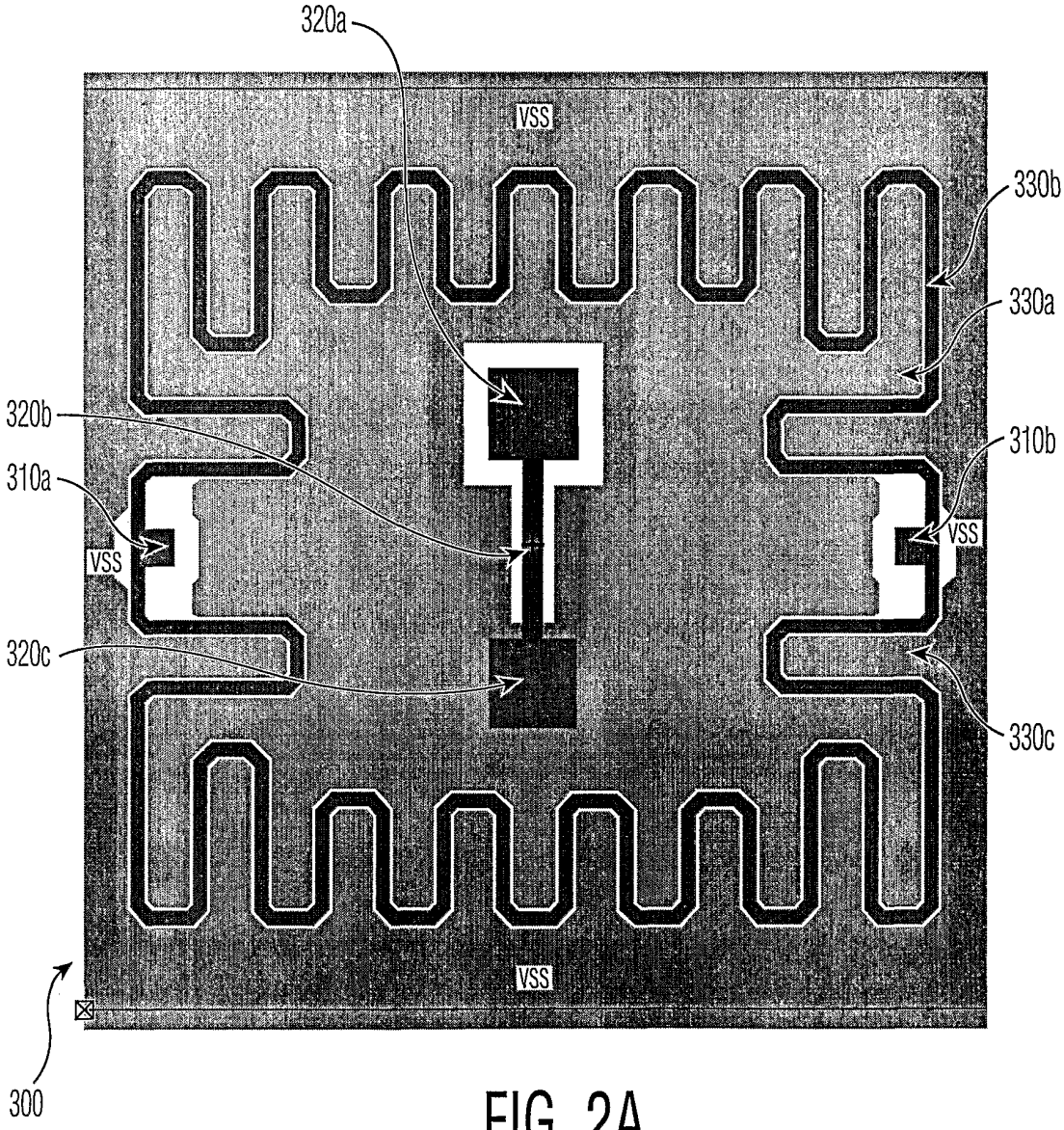
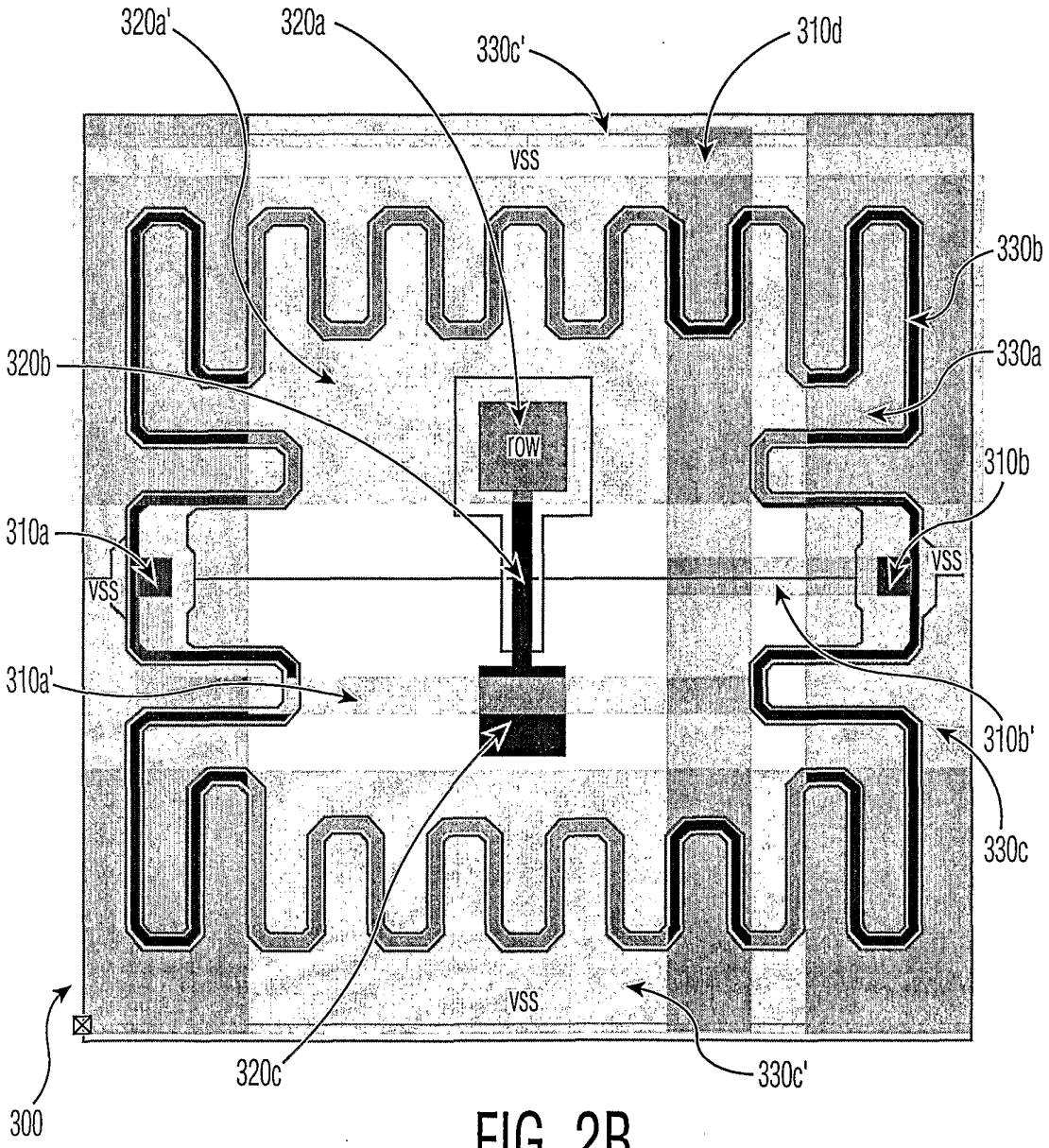


FIG. 2A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320a
330c'
310d
VSS
330b
320b
330a
row
310b
310a
VSS
VSS
310a'
310b'
330c
VSS
320c
330c'
300

FIG. 2B

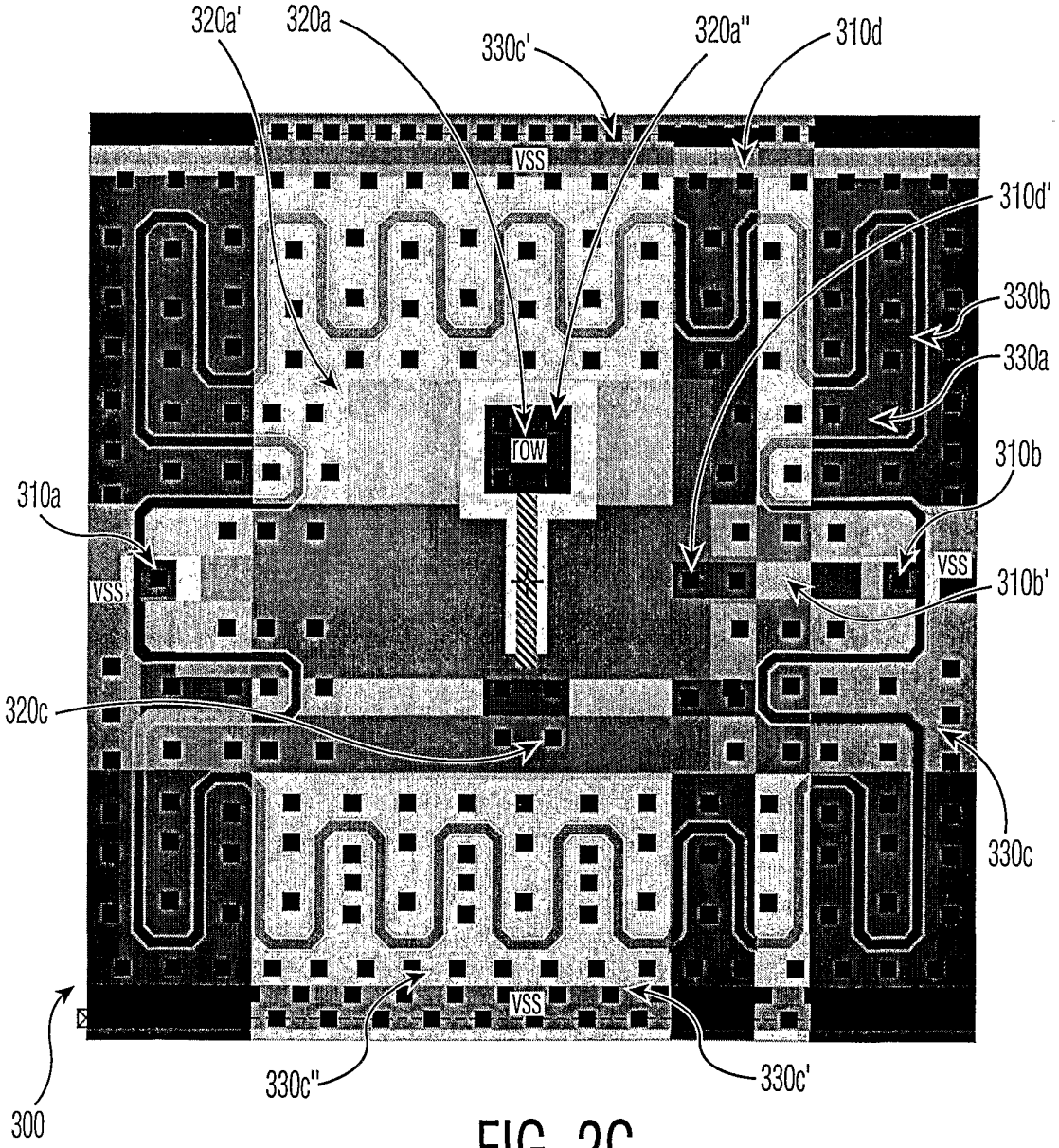
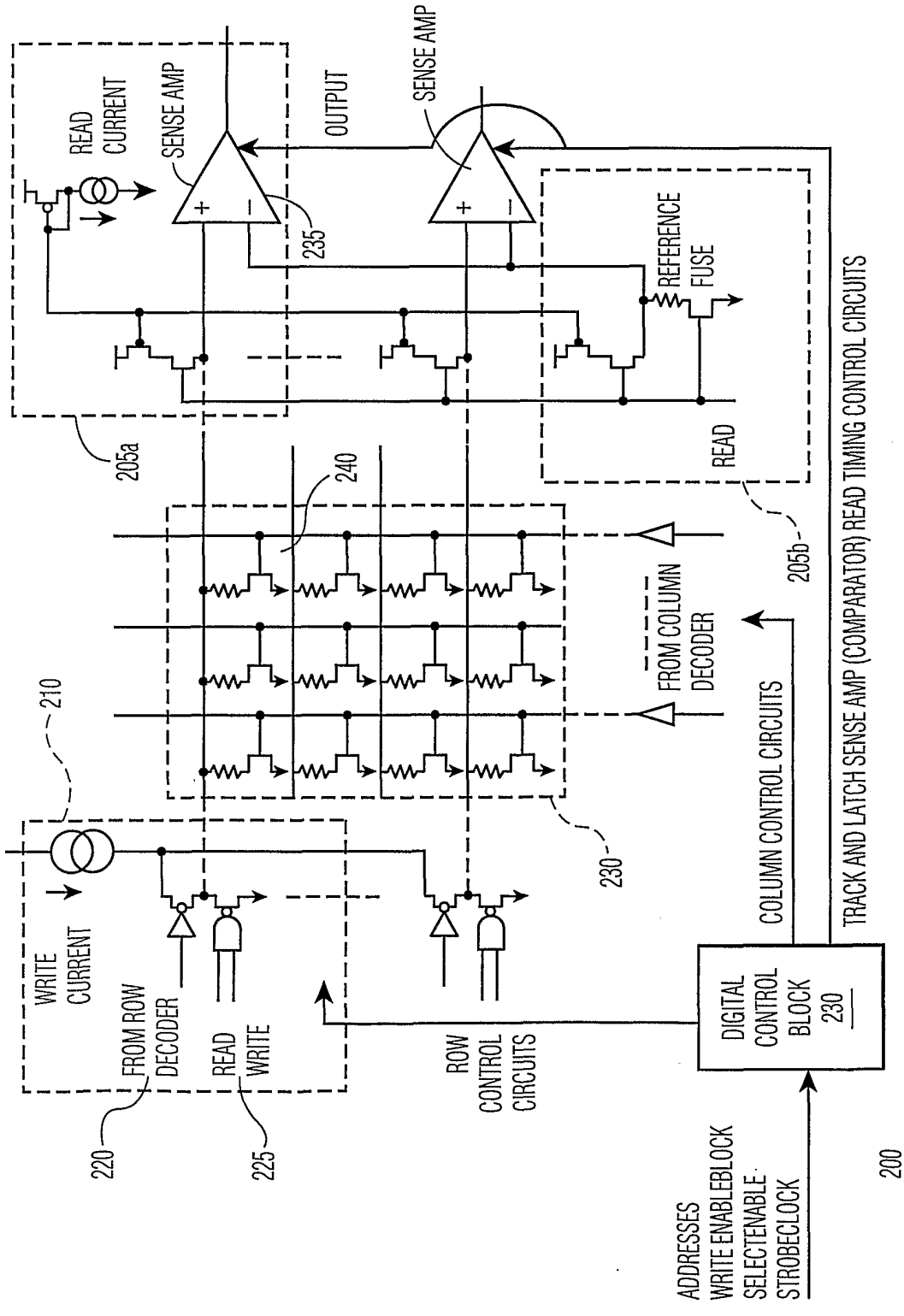

320a'
320a
330c'
320a"
310d
VSS
310d'
330b
330a
ГОW
310b
310a
VSS
VSS
310b'
320c
330c
VSS
330c"
330c'
300

FIG. 2C

FIG. 3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SENSE AMP
OUTPUT
SENSE AMP
235
REFERENCE FUSE
205a
READ
205b
240
FROM COLUMN DECODER
COLUMN CONTROL CIRCUITS
TRACK AND LATCH SENSE AMP (COMPARATOR) READ TIMING CONTROL CIRCUITS
210
230
WRITE CURRENT
FROM ROW DECODER
READ WRITE
ROW CONTROL CIRCUITS
DIGITAL CONTROL BLOCK 230
220
225
ADDRESSES
WRITE ENABLE
BLOCK SELECT
ENABLE STROBE
CLOCK
200