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(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **MALONEY, Timothy** [US/US]; 451 Matadero Avenue, Palo Alto, CA 94306 (US). **POON, Steven** [CA/US]; 1663 Belleville Way, #E, Sunnyvale, CA 94087 (US).

(74) Agent: **STEPHENS, Paul**; Marshall, Gerstein & Borun, 6300 Sears Tower, 233 South Wacker Drive, Chicago, IL 60606 (US).

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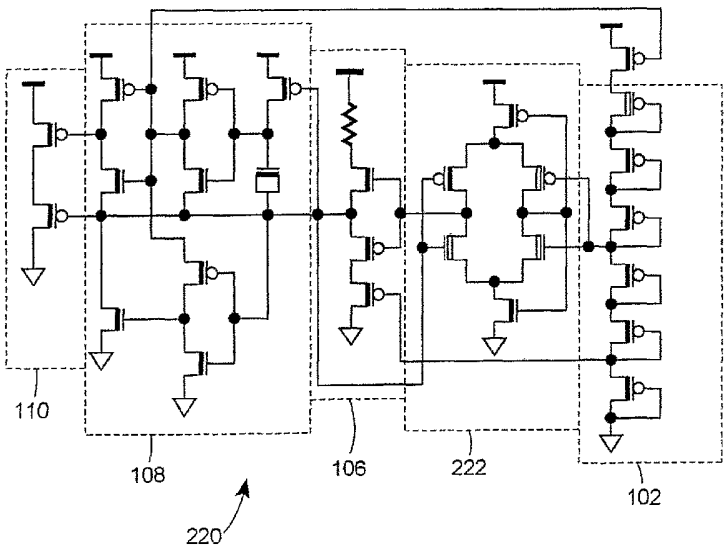
(54) **Title:** MULTI-STACK POWER SUPPLY CLAMP CIRCUITRY FOR ELECTROSTATIC DISCHARGE PROTECTION



(57) **Abstract:** A multi-stack power supply clamp circuit for providing electrostatic discharge (ESD) protection to enhance performance of advanced submicron processes is provided. The clamp circuit includes a bias voltage generator with low leakage and high current drive capabilities, and means to lighten current load on the voltage generator through reduced gate leakage. The bias voltage generator has includes a differential amplifier. The multi-stack clamp circuit provides voltage-tolerant ESD protection with optimized leakage, reduced sensitivity to operating conditions, and tolerance of increased gate current in new process technologies.

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MULTI-STACK POWER SUPPLY CLAMP CIRCUITRY FOR ELECTROSTATIC DISCHARGE PROTECTION

TECHNICAL FIELD

This patent relates generally to electrostatic discharge protection systems and more particularly to protection circuitry for sinking current during an electrostatic discharge.

BACKGROUND

Electrostatic discharge (ESD) refers to the phenomenon of electrical discharge of high current for a short time duration resulting from a build up of static charge on a particular integrated circuit package, or on a nearby human handling that particular IC package. ESD events can have serious detrimental effects on manufacture and performance of integrated circuits (ICs) and other microelectronic devices, systems that contain such devices and manufacturing facilities that produce them. Advances in silicon process technology have led to the development of increasingly smaller sizes for transistors in integrated circuits. In turn, the decreasing size of transistors has made the circuits increasingly susceptible to damage from ESD events.

As we enter the new millennium, the electronic industry continues to scale microelectronic structure to achieve faster devices, new devices, and more per unit area. ESD continues to be a threat for scaled structures produced using various new technologies used in the electronic industry, such as, submicron device technologies, high system operation speeds, higher levels of factory automation, etc. As integrated circuit devices increase in density and their operating supply voltages decrease, the integrated circuits become more sensitive to the effects of ESD. Especially, ESD is a serious problem for semiconductor devices since it has the potential to destroy an entire IC. Because ESD events occur often across the silicon circuits attached to IC package terminals, circuit designers have concentrated their efforts on developing adequate protection mechanisms for these sensitive circuits.

One solution is the use of a grounded gate transistor as a simple ESD protection circuit. The transistor is configured as a diode and has a drain junction breakdown voltage lower than the gate dielectric breakdown voltage. While this circuit provides some protection from ESD events, an ESD protection circuit should also be able to protect an IC

against static discharge by non-destructively passing large currents through a low impedance path in a short time.

Electronic circuits known as power supply clamps have long served the function of protecting power rails during ESD events. Fig. 1 illustrates a block diagram of an exemplary integrated circuit which is well known to one of ordinary skill in the art. FIG. 1 shows an integrated circuit 10 which has a voltage supply input connection 12 for receiving an externally provided high supply voltage from supply circuit 14. An ESD protection circuit 16 is provided to protect internal circuitry 18, designed to perform a predetermined function, from an electrostatic discharge. The ESD protection circuit 16 is described in detail below. The integrated circuit 10 can be any type of integrated circuit which receives a supply voltage, including, but not limited to, processors, controllers, memory devices, application specific integrated circuits (ASIC), etc.

Because certain standardized or legacy supply voltages can be high enough to cause premature failure in metal-oxide semiconductor (MOS) devices used in integrated circuits, redesigned clamp circuits are needed to provide ESD protection to high voltage pins. Such circuits, known as voltage-tolerant clamps or multi-stack claims, are able to withstand high voltages by self-generating bias voltages that are low enough for MOS devices to attach to without causing damage.

A desirable bias voltage circuit should have the characteristics of low power consumption, strong current drive, and limited degradation of the ESD performance of the clamp. Low power consumption may be defined as being negligible compared to the overall power consumption of the clamp. Strong current drive must be measured by its ability to drive large loads while keeping the bias voltage on target. On the other hand, limited degradation of ESD performance should be proven by a negligible shift in the pulse current-voltage characteristics of the clamp under various operating conditions.

Fig. 2 illustrates an exemplary prior art implementation of a voltage tolerant clamp circuit 20. The clamp circuit 20 includes a voltage divider 22 formed by devices 24 and 26 between nodes 28 and 30, a controller circuit 32 including, among other devices, a device 34, and a current sinking device 36 having current sinking device transistors 38 and 40. The transistors 38 and 40 used by the current sinking device 36 may be any of the

commonly used transistors. For example, the transistors 38 and 40 of the exemplary implementation of the current sinking device 36 are p-Channel transistors.

A voltage divider of a clamp circuit, such as the voltage divider 22, generates a bias voltage or a reference voltage, and therefore, is also referred to as a reference voltage generator or a bias voltage generator. As shown in Fig. 2, the simple voltage divider 22 of the prior art is used to reduce the high supply voltage on the node 28 to a smaller voltage on the node 30. For the clamp circuit 20, the major load on the voltage divider 22 is the sub-threshold leakage through the n-channel device 34. For a resistive voltage divider, this load should be small compared to the current consumption of the divider itself in order to maintain good voltage division. This requirement is relaxed in the case of the voltage divider 22, where diode-connected p-channel devices 24 and 26 with non-linear current-voltage characteristics are used instead of resistive elements. Reasonable voltage division can be achieved when the current consumption of the voltage divider 22, defined as the current through device 26 is comparable or even less than the current consumption of a load. Because the device 34 is usually much smaller than the devices 24 and 26, and because the current consumption of the voltage divider 22 is comparable to the leakage through the device 34, the voltage divider 22 can be optimized to consume leakage current that is small compared to the total clamp leakage.

The controller circuit 32 is coupled to a control node of the current sinking device 36 such that the controller circuit 32 couples the control node to a ground potential such that a voltage drop from the control node to the ground potential is less than a threshold voltage of an n-channel transistor, such as the controller transistor 34, during an ESD event on the power supply connection 28. The operation of the controller circuit 32 is explained in further detail in U.S. Patent No. 5,956,219, which is incorporated herein in its entirety.

One of the problems associated with using the clamp circuit 20 is that the leakage of the voltage divider 22 can only be optimized based on a particular loading condition. Whereas the sub-threshold leakage of the device 34 is a strong function of temperature and other process variation, these changes do not affect the devices in the voltage divider 22 to the same extent. In order to assure satisfactory voltage division across all reasonable usage conditions, the current drive of the voltage divider 22 has to increase to meet the

worst case conditions of changes in room temperature, fast process skew, etc. Unfortunately, this may result in significant over-design, which may force current consumption of the voltage divider 22 to become a significant portion of the total clamp leakage under typical operating conditions.

Similarly, it is also desirable to have an improved voltage generation sub-circuit for overall reduction of power consumption of a clamp circuit. A prior art clamp circuit 50 disclosed in Fig. 3 attempts to address this problem by using a low-leakage voltage divider 52 buffered by an analog voltage follower 54 and followed by a controller circuit 56. In the clamp circuit 50, the voltage follower 54 provides low output resistance to drive the leakage through the controller device 58, and furthermore presents only a small load to the voltage divider 52, such that the current consumption of the voltage divider can afford to stay low. Unfortunately, for the voltage follower 54 to work effectively, the input and the output of the voltage follower 54 must differ by one threshold voltage plus an unspecified amount of voltage necessary to turn on one of the transistors in the voltage follower 54. As a result it is difficult to generate highly precise bias voltage using the clamp circuit 50. This is an increasingly important problem with the advances in circuit technology because, as the maximum voltage that transistors in ICs can withstand decreases with each process generation, precision in the voltage reference becomes more critical.

To address the above problems, it is desirable to provide an improved ESD clamp circuit where the internal bias voltage of the clamp tracks the power supply accurately over the entire range of process variations and where the clamp operates with minimal leakage current over a wide range of operating conditions.

BRIEF DESCRIPTION OF THE DRAWINGS

The present patent is illustrated by way of examples and not limitations in the accompanying figures, in which like references indicate similar elements, and in which:

Fig. 1 illustrates a block diagram of an exemplary integrated circuit;

Fig. 2 illustrates an exemplary prior art implementation of a voltage tolerant clamp circuit;

Fig. 3 illustrates another exemplary prior art implementation of a voltage tolerant clamp circuit;

Fig. 4 illustrates a block diagram of a two-stack clamp circuit with improved bias voltage generation;

Fig. 5 illustrates an exemplary circuit diagram of the two-stack clamp circuit of Fig. 4;

Fig. 6 illustrates a simulated pulsed current-voltage characteristic of the clamp circuit of Fig. 5;

Fig. 7 illustrates an exemplary circuit diagram of a two-stack clamp circuit with complementary self-biased differential amplifier;

Fig. 8 illustrates an exemplary circuit diagram of a three-stack clamp circuit with improved bias voltage generation;

Fig. 9 illustrates an exemplary circuit diagram of a two-stack clamp circuit with a gate-leakage-diverting resistor;

Fig. 10 illustrates an exemplary circuit diagram of a two-stack voltage tolerant clamp circuit with gate leakage-diverting pass gate;

Fig. 11 illustrates an exemplary circuit diagram of a two-stack voltage tolerant clamp circuit with gate leakage-diverting PMOS; and

Fig. 12 illustrates an exemplary circuit diagram of a three-stack voltage tolerant clamp circuit with gate leakage-diverting PFETs .

DETAILED DESCRIPTION OF THE EXAMPLES

In the following detailed description of numerous different embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments by which the present patent may be implemented. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the present patent. Other embodiments may be utilized and structural, logical and electrical changes may be made without departing from the scope of the present patent. The following detailed description is therefore, not to be

taken n a limiting sense and the scope of the present patent is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

An embodiment of the present patent illustrates a two-stack ESD clamp circuit having a differential amplifier for providing improved bias voltage. Specifically, the ESD clamp circuit includes a voltage divider, a differential amplifier, a voltage follower, a control circuit and a sinking circuit. The differential amplifier is able to set a required voltage drop across the voltage follower through a negative feedback. Thus, the gain of the differential amplifier tends to drive up the voltage follower input until the two inputs of the differential amplifier are at the same potential.

An alternate embodiment of the present patent illustrates a multi-stack ESD clamp circuit having a differential amplifier for providing improved bias voltage.

Yet another embodiment of the present patent illustrates a two-stack clamp circuit having a resistor connecting a drain of a first transistor device within a current sinking circuit of the clamp circuit with a gate of a second transistor device within the current sinking circuit, wherein the resistor allows reducing the current load on the drain of the second transistor.

Another embodiment of the present patent illustrates a two-stack clamp circuit having a pass-FET connecting a drain of a first transistor device within a current sinking circuit of the clamp circuit with a gate of a second transistor device within the current sinking circuit, wherein the pass-FET allows reducing the current load on the drain of the second transistor.

Yet another embodiment of the present patent illustrates a two-stack clamp circuit having a grounded-gate p-channel FET connecting a drain of a first transistor device within a current sinking circuit of the clamp circuit with a gate of a second transistor device within the current sinking circuit, wherein the p-channel FET allows reducing the current load on the drain of a second transistor within the current sinking circuit.

Now referring to the accompanying figures, Fig. 4 illustrates a block diagram of an exemplary two-stack clamp circuit 100 with improved bias voltage generation. The clamp circuit 100 includes a voltage divider 102, connected via a differential amplifier 104 to a

voltage follower 106, which in turn is connected to a controller circuit 108 controlling a current sinking device 110. A specific implementation of the two-stack clamp circuit 100 is illustrated in further detail in Fig. 5.

Specifically referring to Fig. 5, the voltage divider 102 is a low-leakage voltage divider that includes series transistors 112 to 122, and is connected to voltage supply via a pass gate transistor 124. The voltage divider 102 provides a reference or bias voltage to the differential amplifier 104 at a bias point 126.

The differential amplifier 104 includes transistors 130 to 138. The differential amplifier 104 tends to drive up the input to the voltage follower 106 until inputs to the transistors 134 and 136 are at the same potential. Thus the differential amplifier 104 sets a required voltage drop across the voltage follower 106 through negative feedback. Generally the voltage divider 102 and the voltage follower 106 require only a small amount of leakage current, therefore, to keep the overall current consumption of the clamp circuit 100 to a low amount, it is necessary that the current consumption of the differential amplifier 104 is also kept to a low level.

The two-stack clamp circuit 100 achieves a low level current through the differential amplifier 104 by biasing the gate of the transistor 138 at a low voltage. The low bias voltage at the gate of the transistor 138 can be taken from any of the various nodes provided by the transistors 112 to 122 of the voltage divider 102. To ensure that the loading in the transistor 138 caused by the gate leakage does not disturb the voltage reference provided by the voltage divider 102, the transistor 138 can be made of a relatively small size. The lower amount of current through the differential amplifier 104 also reduces the speed of the differential amplifier 104. Moreover, the differential amplifier 104 only needs to provide a DC voltage reference, therefore, the reduction in switching speed of the differential amplifier 104 is generally not a concern. However, the gain of the differential amplifier 104 affects the precision of the voltage reference provided by the differential amplifier 104, therefore, the gain of the differential amplifier 104 is a main target of optimization. Through various simulations, it has been shown that an acceptable level of gain for the differential amplifier 104 can be achieved at levels that are small compared to the total clamp leakage of the clamp circuit 100.

Due to the use of the differential amplifier 104, the current drive of the bias voltage generator has a very wide range, generally much higher than the traditional clamping circuits disclosed above in figures 2 and 3. When the load at the output of the voltage follower 106 is excessive, for example under burn-in conditions, the input voltage to the voltage follower 106 can float to as high as the output of the differential amplifier 104 can allow. On the other hand, under conditions that result in low leakage, such as low temperature or slow process corner, the input voltage to the voltage follower 106 can also float back to a lower level. Such flexibility in the input voltage to the voltage follower 106 is as a result of the use of the differential amplifier 104. The traditional clamping circuits of Figs. 2-3 do not provide such flexibility. Thus the use of the differential amplifier 104 allows the clamping circuit 100 to provide an accurate voltage reference under a diverse range of operating conditions.

The voltage follower 106 is made of transistors 140-144 and is connected to the supply 146 via a variable resistor 148. Whereas, the controller 108 is made of a number of transistors 150-164 and a resistor (not shown in Fig. 5). Finally the current sinking device 110 includes transistors 170 and 172. Design of the differential amplifier 104, the voltage follower 106 and the controller 108 is well-known to those of ordinary skill in the art and therefore is not discussed here in further detail.

To ensure that the addition of the differential amplifier 104 does not have a negative effect on the functionality of the clamping circuit 100, it is important to make sure that the tendency of the voltage follower transistor 140 to impose a reference voltage on the mid-node 180 does not overcome the ability of the controller transistor 164 to turn on the transistor 172 of the ESD clamping 110. This is accomplished by making the channel width of the voltage follower transistor 140 small compared to the channel width of the controller transistor 164, so that the controller transistor 164 is always able to turn on the current sinking device transistor 172. As a result, during steady state and normal operation, the controller transistor 164 is off and the voltage follower transistor 142 is in control.

An alternate solution for reducing the strength of the voltage follower transistor 140 during an ESD event is using the pass gate transistor 124 at the top of the voltage divider 102, which can be turned off during an ESD event such that the gate voltage on the

differential amplifier transistor 136 is reduced. Yet another embodiment of the clamping circuit 100 may have a capacitor connected between the gate of the differential amplifier transistor 136 and ground such that the gate voltage of the differential amplifier transistor 136 stays low throughout an ESD event.

In each of the various embodiment discussed above, it is required that any of the changes above does not affect the performance of the clamping circuit 100 during an ESD. Results of simulations for the embodiment of the clamping circuit 100 illustrated in Fig. 5 are illustrated in the graph 200 shown in Fig. 6. Specifically the graph 200 depicts the relationship between the clamp voltage and clamp current for a clamping circuit with the differential amplifier (modified clamp) and without the differential amplifier (unmodified clamp). As it can be seen by the graph 200, there is no deterioration in the performance of the clamp circuit 100 having the differential amplifier 104 as compared to a clamp circuit without a differential amplifier.

Results of simulations, including voltage at the mid-node 180, oxide lifetime of the clamping circuit 100 and leakage data for the clamping circuit 100 under various operating conditions show that the clamping circuit 100 clearly offers greater control over the voltage at the mid-node 180 across a wide range of operating conditions, including under conditions of high-voltage and high temperature. For example, under operating conditions having a voltage of 3.08 V and temperature of 125° C, the clamping circuit 100 results in a deviation of only 21.5 mV, compared to much higher deviations of 158.7 mV and 106 mV for the clamping circuits 20 and 50, respectively. The lower deviation of mid-node voltage allows performing time-to-failure studies for the clamping circuit 100 with higher accuracy.

Similarly, simulation results also show that on tope of the advantage of the better control over the mid-node voltage, while the worst case oxide lifetimes of the clamping circuits 20 and 50 are only about 7 years, the worst case oxide lifetime of the clamping circuit 100 is close to 51 years. The increased worst case oxide lifetime also provides increased safety margin for the operation of the clamping circuit 100.

Moreover, the clamping circuit 20, even when highly leakage-optimized so as to have only about seven years of lifetime, has a significantly higher leakage than the clamping circuit 100. Simulation results also show that while the clamping circuit 50 may

give slightly lower clamp current than the clamping circuit 100, the clamping circuit 50 fails the crucial criteria of providing an accurate and stable voltage reference. Note that at higher temperatures, the improvement in the leakage current, between the clamping circuits 20 and 100, is less pronounced. This reduced improvement results because at higher temperatures, the leakage of the current sinking transistors 38 and 40 of the clamping circuit 20 dominates the leakage of the voltage divider 22, whereas the leakage of the transistors 170 and 172 of the clamping circuit 100 dominates the leakage of the voltage divider 102.

However, for leakage sensitive application, such as battery operated real-time clock service, etc., minimizing the leakage at the room temperatures is often necessary in order to meet product specifications, and the clamping circuit 100 provides more flexibility in meeting such requirements. Furthermore, as shown in tables 1 and 2, the clamping circuits 20 and 50 are highly vulnerable to process changes, whereas the clamping circuit 100 is less sensitive in this regard, such that the clamping circuit 100 designed for high performance 90 nm process can also be used in a low power 90 nm process. On the other hand, while the clamping circuit 20 that is designed for the high performance 90 nm process can be used for a low power 90 nm process, in this case the voltage divider 22 of the clamping circuit 20 will be highly over-designed when used in a low–leakage process such as a low power 90 nm process. Moreover, a process change that increases transistor leakage and/or reduces the current drive in a voltage divider results in reduced oxide lifetimes for clamping circuits 20 and 50. Compared to that, the clamping circuit 100 having a stronger voltage reference has a much better chance of surviving routine process changes.

While the above implementation of the clamping circuit 100 uses a simple active-load differential amplifier 104 as a gain element, any other style of differential amplifier that offers a high gain and low leakage can be used. Fig. 7 illustrates an example of a clamping circuit 220 using a complementary self-biased differential amplifier 222 connected between the voltage divider 102 and the voltage follower 106. Note that other types of differential amplifiers, such as cascaded amplifier, etc., also can be used to increase the gain.

While the different implementations of clamping circuits 20, 50, 100 and 220 illustrated in Figs. 2, 3, 5 and 7 use a two stack clamp, such as the current sinking device 110, these clamping circuits can be easily generalized using multi-stack current sinking devices. As an example, Fig. 8 discloses a clamping circuit 240 having a three stack current sinking device 242 and a bias voltage generator 244, where the bias voltage generator 244 includes a common voltage divider 246, a first differential amplifier 248 along with a first voltage follower 250 that provides bias voltage to one stack and a second differential amplifier 252 along with a second voltage follower 254 that provides bias voltage to another stack of the three stack current sinking device 242. The clamping circuit 240 also includes a controller circuit 256 that connects the first voltage follower 250 and the second voltage follower 254 to the three stack current sinking device 242.

The descriptions of the clamping circuits 20, 50, 100, 220 and 240 illustrated in Figs. 2, 3, 5, 7 and 8 are made in the context of a 180 nm technology devices. Starting with an 130 nm technology devices, which is increasingly popular in the industry, the phenomenon of gate leakage has become significant. Generally, gate leakage can be described as the leakage between the gate and drain of a transistor device due to high electric field under the gate and drain overlap region of transistor device, which results in a band-to-band tunneling effect. It has been projected that the gate leakage effect in integrated circuit devices will become comparable to sub-threshold leakage in the near future.

In light of such a possibility, it is necessary to re-analyze the circuits described above to reconsider the effects of the gate leakage current on the current load that the bias voltage generators of clamping circuits need to handle. For example, considering the clamping circuit 20 of Fig. 2, the largest new addition to the current load on the voltage divider 22 is the gate-to-source leakage through the current sinking transistor 40, which adds to the existing sub-threshold leakage of the controller transistor 34. If the gate leakages of each of the transistors 34 and 40 are comparable to their sub-threshold leakages, because of the considerably larger size of the current sinking transistor 40 compared to the controller transistor 34, the gate current through the current sinking transistor 40 will in fact dwarf the leakage through the controller transistor 34. There are also the gate leakages through the control transistors 34 and 42 that affect the current load,

however, they are small compared to the gate leakage of the device 40, again due to the relatively larger size of the current sinking transistor 40. Each of these gate leakages will increase the current drive requirement of the voltage divider 22, much of which is used unproductively by the device 26 of the voltage divider 22.

Furthermore, while the gate leakage of the current sinking transistor 40 is spread across a larger device, the same amount of current, plus the unproductive current through the device 26, all need to go through the relatively small device 24. The resultant density of the current through the device 24 may be high enough to require a designer of the voltage divider 22 to consider electro-migration and other long term reliability issues. The high gate leakage of the current sinking transistor 40 along with the gate leakages of the controller transistors 34 and 42 puts a great strain on simple voltage dividers such as the voltage divider 22. Therefore, a stronger voltage reference, such as the voltage divider 102 of the Fig. 5, is desired.

While there is a large amount of gate-to-drain current through the current sinking transistor 40, there is also a similar amount of gate-to-drain current leakage through the current sinking transistor 38. Thus the drain of the current sinking transistor 40 supports not only the sub-threshold leakage of the current sinking transistor 40, but two doses of gate-to-drain leakage currents, namely those of the current sinking transistor 38 and the current sinking transistor 40. Thus, if one were to be able to direct the gate-to-drain leakage current of the current sinking transistor 38 to the gate of the current sinking transistor 40, then the drain of the current sinking transistor 40 will only need to support the sub-threshold leakage of only one dose of gate-to-drain leakage, namely that of the current sinking transistor 40. This can be done in practice by connecting either a resistor or a pass-FET between the drain of the current sinking transistor 38 and the gate of the current sinking transistor 40.

Fig. 9 shows an alternate implementation of a clamping circuit 270 with a voltage divider 272, a differential amplifier 274, a voltage follower 276, a control circuit 278, and a current sinking device 280, wherein the current sinking device 280 includes a current sinking transistor 282 and a current sinking transistor 284, wherein a resistor 286 is connected between the drain of the current sinking transistor 282 and the gate of the current sinking transistor 284. The resistor 286 allows directing the gate-to-drain leakage

current of the current sinking transistor 282 towards the gate of the current sinking transistor 284, thus reducing the current load on the drain of the current sinking transistor 284.

Fig. 10 shows an alternate implementation of a clamping circuit 300 with a voltage divider 302, a differential amplifier 304, a voltage follower 306, a control circuit 308, and a current sinking device 310, wherein the current sinking device 310 includes a current sinking transistor 312 and a current sinking transistor 314 with a pass-FET 316 is connected between the drain of the current sinking transistor 312 and the gate of the current sinking transistor 314. The pass-FET 316 allows directing the gate-to-drain leakage current of the current sinking transistor 312 towards the gate of the current sinking transistor 314, thus reducing the current load on the drain of the current sinking transistor 314.

Fig. 11 shows an alternate implementation of a clamping circuit 330 with a voltage divider 332, a differential amplifier 334, a voltage follower 336, a control circuit 338, and a current sinking device 340, wherein the current sinking device 340 includes a current sinking transistor 342 and a current sinking transistor 344. The clamping circuit 330 has a p-channel FET 346 connected between the drain of the current sinking transistor 342 and the gate of the current sinking transistor 344, wherein the gate of the p-channel FET 346 is connected either to the drain of the controller transistor 348, or to ground. The p-channel FET 346 allows directing the gate-to-drain leakage current of the current sinking transistor 342 towards the gate of the current sinking transistor 344, thus reducing the current load on the drain of the current sinking transistor 344.

The n-channel device 316, as used in the clamping circuit 300, may be susceptible to destruction or lapsing into a high-current state during snap-back. Compared to that, when using the grounded-gate p-channel FET 346 as in the clamping circuit 330, the grounded-gate p-channel FET 346 should be set in such a way that it is much weaker than the controller transistor 348. This ensures that the controller transistor 348 can overcome the grounded-gate p-channel FET 346 when the resulting clamping circuit is operating in an ESD mode. On the other hand, when the n-channel device 316 is employed as in the clamping circuit 300, it can be turned off during an ESD event, which allows using an n-channel device of arbitrary strength.

The various solutions employed to address the problem of the gate-to-drain leakage current, as shown by the clamping circuits 270, 300 and 330, also provide a very welcome benefit of reducing the load on the respective bias-voltage generators 272, 302 and 332. This is as a result of supplying the gate leakage of the current sinking transistors 284, 314 and 344 via the current sinking transistors 282, 312 and 342, respectively, instead of via the respective voltage references of each of these clamping circuits.

The solutions described above are generally optimized for gate leakage so that the entire amount of the gate current through the current sinking transistors 282, 312 and 342 is diverted to the gate of the current sinking transistors 284, 314 and 344, respectively. However, because the gate-to-source voltage of the current sinking transistors 284, 314 and 344 is non-zero due to body effect, if each of the pairs 282 and 284, 312 and 314, and 342 and 344 are contained in the same well, then it is possible to divert more than optimized current to the current sinking transistors 284, 314 and 344. As a result an overshooting results in a decrease in the gate leakage and an increase in the sub-threshold leakage for the current sinking transistors 284, 314 and 344, and depending on the ratio of the gate leakage current and the sub-threshold leakage of the technology used, the solutions described above may or may not result in current savings. Nonetheless, the benefit of reducing the load on the voltage references 272, 302 and 332 as described above still stands.

In an alternate scenario, where each of the pairs 282 and 284, 312 and 314, and 342 and 344 are contained in different wells with bulk shorted to the source of each of the current sinking transistors, the sub-threshold leakages will be minimized when gate-to-source voltages of the current sinking transistors 274, 304 and 334 are zero. In this scenario, the solutions described above will only have beneficial effects for circuits 270, 300 and 330.

Simulation results have shown that the addition of the pass-FET 316, as shown in Figl 10, reduces the current load on the voltage reference 302 by a significant amount. This is because the pass-FET 316 provides most of the gate current through the current sinking transistor 314.

While the strongest justification for incorporating the pass-FET 316 in the clamping circuit 300 or the resistor 286 in the clamping circuit 270 lies in the increased

accuracy of and reduced reliability concerns for the voltage references of the respective clamping circuits 300 and 270, these changes also result in reduced overall current. For example, simulation results have shown that the reduction in the total current in the clamping circuit 300 as a result of using the pass-FET 316 is in the order of thirty percent.

As discussed earlier, while the above implementations of clamping circuits 270, 300 and 330 are shown using two-stack current sinking devices 280, 310 and 340, these clamping circuits can also be implemented using multi-stack current sinking devices. Fig. 12 illustrates an implementation of a clamping circuit 360 using a three stack current sinking device 374 using a load reducing technique similar to the one employed in the clamping circuit 300. More specifically the clamping circuit 360 employs a voltage divider 362 that provides a set of voltage references, differential amplifiers 364 and 366, voltage followers 368 and 370, a control circuit 372, and a three stack current sinking device 374. The three-stack current sinking device 374 includes current sinking transistors 376, 378 and 380, wherein a first pass-FET 382 connected between the drain of the current sinking transistor 376 and the gate of the current sinking transistor 378, and a second pass-FET 384 connected between the drain of the current sinking transistor 378 and the gate of the current sinking transistor 380.

Because each of the current sinking transistors 376, 378 and 380 needs its own gate current, the three-stack current sinking device 374 without the proposed pass-FET devices 382 and 384 will need three doses of gate current, whereas the proposed current sinking device 374 with the pass-FET devices 382 and 384 needs only one dose of gate current, resulting in reduction of total clamping load current. As it will be obvious to one of ordinary skill in the art, the benefit of reduced clamp load current can be extrapolated to an n-stack clamping circuit, where instead of n doses of gate current, only one dose of gate current is required in the n-stack current sinking device using pass-FETs to connect drain of first n-1 current sinking transistors to the gates of the following n-1 current sinking transistors.

Although the forgoing text sets forth a detailed description of numerous different embodiments, it should be understood that the scope of the patent is defined by the words of the claims set forth at the end of this patent. The detailed description is to be construed as exemplary only and does not describe every possible embodiment because describing

every possible embodiment would be impractical, if not impossible. Numerous alternative embodiments could be implemented, using either current technology or technology developed after the filing date of this patent, which would still fall within the scope of the claims of this patent.

Thus, many modifications and variations may be made in the techniques and structures described and illustrated herein without departing from the spirit and scope of the present patent. Accordingly, it should be understood that the methods and apparatus described herein are illustrative only and are not limiting upon the scope of the patent.

What is claimed is:

1. A power supply clamp circuit comprising:

a switchable current sinking circuit connected to a power supply node, the switchable current sinking circuit having a plurality of series coupled transistors;

a control circuit connected to a control node of the switchable current sinking circuit, the control circuit adapted to couple the control node to a ground potential such that during an electrostatic discharge event on the power supply node a voltage drop from the control node to the ground potential is less than a threshold voltage of an n-type load transistor within the control circuit;

a voltage divider circuit connected to the power supply node and adapted to provide a reference voltage to the controller circuit;

a voltage follower circuit adapted to to present a low output resistance to the voltage divider circuit and connected to the control circuit at the control node of the switchable current sinking circuit; and

a differential amplifier circuit adapted to to set a required voltage drop across the voltage follower through a negative feedback.

2. A power supply clamp circuit of claim 1, wherein the differential amplifier circuit is a current mirror differential amplifier circuit

3. A power supply clamp circuit of claim 1, wherein the plurality of series coupled transistors are p-type complementary metal oxide semiconductor (CMOS) transistors.

4. A power supply clamp circuit of claim 1, wherein the differential amplifier circuit is a complementary self-biased differential amplifier.

5. A power supply clamp circuit of claim 1, wherein the plurality of series coupled transistors includes a first p-type sinking transistor and a second p-type sinking transistor with the source of the first p-type sinking transistor connected to the power supply node, the drain of the first p-type sinking transistor connected to the source of the second p-type sinking transistor, the drain of the second p-type sinking transistor connected to the ground and the gate of the second p-type sinking transistor being the control node of the switchable current sinking circuit.

6. A power supply clamp circuit of claim 5, wherein the drain of the first p-type sinking transistor is connected to the gate of the second p-type sinking transistor via a resistor.

7. A power supply clamp circuit of claim 5, wherein the drain of the first p-type sinking transistor is connected to the gate of the second p-type sinking transistor via a pas-FET with the gate of the pass-FET connected to the gate of the first p-type sinking transistor.

8. A power supply clamp circuit of claim 5, wherein the drain of the first p-type sinking transistor is connected to the gate of the second p-type sinking transistor via a p-type grounded gate transistor.

9. A power supply clamp circuit of claim 1, wherein the differential amplifier circuit receives a first input from the voltage divider circuit and a second input from the voltage follower circuit, and wherein the differential amplifier is adapted to drive up an input voltage to the voltage follower in a manner so that the first input and the second input to the differential amplifier are at the same potential.

10. A power supply clamp circuit of claim 1, wherein the plurality of series coupled transistors includes a first p-type sinking transistor, a second p-type sinking transistor and a third p-type sinking transistor, and wherein the source of the first p-type sinking transistor is connected to the power supply node, the drain of the first p-type sinking transistor is connected to the source of the second p-type sinking transistor, the drain of the

second p-type sinking transistor connected to the source of the third p-type sinking transistor, the drain of the third p-type sinking transistor connected to the ground and the gate of the third p-type sinking transistor connected to the control node.

11. A power supply clamp circuit of claim 10, wherein the voltage follower circuit comprises a first voltage follower circuit connected between the power supply node and the control node and a second voltage follower circuit connected between the control node and the ground, and wherein the differential amplifier circuit comprises a first differential amplifier circuit to set a first required voltage drop across the first voltage follower circuit and a second differential amplifier circuit to set a second required voltage drop across the second voltage follower circuit.

12. A power supply clamp circuit of claim 11, wherein the first differential amplifier circuit and the second differential amplifier circuit are current mirror differential amplifier circuits.

13. A power supply clamp circuit of claim 11, wherein the drain of the first p-type sinking transistor is connected to the gate of the second p-type sinking transistor via a first pass-FET and the drain of the second p-type sinking transistor is connected to the gate of the third p-type sinking transistor via a second pass-FET and wherein the gate of the first pass-FET is connected to the gate of the first p-type sinking transistor and the gate of the second pass-FET is connected to the gate of the second p-type sinking transistor.

14. A power supply clamp circuit of claim 11, wherein the drain of the first p-type sinking transistor is connected to the gate of the second p-type sinking transistor via a first resistor and the drain of the second p-type sinking transistor is connected to the gate of the third p-type sinking transistor via a second resistor.

15. An integrated circuit assembly comprising:

an integrated circuit connected between a power supply node and a ground node; and

an electrostatic discharge (ESD) protection device connected between the power supply node and the ground node, wherein the ESD protection device includes:

a switchable current sinking circuit connected to the power supply node, the switchable current sinking circuit having a plurality of series coupled transistors,

a control circuit connected to a control node of the switchable current sinking circuit, the control circuit adapted to couple the control node to a ground potential such that during an electrostatic discharge event on the power supply node a voltage drop from the control node to the ground potential is less than a threshold voltage of an n-type load transistor within the control circuit,

a voltage divider circuit connected to the power supply node to provide a reference voltage to the controller circuit,

a voltage follower circuit to present a low output resistance to the voltage divider circuit and connected to the control circuit at the control node of the switchable current sinking circuit, and

a differential amplifier circuit to set a required voltage drop across the voltage follower through a negative feedback.

16. An integrated circuit assembly of claim 15, wherein the differential amplifier circuit is a complementary self-biased differential amplifier.

17. An integrated circuit assembly of claim 15, wherein the switchable current sinking circuit includes a first p-type sinking transistor and a second p-type sinking transistor with the source of the first p-type sinking transistor connected to the power supply node, the drain of the first p-type sinking transistor connected to the source of the second p-type sinking transistor, the drain of the second p-type sinking transistor connected to the ground and the gate of the second p-type sinking transistor being the control node of the switchable current sinking circuit, and wherein the switchable sinking circuit is adapted to provide a

current drain mechanism to drain gate leakage current of the first p-type sinking transistor via gate of the second p-type sinking transistor.

18. An integrated circuit assembly of claim 17, wherein the current drain mechanism is one of (1) a resistor, (2) a pass-FET and (3) a grounded gate p-channel FET.

19. An integrated circuit assembly of claim 15, wherein the switchable current sinking circuit includes three p-type sinking transistors, the voltage follower circuit includes a first voltage follower circuit connected between the power supply node and the control node and a second voltage follower circuit connected between the control node and the ground, and wherein the differential amplifier circuit includes a first differential amplifier to set a first required voltage drop across the first voltage follower circuit and a second differential amplifier circuit to set a second required voltage drop across the second voltage follower circuit.

20. A method of providing electrostatic discharge (ESD) protection to an integrated circuit connected between a power supply node and a ground node by draining the current between the power supply node and the ground node via a switchable current sinking circuit connected to the power supply node, the switchable current sinking circuit having a plurality of series coupled transistors, wherein draining the current between the power supply node and the ground node comprises:

coupling a control node within the switchable current sinking circuit to a ground potential during an ESD event;

dividing the voltage between the power supply node and the ground node using a voltage divider circuit to provide a reference voltage potential to the control circuit;

presenting a low voltage output resistance to the voltage divider circuit by using a voltage follower circuit; and

setting a required voltage drop across the voltage follower circuit by using a differential amplifier circuit.

21. A method of claim 20, further comprising draining gate leakage current from drain of one of a plurality of transistors within switchable current sinking circuit to gate of another of the plurality of transistors via a resistor connected between drain of the one of the plurality of transistors and the gate of the another of the plurality of transistors.

22. A method of claim 20, wherein setting a required voltage drop across the voltage follower circuit includes providing negative feedback to the voltage follower circuit through the differential amplifier circuit.

23. A method of claim 22, wherein providing negative feedback to the voltage follower circuit includes driving up an input to the voltage follower circuit until two inputs to the differential amplifier circuits are at a same potential.

24. A power supply clamp circuit of claim 1, wherein the plurality of series coupled transistors are n-type complementary metal oxide semiconductor (CMOS) transistors.

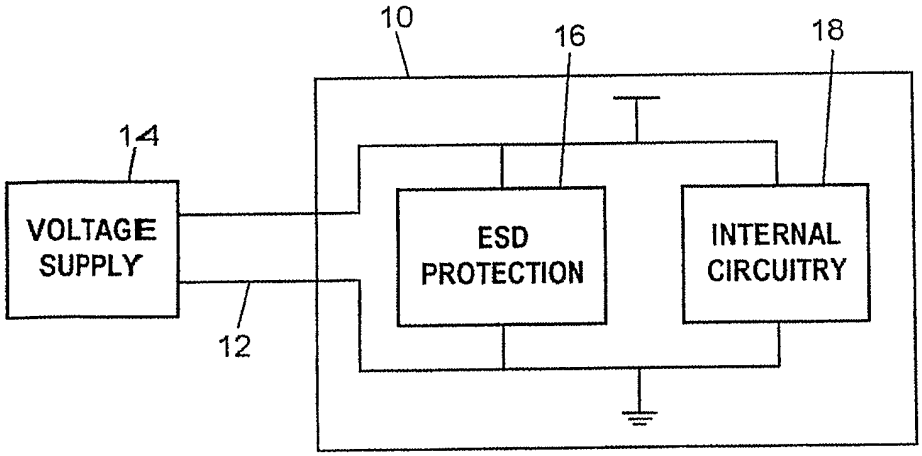
25. A power supply clamp circuit of claim 1, wherein the plurality of series coupled transistors includes a first n-type sinking transistor and a second n-type sinking transistor with the drain of the first n-type sinking transistor connected to the power supply node, the source of the first n-type sinking transistor connected to the drain of the second n-type sinking transistor, the source of the second n-type sinking transistor connected to the ground and the gate of the second n-type sinking transistor being the control node of the switchable current sinking circuit.

26. A power supply clamp circuit of claim 25, wherein the gate of the first n-type sinking transistor is connected to the drain of the second n-type sinking transistor via a resistor.

27. A power supply clamp circuit of claim 25, wherein the gate of the first n-type sinking transistor is connected to the drain of the second n-type sin king transistor via a pass-FET with the gate of the pass-FEt connected to the gate of the second n-type sinking transistor.

28. A power supply clamp circuit of claim 25, wherein the gate of the first n-type sinking transistor is connected to the drain of the second n-type sinking transistor via a n-type transistor having the gate of the n-type transistor connected to the power supply.

FIG. 1
(PRIOR ART)



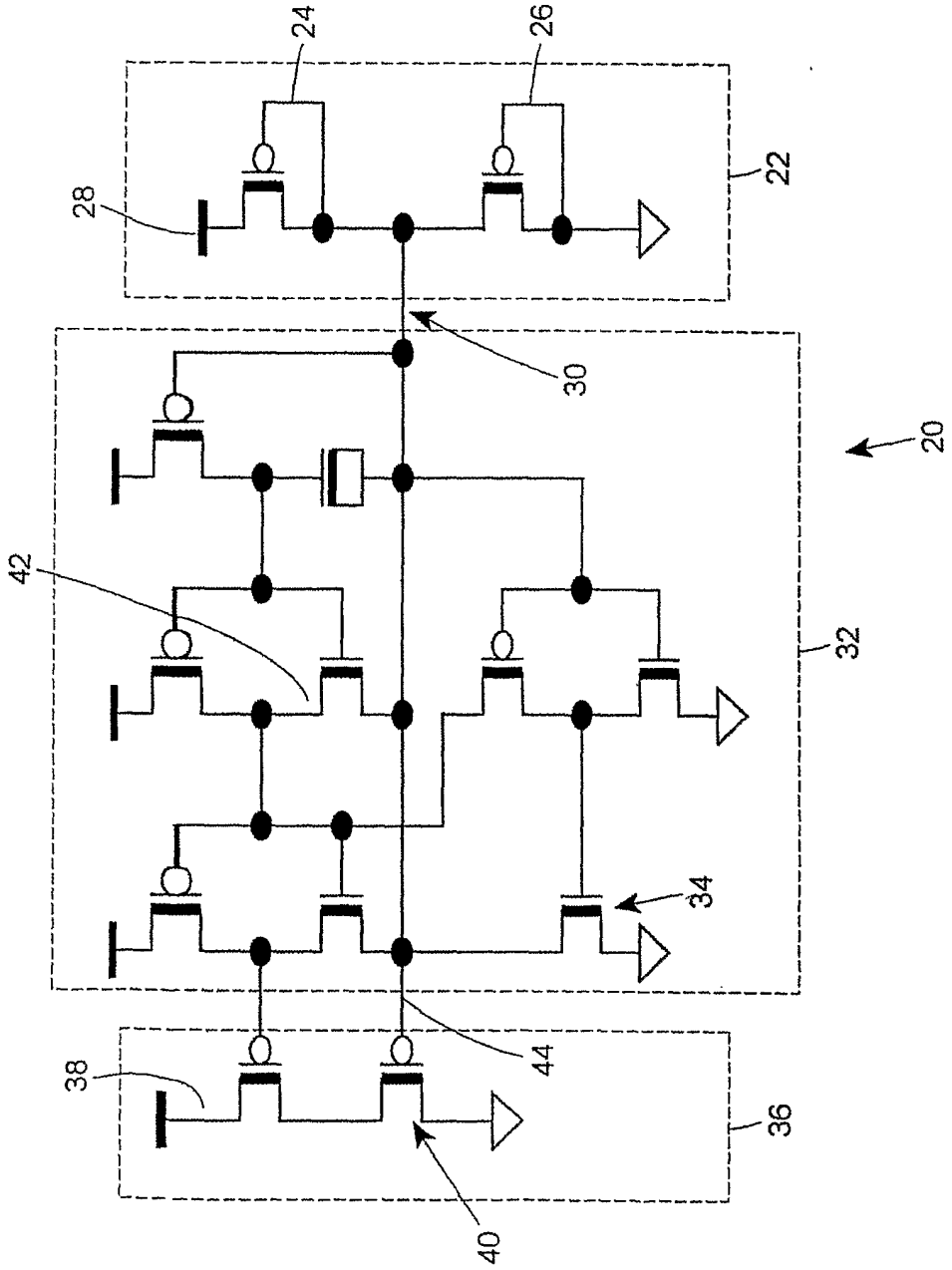


FIG. 2
(PRIOR ART)

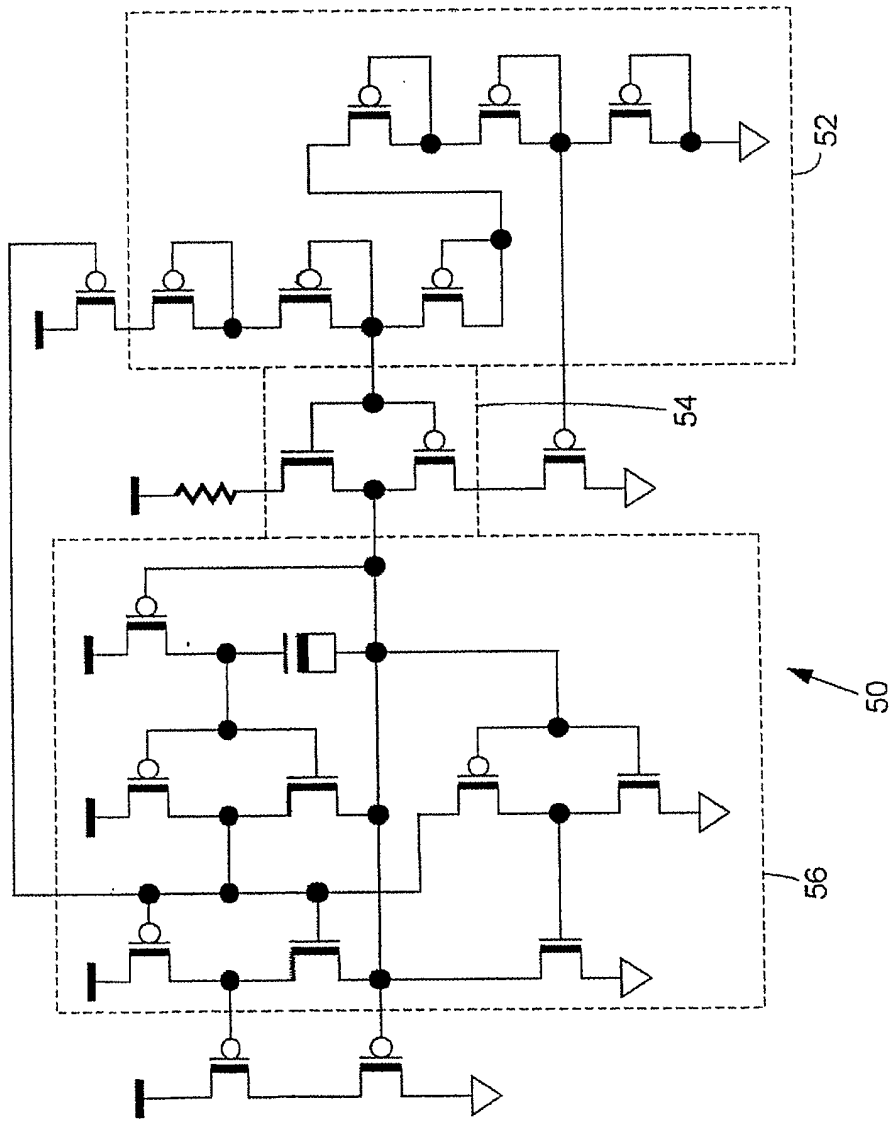


FIG. 3
(PRIOR ART)

FIG. 4

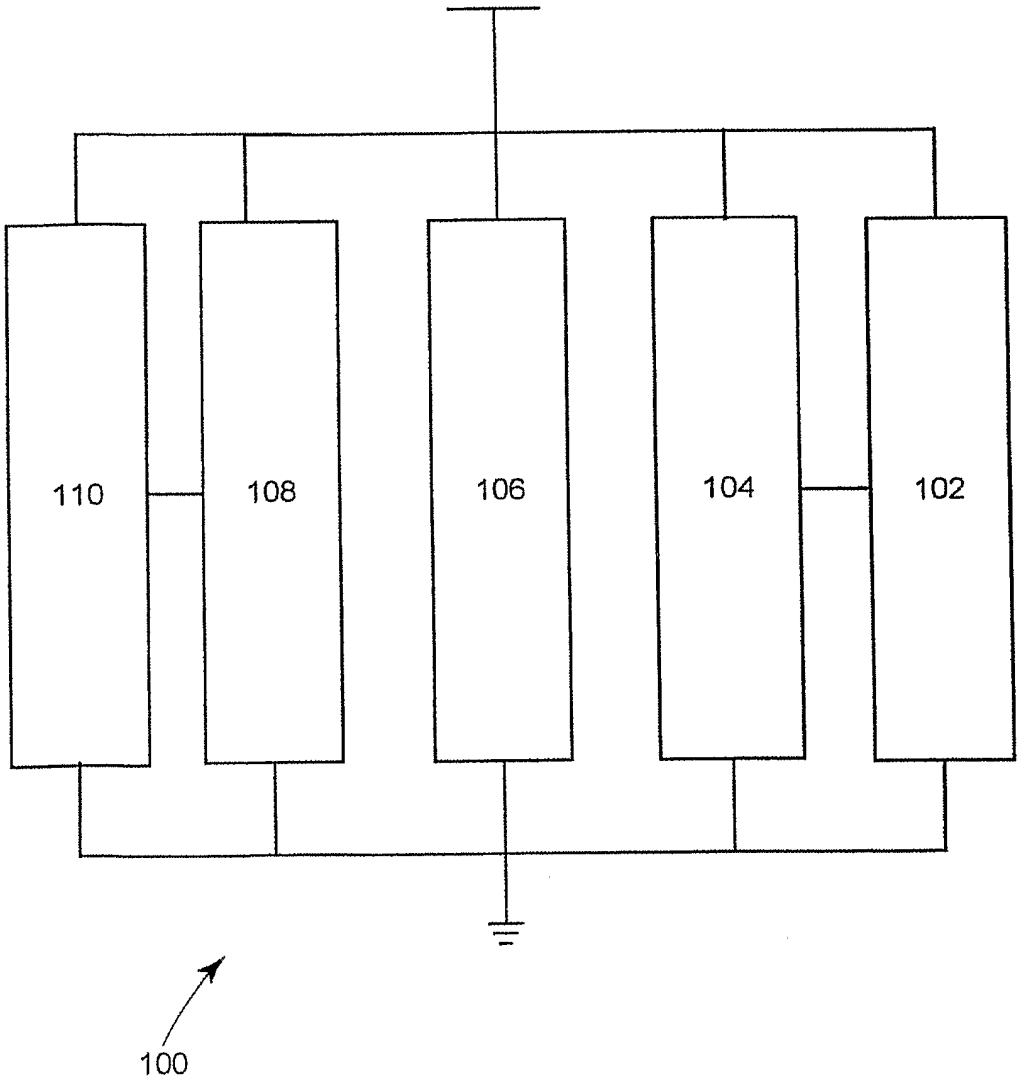


FIG. 5

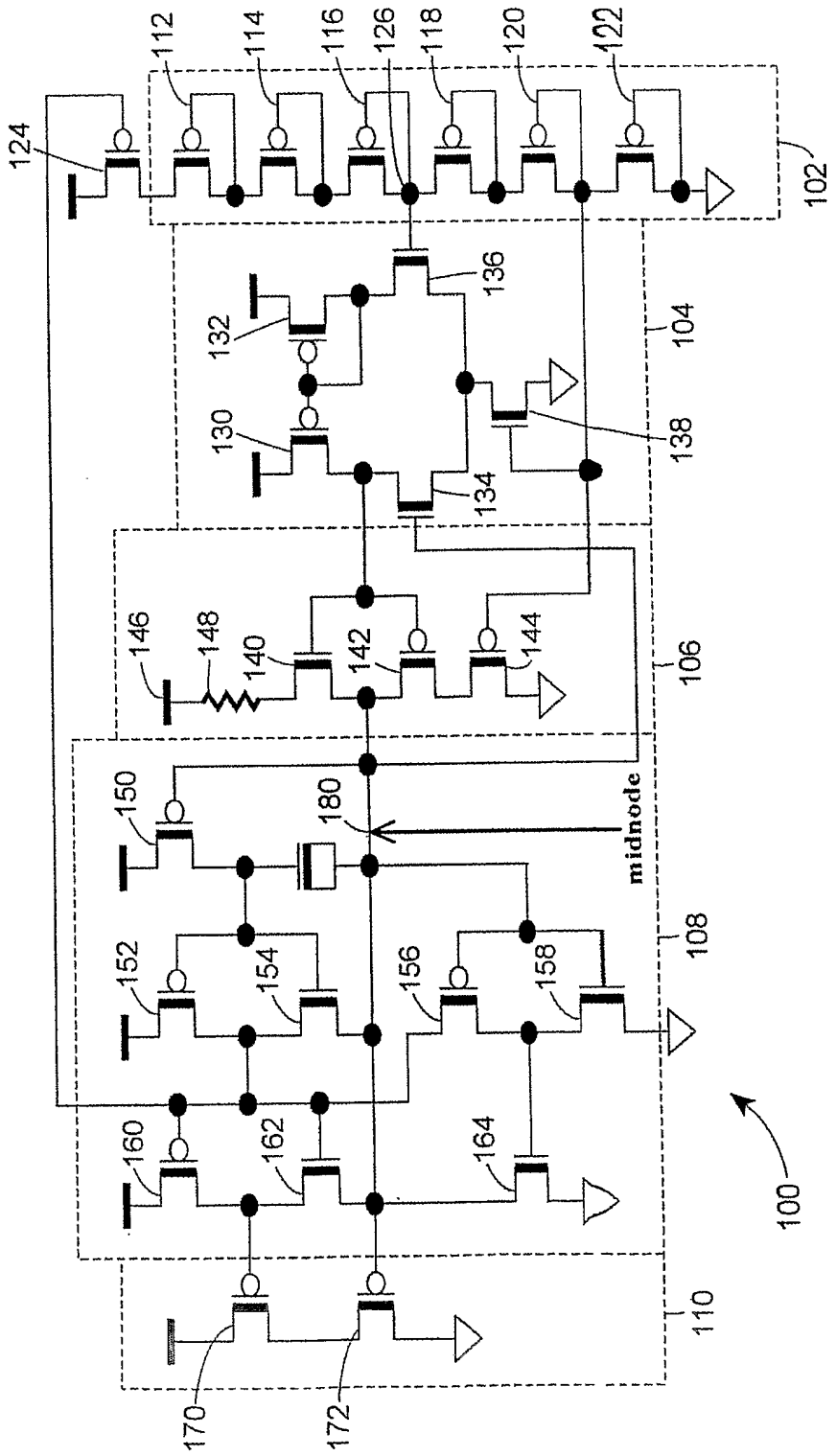

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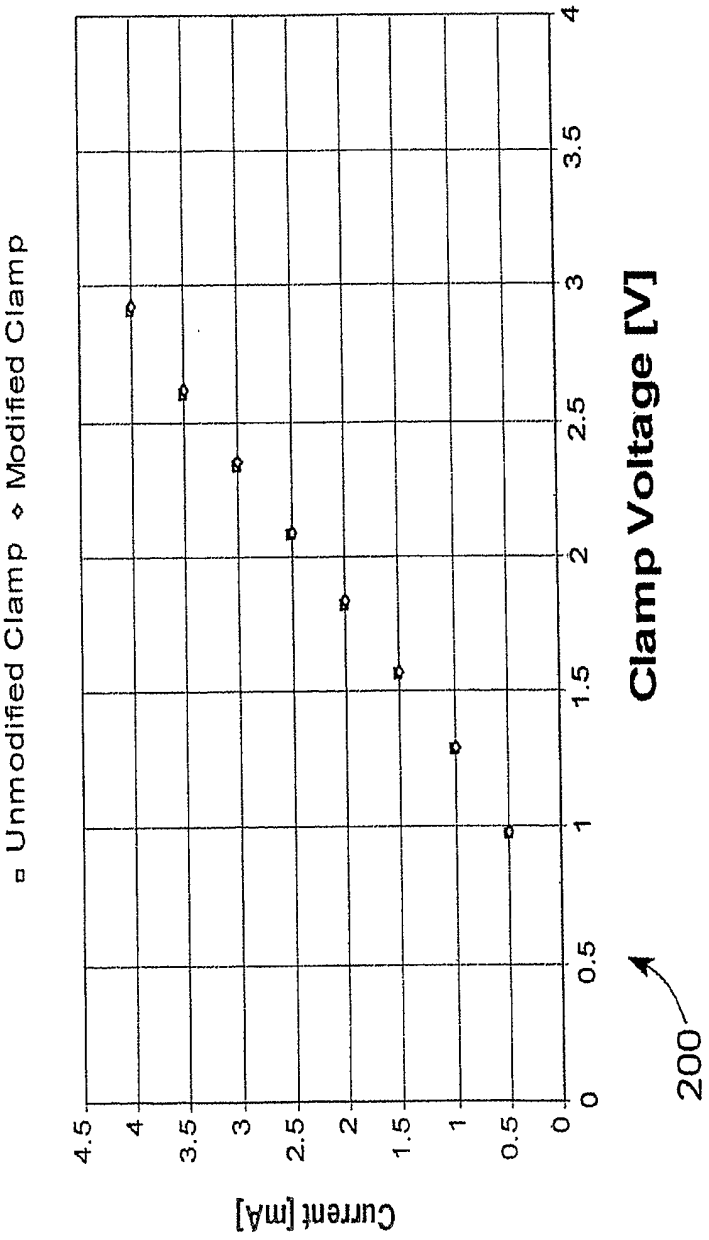
FIG. 6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Modified Clamp
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Clamp Voltage [V]
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1
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2
2.5
3
3.5
4
4.5

FIG. 7

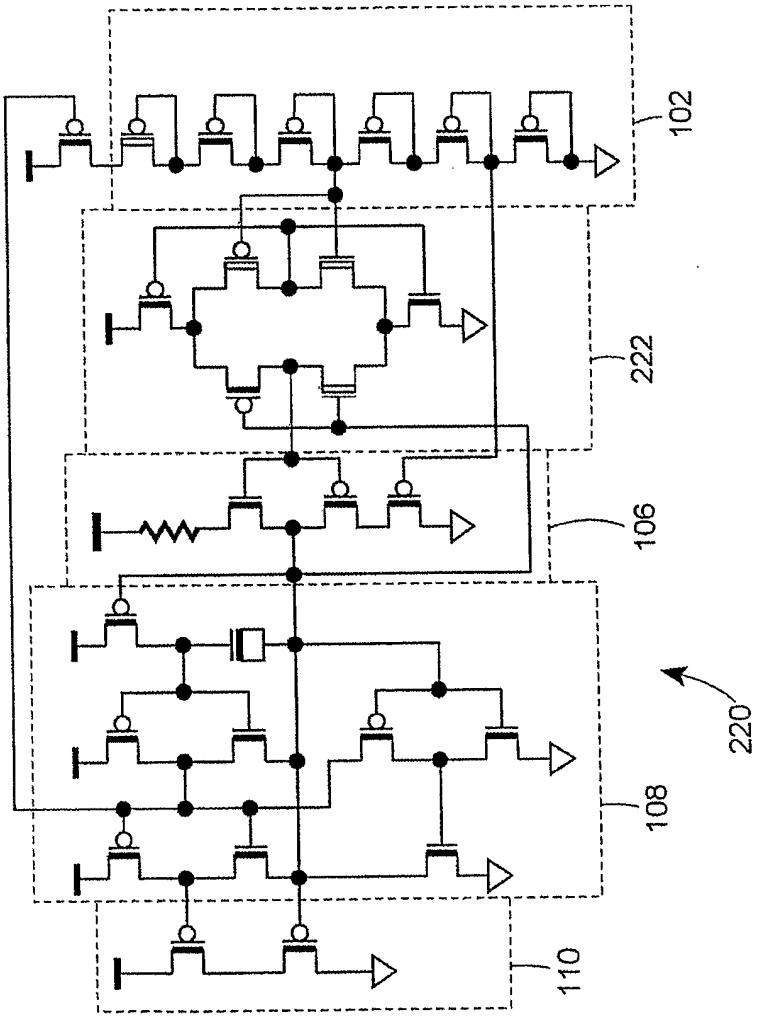


FIG. 8

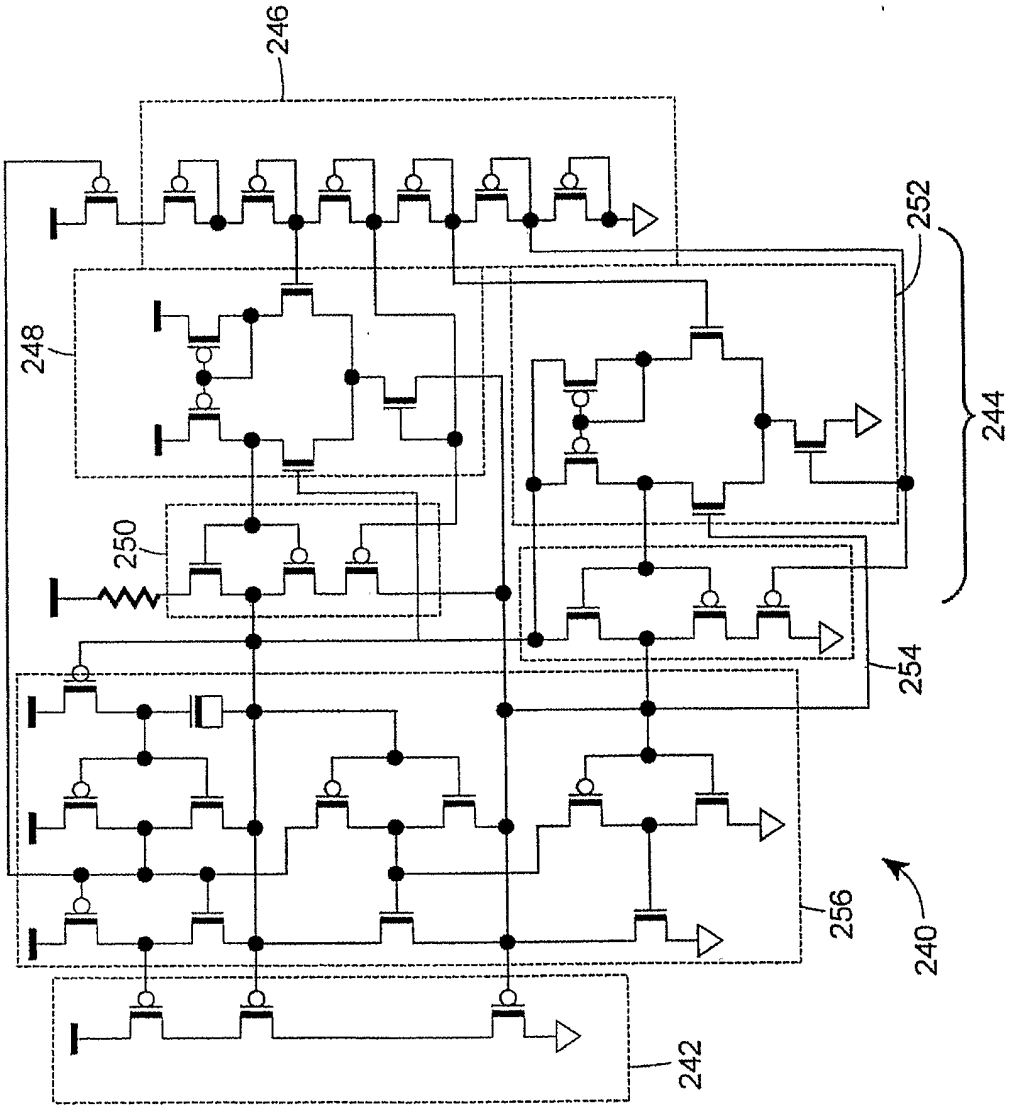


FIG. 9

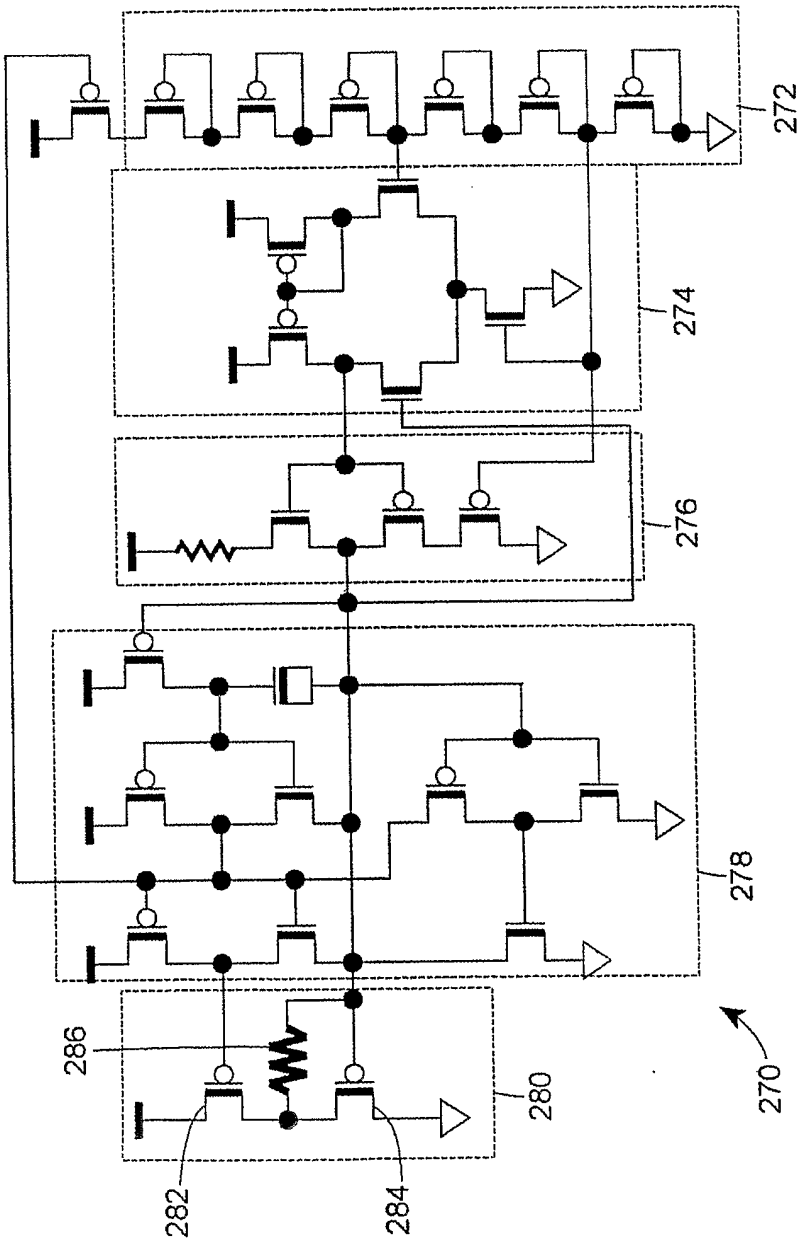


FIG. 10

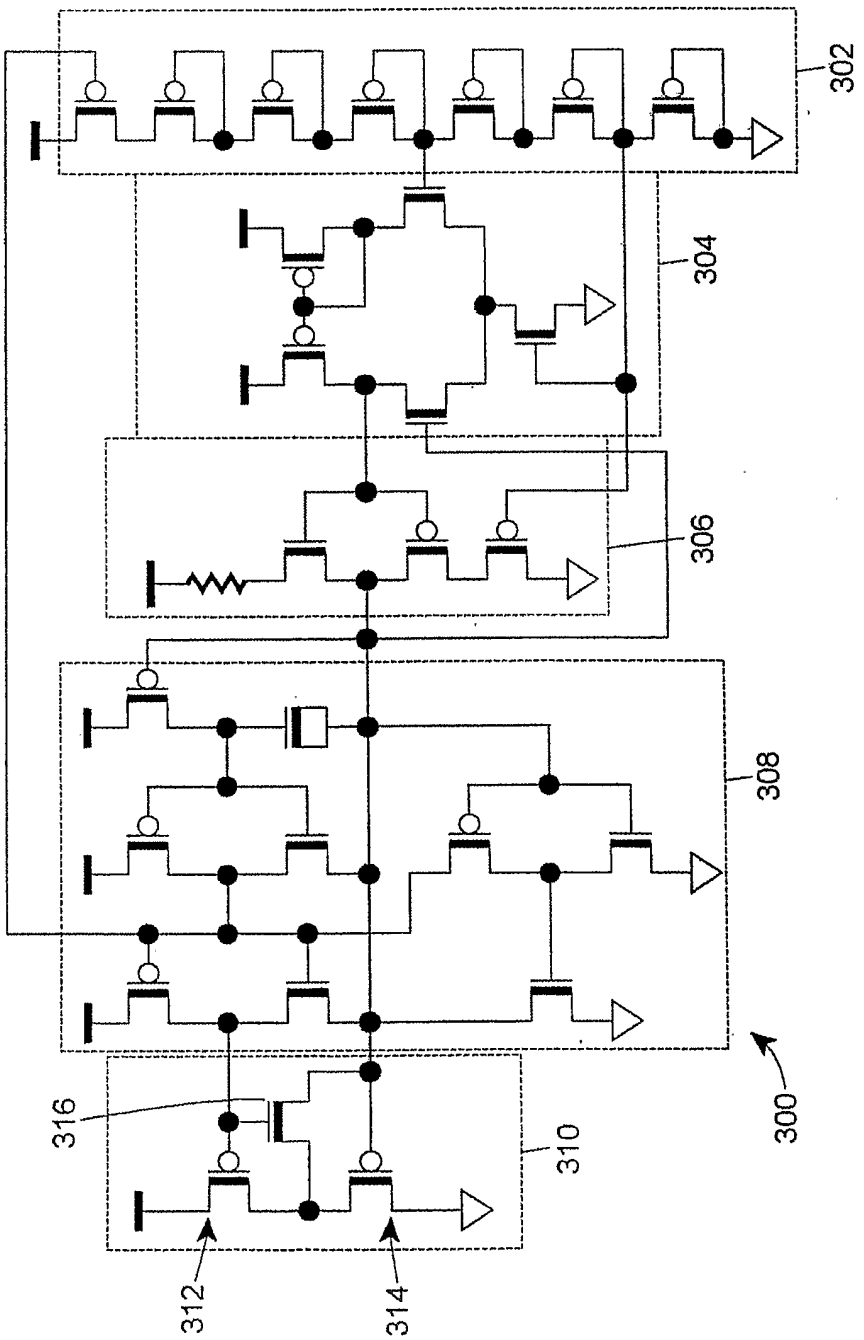


FIG. 11

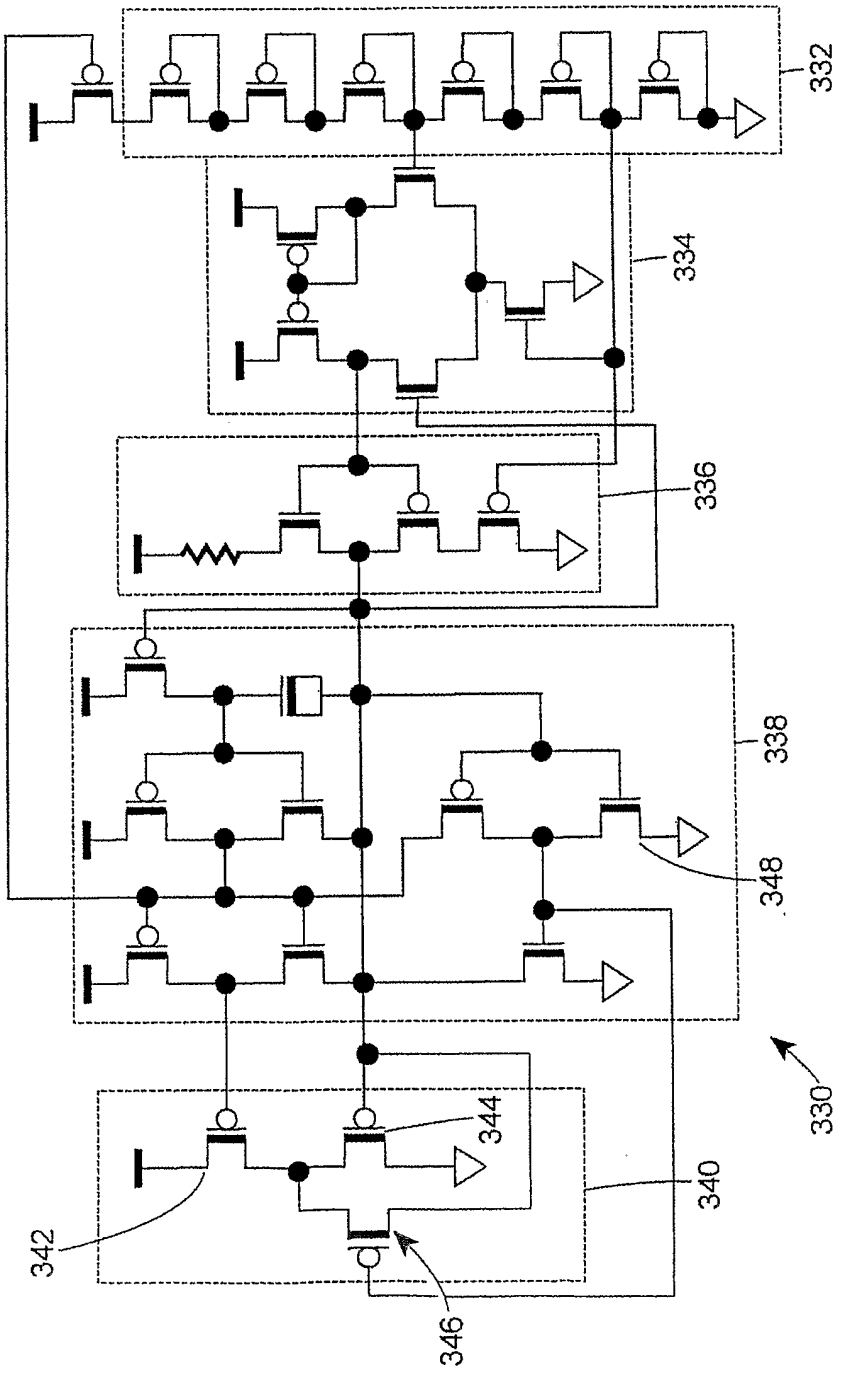
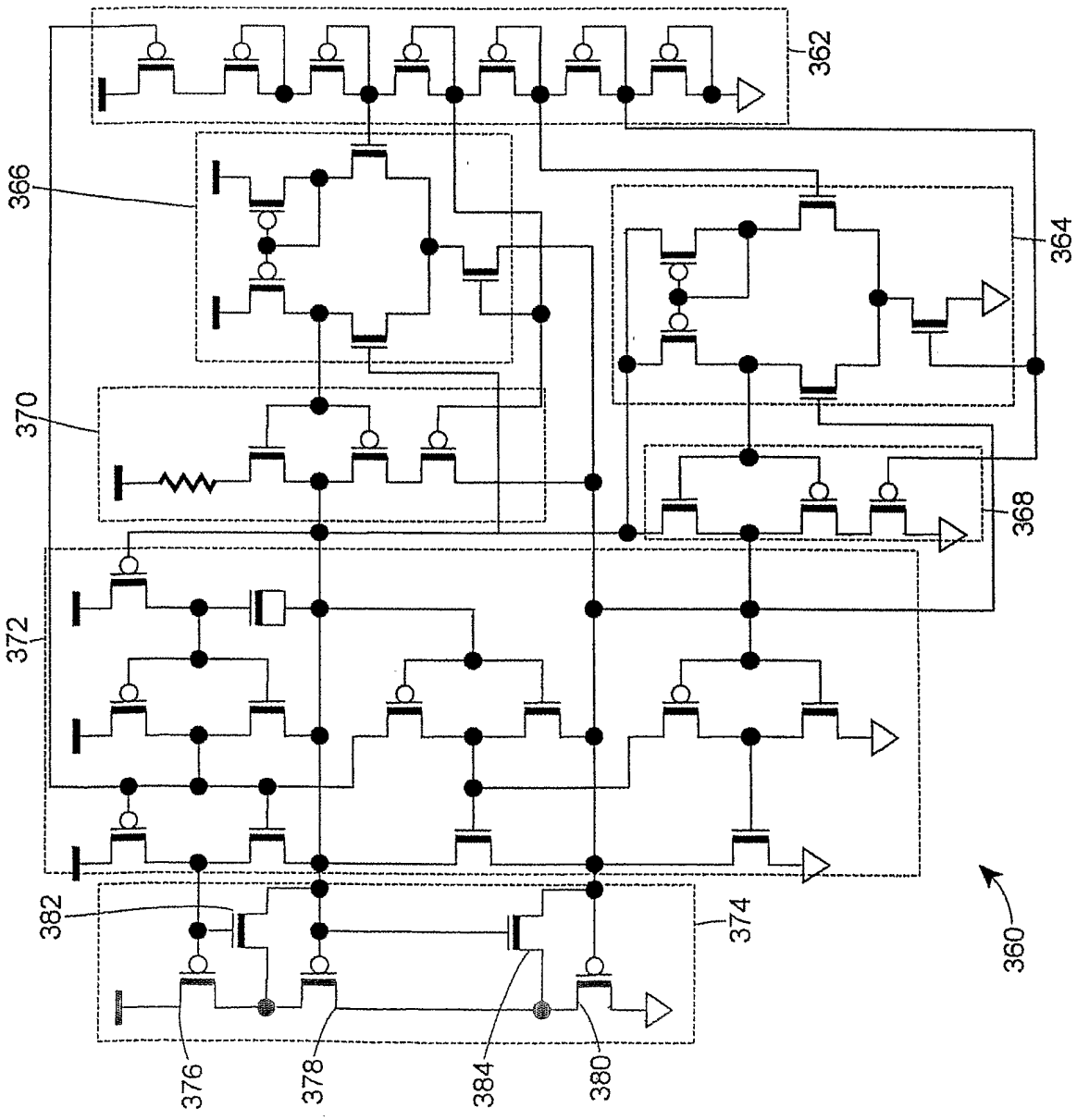


FIG. 12



INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/035421

A. CLASSIFICATION OF SUBJECT MATTER
H01L27/02

CORRECTED VERSION

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L H03K H02H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2003/072116 A1 (MALONEY TIMOTHY J ET AL) 17 April 2003 (2003-04-17) paragraphs [0018] - [0020], [0023] - [0027], [0031] figure 4	1-28
A	US 2002/131221 A1 (LIEN CHUEN-DER ET AL) 19 September 2002 (2002-09-19) paragraphs [0009], [0010] paragraphs [0034] - [0039] figure 6	1-28
A	US 2003/222285 A1 (NEGISHI TAKEMI ET AL) 4 December 2003 (2003-12-04) abstract paragraphs [0028], [0029] paragraphs [0043] - [0045] figures 2-4	1-28

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 March 2006	24 03 2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Morena, E

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2005/035421

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003072116 A1	17-04-2003	NONE	
US 2002131221 A1	19-09-2002	NONE	
US 2003222285 A1	04-12-2003	JP 2003347921 A	05-12-2003