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(54) **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**

(75) Inventors: **Masaya TANAKA**, Gifu-city (JP); **Tetsuo Fujii**, Toyohashi-city (JP)

(73) Assignee: **DENSO CORPORATION**, Kariya-city (JP)

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Publication Classification

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(52) **U.S. Cl.** **257/415**; 438/50; 257/E29.324; 257/E21.002

(57) **ABSTRACT**

A semiconductor device includes a base substrate made of silicon, a cap substrate and a leading electrode having a metal part. The base substrate has base semiconductor regions being insulated and separated from each other at a predetermined portion of a surface layer thereof. The cap substrate is bonded to the predetermined portion of the surface layer of the base substrate. The leading electrode has a first end connected to one of the plurality of base semiconductor regions of the base substrate and extends through the cap substrate such that a second end of the leading electrode is located adjacent to a surface of the cap substrate for allowing an electrical connection with an external part, the surface being opposite to a bonding surface at which the base substrate and the cap substrate are bonded. The leading electrode defines a groove between an outer surface thereof and the cap substrate.

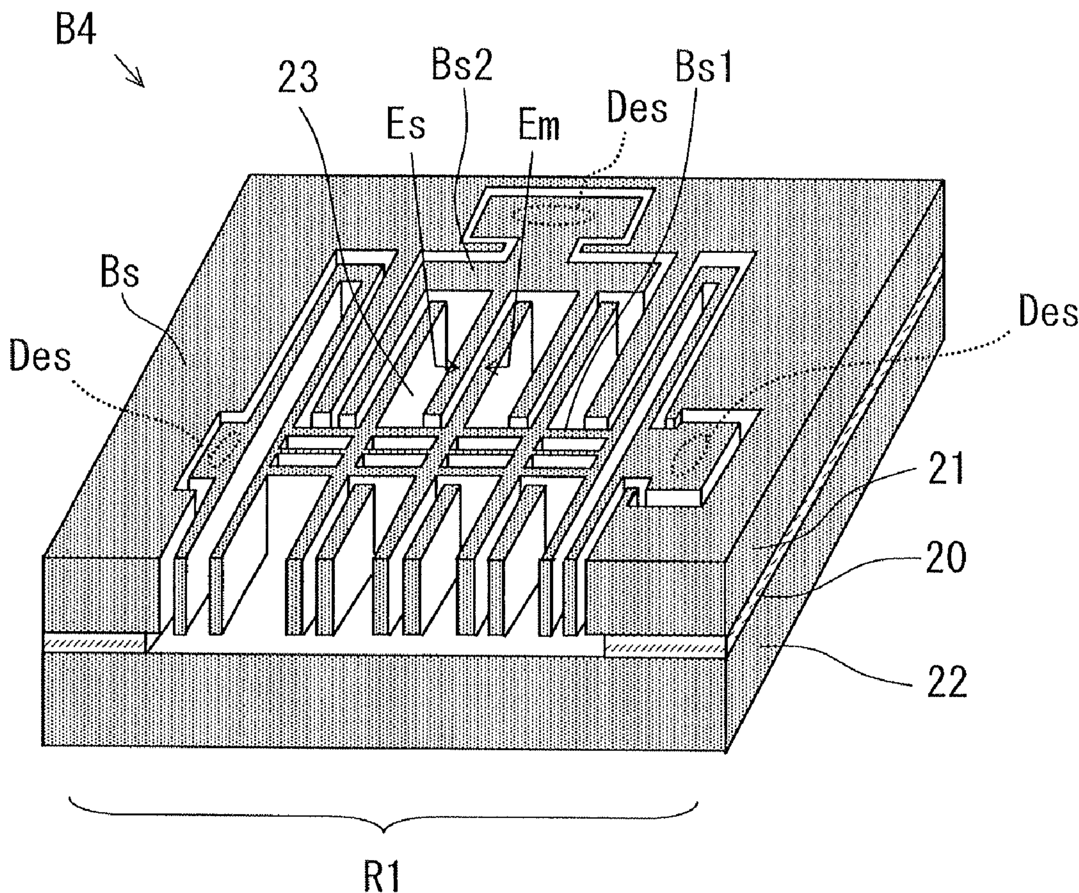


FIG. 1A

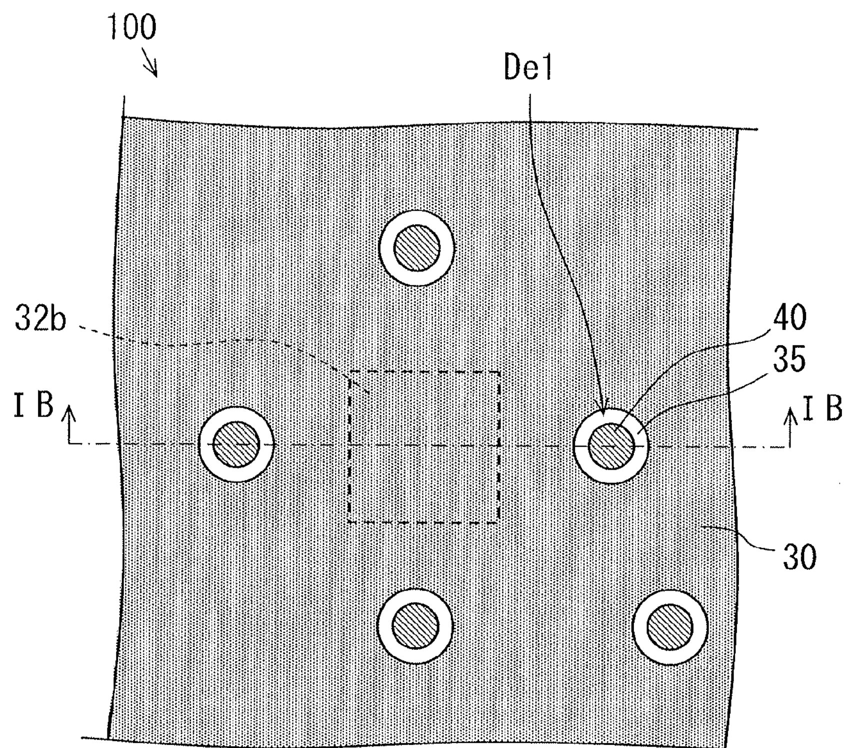


FIG. 1B

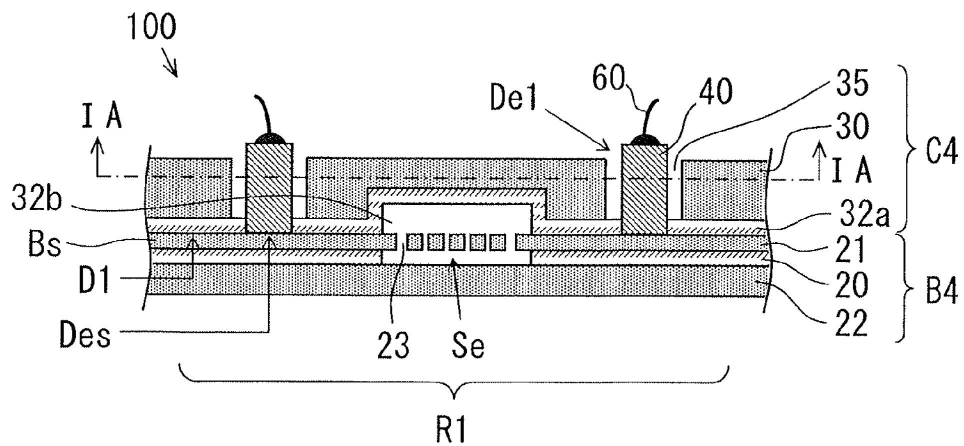


FIG. 2

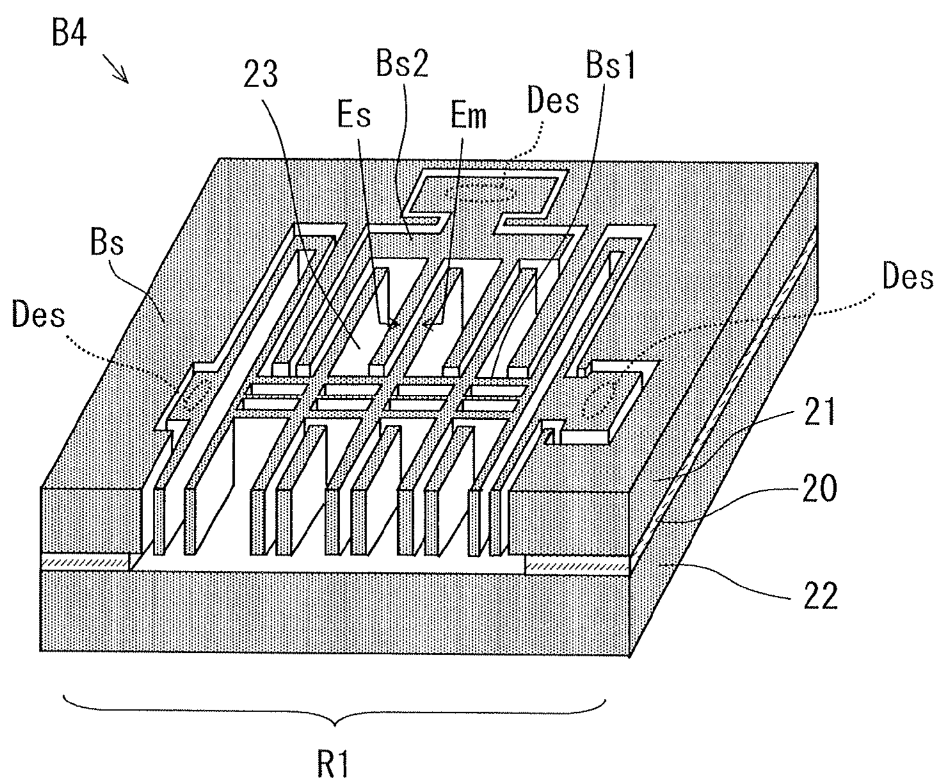


FIG. 3A

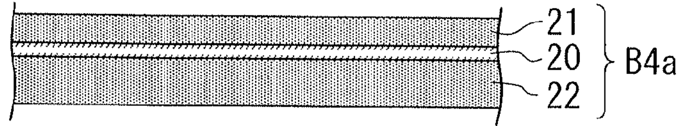


FIG. 3B

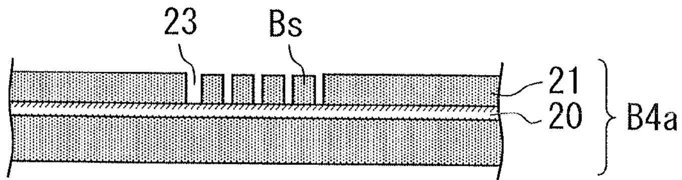


FIG. 3C

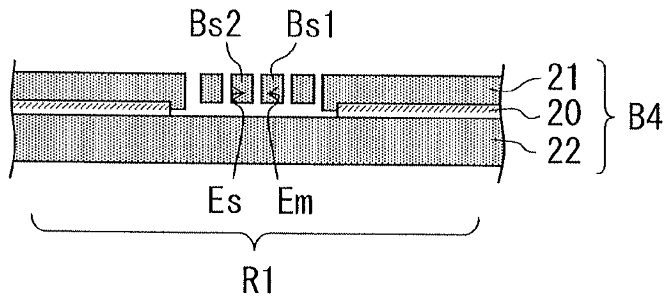


FIG. 4A

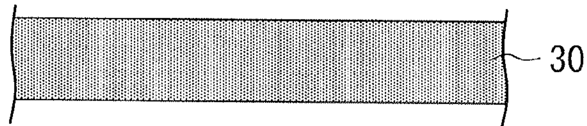


FIG. 4B

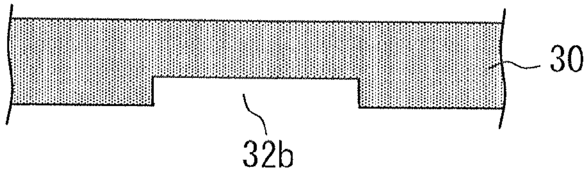


FIG. 4C

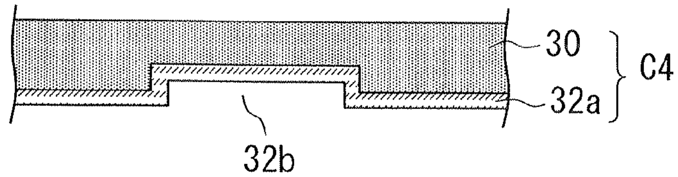


FIG. 5A

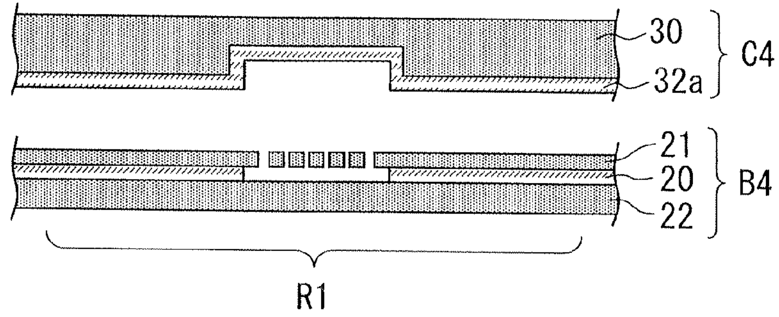


FIG. 5B

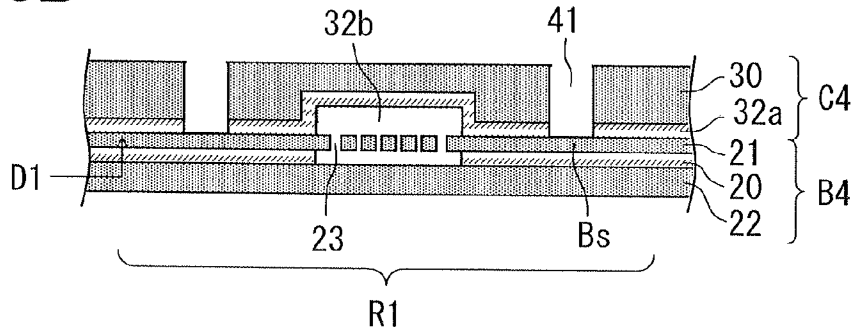


FIG. 5C

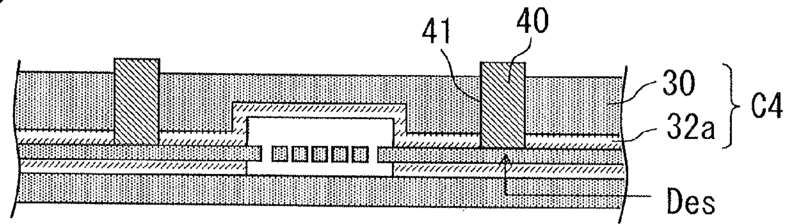


FIG. 5D

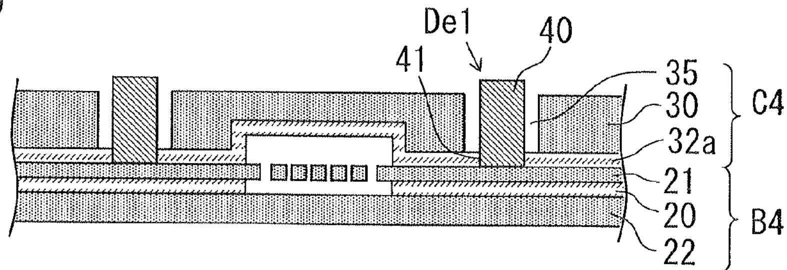


FIG. 6A

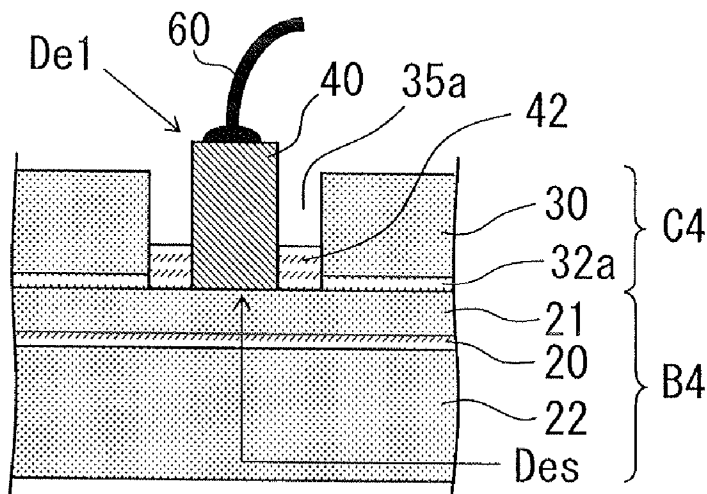


FIG. 6B

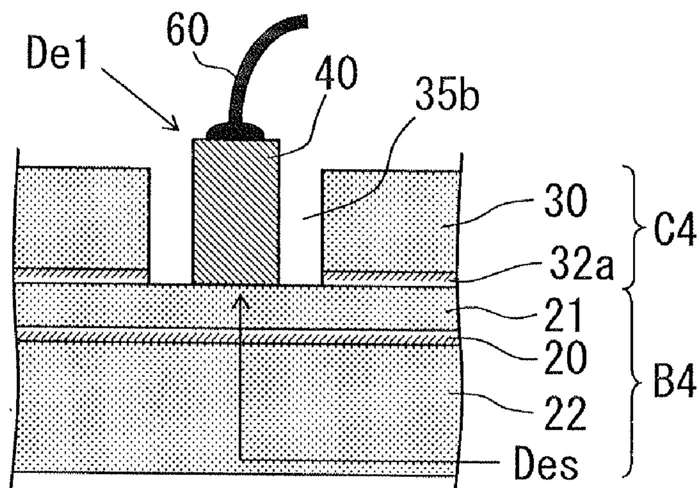


FIG. 7A

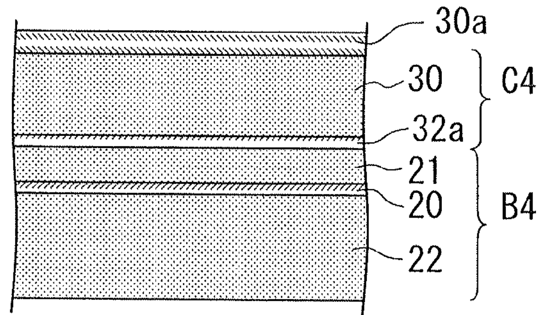


FIG. 7B

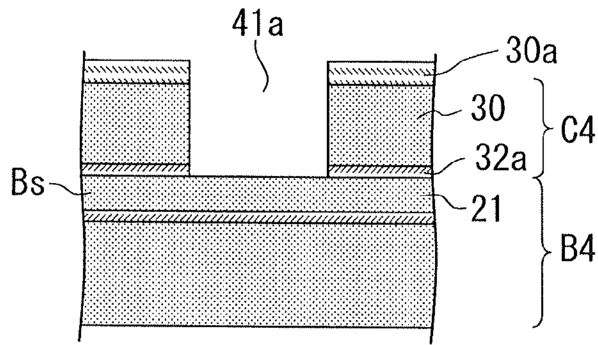


FIG. 7C

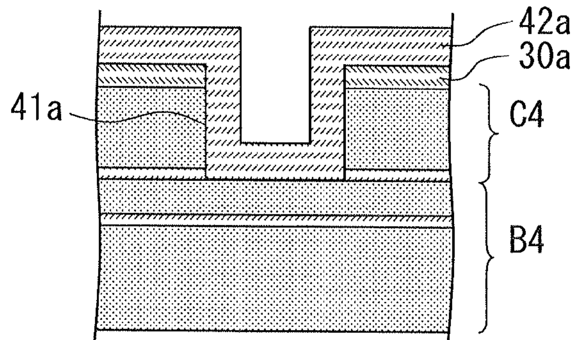


FIG. 7D

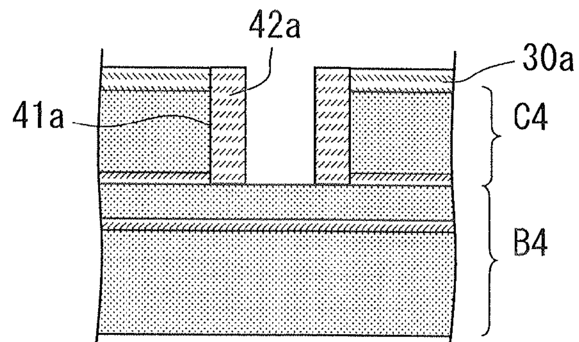


FIG. 8A

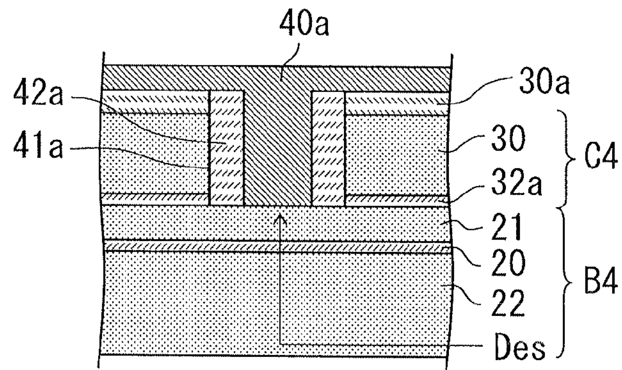


FIG. 8B

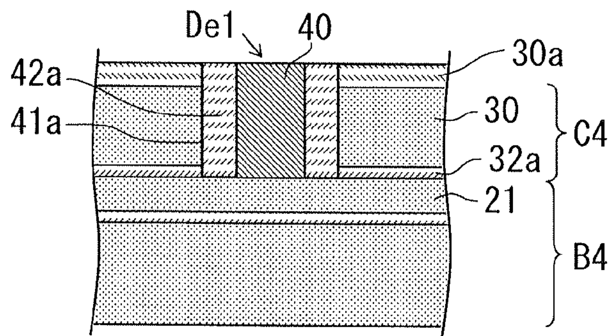


FIG. 8C

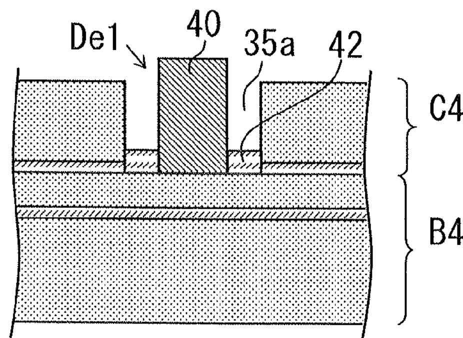


FIG. 8D

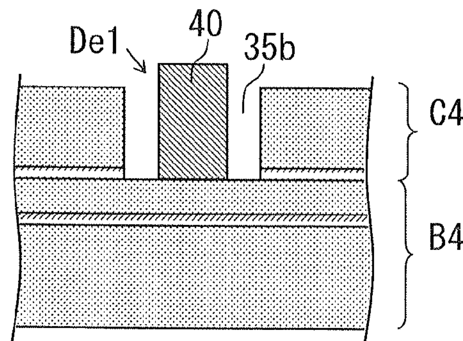


FIG. 9A

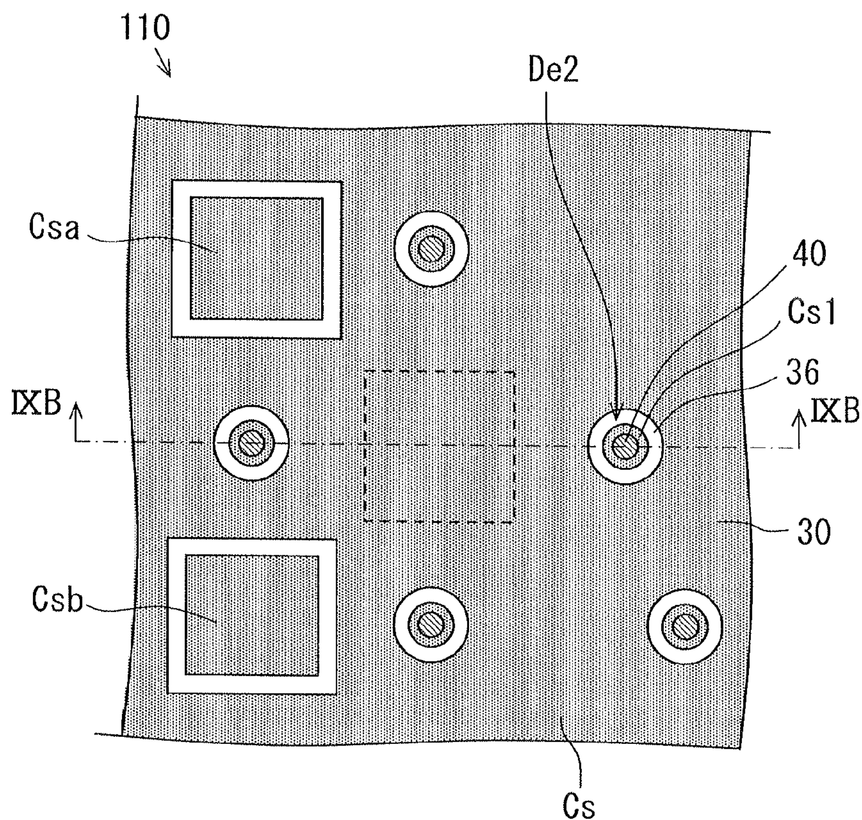


FIG. 9B

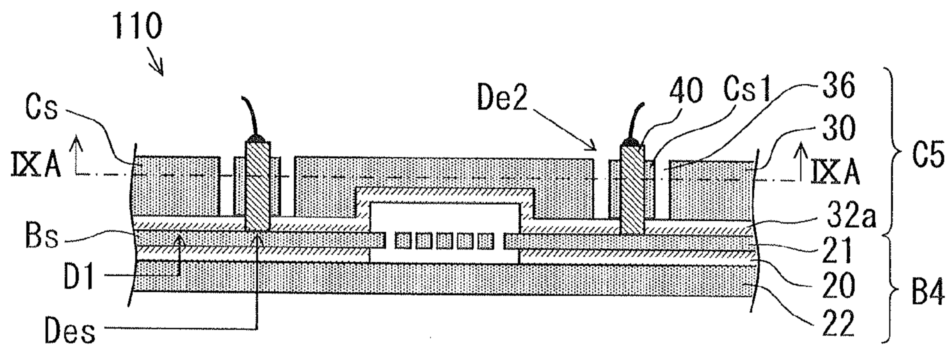


FIG. 10A

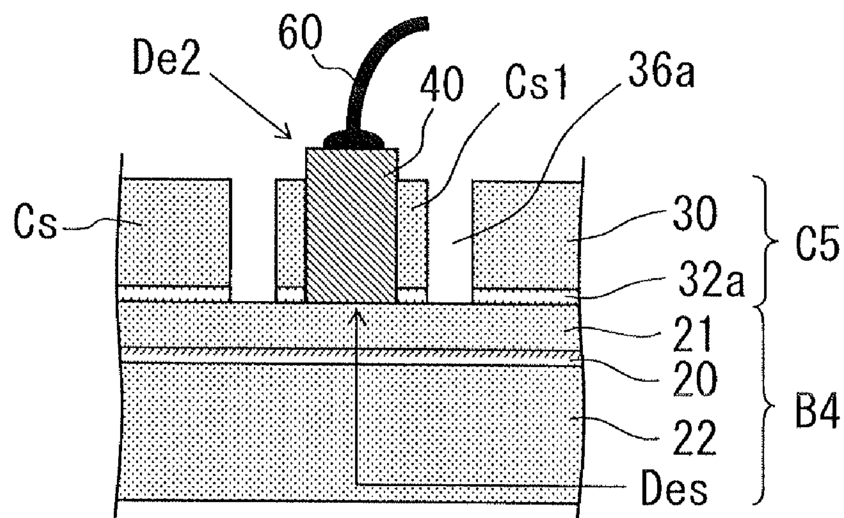


FIG. 10B

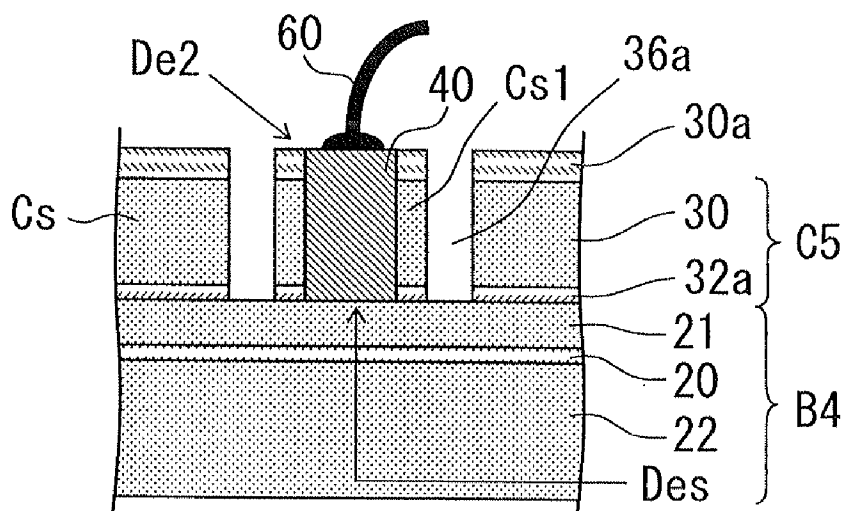


FIG. 11A

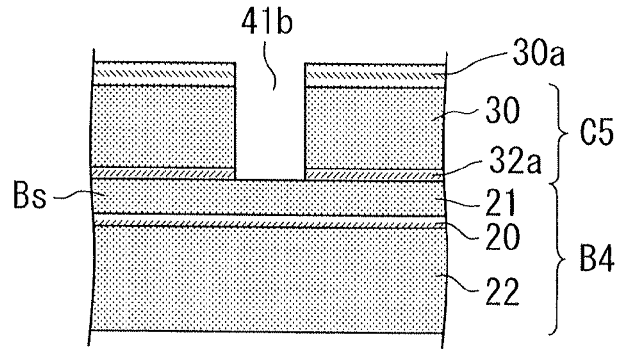


FIG. 11B

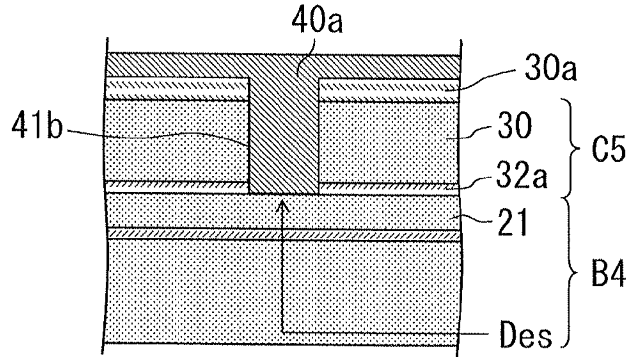


FIG. 11C

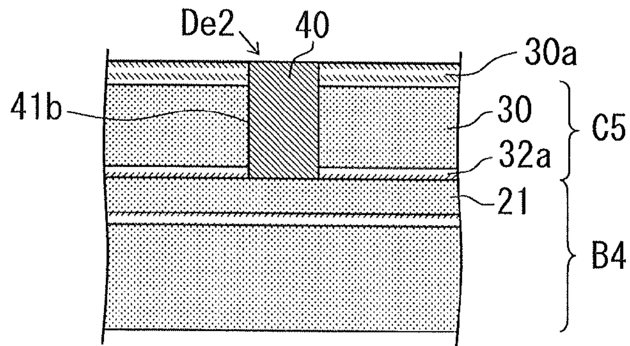


FIG. 11D

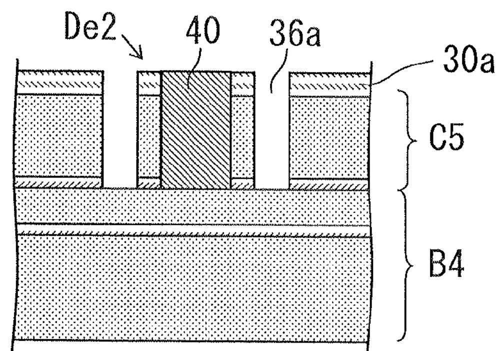


FIG. 12A

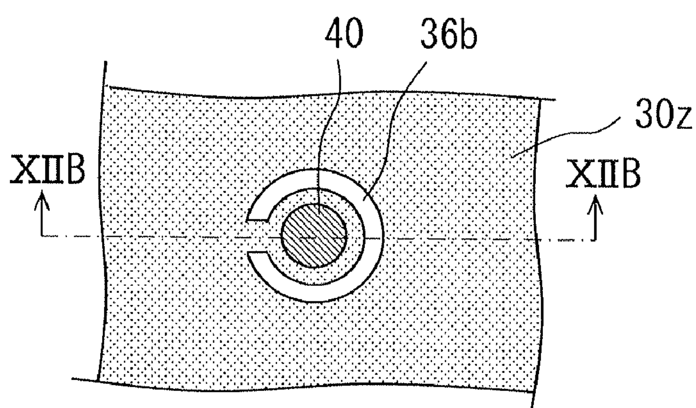


FIG. 12B

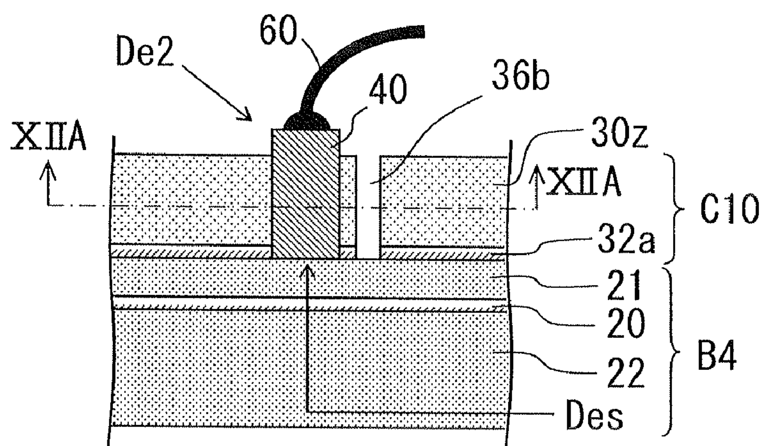


FIG. 13A

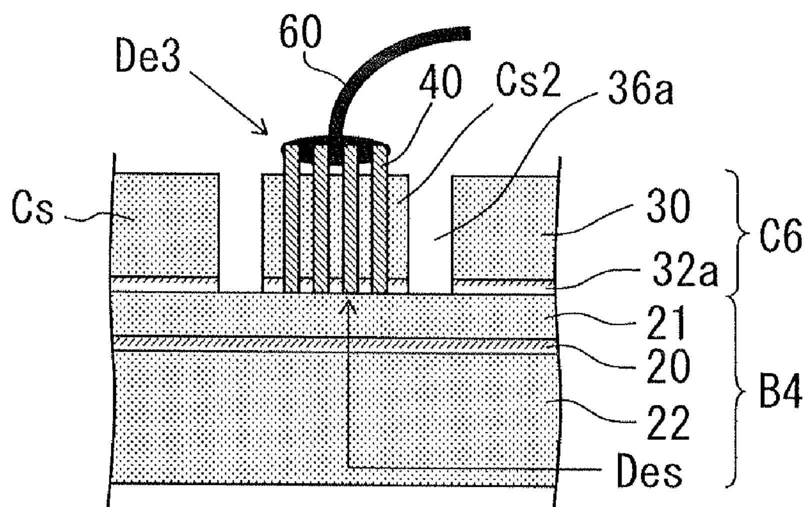


FIG. 13B

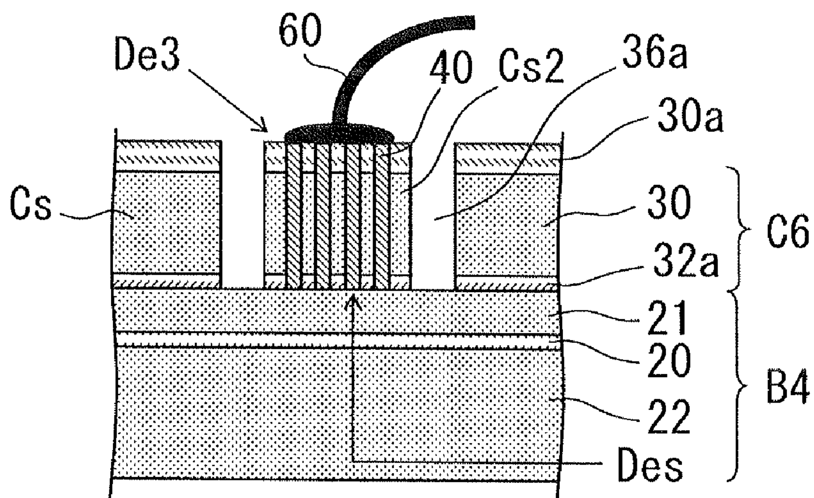


FIG. 14A

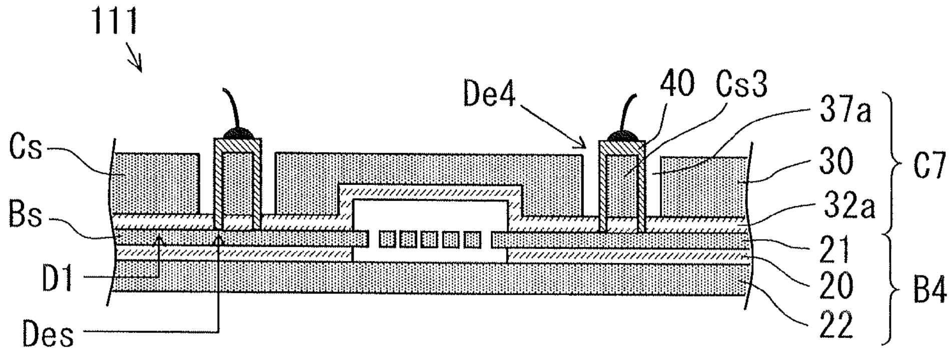


FIG. 14B

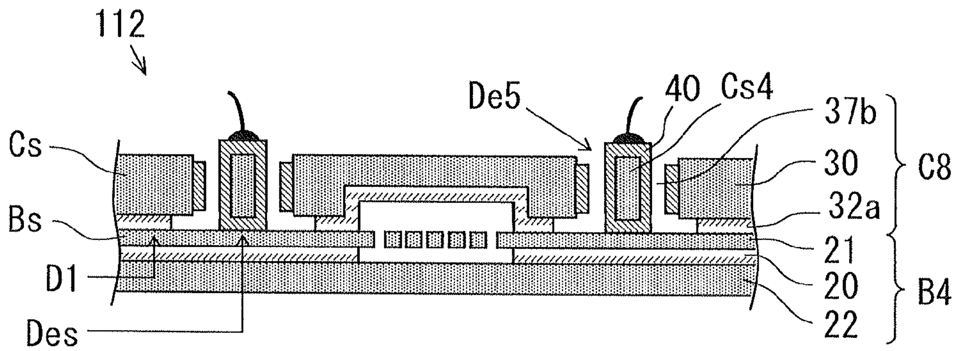


FIG. 14C

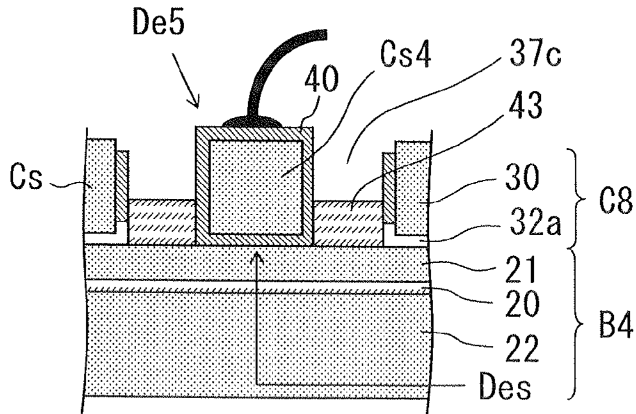


FIG. 15A

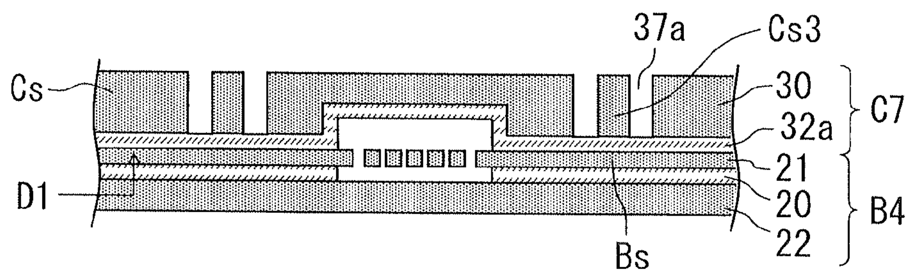


FIG. 15B

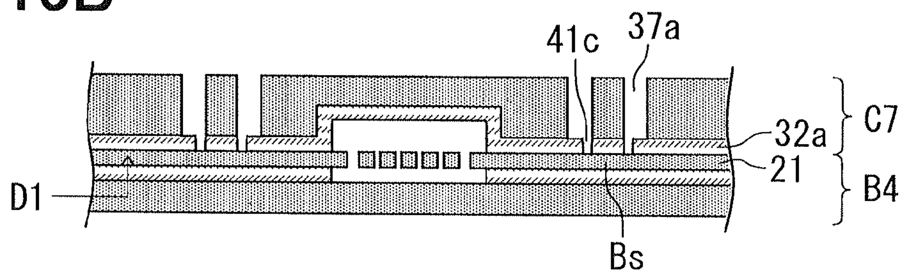


FIG. 15C

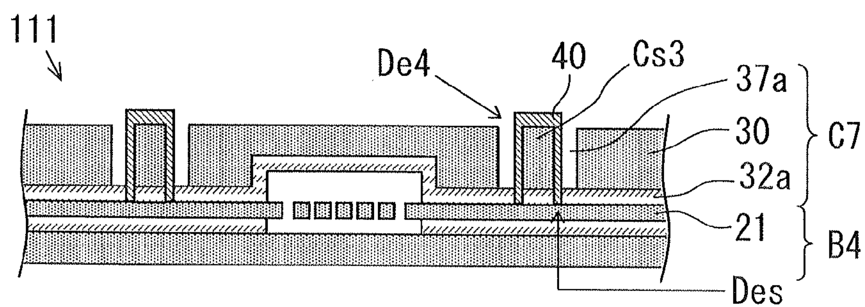


FIG. 16A

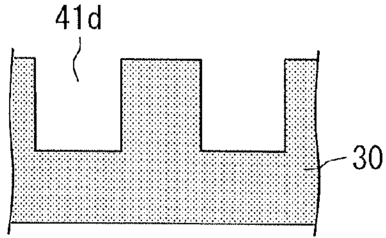


FIG. 17A

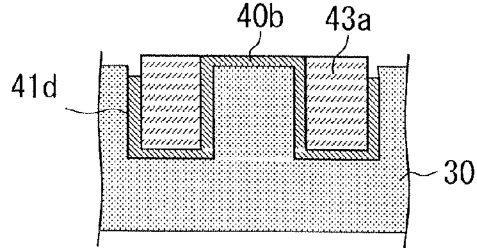


FIG. 16B

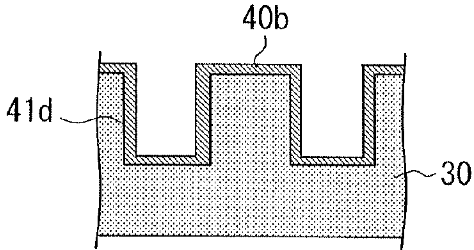


FIG. 17B

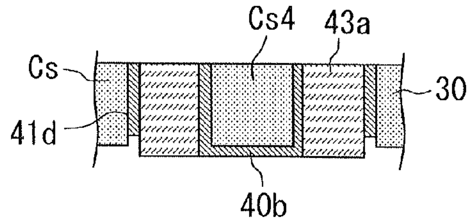


FIG. 16C

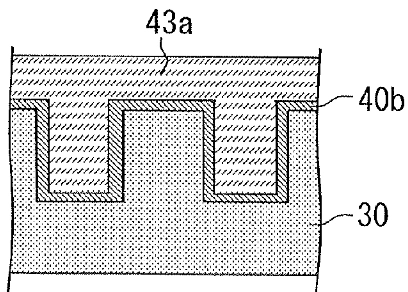


FIG. 17C

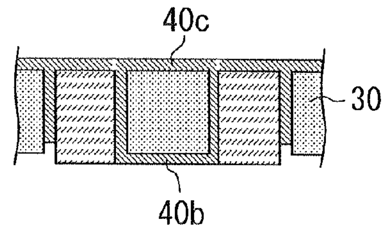


FIG. 16D

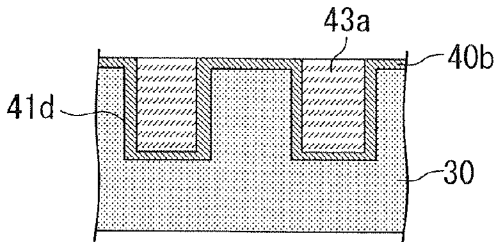


FIG. 17D

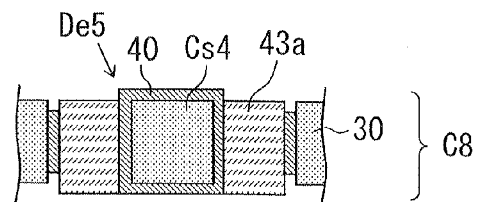


FIG. 18A

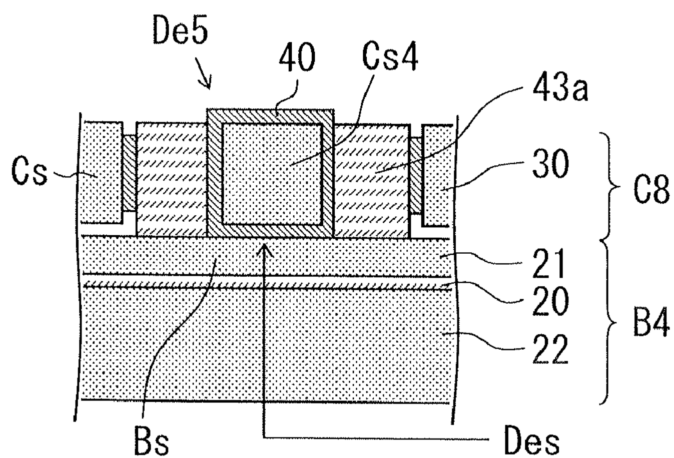


FIG. 18B

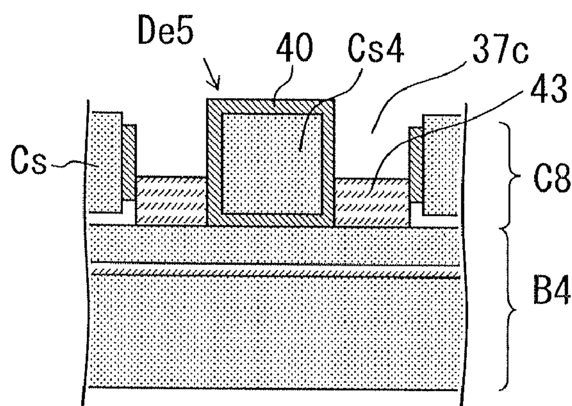


FIG. 18C

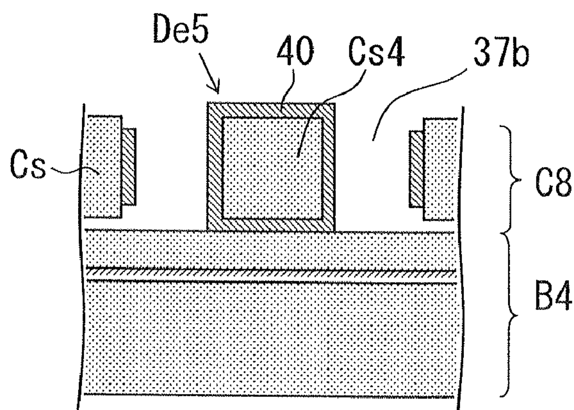


FIG. 19A

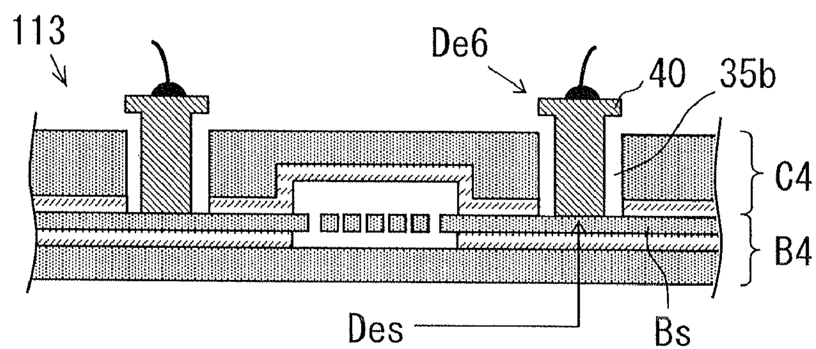


FIG. 19B

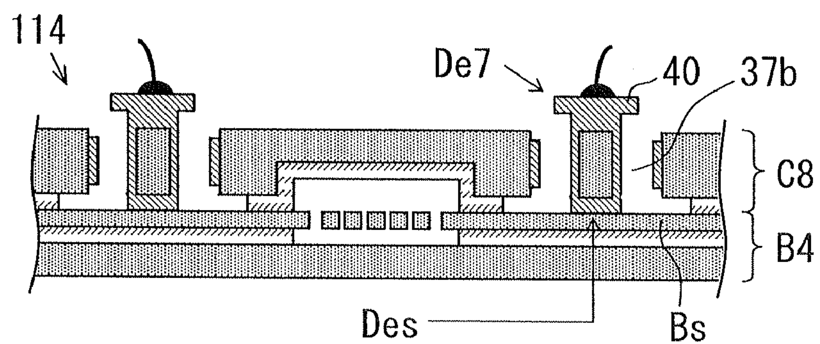


FIG. 20A

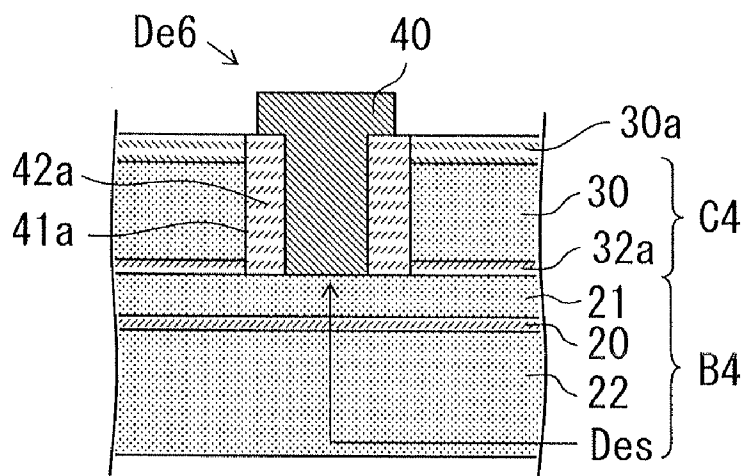


FIG. 20B

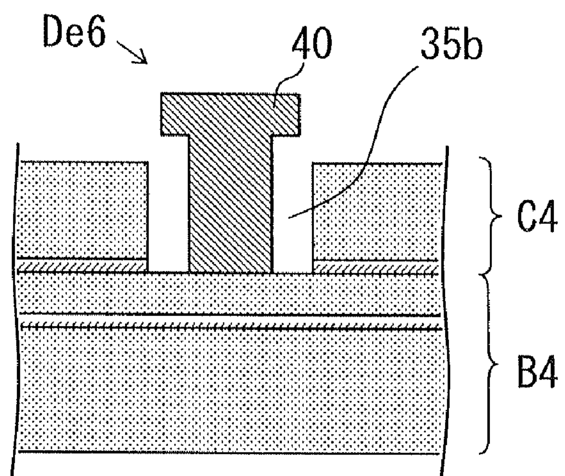


FIG. 21A

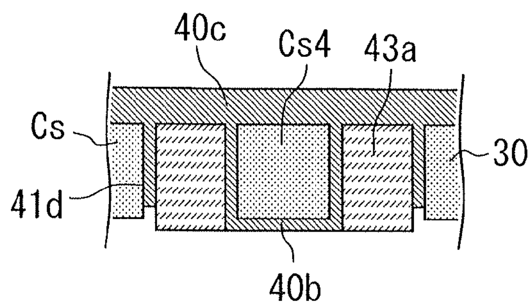


FIG. 21B

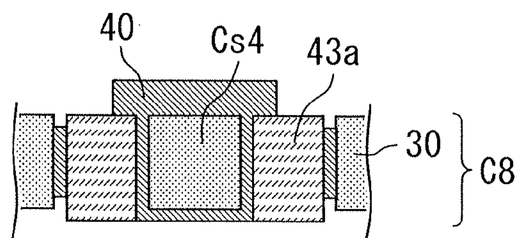


FIG. 21C

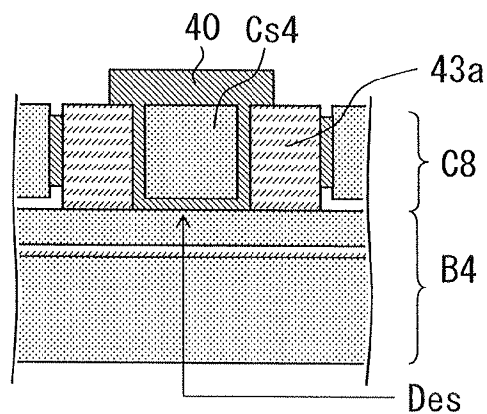


FIG. 21D

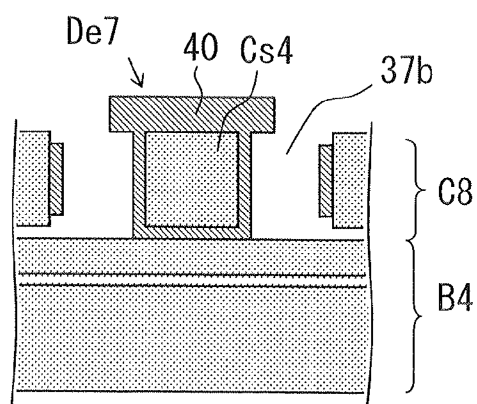


FIG. 22

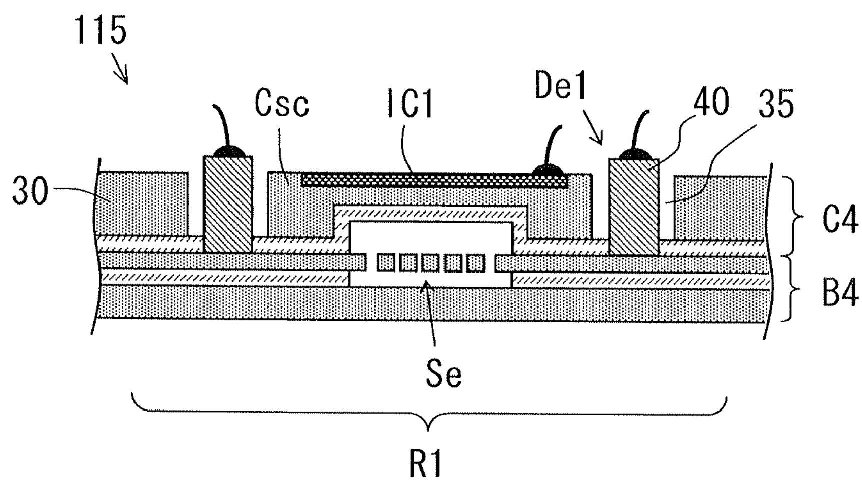


FIG. 23

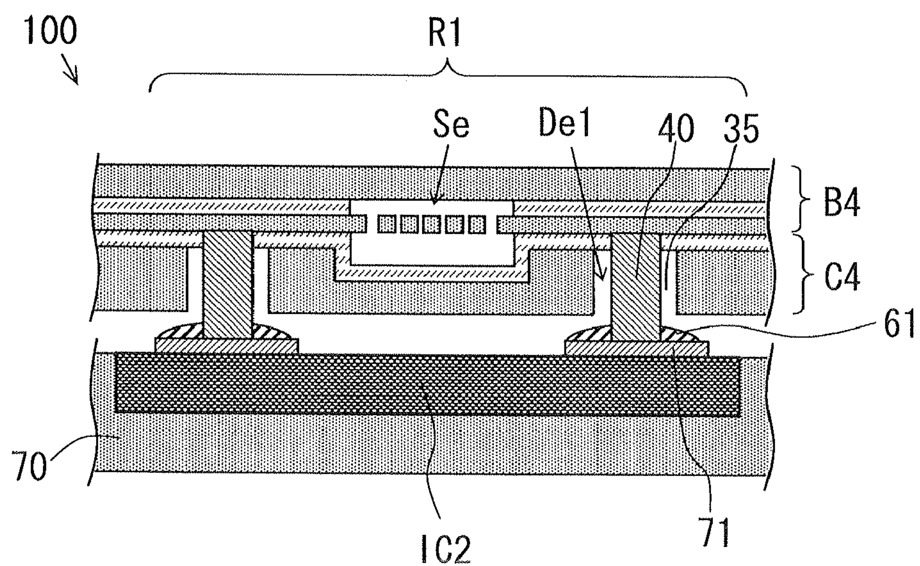


FIG. 24

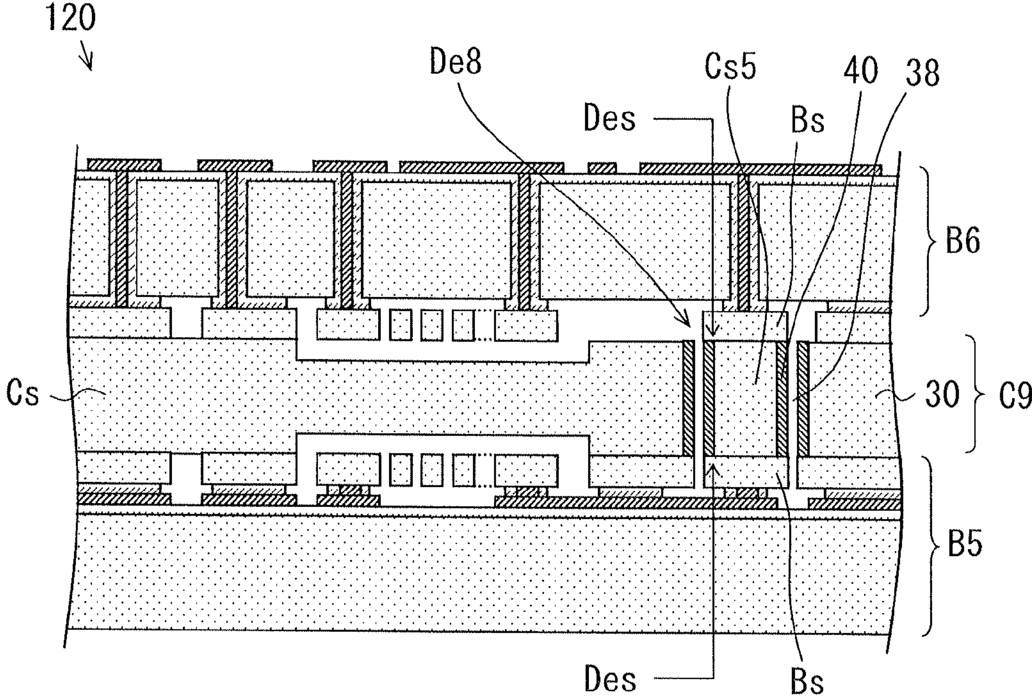


FIG. 25A

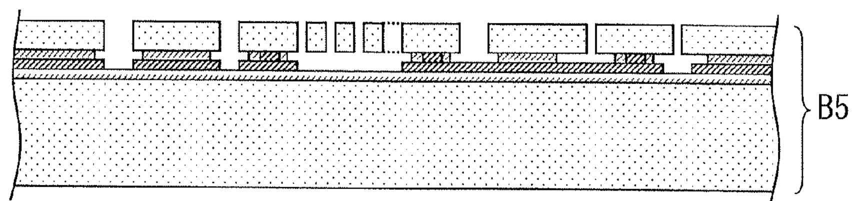


FIG. 25B

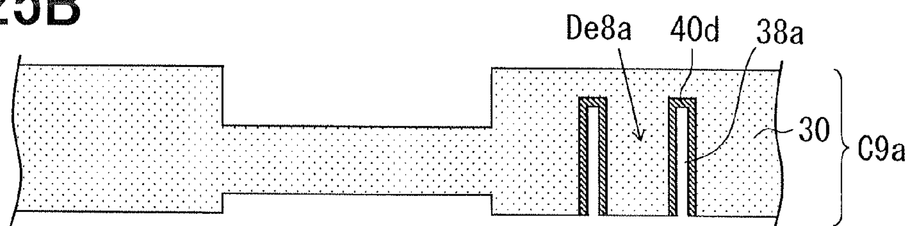


FIG. 25C

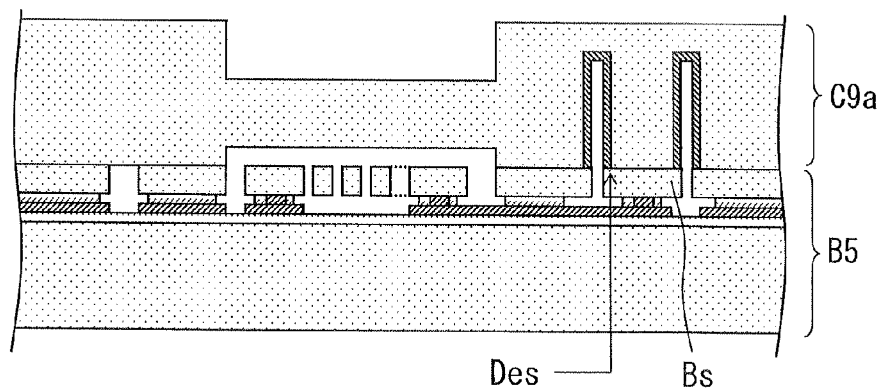


FIG. 25D

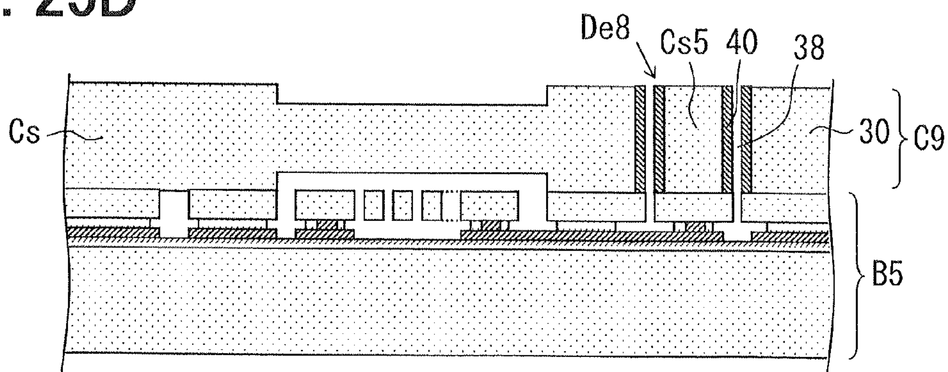


FIG. 26A

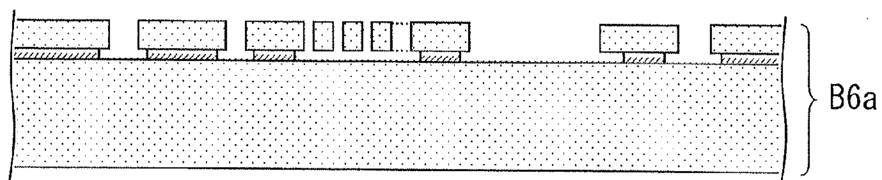


FIG. 26B

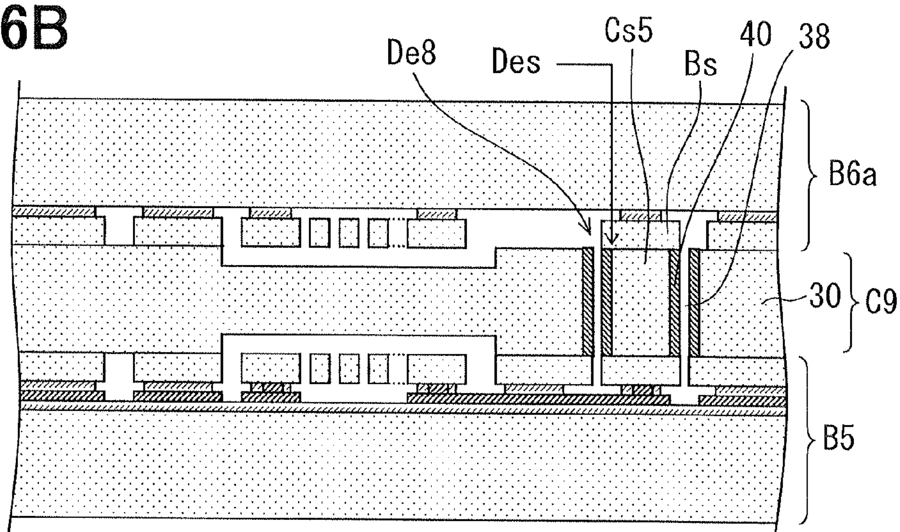


FIG. 26C

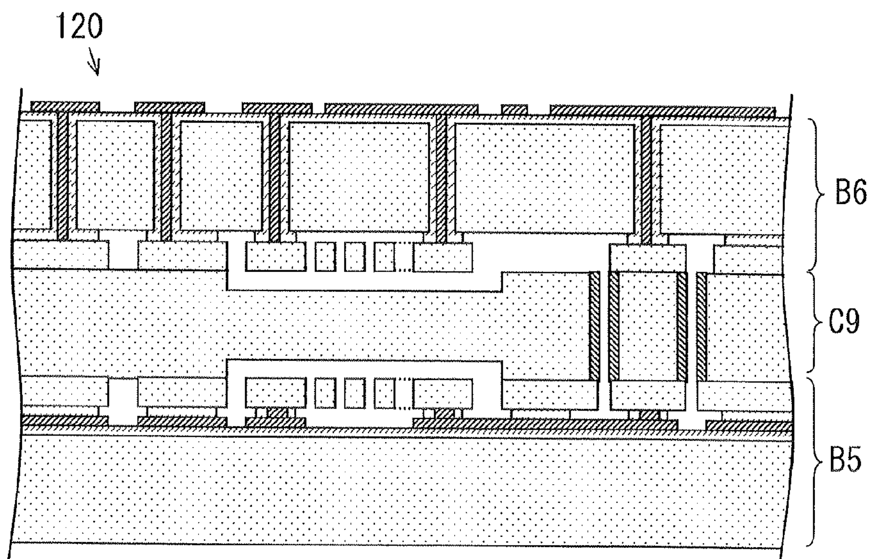


FIG. 27

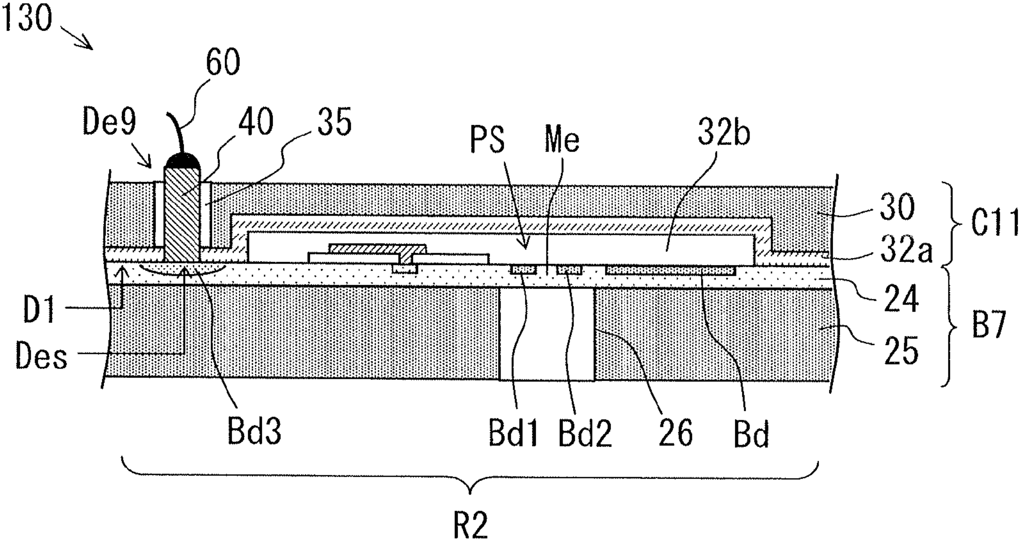


FIG. 28A

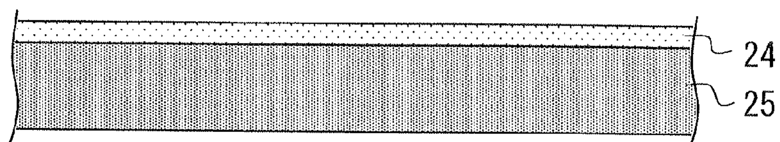


FIG. 28B

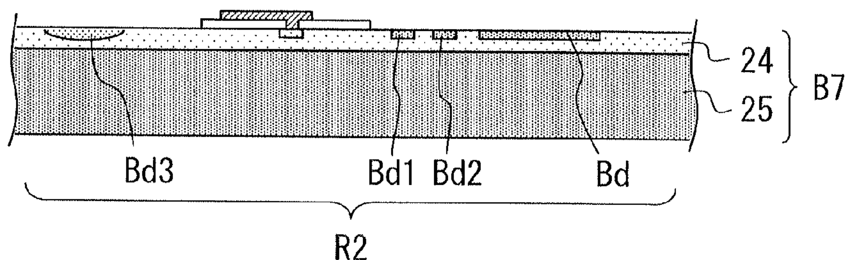


FIG. 28C

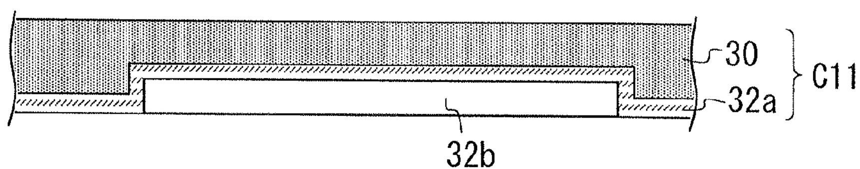


FIG. 28D

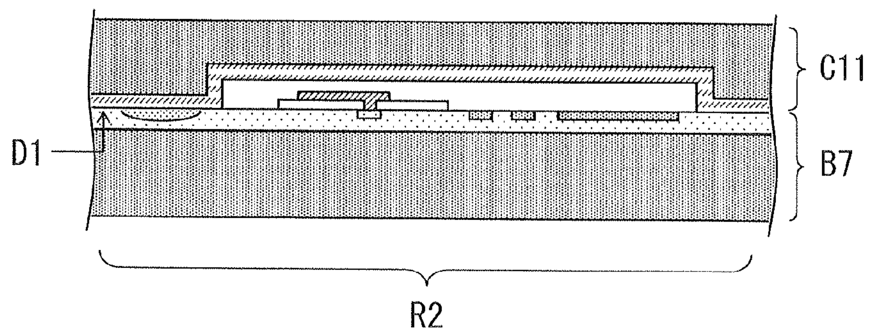


FIG. 29A

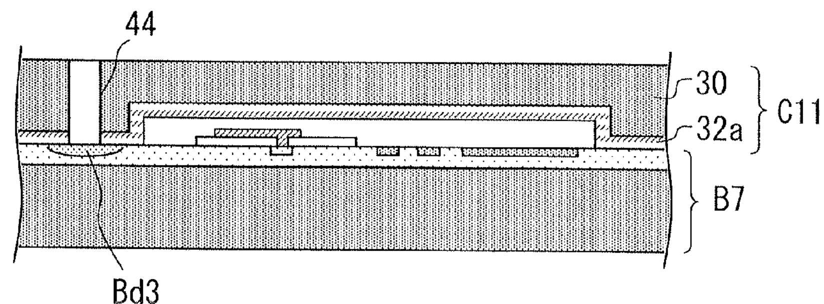


FIG. 29B

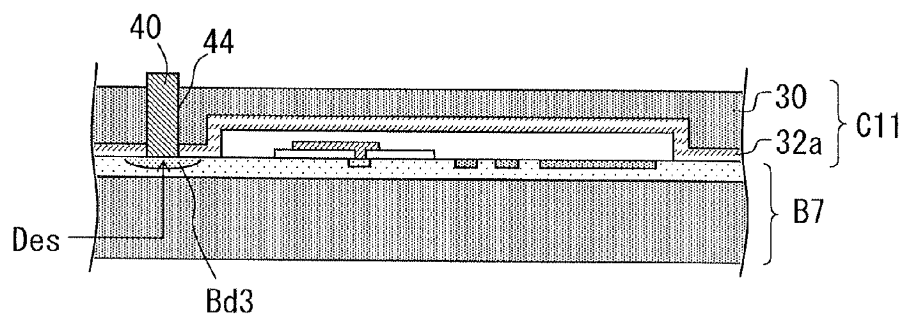


FIG. 29C

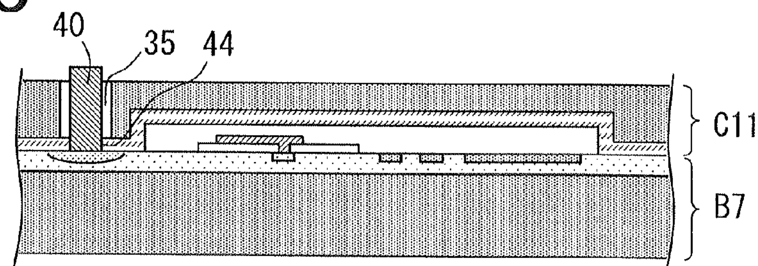


FIG. 29D

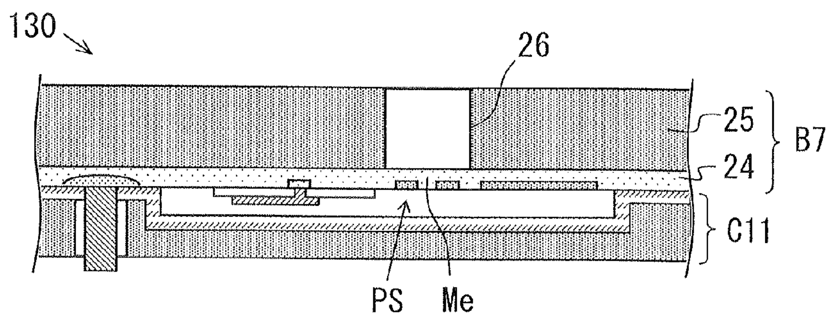


FIG. 30
PRIOR ART

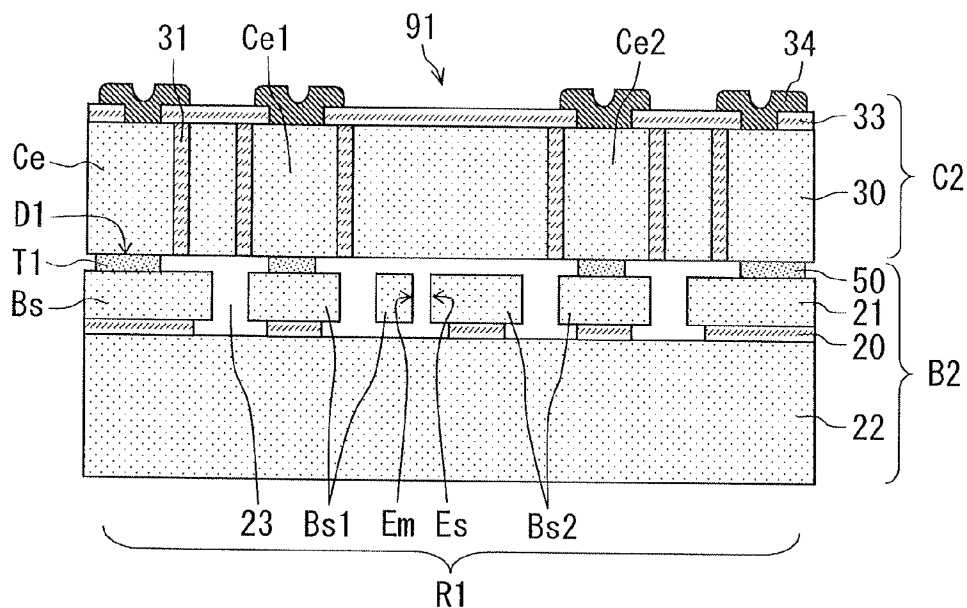
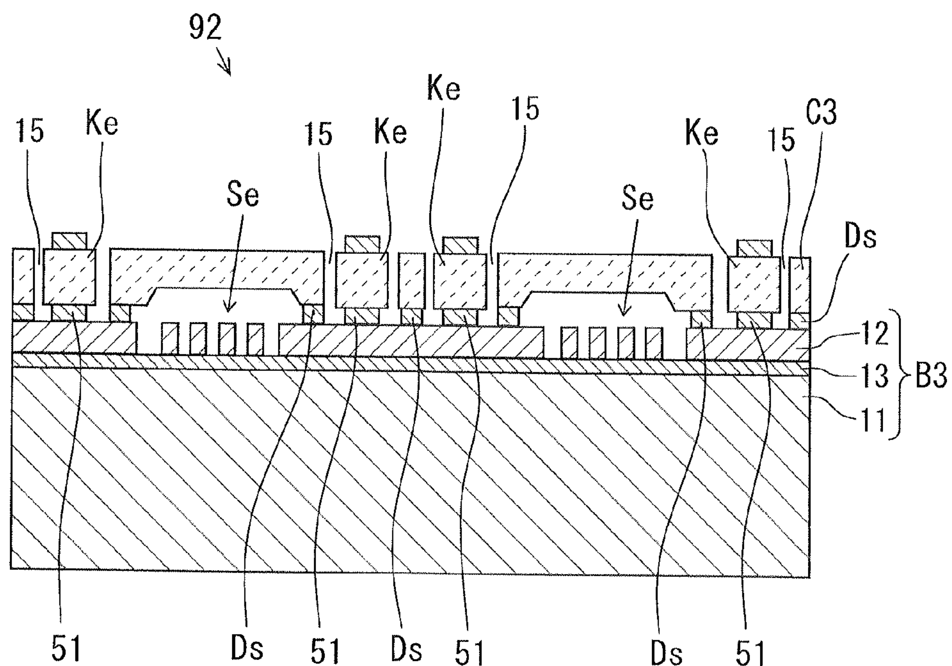


FIG. 31
PRIOR ART



SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is based on Japanese Patent Applications No. 2009-286874 filed on Dec. 17, 2009 and No. 2010-251092 filed on Nov. 9, 2010, the disclosure of which are incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to a semiconductor device and a method of manufacturing the same. More particularly, the present invention relates to a semiconductor device having a cap substrate bonded to a base substrate made of silicon for protecting various elements formed in a surface layer of the base substrate, and a method of manufacturing the same.

BACKGROUND OF THE INVENTION

[0003] In a semiconductor device, it is known to bond a cap substrate to a base substrate for protecting various element formed in a surface layer of the base substrate.

[0004] In such a semiconductor device, an electrical connection for electrically connecting the base substrate and an external part is necessary. For example, it is known to make a bonding wire directly on the surface of the base substrate through a through hole formed in the cap substrate. In such a method, however, a large through hole is required in the cap substrate to conduct wire bonding. That is, an area necessary for making the electrical connection is likely to increase.

[0005] In order to ease the electrical connection between the element and the external part by the wire bonding, soldering or the like in a small area, a leading electrode that extends from the base substrate to the surface of the cap substrate and allows the electrical connection at the end can be employed.

[0006] It has been known to use a portion of the cap substrate as the leading electrode. For example, the cap substrate made of silicon is divided into partial regions by an insulating and separating trench, and a specific region of the partial regions, which connects to an insulated and separated base semiconductor region of the base substrate, is used as a leading conductive region. The upper end of the specific region is electrically connected to the external part by the wire bonding, soldering or the like.

[0007] A semiconductor device having such an electrical connection structure is, for example, described in Japanese Patent Application Publications No. JP2008-229833A (Publication 1, corresponding to US2008/0290490A1) and No. JP2008-256495 (Publication 2).

[0008] FIG. **30** shows an example of the semiconductor device described in Publication 1. A semiconductor device **91** shown in FIG. **30** has a semiconductor base substrate B**2** and a conductive cap substrate C**2** bonded to the base substrate B**2**.

[0009] The base substrate B**2** is a SOI (Silicon On Insulator) substrate in which an embedded oxide film **20** is interposed between a SOI layer **21** and a support substrate **22**. Insulated and separated multiple base semiconductor regions Bs are formed in a surface layer of the base substrate B**2**. The base semiconductor regions Bs are provided by the SOI layer **21**, and are insulated and separated from adjacencies by a trench **23** that reaches the embedded oxide film **20**. Projections T**1** are formed above the base semiconductor regions Bs. The projections T**1** are provided by a conductive film **50**, which is made of poly crystal silicone, metal or the like.

[0010] The semiconductor device **91** includes a mechanical quantity sensor element for measuring a mechanical quantity, such as acceleration and angular velocity, using an inertia force. The mechanical quantity sensor element is constructed of the multiple base semiconductor regions Bs. Specifically, the base semiconductor regions Bs include at least two base semiconductor regions Bs**1** and two base semiconductor regions Bs**2**.

[0011] The base semiconductor regions Bs**1** constitute a movable semiconductor region. The base semiconductor regions Bs**1** are formed by performing sacrifice layer etching on a part of the embedded oxide film **20**. The base semiconductor regions Bs**1** as the movable semiconductor region include a movable electrode Em, which is formed to be displaceable.

[0012] The base semiconductor regions Bs**2** constitute a fixed semiconductor region including a fixed electrode Es opposed to the movable electrode Em. The two base semiconductor region Bs**1** and the two base semiconductor region Bs**2** each form a continuous and integrated region on a plane.

[0013] In the semiconductor device **91**, a capacitance is created between opposed surfaces of the movable electrode Em and the fixed electrode Es. As the movable electrode Em is displaced in a direction perpendicular to the opposed surfaces in accordance with the applied mechanical quantity, the capacitance changes in accordance with a change in the distance between the movable electrode Em and the fixed electrode Es. Thus, the applied mechanical quantity is detected by measuring the change in capacitance.

[0014] The cap substrate C**2** is provided by a single crystal silicon substrate **30** on which multiple cap conductive regions Ce as partial regions are formed. The cap conductive regions Ce are divided by an insulating and separating trench **31** that passes through the single crystal silicon substrate **30**. The cap substrate C**2** has a surface protection layer **33** made of silicon oxide (SiO_2) or the like, and electrode pads **34** made of aluminum (Al) or the like.

[0015] The cap substrate C**2** is bonded to the projections T**1** formed on the base semiconductor regions Bs, and a bonding surface D**1** is formed therebetween. The bonding surface D**1** has a loop shape in a predetermined region R**1** of the base substrate B**2**. Thus, a space sealed in a highly vacuum condition is provided between the surface of the predetermined region R**1** and the surface of the cap substrate C**2** by bonding the base substrate B**2** and the cap substrate C**2**.

[0016] Also, as the base substrate B**2** and the cap substrate C**2** are bonded, specific cap conductive regions Ce**1**, Ce**2** are electrically connected to the specific base semiconductor regions Bs**1**, Bs**2**, respectively, to serve as leading conductive regions. In other words, the leading conductive regions Ce**1**, Ce**2** are respectively connected to the movable semiconductor region Bs**1** and the fixed semiconductor region Bs**2**, respectively.

[0017] FIG. **31** shows an example of a semiconductor device described in Publication 2. A semiconductor device **92** of FIG. **31** has a semiconductor mechanical quantity sensor element for detecting a mechanical quantity, such as acceleration and angular velocity, similar to the semiconductor device **91** of FIG. **30**.

[0018] The semiconductor device **92** has a base substrate B**3** provided by a Sal substrate. The SOI substrate includes a support substrate **11** made of silicon semiconductor and a poly silicon layer **12** disposed on the support substrate **11** through an oxide film **13**. Sensing portions Se are formed by the poly silicon layer **12** disposed on the support substrate **11**.

[0019] Similar to the semiconductor device **91** of FIG. **30**, the sensing portions Se include a movable electrode and a fixed electrode. The movable electrode and the fixed electrode are provided by a beam structure, which is generally used in conventional acceleration sensors and angular velocity sensors. As the movable electrode is displaced in accordance with the applied acceleration or angular velocity, the capacitance between the movable electrode and the fixed electrode is changed. A voltage signal indicative of the change in capacitance is produced.

[0020] Further, a cap C**3** is fixed to the base substrate B**3** to surround the sensing portions Se. The cap C**3** is bonded to the poly silicon layer **12** through an adhesive layer Ds made of a resin adhesive or the like. The cap C**3** is provided with penetrating electrodes Ke. The cap C**3** is made of silicon semiconductor in which impurities, such as phosphorous (P) and boron (B), are preferably doped so as to have electrical conductivity.

[0021] The penetrating electrodes Ke pass through the cap C**3** in a direction in which a thickness of the cap C**3** is measured. The penetrating electrodes Ke serve to lead electrical signals from the sensing portions Se, which are located under the cap C**3**, to the upper surface of the cap C**3**. The penetrating electrodes Ke are constituted as portions of the cap C**3** having the electrical conductivity.

[0022] Further, the cap C**3** is formed with grooves **15**, which are referred to as air isolations, on peripheries of the penetrating electrodes Ke. The grooves **15** surround the penetrating electrodes Ke, and pass through the cap C**3** in the direction in which the thickness of the cap C**3** is measured.

[0023] Thus, the penetrating electrodes Ke and portions of the cap C**3** on the peripheries of the penetrating electrodes Ke are insulated by means of the grooves **15**. That is, the grooves **15** serve as electrically insulating portions to electrically insulate the penetrating electrodes Ke from the peripheral portions thereof in the cap C**3**. The penetrating electrodes Ke are in contact with the poly silicon layer **12** through connecting electrodes **51**, which are made of aluminum, Al—Si or the like, to make electrical connection with the sensing portions Se.

[0024] In the semiconductor device **91** of FIG. **30**, the cap substrate C**2** serves as a sealing cap for protecting the mechanical quantity sensor element formed in the predetermined region R**1** of the surface layer of the base substrate B**2**. The cap conductive regions Ce**1**, Ce**2** of the cap substrate C**2**, which are electrically connected to the base semiconductor regions Bs**1**, Bs**2** of the base substrate B**2**, serve as leading conductive regions.

[0025] In such a structure, however, the insulating and separating trench **31** exist on the peripheries of the leading conductive regions Ce**1**, Ce**2** to isolate the leading conductive regions Ce**1**, Ce**2** from the peripheral cap conductive regions. Therefore, parasitic capacitance is produced due to the insulating and separating trench **31** being an electric substance, and is likely to affect performance of the semiconductor device **91**.

[0026] In the semiconductor device **92** of FIG. **31**, on the other hand, the penetrating electrodes Ke are electrically insulated from the peripheral portions in the cap C**3** by the grooves **15** as the air isolations. Therefore, the electric permittivity at the grooves **15** is smaller than that at the trench **31** of the semiconductor device **91** in which the electric substance is embedded. That is, the semiconductor device **92** of FIG. **31** is less apt to generate the parasitic capacitance, as compared with the semiconductor device **91** of FIG. **30**.

[0027] The semiconductor device **91** employs the cap substrate C**2** made of single crystal silicon. The semiconductor device **92** employs the cap substrate C**3** made of silicon semiconductor. In general, silicon is less expensive than other substrate materials, and a trench is easily formed in a silicon substrate. However, silicon has a relatively large specific resistance. Therefore, the leading conductive regions Ce**1**, Ce**2** and the penetrating electrodes Ke are likely to increase resistance, and hence the applicable range of such semiconductor devices may be restricted.

SUMMARY OF THE INVENTION

[0028] It is an object of the present invention to provide a semiconductor device having a base substrate and a cap substrate bonded to the base substrate for protesting the base substrate, in which a leading electrode for allowing an electrical connection between the base substrate and an external part has a structure capable of reducing resistance, and the leading electrode and a neighboring portion thereof have a structure capable of reducing occurrence of parasitic capacitance, and a method of manufacturing the semiconductor device.

[0029] According to an aspect of the present invention, a semiconductor device includes a base substrate, a cap substrate and a leading electrode for allowing an electrical connection between the base substrate and an external device. The base substrate is made of silicon and has a plurality of base semiconductor regions in a predetermined portion of a surface layer thereof. The cap substrate is bonded to the predetermined portion of the surface layer of the base substrate. The leading electrode includes a metal part. The leading electrode passes through the cap substrate. A first end of the leading electrode is connected to one of the plurality of base semiconductor regions. A second end of the leading electrode is located adjacent to a surface of the cap substrate, the surface being opposite to a bonding surface at which the base substrate and the cap substrate are bonded, to allow the electrical connection with an external part. Further, a groove is formed between the leading electrode and the cap substrate.

[0030] The leading electrode has the metal part having conductivity higher than that of silicon. Hence, the resistance at the leading electrode can be reduced, as compared with a conventional semiconductor device. Further, the groove is formed between the leading electrode and the cap substrate. That is, because the leading electrode has an air isolation structure, the conventional insulating and separating trench for forming the leading conductive region is not employed. Therefore, parasitic capacitance will not be easily created. In addition, stress due to a thermal expansion difference between the metal part and the cap substrate is reduced.

[0031] According to a second aspect of the present invention, a method of manufacturing a semiconductor device includes: forming a base substrate made of silicon; forming a cap substrate; bonding the cap substrate to a predetermined portion of the base substrate; and forming a leading electrode

including a metal part. The base substrate has a plurality of base semiconductor regions in the predetermined portion of a surface layer thereof, and the plurality of base semiconductor regions is insulated and separated from each other. The leading electrode passes through the cap substrate. The leading electrode has a first end connected to one of the plurality of base semiconductor regions and a second end located adjacent to a surface of the cap substrate. The leading electrode defines a groove between an outer surface thereof and the cap substrate.

[0032] In the semiconductor device manufactured by the above method similar effects as described in the above are achieved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] Other objects, features and advantages of the present invention will become more apparent from the following detailed description made with reference to the accompanying drawings, in which like parts are designated by like reference characters and in which:

[0034] FIG. **1**A is a schematic cross-sectional view of a part of a semiconductor device as an example according to an embodiment of the present invention;

[0035] FIG. **1**B is a schematic cross-sectional view taken along a line IB-IB in FIG. **1**A;

[0036] FIG. **2** is a perspective view of a base substrate of the semiconductor device shown in FIGS. **1**A and **1**B;

[0037] FIGS. **3**A to **3**C are schematic cross-sectional views for showing a process of forming the base substrate shown in FIG. **2**;

[0038] FIGS. **4**A to **4**C are schematic cross-sectional views for showing a process of forming a cap substrate of the semiconductor device shown in FIGS. **1**A and **1**B;

[0039] FIGS. **5**A to **5**D are schematic cross-sectional views for showing a process of manufacturing the semiconductor device using the base substrate and the cap substrate formed by the processes shown in FIGS. **3**A to **3**C and **4**A to **4**C;

[0040] FIG. **6**A is a schematic cross-sectional view of a leading electrode thereof as a modification of a leading electrode of the semiconductor device shown in FIGS. **1**A and **1**B.

[0041] FIG. **6**B is a schematic cross-sectional view of a leading electrode as another modification of the leading electrode of the semiconductor device shown in FIGS. **1**A and **1**B.

[0042] FIGS. **7**A to **7**D and **8**A to **8**D are schematic cross-sectional views for showing a process of forming the leading electrodes shown in FIGS. **6**A and **6**B;

[0043] FIG. **9**A is a schematic cross-sectional view of a part of a semiconductor device as a modification of the semiconductor device shown in FIGS. **1**A and **1**B;

[0044] FIG. **9**B is a schematic cross-sectional view taken along a line IXB-IXB in FIG. **9**A;

[0045] FIG. **10**A is a schematic cross-sectional view of a leading electrode as a modification of a leading electrode of the semiconductor device shown in FIGS. **9**A and **9**B;

[0046] FIG. **10**B is a schematic cross-sectional view of a leading electrode as a modification of the leading electrode of the semiconductor device shown in FIGS. **9**A and **9**B;

[0047] FIGS. **11**A to **11**D are schematic cross-sectional views for showing a process of forming the leading electrode shown in FIG. **10**B;

[0048] FIG. **12**A is a schematic cross-sectional view of a leading electrode as further another modification of the leading electrode of the semiconductor device shown in FIGS. **9**A and **9**B;

[0049] FIG. **12**B is a schematic cross-sectional view taken along a line XIIA-XIIA in FIG. **12**A;

[0050] FIG. **13**A is a schematic cross-sectional view of a leading electrode as yet another modification of the leading electrode of the semiconductor device shown in FIGS. **9**A and **9**B;

[0051] FIG. **13**B is a schematic cross-sectional view of a leading electrode as still another modification of the leading electrode of the semiconductor device shown in FIGS. **9**A and **9**B;

[0052] FIG. **14**A is a schematic cross-sectional view of a part of a semiconductor device as a modification of the semiconductor device shown in FIGS. **9**A and **9**B;

[0053] FIG. **14**B is a schematic cross-sectional view of a part of a semiconductor device as another modification of the semiconductor device shown in FIGS. **9**A and **9**B;

[0054] FIG. **14**C is a schematic cross-sectional view of a leading electrode as a modification of a leading electrode of the semiconductor device shown in FIG. **14**B;

[0055] FIGS. **15**A to **15**C are schematic cross-sectional views for showing a process of manufacturing the semiconductor device shown in FIG. **14**A;

[0056] FIGS. **16**A to **16**D, **17**A to **17**D and **18**A to **18**C are schematic cross-sectional views for showing a process of forming the leading electrodes shown in FIGS. **14**B and **14**C;

[0057] FIG. **19**A is a schematic cross-sectional view of a part of a semiconductor device as a modification of the semiconductor device shown in FIGS. **1**A and **1**B;

[0058] FIG. **19**B is a schematic cross-sectional view of a part of a semiconductor device as another modification of the semiconductor device shown in FIG. **14**B;

[0059] FIGS. **20**A and **20**B are schematic cross-sectional views for showing a process of forming a leading electrode of the semiconductor device shown in FIG. **19**A;

[0060] FIGS. **21**A to **21**D are schematic cross-sectional views for showing a process of forming a leading electrode of the semiconductor device shown in FIG. **19**B;

[0061] FIG. **22** is a schematic cross-sectional view of a part of a semiconductor device as further another modification of the semiconductor device shown in FIGS. **1**A and **1**B;

[0062] FIG. **23** is a schematic cross-sectional view of a part of a semiconductor device as an example of another use of the semiconductor device shown in FIGS. **1**A and **18**;

[0063] FIG. **24** is a schematic cross-sectional view of a part of a semiconductor device as an example of the semiconductor device according to the embodiment;

[0064] FIGS. **25**A to **25**D and **26**A to **26**C are schematic cross-sectional views for showing a process of manufacturing the semiconductor device shown in FIG. **24**

[0065] FIG. **27** is a schematic cross-sectional view of a part of a semiconductor device as an example of the semiconductor device according to the embodiment;

[0066] FIGS. **28**A to **28**D and **29**A to **29**D are schematic cross-sectional views for showing a process of manufacturing the semiconductor device shown in FIG. **27**;

[0067] FIG. **30** is a schematic cross-sectional view of a part of a semiconductor device of a prior art; and

[0068] FIG. **31** is a schematic cross-sectional view of a part of a semiconductor device of another prior art.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENT

[0069] FIG. **1**A is a schematic plan view of a part of a semiconductor device **100** as an example of the semiconductor device according to an embodiment. FIG. **1**B is a schematic cross-sectional view taken along a line IB-IB in FIG. **1**A. FIG. **1**A is also a cross-section taken along a line IA-IA in FIG. **1**B. FIG. **2** is a perspective view of a base substrate of the semiconductor device **100** shown in FIGS. **1**A and **1**B.

[0070] In FIGS. **1**A, **1**B and **2** like parts which correspond to parts of the semiconductor devices **91**, **92** of FIGS. **30** and **31**, are designated with like reference characters.

[0071] Referring to FIGS. **1**A and **1**B, the semiconductor device **100** has a base substrate B**4** made of silicon and a cap substrate C**4** made of silicon. The base substrate B**4** and the cap substrate C**4** are bonded to each other at a bonding surface D**1**.

[0072] The semiconductor device **100** includes a mechanical quantity sensor element using an inertia force. A sensing portion Se for detecting mechanical quantity such as acceleration and angular velocity is formed in a predetermined region R**1** of the base substrate B**4**.

[0073] The cap substrate C**4** is formed with a recess **32***b*. The cap substrate C**4** is bonded to the base substrate B**4** to oppose the predetermined region R**1** where the sensing portion Se is formed. Thus, the cap substrate C**4** seals a space defined by the recess **32***b* and a trench **23** of the base substrate B**4**.

[0074] The base substrate B**4** is a SOI (Silicon On Insulator) substrate having an embedded oxide film **20**, a SOI layer **21** and a support substrate **22**. The embedded oxide film **20** is disposed between the SOI layer **21** and the support substrate **22**. The base substrate B**4** has multiple base semiconductor regions Bs including base semiconductor regions Bs**1**, Bs**2** in a surface layer thereof. The base semiconductor regions Bs are provided by the SOI layer **21**. The base semiconductor regions Bs are insulated and separated from each other by the trench **23** that reaches the embedded oxide film **20**.

[0075] The sensing portion Se includes a mechanical quantity sensor element for measuring acceleration or angular velocity. The mechanical quantity sensor element is constructed of some of the base semiconductor regions Bs.

[0076] The base semiconductor region Bs**1** is a movable semiconductor region including a movable electrode Em. The movable electrode Em is formed by performing sacrifice layer etching on a part of the embedded oxide film **20**. The movable electrode Em is displaceable. The base semiconductor region Bs**2** is a fixed semiconductor region including a fixed electrode Es that is opposed to the movable electrode Em.

[0077] In the semiconductor device **100**, capacitance is created between the opposed surfaces of the movable electrode Em and the fixed electrode Es. As the mechanical quantity is applied to the movable electrode Em, the movable electrode Em is displaced in a direction perpendicular to the opposed surfaces. The capacitance changes in accordance with a change in a distance between the opposed surfaces of the movable electrode Em and the fixed electrode Es. The change in capacitance is measured to detect the applied mechanical quantity. It is noted that, in the base substrate B**4**, other elements and circuits may be formed in regions other than the predetermined region R**1**.

[0078] The cap substrate C**4** includes a single crystal silicon **30**, which can be precisely processed at a relatively low cost. In the cap substrate C**4**, the recess **32***b* is formed at a position corresponding to the sensing portion Se of the base substrate B**4**. An insulating layer **32***a* is formed on a lower surface of the single crystal silicon substrate **30** bonded to the base substrate B**4**. The insulating layer **32***a* is, for example, made of silicon oxide (SiO_2).

[0079] In the semiconductor device **100**, as described above, the base substrate B**4** and the cap substrate C**4** are bonded to each other through the bonding surface D**1**. In a semiconductor device having a cap substrate as the semiconductor device **100**, the cap substrate is generally employed to protect various elements formed in a surface layer of a base substrate.

[0080] In the semiconductor device having the cap substrate, as a method of forming an electrical connection between the various elements formed in the surface layer of the base substrate and external parts, it may be possible to directly connect a bonding wire to a surface of, the base substrate by a wire bonding technique through a through hole formed in the cap substrate.

[0081] In such a method, however, the through hole of the cap substrate needs to be large enough to allow the wire bonding. Thus, an area for making the electrical connection is likely to increase.

[0082] In order to ease the electrical connection with a small area, a semiconductor device having a cap substrate needs a leading electrode that extends from the surface of a base substrate to an upper surface of the cap substrate to allow the electrical connection with an external part at an upper end thereof.

[0083] The semiconductor device **100** has a leading electrode De**1** that extends from the surface of the base substrate B**4** to an upper surface of the cap substrate C**4** for facilitating an electrical connection between the mechanical quantity sensor element of the base substrate B**4** and the external part.

[0084] The leading electrode De**1** includes a metal part **40** made of metal such as aluminum (Al), copper (Cu), chrome (Cr) tungsten (W), and platinum (Pt). A lower end of the leading electrode De**1** is connected to a predetermined base semiconductor region Bs. The leading electrode De**1** extends from the predetermined base semiconductor region Bs to the upper surface of the cap substrate C**4**, while passing through the cap substrate C**4**. Here, "extending to the upper surface of the cap substrate C**4**" means that an upper end of the leading electrode De**1** is located adjacent to the upper surface of the cap substrate C**4**. For example, the upper end of the leading electrode De**1** is located at the same height as or higher than the upper surface of the cap substrate C**4**.

[0085] A groove **35** is formed on a periphery of the leading electrode De**1**. In other words, the groove **35** is formed between an outer surface of the leading electrode De**1** and the cap substrate C**4**. The leading electrode De**1** is separated from the cap substrate C**4** by the groove **35**. FIG. **1**B shows a condition where a bonding wire **60** is connected to the upper end of the leading electrode De**1**.

[0086] In the semiconductor device **91** of FIG. **30**, the silicon cap substrate C**2** is divided into partial regions Ce through the insulating and separating trench **31**, and predetermined conductive regions Ce**1**, Ce**2** of the partial regions Ce, which connect to the insulated and separated base semiconductor region Bs, are used as the leading conductive regions to make electrical connections at the upper end thereof with the external parts by wire bonding, soldering or the like.

[0087] In the semiconductor device 92 of FIG. 31, the penetrating electrodes Ke, which are provided by portions of the silicon cap substrate C3 and separated through the grooves 15, are used to make electrical connections at the upper end thereof with the external parts by the wire bonding, soldering or the like.

[0088] In such structures, however, since the resistance of the silicon conductive regions and the silicon penetrating electrodes Ke is large, the applicable ranges of the semiconductor devices are likely to be restricted.

[0089] In the semiconductor device 100, on the other hand, the leading electrode De1 is provided by the metal part 40, which has high electric conductivity. The metal part 40 connects to the predetermined base semiconductor region Bs, that is, at a bonding portion Des shown by a dashed line in FIG. 2. The metal part 40 passes through the cap substrate C4, and the upper end of the metal part 40 is located higher than the upper surface of the cap substrate C4. Therefore, the resistance of the leading electrode De1 is smaller than the resistance of the conductive regions Ce1, Ce2 and the penetrating electrodes Ke of the semiconductor devices 91, 92, which utilize portions of the silicone cap substrates C2, C3. Accordingly, the applicable range of the semiconductor device 100 increases.

[0090] Further, the groove 35 is provided between the leading electrode De1 and the cap substrate C4. That is, the leading electrode De1 has a so-called air isolation structure. The cap substrate C4 of the semiconductor device 100 does not have the insulating and separating trench 31 for forming the partial regions Ce as the semiconductor device 91.

[0091] In the semiconductor device 100, therefore, parasitic capacitance will not be easily formed due to the electric substance such as the insulating and separating trench 31. Further, since the groove 35 is formed around the leading substrate de1, stress due to a thermal expansion difference between the leading electrode De1 and the cap substrate C4 can be reduced.

[0092] In the semiconductor device 92 of FIG. 31, since the groove 15 is formed around the penetrating electrode Ke, the parasitic capacitance will not be easily formed. In the semiconductor device 92 of FIG. 31, the groove 15 reaches the base substrate B3. In the semiconductor device 100 of FIGS. 1A and 1B, on the other hand, the insulating layer 32*a* is formed under the groove 35, and thus the groove 35 does not reach the base substrate B4.

[0093] In view of reducing the parasitic capacitance, the groove 15 passing through the cap substrate C3 and reaching the base substrate B3 is preferable as in the semiconductor device 92 of FIG. 31. Thus, it may be possible to form the groove 35 to reach the base substrate B4 in the semiconductor device 100.

[0094] In the semiconductor device 100, however, the insulating layer 32*a* is positioned at the bottom of the groove 35. That is, the insulating layer 32*a* is exists around the base of the leading electrode De1. Therefore, the insulating layer 32*a* serves as a support portion to increase the strength of the leading electrode De1, which is particularly required during the wire bonding or soldering the upper end of the leading electrode De1.

[0095] In the example shown in FIG. 1B, the upper end of the leading electrode De1 is located higher than the upper surface of the cap substrate C4. As compared with a case where the upper end of the leading electrode De1 is at the same height as or lower than the upper surface of the cap substrate C4, interference with peripheral portions is reduced. Therefore, the wire bonding and the soldering are easily conducted at the upper end of the leading electrode De1.

[0096] Accordingly, in the semiconductor device 100, the resistance of the leading electrode De1 is reduced and the parasitic capacitance will not be easily formed around the leading electrode De1.

[0097] As described above, the cap substrate C4 is provided by the single crystal silicon substrate 30, which is easily processed at a relatively low cost. Further, since the leading electrode De1 is constructed of the metal part 40, the cap substrate C4 can be provided by a poly crystal substrate, an intrinsic silicon substrate in which glass and impurities are not doped, or other similar insulating substrates, in place of the single crystal silicon substrate.

[0098] Next, a method of manufacturing the semiconductor device 100 will be described.

[0099] FIGS. 3A-3C are schematic cross-sectional views for showing a process of forming the base substrate B4.

[0100] In FIG. 3A, a SOI substrate B4*a* including the embedded oxide film 20 between the SOI layer 21 and the support substrate 22 is prepared. The SOI substrate B4*a* is formed by a substrate bonding technique, for example. The embedded oxide film 20 is a silicon oxide (SiO_2) film, and the support substrate 22 is a single crystal silicon substrate having a specific resistance in a range of 0.001 to 1 Ωcm, for example.

[0101] The SOI layer 21 is used for forming various elements. The SOI layer 21 is a single crystal silicon layer containing N+ type impurities such as arsenic (As) and phosphorous (P) with a specific resistance of 0.001 to 1 Ωcm and a thickness of 1 to 50 μm. For example, the SOI layer 21 has a thickness of 10 to 20 μm, and the SOI layer 21 and the support substrate 22 are formed by bonding N+ type single crystal substrates containing impurities at high concentrations.

[0102] In the case where the base semiconductor regions Bs are partly used as the movable semiconductor region Bs1 including the movable electrode Em and the fixed semiconductor region Bs2 including the fixed electrode Es, it is preferable that the concentration of impurities of the SOI layer 21 is as high as possible, that is, the specific resistance of the SOI layer 21 is as small as possible. In the above-described example, the SOI layer 21 contains the N+ type impurities. As another example, all the impurities can be P+ type impurities, such as born (B).

[0103] In FIG. 3B, a mask pattern (not shown) of such as a photoresist and an oxide film is formed on the SOI layer 21. A trench 23 that has substantially perpendicular walls and reaches the oxide film 20 is formed by photolithography and deep-etching techniques. By the trench 23, the SOI layer 21 is divided to form the multiple base semiconductor regions Bs, which are insulated and separated from adjacencies, in a surface layer of the SOI substrate B4*a*.

[0104] In FIG. 3C, after the mask pattern is removed from the SOI layer 21, the embedded oxide film 20 is partly removed through the trench 23 by an etching technique with hydrogen fluoride (HF) gas. Thus, the movable semiconductor region Bs1 including the movable electrode Em, the fixed semiconductor region Bs2 including the fixed electrode Es, and the like are formed. In this case, the portions of the oxide film 20 under the movable electrode Em and the fixed electrode Es are thoroughly removed, as shown in FIG. 3C.

[0105] In this way, the base substrate B**4** for the semiconductor device **100** is formed.

[0106] FIGS. **4**A to **4**C are schematic cross-sectional views for showing a process of forming the cap substrate C**4**.

[0107] In FIG. **4**A, the single crystal silicon substrate **30** is prepared. In FIG. **4**B, a mask pattern (not shown) of such as a photoresist or an oxide film is formed on a lower surface of the silicon substrate **30**. Then, the recess **32***b* is formed by photolithography and etching techniques.

[0108] In FIG. **4**C, the insulating layer **32***a* of the silicon oxide (SiO_2) is formed on the lower surface of the silicon substrate **30** by a thermal oxidation technique. In this way, the cap substrate C**4** for the semiconductor device **100** is formed.

[0109] FIGS. **5**A to **5**D are schematic cross-sectional views for showing process of manufacturing the semiconductor device **100** using the base substrate B**4** and the cap substrate C**4** respectively formed by the processes shown in FIGS. **3**A to **3**C and FIGS. **4**A to **4**D.

[0110] As shown in FIGS. **5**A and **5**B, the base substrate B**4** and the cap substrate C**4** are bonded to each other.

[0111] Specifically, in FIG. **5**A, the cap substrate C**4** is positioned relative to the base substrate B**4** such that the cap substrate C**4** is opposed to the predetermined region R**1** where the mechanical quantity sensor element has been formed, and is laid on the base substrate B**4**.

[0112] In FIG. **5**B, the lower surface of the cap substrate C**4** is bonded to the upper surface of the base substrate B**4**. Here, the cap substrate C**4** and the base substrate B**4** are bonded using an arbitrary adhesive. Thus, the cap substrate C**4** and the base substrate B**4** are securely bonded at the bonding surface D**1**, and the space defined by the recess **32***b* and the trench **23** is fully sealed.

[0113] Next, the leading electrode De**1** is formed, as shown in FIGS. **5**B to **5**D.

[0114] First, as shown in FIG. **5**B, a trench **41** is formed at a predetermined position of the cap substrate C**4**. In this case, the trench **41** is formed to reach the predetermined base semiconductor region Bs of the base substrate B**4**.

[0115] In FIG. **5**C, the metal part **40** is embedded in the trench **41**, and then an upper surface of the cap substrate C**4** is etched so that the upper end of the metal part **40** becomes higher than the upper surface of the cap substrate C**4**.

[0116] In FIG. **5**D, a portion of the silicon substrate **30** around the trench **41** in which the metal part **40** is embedded is etched to form the groove **35** around the trench **41**.

[0117] In this way, the leading electrode De**1** is formed, and the semiconductor device **100** is manufactured. It is noted that, in an actual manufacturing process, the base substrate B**4** and the cap substrate C**4** are prepared in the condition of wafers, and the finished semiconductor devices **100** are produced by cutting the wafers into multiple chips after the process of FIGS. **5**A to **5**D.

[0118] Next, modifications of the leading electrode De**1** and a neighboring structure thereof will be described in detail.

[0119] FIG. **6**A is a schematic cross-sectional view of the leading electrode De**1** and the neighboring structure thereof as a modification. FIG. **6**B is a schematic cross-sectional view of the leading electrode De**1** and the neighboring structure thereof as another modification.

[0120] In the modification shown in FIG. **6**A, an insulating layer **42** is formed at the bottom portion of the groove **35***a*. The insulating layer **42** is separate from the insulating layer **32***a*, and has a thickness greater than a thickness of the insulating layer **32***a*. In this case, therefore, strength of the leading electrode De**1** required for forming the electrical connection to the external part, that is, for conducting the wire bonding and the soldering, can be increased, as compared with a structure shown in FIG. **1**B.

[0121] In the modification shown in FIG. **5**B, a groove **35***b* is formed around the leading electrode De**1**. The groove **35***b* reaches the base substrate B**4**, similar to the structure around the penetrating electrode Ke of the semiconductor device **92** shown in FIG. **31**. In this case, therefore, parasitic capacitance due to the leading electrode De**1** can be further reduced, as compared with the structures shown in FIGS. **1**B and **6**A.

[0122] FIGS. **7**A to **7**D and **8**A to **8**D are schematic cross-sectional views for showing a process of forming the structures shown in FIGS. **6**A and **6**B. The process shown in FIGS. **7**A to **7**D and **8**A to **8**D is performed after the base substrate B**4** and the cap substrate C**4** are bonded in the manner shown in FIGS. **5**A and **5**B.

[0123] In FIG. **7**A, a silicon nitride (Si_3N_4) film **30***a* is formed on the single crystal silicon substrate **30** of the cap substrate C**4** by a low pressure chemical vapor deposition (LPCVD) technique or a plasma chemical vapor deposition (CVD) technique. The silicon nitride film **30***a* can be formed on the single crystal silicon substrate **30** before the cap substrate C**4** is bonded to the base substrate B**4**.

[0124] In FIG. **7**B, a mask pattern (not shown) of a photoresist is formed on the silicon nitride film **30***a*, and then a trench **41***a* is formed at a predetermined position of the cap substrate C**4** by etching from the top of the silicon nitride film **30***a*. The trench **41***a* is formed to reach the predetermined base semiconductor region Bs.

[0125] In FIG. **7**C, a silicon oxide film **42***a* is deposited on an entire surface, that is, on the silicon nitride film **30***a* and walls of the trench **42***a* by a plasma CVD technique.

[0126] In FIG. **7**D, the silicon oxide film **42***a* formed on the silicon nitride film **30***a* and the bottom wall of the trench **41***a* is removed. Thus, the silicon oxide film **42***a* on the side wall of the trench **41***a* remains.

[0127] Next, in FIG. **8**A, a metal layer **40***a*, which is for example made of aluminum (Al), is deposited on an entire surface, that is, on the silicon nitride film **30***a* and inside of the trench **41***a*. The trench **41***a* is filled with the metal layer **40***a*.

[0128] In FIG. **8**B, the metal layer **40***a* on the silicon nitride film **30***a* is removed by an etchback technique. Thus, the metal layer **40***a* inside of the trench **41***a* remains to form the metal part **40** of the leading electrode De**1** of FIGS. **6**A and **6**B.

[0129] In FIG. **8**C, the groove **35***a* is formed by removing the silicon oxide film **42***a* formed on the side wall of the trench **41***a*. The silicon oxide film **42***a* remains at a lower portion of the groove **35***a*. Thus, the insulating layer **42** shown in FIG. **6**A is formed.

[0130] In this way, the leading electrode De**1** and its neighboring portion shown in FIG. **6**A are formed.

[0131] The leading electrode De**1** and its neighboring portion shown in FIG. **6**B are formed by entirely removing the silicon oxide film **42***a* from the side walls of the trench **41***a*, as shown in FIG. **8**D.

[0132] As described in the above, after a bonding step shown in FIG. **7**A, trench forming step for forming the trench **41***a* in the cap substrate C**4** to reach the predetermined base semiconductor region Bs is performed. In a subsequent leading electrode forming step, the meal layer **40***a* is embedded in

the trench **41***a* to form the metal part **40** of the leading electrode De**1**. Then, the groove **35***a*, **35***b* is formed at portions of the trench **41***a*.

[0133] FIG. **9**A is a schematic plan view of a part of a semiconductor device **110** as a modification of the semiconductor device **100** shown in FIGS. **1**A and **1**B. FIG. **9**B is a schematic cross-sectional view taken along a line IXB-IXB in FIG. **9**A. FIG. **9**A is also a schematic cross-sectional view taken along a line IXA-IXA in FIG. **9**B. In the semiconductor device **110** shown in FIGS. **9**A and **9**B, like parts are denoted by like reference characters as those of the semiconductor device **100** shown in FIGS. **1**A and **1**B.

[0134] As shown in FIGS. **9**A and **9**B, the semiconductor device **110** has the same base substrate B**4** as that of the semiconductor device **100** of FIGS. **1**A and **1**B. With regard to a cap substrate C**5** of the semiconductor device **110**, a leading electrode De**2** and its neighboring structure are different from the leading electrode De**1** and its neighboring structure of the cap substrate C**4** of the semiconductor device **100**

[0135] The leading electrode De**1** of the semiconductor device **100** is constructed of only the metal part **40**. Further, although the groove **35** is formed between the cap substrate C**4** and the leading electrode De**1**, the cap substrate C**4** is constructed of a single member, that is, the silicon substrate **30**.

[0136] With regard to the cap substrate C**5** of the semiconductor device **110**, on the other hand, a groove **36** is formed in the single crystal silicon substrate **30** to divide the single crystal silicon substrate **30** into a portion surrounding the leading electrode De**2** and its peripheral portion. That is, the cap substrate C**5** is divided into multiple partial regions Cs by the grooves **36**. The partial regions Cs are insulated and separated by the grooves **36**. The leading electrode De**2** is constructed of a predetermined partial region Cs**1** and the metal part **40** formed in the predetermined partial region Cs**1**.

[0137] Similar to the semiconductor device **100** of FIGS. **1**A and **1**B, the leading electrode De**2** of the semiconductor device **110** has the metal part **40** that contacts the base semiconductor region Bs and extends to the upper surface of the cap substrate C**5**. As such, the resistance of the leading electrode De**2** is reduced, as compared with that in the semiconductor devices **91**, **92** of FIGS. **30**, **31**. With this, the applicable range increases.

[0138] The groove **36** is formed between the leading electrode De**2** and the cap substrate C**5**, similar to the semiconductor device **100** of FIGS. **1**A and **1**B Therefore the parasitic capacitance will not be easily formed on a periphery of the leading electrode De**2**.

[0139] The leading electrode De**2** of the semiconductor device **110** is different from the leading electrode De**1** of the semiconductor device **100** since the leading electrode De**2** includes the predetermined partial region Cs**1** as an element in addition to the metal part **40**. The predetermined partial region Cs**1** is formed around the metal part **40**, but is insulated and separated from the adjacent partial portion Cs by the groove **36**.

[0140] In the semiconductor device **110**, therefore, the resistance can be reduced by the metal part **40** as the element of the leading electrode De**2**. Furthermore, because the predetermined partial region Cs**1** around the metal part **40** serves as a support part, strength of the leading electrode De**2** required at the time of wire bonding and soldering can be increased.

[0141] In the case where the cap substrate C**5** is divided into multiple partial regions Cs, which are insulated and separated from each other, as the semiconductor device **110**, integrated circuits (IC circuits) can be formed in other partial regions Csa, Csb of the partial regions Cs, as shown in FIG. **9**A.

[0142] FIGS. **10**A and **10**B are schematic cross-sectional views of the leading electrode De**2** and the neighboring portion thereof as modifications of the structure shown in FIGS. **9**A and **9**B.

[0143] In the modification shown in FIG. **10**A, a groove **36***a* is formed to pass through the cap substrate C**5** and reach the base substrate B**4**, similar to the groove **35***b* shown in FIG. **6**B. Therefore, in the structure shown in FIG. **10**A parasitic capacitance due to the leading electrode De**2** is further reduced, as compared with the structure shown in FIGS. **9**A and **9**B.

[0144] In the modification shown in FIG. **10**B, the silicon nitride film **30***a* remains, which has been formed at the beginning of the forming of the leading electrode De**2** as shown in FIG. **7**A, on the single crystal silicon substrate **30**. Further, the upper end of the metal part **40** is on the same height as the upper surface of the silicon nitride film **30***a*. That is, the silicon nitride film **30***a* is formed above the predetermined partial region Cs**1** formed around the metal part **40**, and the upper surface of the silicon nitride film **30** is coplanar with the upper surface of the metal part **40**.

[0145] In such a structure, because the silicon nitride film **30***a* serves as a support portion, strength of the leading electrode De**2** required at the time of wire bonding and soldering is increased, as compared with that of the leading electrode shown in FIG. **10**A.

[0146] FIGS. **11**A to **11**D are schematic cross-sectional views for showing a process of forming the leading electrode De**2** and its neighboring structure shown in FIG. **10**B.

[0147] The process begins from the similar condition shown in FIG. **7**A after the base substrate B**4** and the cap substrate C**5** are bonded. As shown in FIG. **11**A, a mask pattern (not shown) of a photoresist is formed on the silicon nitride film **30***a*, and then a trench **41***a* is formed at a predetermined position of the cap substrate C**5** by etching from the top of the silicon nitride film **30***a*. The trench **41***a* is formed to reach the predetermined base semiconductor region Bs.

[0148] In FIG. **11**B the metal layer **40***a* is deposited on an entire surface, that is, over the silicon nitride film **30***a* and inside of the trench **41***a*. Thus, the trench **41***b* is filled with the metal layer **40***a*.

[0149] In FIG. **11**C, the metal layer **40***a* above the silicon nitride film **30***a* is removed by an etchback technique. The metal layer **40***a* inside of the trench **41***b* remains to form the metal part **40** of the leading electrode De**2** shown in FIG. **10**B.

[0150] In FIG. **11**D, a mask pattern (not shown) of a photoresist is formed on the silicon nitride film **30***a*, and the groove **36***a* is formed by etching from the top of the mask pattern.

[0151] In this way, the leading electrode De**2** and its neighboring structure shown in FIG. **10**B are formed. It is noted that the leading electrode De**2** and its neighboring structure shown in FIG. **10**A are formed by removing the silicon nitride film **30***a* after the step shown in FIG. **11**D. It is also noted that the leading electrode De**2** and its neighboring structure shown in FIG. **9**B are formed by forming the groove **36***a* while remaining the insulating layer **32***a* at the bottom of the groove **36***a* in the step of FIG. **11**D and further removing the silicon nitride film **30***a* after the step of FIG. **11**D.

[0152] FIG. **12**A is a plan view of the leading electrode De**2** and the neighboring structure thereof as further another modification of the structure shown in FIGS. **9**A and **9**B. FIG. **12**B is a schematic cross-sectional view taken along a line XIIB-XIIB in FIG. **12**A. FIG. **12**A is also across-section taken along a line XIIA-XIIA in FIG. **12**B.

[0153] A cap substrate C**10** shown in FIGS. **12**A and **12**B includes an insulating substrate **30***z* made of intrinsic silicon in which impurities are not doped. That is, the cap substrate C**10** is different from the cap substrate C**5** of FIGS. **9**A, **9**B, **10**A and **10**B, which includes the single crystal silicon substrate **30** in which the impurities are doped.

[0154] Further, as shown in FIG. **12**A, a groove **36***b* having a substantially C-shape is formed around the metal part **40** of the leading electrode De**2**. A portion of the substrate **30***z* formed around the metal, part **40** is connected to an adjacent portion of the substrate **30***z*, that is, on a periphery of the groove **36***b* through an opening of the C-shape of the groove **36***b*.

[0155] Therefore, in the structure shown in FIGS. **12**A and **12**B, strength of the leading electrode De**2** required at the time of wire bonding and soldering is further increased, as compared with the structures shown in FIGS. **9**A, **9**B and **10**A. Since the substrate **30***z* has an insulating property, the metal part **40** of the leading electrode De**2** is electrically insulated from a peripheral portion.

[0156] FIGS. **13**A and **13**B are schematic cross-sectional views of a leading electrode De**3** and a neighboring structure thereof as still other modifications of the structure shown in FIGS. **9**A and **9**B.

[0157] The leading electrodes De**3** shown in FIGS. **13**A and **13**B are provided by subdividing the leading electrodes De**2** of FIGS. **10**A and **10**B, respectively. That is, the metal part **40** is constructed of multiple portions in a predetermined partial region Cs**2**, which is one of the partial regions Cs and separated and insulated from a peripheral partial region Cs by the groove **36***a*.

[0158] In the structure shown in FIG. **13**A, the silicon nitride film **30***a* formed above the single crystal silicon substrate **30** during the manufacturing process is removed. In the structure shown in FIG. **13**B, the silicon nitride film **30***a* remains on the single crystal silicon substrate **30**.

[0159] In the structures shown in FIGS. **13**A and **13**B, stress due to a thermal expansion difference between the metal part **40** and the partial region Cs**2** made of silicon is further reduced, as compared with the structures shown in FIGS. **10**A and **10**B.

[0160] In the structure shown in FIG. **13**A, at the time of wire bonding or soldering, the bonding wire **60** and the solder can be embedded between the divided portions of the metal part **40**, which protrude higher than the upper surface of the partial region Cs**2**. Therefore, reliability of connection improves.

[0161] FIG. **14**A is a schematic cross-sectional view of a part of a semiconductor device **111** as a modification of the semiconductor device **110** shown in FIGS. **9**A and **9**B. FIG. **14**B is a schematic cross-sectional view of a part of a semiconductor device **112** as another modification of the semiconductor device **110** shown in FIGS. **9**A and **9**B. FIG. **14**C is a schematic cross-sectional view of a leading electrode De**5** and its neighboring structure as a modification of a leading electrode De**5** and its neighboring structure of the semiconductor device **112** shown in FIG. **14**B.

[0162] The base substrates B**4** of the semiconductor devices **111**, **112** are the same as the base substrates B**4** of the semiconductor devices **100**, **110** of FIGS. **1**A, **1**B, **9**A and **9**B. The semiconductor devices **111**, **112** have cap substrates C**7**, C**8** and leading electrodes De**4**, De**5**, which have different structures from the cap substrates C**5** and the leading electrode De**2** of the semiconductor device **110** of FIGS. **9**A and **9**B.

[0163] The leading electrode De**2** of the semiconductor device **110** is constructed of the predetermined partial region Cs**1** and the metal part **40** formed at the center of the partial region Cs**1**. On the other hand, the leading electrode De**4** of the semiconductor device **111** is constructed of a predetermined partial region Cs**3**, which is one of the partial regions Cs, and the metal part **40** that covers a side wall and an upper surface of the partial region Cs**3**.

[0164] That is, in the leading electrode De**4** of the semiconductor device **111**, since the metal part **40** covers the upper surface of the partial region Cs**4**, connecting area between the metal part **40** and the bonding wire or the solder is increased, as compared with the leading electrode De**2** of the semiconductor device **110** shown in FIGS. **9**A and **9**B in which the metal part **40** does not cover the upper surface of the partial region Cs**1**. Therefore, the electrical connection further improves.

[0165] The leading electrode De**5** of the semiconductor device **112** is constructed of the predetermined partial region Cs**4** and the metal part **40** covering a lower surface of the partial region Cs**4** in addition to the side wall and the upper surface of the partial region Cs**4**. In this case, the connection between the leading electrode De**5** and the predetermined base semiconductor region Bs of the base substrate B**4** further improves, as compared with the connection between the leading electrode De**4** and the predetermined base semiconductor region Bs of the semiconductor device **111** shown in FIG. **14**A.

[0166] The metal part **40** of the leading electrode De**4** of the semiconductor device **111** connects to the base semiconductor region Bs and extends to the same height as or higher than the upper surface of the cap substrate C**7**. Similarly, the metal part **40** of the leading electrode De**5** of the semiconductor device **112** connects to the base semiconductor region Bs and extends to the same height as or higher than the upper surface of the cap substrate C**8**. As such, in the semiconductor devices **111**, **112**, resistance of the leading electrodes De**4**, De**5** is reduced, as compared with that of the semiconductor devices **91**, **92** of FIGS. **30** and **31**. Therefore, the applicable ranges of the semiconductor devices **111**, **112** increase.

[0167] In addition, in the semiconductor device **111** of FIG. **14**A, a groove **37***a* is formed between the leading electrode De**4** and the cap substrate C**7**. Therefore parasitic capacitance will not be easily formed on a periphery of the leading electrode De**4**.

[0168] Likewise in the semiconductor device **112** of FIG. **14**B, a groove **37***b* is formed between the leading electrode De**5** and the cap substrate C**8**. Therefore, parasitic capacitance will not be easily formed on a periphery of the leading electrode De**5**.

[0169] In the leading electrode De**5** and the neighboring structure thereof shown in FIG. **14**C, a groove **37***c* is formed around the leading electrode De**5**, and an insulating layer **43**, which is separate from the insulating layer **32***a* of the cap substrate C**8**, is formed at the bottom portion of the groove **37***c*. Therefore, strength of the leading electrode De**5** of FIG.

140 required at the time of wire bonding and soldering is increased, as compared with that of the leading electrode De5 of FIG. 14B.

[0170] FIGS. 15A to 15C are schematic cross-sectional views for showing a process of forming the semiconductor device 111 of FIG. 14A.

[0171] In FIG. 15A, after the base substrate B4 and the cap substrate C7 are bonded to each other in a similar manner as shown in FIGS. 5A and 5B, the groove 37a is formed at a predetermined position of the cap substrate C7 to reach the insulating layer 32a. Thus, the single crystal silicon substrate 30 is divided into the partial regions Cs including a partial region Cs3.

[0172] In FIG. 15B, the insulating layer 32a at the bottom portion of the groove 37a is further etched to form a trench 41c reaching the predetermined base semiconductor region Bs of the base substrate B4.

[0173] In FIG. 15C, the metal part 40 is formed successively inside the trench 41c, on the side wall of the partial region Cs3, and on an upper surface of the partial region Cs3.

[0174] In this way, the leading electrode De4 is formed, and thus the semiconductor device 111 of FIG. 14A is manufactured.

[0175] FIGS. 16A to 16D, 17A to 17D and 18A to 180 are schematic cross-sectional views for showing a process of forming the leading electrodes De5 and neighboring structures thereof shown in FIGS. 14B and 14C.

[0176] The process of forming the leading electrode De5 of the semiconductor device 112 shown in FIG. 14B is different from the processes of forming the leading electrodes De1 to De4. To form the leading electrode De5 of the semiconductor device 112 shown in FIG. 14B necessary structures are formed in the cap substrate C8 before the base substrate B4 and the cap substrate C8 are bonded to each other.

[0177] In FIG. 16A, the single crystal silicon substrate 30 is prepared. A mask pattern (not shown) of a photoresist is formed on the single crystal silicon substrate 30, and then a trench 41d is formed by etching from the top.

[0178] In FIG. 16B, a metal layer 40b made of such as aluminum (Al) is deposited entirely over the single crystal silicon substrate 30 including the trench 41d.

[0179] In FIG. 16C, a silicon oxide (SiO_2) film 43a is deposited entirely over the metal layer 40b by a plasma CVD technique.

[0180] In FIG. 16D, the silicon oxide film 43a is removed by an etchback technique so that the metal layer 40b on the surface of the single crystal silicon substrate 30 exposes, and only, the silicon oxide film 43a inside of the trench 41d remains.

[0181] Next, in FIG. 17A, a predetermined mask pattern (not shown) is formed, and the metal layer 40b is partly removed by an etching technique.

[0182] In FIG. 17B, the single crystal silicon substrate 30 is turned upside down, and then is grinded from the top so that the silicon oxide film 43a embedded inside of the trenches 41d is exposed. In this way, the single crystal silicon substrate 30 is divided to form the insulated and separated multiple partial regions Cs including a partial region Cs4.

[0183] In FIG. 17C, a metal layer 40c made of such as aluminum (Al) is deposited entirely over the single crystal silicon substrate 30.

[0184] In FIG. 17D, a predetermined mask pattern (not shown) is, formed on the metal layer 40c, and then the metal layer 40c is partly removed by etching. Thus, the metal part 40 that covers the side wall, the upper surface and the lower surface of the partial region Cs4 is formed.

[0185] By the above steps, the cap substrate C8 before being bonded is formed.

[0186] Next, in FIG. 18A, the base substrate B4 and the cap substrate C8, which have been formed beforehand, are bonded to each other.

[0187] In FIG. 18B, the trench 37c is formed by etching the silicon oxide film 43a from the top. The silicon oxide film 43a remains at the bottom of the trench 37c to provide the insulating layer 43.

[0188] By the above steps, the leading electrode De5 and its neighboring structure shown in FIG. 14C are formed.

[0189] If the silicon oxide film 43a is fully removed by the etching, the groove 37b is formed as shown in FIG. 18C. Thus, the leading electrode De5 and its neighboring structure shown in FIG. 14B are formed.

[0190] As described in the above, the leading electrode forming process can be partly conducted during the cap substrate forming process. That is, the leading electrode De5 can be formed in a condition of being connected to the cap substrate C8 while the cap substrate C8 is formed. Then, the lower surface of the leading electrode De5 is connected to the predetermined base semiconductor region Bs while the cap substrate C8 is bonded to the base substrate B4. Thereafter, the grooves 37b, 37c are formed.

[0191] FIG. 19A is a schematic cross-sectional view of a part of a semiconductor device 113 as a modification of the semiconductor device 100 shown in FIGS. 1A and 1B. FIG. 19B is a schematic cross-sectional view of a part of a semiconductor device 114 as a modification of the semiconductor device 112 shown in FIG. 14B.

[0192] In the semiconductor device 113 shown in FIG. 19A, a leading electrode De6 has an upper surface to which the electrical connection is formed such as by the wire bonding and the soldering. The upper surface has an area greater than that of a lower surface, which is connected to the base semiconductor region Bs to form the bonding portion Des. Similarly, a leading electrode De7 of the semiconductor device 114 shown in FIG. 19B has an upper surface with an area greater than a lower surface thereof.

[0193] In such cases, a pad area increases, as compared with a case where the upper surface of a leading electrode has an area smaller than or the same as an area of the lower surface thereof. Therefore, the wire bonding and the soldering to the upper surface of the leading electrodes De6, De7 are easily conducted.

[0194] FIGS. 20A and 20B are schematic cross-sectional views for showing a process of forming the leading electrode De6 and its neighboring structure of the semiconductor device 113 shown in FIG. 19A.

[0195] As shown in FIG. 20A, the process begins from the condition shown in FIG. 8A. In FIG. 20A, the metal layer 40a formed on the silicon nitride film 30a is etched in a predetermined pattern so that the metal part 40 having the upper surface with the greater area than its lower surface is formed.

[0196] In FIG. 20B, the silicon oxide film 42a on the side wall of the trench 41a and the silicon nitride film 30a on the single crystal silicon substrate 30 are removed in a predetermined order to form the groove 35b.

[0197] In this way, the leading electrode De6 and its neighboring structure of the semiconductor device 113 shown in FIG. 19A are formed.

[0198] FIGS. **21**A to **21**D are schematic cross-sectional views for showing a process of forming the leading electrode De**7** and its neighboring structure of the semiconductor device **114** shown in FIG. **19**B.

[0199] As shown in FIG. **21**A, the process begins from the condition shown in FIG. **17**B. In FIG. **21**A, the metal layer **40***c* made of such as aluminum (Al) is deposited over an entire surface of the single crystal silicon substrate **30** with a thickness greater than a thickness of the metal layer **40***c* of FIG. **17**C

[0200] In FIG. **21**B, the metal layer **40***c* is etched in a predetermined pattern. Thus, the metal part **40** having the upper surface with the greater area than that of the lower surface is formed.

[0201] In FIG. **21**C, the base substrate B**4** and the cap substrate C**8**, which have been prepared beforehand are bonded to each other.

[0202] In FIG. **21**D the silicon oxide film **43***a* is fully removed by an etching technique to form the groove **37***b*.

[0203] In this way, the leading electrode De**1** and its neighboring structure of the semiconductor device **114** shown in FIG. **19**B is formed.

[0204] FIG. **22** is a schematic cross-sectional view of a part of a semiconductor device **115** as further another modification of the semiconductor device **100** shown in FIGS. **1**A and **1**B.

[0205] The semiconductor device **115** shown in FIG. **22** has an integrated circuit (IC circuit) **101** on a partial region Csc of the single crystal silicon substrate **30** in addition to the structure of the semiconductor device **100** shown in FIG. **1**B. The partial region Csc is one of the partial regions Cs of the cap substrate C**4**, and seals the sensing portion Se of the base substrate B**4**. In the case where the single crystal silicon substrate is used for the cap substrate, in this way, the integrated circuit can be formed in the predetermined partial region of the cap substrate, which is insulated and separated.

[0206] FIG. **23** is a schematic cross-sectional view of a part of the semiconductor device **100** for showing another applicable example.

[0207] In the example shown in FIG. **1**B, the upper end of the leading electrode De**1** is exemplarily connected to the wire bonding **60** to be electrically connected to an external part. In the example shown in FIG. **23**, on the other hand, the semiconductor device **100** is mounted to a separate single crystal silicon substrate **70** having an integrated circuit (IC circuit) IC**2** by a flip-chip technique. The end surfaces of the metal parts **40** constructing the leading electrodes De**1** are electrically connected to pad electrodes **71** formed on the single crystal silicon substrate **70** by solders **61**. In this way, the electrical connections of the end surfaces of the leading electrodes De**1** to the external parts can be formed by either the wire bonding or the soldering.

[0208] FIG. **24** is a schematic cross-sectional view of a part of a semiconductor device **120** as an example of the semiconductor device according to the embodiment. The semiconductor device **120** has two base substrates B**5**, B**6** and a cap substrate C**9**. The base substrates B**5**, B**6** are bonded on opposite sides of the cap substrate C**9**.

[0209] For example, the base substrate B**5** is provided with an angular velocity sensor element (a gyro sensor element). The base substrate B**6** is provided with an acceleration sensor element.

[0210] In the semiconductor device **120** shown in FIG. **24**, the base substrate B**5** and the second substrate B**6** are electrically connected to each other through leading electrodes De**8** formed in the cap substrate C**9**. Although the semiconductor device **120** carries the angular velocity sensor element and the acceleration sensor element, it is configured compact and wiring resistance of the semiconductor device **120** is reduced.

[0211] The cap substrate C**9** has a groove **38** formed to divide the single crystal silicon substrate **30**. That is, the cap substrate C**9** is divided into multiple partial regions Cs, which are insulated and separated from each other, by the groove **38**. The leading electrode De**8** is constructed of the predetermined partial region Cs**5** of the partial regions Cs and the metal part **40** formed around the partial region Cs**5**. For example, the metal part **40** is formed on the side wall of the partial region Cs**5**.

[0212] The metal part **40** connects to the base semiconductor region Bs and extends to the upper surface of the cap substrate C**9**. For example, both the end surfaces of the metal part **40** are on the same heights as the opposite surfaces of the cap substrate C**9** and connect to the base semiconductor regions Bs of the base substrates **85**, B**6**.

[0213] Also in such a case, resistance of the leading electrode De**8** is reduced, and thus the applicable range, of the semiconductor device **120** increases. Further, the groove **38** is formed between the leading electrode De**8** and the cap substrate C**9**. Thus, parasitic capacitance will not be easily formed on a periphery of the leading electrode De**8**.

[0214] FIGS. **25**A to **25**D and FIGS. **26**A to **26**C are schematic cross-sectional views for showing a process of manufacturing the semiconductor device **120** shown in FIG. **24**.

[0215] In FIG. **25**A, the base substrate B**5** having the angular velocity sensor element is formed.

[0216] In FIG. **25**B, a primary cap substrate C**9***a* having a primary leading electrode De**8***a*, which will be the leading electrode De**8**, is formed. For example, a primary groove **38***a* is formed in the single crystal silicon substrate **30** of the primary cap substrate C**9***a*, and further a metal layer **40***d* is formed inside of the primary groove **38***a*.

[0217] In FIG. **25**C, the primary cap substrate C**9***a* shown in FIG. **25**B is bonded to the base substrate B**5** shown in FIG. **25**A. For example, the primary cap substrate C**9***a* and the base substrate B**5** are bonded to each other by a silicon direct bonding technique, which is conducted at a low temperature in a vacuum state.

[0218] In FIG. **25**D, the primary cap substrate C**9***a* is grinded from the top to a position where the primary groove **38***a* penetrates through the primary cap substrate C**9***a*. In this way, the groove **38** of the semiconductor device **120** is formed. The cap substrate C**9** is provided by the primary cap substrate C**9***a*, which is divided into the multiple partial regions Ce by the groove **38**, and the metal part **40** as the element of the leading electrode De**8** is provided by the metal layer **40***d*.

[0219] Next, in FIG. **26**B, the primary base substrate B**6***a*, which has been formed to have the acceleration sensor element as shown in FIG. **26**A, is turned upside down and bonded to the cap substrate C**9**.

[0220] Then, in FIG. **26**C, wiring processing for making electrical connections is conducted in the primary base substrate B**6***a*, and thus the base substrate B**6** is finished.

[0221] In this way, the semiconductor device **120** shown in FIG. **24** is manufactured.

[0222] As described in the above, the primary groove **38***a* is formed in the primary cap substrate C**9***a* in the cap substrate forming step. Then, the metal layer **40***d* is formed on the side wall of the primary groove **38***a*, as a part of the leading electrode forming step, to form a primary leading electrode De**8***a*. In a substrate bonding step shown in FIG. **25**C, the base substrate B**5** and the primary cap substrate C**9***a* are bonded in such a manner that the opening of the primary groove **38***a* is opposed to the upper surface of the base substrate B**5**. After the substrate bonding step, as shown in FIG. **25**D, the primary cap substrate C**9***a* is grinded from the top, that is, from a side opposite to the base substrate B**5**, to make the cap substrate C**9**. Thus, the primary leading electrode De**8***a* and the primary groove **38***a*, respectively, become the leading electrode De**8** and the groove **38**. The metal layer **40***d* formed on the side wall of the primary groove **38***a* becomes the metal part **40** of the leading electrode De**8**.

[0223] In each of the above-described semiconductor devices **100**, **110** to **114** and **120** as examples of the semiconductor device according to the embodiment, the cap substrate C**4** to C**10** is bonded to the base substrate B**4** to B**6** to protect the base substrate B**4** to B**6**. Further, the leading electrode De**1** to De**8** for making the electrical connection with the external part at the end thereof is formed such that the resistance of the leading electrode De**1** to De**8** is reduced and the parasitic capacitance around the leading electrode De**1** to De**8** will not be easily formed.

[0224] The above-described semiconductor devices **110**, **110** to **114** and **120** as examples of the semiconductor device according to the embodiment each has the mechanical quantity sensor element for detecting acceleration and/or angular velocity. As another example, the semiconductor device according to the embodiment can have pressure sensor element, micro electro mechanical system (MEMS) resonator, infrared radiation sensor element, or any other semiconductor sensor element.

[0225] FIG. **27** is a schematic cross-sectional view of a semiconductor device **130** having a pressure sensor element PS as an example of the semiconductor device according to the embodiment. In FIG. **27**, parts similar to the preceding parts are denoted with like reference characters.

[0226] The semiconductor device **130** has a base substrate B**7**. The base substrate B**7** includes a single crystal silicon substrate **25**. The thin single crystal silicon layer **24** having different conductivity types is formed at an upper surface layer of the single crystal silicon substrate **25**. A deep, groove **26** is formed at a predetermined region R**2** of the base substrate B**7**. The groove **26** extends from a bottom surface to an upper surface of the single crystal silicon substrate **25**, and a membrane Me is formed above the groove **26**. The single crystal silicon layer **24** has multiple impurity diffused regions (base semiconductor regions) Bd, which are insulated and separated from adjacencies by PN-junction separation, in the predetermined region R**2**.

[0227] The membrane Me also has impurity diffused regions Bd**1**, Bd**2**. The impurity diffused regions Bd**1**, Bd**2** serve as a pressure sensor element PS. That is, in the semiconductor device **130**, the membrane Me displaces in accordance with pressure applied through the groove **26**. Thus, a change in resistance of the impurity diffused regions Bd**1**, Bd**2** in accordance with the displacement is measured to detect the applied pressure.

[0228] Also in the semiconductor device **130**, a cap substrate C**11** is bonded to the base substrate B**7** made of silicon at the bonding surface D**1** and a sealed space is formed above the membrane Me. The semiconductor device **130** has a leading electrode De**9** constructed of the metal part **40**. A lower end of the leading electrode De**9** connects to an impurity diffused region (base semiconductor region) Bd**3** of the base substrate B**7**. The leading electrode De**9** extends from the upper surface of the base substrate B**7** to the upper surface of the cap substrate C**4** through the groove **35** of the cap substrate C**11**. For example, an upper end of the metal part **40** is located higher than the upper surface of the cap substrate C**11**. The bonding wire **60** is connected to an upper end of the leading electrode De**9**.

[0229] FIGS. **28**A to **28**D and FIGS. **29**A to **29**D are schematic cross-sectional views for showing a process of manufacturing the semiconductor device **130** shown in FIG. **27**.

[0230] In FIG. **28**A, the base substrate **87** is formed. Specifically, the thin single crystal silicon layer **24** having the different conductivity types is formed at the upper surface layer of the single crystal silicon substrate **25**.

[0231] In FIG. **18**B, structures such as the impurity diffused regions (base semiconductor regions) Bd, Bd**1** to Bd**3** as shown in FIG. **27**, except the groove **26**, are formed in the predetermined region R**2** of the single crystal silicon layer **24**.

[0232] In FIG. **28**C, the cap substrate C**11** is formed. For example, the insulating layer **32***a* and the recess **32***b* are formed on the lower surface of the single crystal silicon substrate **30**, in the similar manner as the cap substrate forming process shown in FIGS. **4**A to **4**C.

[0233] In FIG. **28**D, the base substrate B**7** formed in the step shown in FIG. **28**B and the cap substrate C**11** formed in the step shown in FIG. **28**C are positioned relative to each other and bonded to each other.

[0234] Next, in FIG. **29**A, a trench **44** is formed at a predetermined position of the cap substrate C**11** to reach the impurity diffused region Bd**3** of the base substrate B**7**.

[0235] In FIG. **29**B, the metal part **40** is embedded in the trench **44**, and then the upper surface of the cap substrate C**11**, that is, the upper surface of the single crystal silicon substrate **30** is etched such that the upper end of the metal part **40** is located higher than the upper surface of the cap substrate C**11**.

[0236] In FIG. **29**C, a peripheral portion of the trench **44** in which the metal part **44** has been embedded is etched to form the groove **35**.

[0237] In FIG. **29**D, the bonded base substrate B**7** and cap substrate C**11** is turned upside down, and the groove **26** is formed from a back side, that is, from the top in FIG. **29**D. Thus, the membrane Me, as a thin membrane portion, is formed. Accordingly, the pressure sensor element PS is formed.

[0238] In this way, the semiconductor device **130** shown in FIG. **27** is manufactured.

[0239] Similar to the semiconductor device **100** shown in FIGS. **1**A and **1**B, the semiconductor device **130** shown in FIG. **27** has the leading electrode De**9** constructed of the metal part **40**, and the groove **35** is formed between the metal part **40** and the cap substrate C**11**. The upper end of the leading electrode De**9** allows the electrical connection with the external part. Therefore, resistance of the leading electrode De**9** is reduced, and parasitic capacitance will not be easily formed around the leading electrode De**9**.

[0240] The semiconductor device according to the embodiment can be implemented by combining the above described exemplary semiconductor devices in various ways. Also, as an example of the semiconductor device according to the embodiment, a semiconductor device having a chip in which the mechanical quantity sensor elements, such as the acceleration sensor element and the angular velocity sensor element as shown in FIG. **1** and the pressure sensor element PS as shown in FIG. **27** are formed and the leading electrode constructed of the metal part separated from the cap substrate by the groove is applicable.

[0241] Additional advantages and modifications will readily occur to those skilled in the art. The invention in its broader term is therefore not limited to the specific details, representative apparatus, and illustrative examples shown and described.

What is claimed is:

1. A semiconductor device comprising:

a base substrate made of silicon, the base substrate having a plurality of base semiconductor regions in a predetermined portion of a surface layer thereof, the plurality of base semiconductor regions being insulated and separated from each other;

a cap substrate bonded to the predetermined portion of the surface layer of the base substrate; and

a leading electrode including a metal part, the leading electrode passing through the cap substrate, the leading electrode having a first end connected to one of the plurality of base semiconductor regions of the base substrate and a second end located adjacent to a surface of the cap substrate for allowing an electrical connection with an external part, the surface being opposite to a bonding surface at which the base substrate and the cap substrate are bonded, wherein the leading electrode defines a groove between an outer surface thereof and the cap substrate.

2. The semiconductor device according to claim **1**, wherein the cap substrate is made of silicon.

3. The semiconductor device according to claim **2**, wherein

the cap substrate has a plurality of partial regions insulated and separated from each other,

the leading electrode is constructed of the metal part and one of the plurality of partial regions, and

the metal part is disposed around the one of the plurality of partial regions.

4. The semiconductor device according to claim **3**, wherein

the metal part is disposed to cover an end surface of the one of the partial regions, the end surface being adjacent to the second end of the leading electrode.

5. The semiconductor device according to claim **1**, wherein the cap substrate is made of single crystal silicon.

6. The semiconductor device according to claim **5**, wherein

the cap substrate includes a plurality of partial regions insulated and separated from each other, and

one of the plurality of partial regions is provided with an integrated circuit.

7. The semiconductor device according to claim **1**, wherein

the second end of the leading electrode is located further from the bonding surface than the surface of the cap substrate.

8. The semiconductor device according to claim **7**, wherein the second end of the leading electrode has an area greater than an area of the first end.

9. The semiconductor device according to claim **1**, further comprising an insulating layer at a bottom portion of the groove to avoid the groove reaching the base substrate.

10. The semiconductor device according to claim **1**, wherein

the cap substrate is bonded to the predetermined portion of the base substrate such that a sealed space is provided between the cap substrate and the predetermined region of the base substrate.

11. The semiconductor device according to claim **1**, wherein

the base substrate includes a SOI substrate having an embedded oxide film and a SOI layer along the embedded oxide film,

the plurality of base semiconductor regions is provided by the SOI layer and is insulated and separated from each other through a trench formed in the SOI layer, the trench reaching the embedded oxide film.

12. The semiconductor device according to claim **1**, wherein

at least one of the plurality of base semiconductor regions provides a fixed semiconductor region including a fixed electrode,

at least another one of the plurality of base semiconductor regions provides a movable semiconductor region including a movable electrode opposed to the fixed electrode and displaceable relative to the fixed electrode, the movable electrode is formed by conducting a sacrifice layer etching at a portion of the embedded oxide film,

the leading electrode is connected to each of the fixed semiconductor region and the movable semiconductor region,

the fixed semiconductor region and the movable semiconductor region constitute a mechanical quantity sensor element for detecting a mechanical quantity applied thereto, the mechanical quantity being detected based on a change in capacitance between the fixed electrode and the movable electrode in accordance with a change in distance between the fixed electrode and the movable electrode due to the movable electrode being displaced relative to the fixed electrode by the mechanical quantity.

13. The semiconductor device according to claim **12**, wherein

the mechanical quantity includes one of acceleration and angular velocity.

14. The semiconductor device according to claim **1**, wherein

the base substrate includes a single crystal silicon substrate,

the plurality of base semiconductor regions include impurity diffused regions that are insulated and separated by PN-junction separation.

15. The semiconductor device according to claim **14**, wherein

the single crystal silicon substrate has a membrane at a surface portion thereof,

at least one of the impurity diffused regions is disposed in the membrane and constitutes a pressure sensor element for detecting a pressure applied to the membrane based on a change in resistance of the impurity diffused region in accordance with displacement of the membrane by the pressure.

16. A method of manufacturing a semiconductor device, comprising:

forming a base substrate made of silicon, wherein the base substrate has a plurality of base semiconductor regions in a predetermined portion of a surface layer thereof, the plurality of base semiconductor regions is insulated and separated from each other;

forming a cap substrate;

bonding the cap substrate to the predetermined portion of the base substrate; and

forming a leading electrode including a metal part, wherein the leading electrode passes through the cap substrate, the leading electrode has a first end connected to one of the plurality of base semiconductor regions and a second end located adjacent to, a surface of the cap substrate, and the leading electrode defines a groove between an outer surface thereof and the cap substrate.

17. The method according to claim **16**, further comprising:

forming a trench in the cap substrate to reach the one of the plurality of base semiconductor regions after the bonding, wherein

the forming of the leading electrode includes embedding a metal for providing the metal part in the trench and forming the groove on a periphery of the trench.

18. The method according to claim **16**, wherein

the forming of the leading electrode is partly conducted in the forming of the cap substrate so that the leading electrode is formed in condition of being connected to the cap substrate,

the bonding includes connecting the first end of the leading electrode to the one of the plurality of base semiconductor regions, and

the remainder of the forming of the leading electrode is performed after the bonding.

19. The method according to, claim **16**, wherein

the forming of the cap substrate includes forming a primary groove in a primary cap substrate,

the forming of the cap substrate further includes forming a primary leading electrode, as a part of the forming of the leading electrode, by applying a metal on a side wall of the primary groove, and

the bonding includes connecting the primary cap substrate to the base substrate such that an opening of the primary groove is opposed to the base substrate,

the method further comprising:

grinding a surface of the primary cap substrate, the surface being opposite to a bonding surface at which the primary cap substrate and the base substrate are bonded, so that the cap substrate is provided by the primary cap substrate, and the leading electrode and the groove are respectively provided by the primary leading electrode and the primary groove.

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