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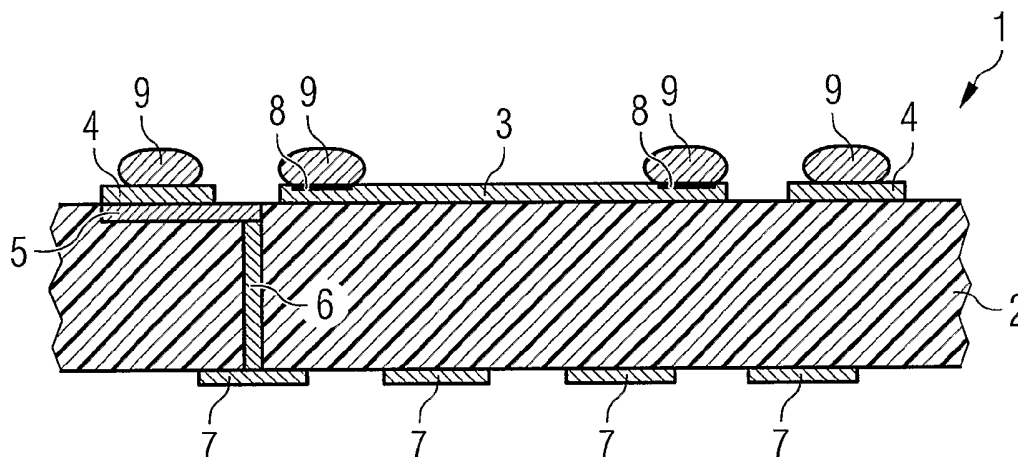
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(54) Title: CARRIERS FOR SEMICONDUCTOR PACKAGES, SEMICONDUCTOR PACKAGES AND METHODS TO ASSEMBLE THEM



(57) Abstract: A carrier for a semiconductor package (30; 31) comprises at least one package position (1; 28). Each package position (1; 28) includes a chip mounting area (3; 18), at least one grounding area (8; 22) and an electrically conductive redistribution structure (2; 17). The redistribution structure (2; 17) includes inner contact pads (4; 21). The carrier further includes at least one precursor bump (9; 23) disposed on the carrier.

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Description

Carriers for semiconductor packages, semiconductor packages and methods to assemble them

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The invention relates to carriers for semiconductor packages, semiconductor packages and methods to assemble them.

10 Semiconductor packages are typically assembled by providing a carrier which includes a plurality of package positions. The carrier may be, for example, a lead frame strip or a substrate such as a redistribution or rewiring board. Each package position includes a chip or die mounting area and inner contact pads. Additionally, the chip mounting area may include one or
15 more grounding areas or grounding pads.

The semiconductor package is assembled by attaching the passive rear surface of the chip to the chip mounting area using die attach material such as an epoxy resin. Bond wires are
20 then formed between the chip contact areas and the grounding pads and between the chip contact pads and the inner contact pads. The semiconductor chip, the bond wires and the inner contact pads are then encapsulated in mold material and the individual semiconductor packages separated from the carrier.
25 Such a process is disclosed by US 5,710,064 for example.

The known assembly processes suffer from the problem that the die attach material may spread laterally outwards from the interface formed between the passive rear surface of the chip
30 and the chip mounting area. The die attach material may partially or completely cover the grounding pads and, possibly, also the inner contact pads and contaminate the surface of the

pads. This results in the problem that a poor electrical connection between the bond wire and contaminated pad is made due to the presence of the die attach material in the interface between the bond wire and the pad.

5

This problem is not usually detected until the final testing stage of the package when the defective packages have to be discarded. Manufacturing costs are, therefore, increased due to this wastage.

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An object of the invention is to provide more reliable semiconductor packages and methods to assemble them which avoid the problems associated with undesired spreading of the die attach material.

15

This object is solved by the subject matter of the independent claims. Further improvements result from the subject matter of the dependent claims.

20 The invention provides a carrier for a semiconductor package with at least one package position. The package position is suitable for use in a semiconductor package and includes a chip mounting area, at least one grounding area and an electrically conductive redistribution structure.

25

The redistribution structure includes inner contact pads which, preferably, are electrically connected to outer contact areas by electrically conductive paths. The outer contact areas provide the electrical connections between the semiconductor package and an external substrate such as a printed circuit board.

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The at least one grounding area is, preferably, located on the chip mounting area or die pad or die paddle. The grounding area, advantageously, includes a layer of a metal or metal alloy which provides an improved electrical connection between the electrical connection to the semiconductor chip, for example a bond wire, and the material of the chip mounting area. The grounding area also, advantageously, includes two or more layers of different metals or alloys in order to further improve the mechanical and electrical integrity of the interfaces between the electrical connection means, the grounding area and the chip mounting area.

The carrier also comprises least one precursor bump which is disposed on the carrier. The precursor bump is attached to the carrier before the package assembly process, i.e. before the semiconductor chip is attached to the chip mounting area. This advantageously enables the precursor bump to have a better electrical connection to the carrier than possible in prior art carriers since the precursor bump is attached to the carrier before the surface of the carrier may become contaminated during subsequent processing steps. In particular, the contamination of the interface between the precursor bump and the surface of the carrier during subsequent assembly steps is avoided. Therefore, the interface remains unaffected by any undesired spreading of the die attach material.

The upper surface of the precursor bump advantageously provides a raised surface for the subsequent electrical connections between the semiconductor chip and the carrier. This raised upper surface of the precursor bump lies in a plane above that in which the die attach material spreads and, therefore, remains uncontaminated.

Additionally, a wider range of deposition conditions can be used to provide a precursor bump. Therefore, a precursor bump with improved interfacial electrical conductivity between the precursor bump and the carrier can be provided. This can be carried out by optimising the formation conditions, for example, by using a higher temperature or a longer bonding time. In a diffusion bonding process, this advantageously increases the interfacial diffusion and provides an interface with a lower electrical resistance.

Since the precursor bumps are formed on the carrier before the carrier is used in for the assembly of semiconductor packages, possible damage to other parts of the package, in particular the semiconductor chip, is avoided. Therefore, the precursor bump may be formed on the carrier using higher temperatures than possible using prior art carriers.

Preferably, at least one precursor bump is disposed on a grounding area. Since the grounding areas are typically located on the chip mounting area, they are in close proximity to the chip. Therefore, the possible lateral spreading of the die attach material is most likely to cover and adversely contaminate the grounding areas leading to a poor electrical connection. This problem is avoided by the use of the carrier according to the invention.

At least one precursor bump is, preferably, disposed on an inner contact pad of the redistribution structure. This advantageously, also, provides a good electrical connection between the precursor bump and the inner contact pad which leads to an improved electrical connection with a lower contact resistance

between the semiconductor chip and the inner contact pad. Furthermore, the possible contamination of the interface between the electrical connection located between the semiconductor chip and the inner contact pad is avoided as contamination of the surface of the inner contact pad by the die attach material is avoided.

Preferably, a precursor bump is attached to each of the grounding areas provided on the carrier. This provides a good contact for each of the grounding areas and also simplifies the manufacturing process. A precursor bump is also, preferably, disposed on each of the inner contact areas. This also avoids the contamination of the inner contact pads by die attach material and simplifies the manufacturing process. A precursor bump may be formed on each of the ground pads and each of the inner contact pads in the same process steps. The costs of producing both the carrier and the semiconductor packages assembled on the carrier are, therefore, reduced.

In a first embodiment of the invention, the redistribution structure of the carrier is, preferably, provided by a leadframe. A leadframe has the advantage that the technology is well-known and widely used and, therefore, cost-effective. A leadframe strip includes a plurality of package positions, each package position providing a leadframe for the assembly of a semiconductor package. Leadframe strips are also widely used and provide a cost-effective carrier for the redistribution structure. A leadframe strip also enables the assembly of a plurality of semiconductor packages during the same process steps and the automated conveying of the strip in a process and/or between process steps.

The lead frame, preferably, comprises a chip mounting area or die pad or die paddle in approximately its lateral centre. The die pad is laterally surrounded by a plurality of leadfingers. The inner contact pads are, therefore, provided on the inner
5 portion of the each of the leadfingers of the leadframe. The outer portion of each leadfinger provides the external contact areas of the redistribution structure and the length of the leadfinger provides the electrically conducting path between the inner and outer contact areas. The leadframe, preferably,
10 comprises copper or a copper alloy.

The grounding areas are, preferably, provided on the die pad. More preferably, the grounding areas are provided towards the periphery of the die pad laterally outside of the area re-
15 quired to mount the semiconductor chip. The grounding areas are, therefore, easily accessible and suitable for electrically connections between the semiconductor chip and the grounding areas. The chip mounting area or die pad is, therefore, laterally larger than the lateral dimensions or foot-
20 print of the semiconductor chip.

Alternatively, the redistribution structure of the carrier is provided by a redistribution or rewiring board. The redistribution board comprises an electrically insulating body or
25 board such as FR4 or BT. The upper surface of the redistribution board, preferably, includes a chip mounting area positioned in approximately the lateral centre of the package position. A plurality of inner contact pads are disposed on the upper surface of the redistribution board towards the periph-
30 ery of the package position. The inner contact pads, therefore, laterally surround the chip mounting area. The inner contact areas are connected to external contact areas which

are located on the opposing bottom surface of the body of the redistribution board by electrically conducting conductor tracks and vias.

- 5 A redistribution board has the advantage that, as redistribution boards are widely used, start-up costs are not high so that a cost-effective carrier is provided. A redistribution board also has the advantage that the arrangement of the external contact areas is very flexible since the relationship
- 10 between the arrangement of the inner contact areas and the external contact areas can be controlled in a desired fashion by the appropriate provision of the conductor tracks and conducting vias.
- 15 Preferably, the precursor bump comprises gold or a gold alloy. Gold or a gold alloy is, advantageously, used since gold has a low electrical resistance and is easily formed by conventional techniques. Therefore, the manufacturing costs are reduced.
- 20 Preferably, the carrier includes a plurality of package positions. Each package position is essentially the same and is suitable for the assembly of a semiconductor package. The provision of a carrier with a plurality of package positions enables the assembly of packages in a batch or a continuous
- 25 process which increases the production speed, simplifies the production process and reduces the manufacturing costs. The package positions are, preferably, provided in a regular array of rows and columns which further simplifies the assembly of the packages. This arrangement also provides a high packing
- 30 density of the package positions in the carrier which reduces the materials costs as wastage of the carrier material is reduced.

The invention also relates to methods to assemble a carrier for a semiconductor package. Firstly, a carrier is provided with at least one package position. The carrier, preferably, comprises a plurality of package positions. A package position includes a chip mounting area, at least one grounding area and an electrically conductive redistribution structure. The redistribution structure includes inner contact pads which are, preferably, connected to external contact areas by electrically conducting conductor paths. The chip mounting area is, preferably, positioned in approximately the lateral centre of each package position. The inner contact pads, preferably, laterally surround the chip mounting position.

At least one precursor bump is then formed on the carrier. This provides a carrier including at least one precursor bump which is used in the assembly of semiconductor packages. The carrier, according to the invention, does not include a semiconductor chip, bond wires or encapsulation material.

Preferably, at least one precursor bump is formed on a grounding area and, more preferably, a precursor bump is formed on each of the grounding areas in the same process step. This simplifies the manufacturing of the carrier and reduces the production costs.

At least one precursor bump is, preferably, formed on an inner contact pad. More preferably, a precursor bump is formed on each of the inner contact pads during the same process step. Advantageously, a precursor bump is formed on each of the grounding pads and each of the inner contact pads in the same

process step. This further simplifies the manufacturing of the carrier and further reduces the production costs.

5 The precursor bumps are, preferably, formed by a ball-bonding technique. Ball-bonding techniques are well-known and widely used so that the cost and complexity of the production of the carrier is not unnecessarily increased.

10 Preferably, the precursor bumps are formed using a ball-bonding technique whereby the mass of the precursor bump undergoes a downward pressing force while being subjected to heating. This leads to the formation of a flattened or squashed precursor bump. This provides a precursor bump with a wedge-type shape and increases the lateral size of the bump in
15 comparison with the diameter of the wire from which it is formed.

This method is advantageous as the interfacial area between the bump and the grounding area or inner contact pad is increased. This reduces the contact resistance. Also, advantageously, the upper surface of the precursor bumps has a relatively flat surface which lies in a plane approximately parallel to the plane of the surface of the carrier. This enables the reliable formation of an electrical contact between the
25 semiconductor chip and the precursor bump.

The area available for the subsequent formation of a bond wire connection on top of the precursor bump is also advantageously increased. The reliability of the bonding process is increased
30 and, therefore, the failure rate of the bonding process is reduced. Costs are, therefore, further reduced as the number of defective packages produced is reduced.

In the method according to the invention, the precursor bumps are formed on the carrier and the carrier used in the package assembly process. In particular, the precursor bumps are
5 formed on the carrier before the semiconductor chip is mounted on the chip mounting area. Therefore, a carrier including at least one precursor bump is provided which is subsequently used in the assembly of semiconductor packages. This is in contrast to the methods of the prior art in which the carrier
10 fails to include precursor bumps.

The invention also relates to methods to assemble a semiconductor package using the carrier. Firstly, a carrier including at least one precursor bump according to one of the embodi-
15 ments previously described is provided. A semiconductor chip having an active surface with integrated circuit devices and chip contact pads and a passive surface is provided. The passive surface of the semiconductor chip is attached to and mounted on the chip mounting area using adhesive means. The
20 adhesive means, preferably, comprises die attach materials which are well-known in the art.

In the next stage of the assembly process, electrical connections are formed between the chip contact pads and inner contact pads of the carrier and between the chip contact pads and
25 grounding areas of the carrier. This enables the semiconductor chip to be grounded and enables the chip to be electrically accessible from the external contact areas of the carrier. The external contact areas remain outside of the semiconductor
30 package.

At least the semiconductor chip and the electrical connections are encapsulated in plastic material. The plastic material, preferably, comprises mold compounds such as epoxy resin which are well-known in the art. The encapsulation protects the semiconductor chip and the electrical connections, such as the bond wires, and the precursor bumps from mechanical and environmental damage.

The carrier, preferably, includes a plurality of package positions and a semiconductor package is assembled in each of the package positions. The same assembly step is carried out in each package position in the same step. After the molding process, the individual semiconductor packages are then singulated from the carrier. This is advantageously performed using well-known sawing, cutting and stamping techniques. Conventional and reliable assembly techniques can, therefore, be used to assemble packages using the carrier according to the invention. Manufacturing costs are, therefore, reduced.

Preferably, the electrical connections are formed by a wire-bonding technique. Wire-bonding techniques are well-known in the art and, therefore, can be cost-effectively used. Also, wire-bonding techniques are automated so that the desired electrical connections can be made quickly and reliably between the chip and the carrier for each of the package positions on the carrier.

Preferably, electrical connections are formed between the chip contact pads and the precursor bumps which are located on the carrier. More preferably, these electrical connections are provided by bond wires which reach between a chip contact pad and the precursor bump.

The bond wire is, therefore, in mechanical and electrical connection with both the chip contact pad and the precursor bump. A good electrical connection is produced between the chip contact pad and the carrier since an uncontaminated interface between the precursor bump and the carrier and between the precursor bump and the bond wire is provided.

The bond wire is, preferably, formed by first forming a ball-bond on the chip contact pad, spooling the wire and forming a wedge-bond on the precursor bump. The wire is then cut and the bonding tool moved to the next desired position.

The invention also relates to a semiconductor package. The semiconductor package comprises the carrier including at least one precursor bump according to one of the embodiments previously described. The semiconductor package further includes a semiconductor chip having an active surface with chip contact pads and a passive surface. The passive surface of the semiconductor chip is attached to the chip mounting area by adhesive means. The adhesive means is, preferably, a die attach material or an epoxy resin as is well-known in the art. The package also includes electrical connections between the chip contact pads and the inner contact pads and between the chip contact pads and grounding areas. At least the semiconductor chip and electrical connections are encapsulated in mold material.

Preferably, at least one electrical connection is positioned between a chip contact pad and a precursor bump and mechanically connects and electrically connects the chip contact pad and the precursor bump. The electrical connection, preferably,

electrically connects the chip contact pad with the grounding area and/or inner contact pad. Preferably, the electrical connections are provided by bond wires.

5 To summarize, the invention provides a carrier for a semiconductor package which includes at least one precursor bump. In contrast to prior art carriers and prior art assembly methods, the precursor bump is formed on the carrier before the semiconductor chip is attached to the carrier. This advantageously
10 provides an improved electrical connection between the precursor bump and the carrier. The precursor bump provides a raised surface onto which the electrical connection between the chip and the redistribution structure is made. This surface is raised above the surface of the chip mounting position or die
15 pad.

The precursor bumps are, preferably, provided on each of the grounding areas and may also be provided on the inner contact pads of the carrier. This simplifies the manufacturing of the
20 precursor bumps. Therefore, when the semiconductor chip is attached to the chip mounting position by die attach material, if the die attach material spreads laterally outwards from the interface between the chip and the die pad, it cannot contaminate the area of the grounding area or inner contact pad which
25 is to provide the electrical connection. The interface between the precursor bump and the grounding area remains uncontaminated and provides an improved electrical connection.

The manufacturing process is, therefore, simplified since it
30 is no longer necessary to inspect and clean each package position after the semiconductor chip has been mounted and before the wire-bonding process is performed. It is also no longer

necessary to control the surface topography at the plating process, further simplifying the manufacturing process.

5 The electrical connections between the chip and the redistribution structure and the grounding areas are then simply made using conventional bond-wire techniques. A bond wire is provided for each of the desired electrical connections. A bond wire stretches between and mechanically and electrically connects a chip contact pad and a precursor bump, if a precursor
10 bump is provided, or connects a chip contact pad and the grounding area or inner contact pad if a precursor bump is not provided.

Therefore, a more reliable semiconductor package is provided
15 by providing a carrier which includes precursor bumps as a good wire bond integrity is provided even if the die attach material or epoxy undesirably spreads or bleeds out from the interface between the chip and the die pad or paddle.

20 A more reliable package is also provided since the precursor bumps are formed on the carrier before the semiconductor chip is attached to the carrier. The precursor bump may be formed on the carrier using the optimum conditions for providing a good low resistance contact to the carrier. In the case of a
25 diffusion bond, for example, a higher temperature can be used to provide a lower resistance contact while avoiding the possibility of damage to the semiconductor chip caused by the high temperatures. This is particularly advantageous for the precursor bumps attached to grounding areas which are located
30 on the die pad or chip mounting area since the chip and the grounding area are in close thermal proximity.

The advantages provided by the provision of precursor bumps on a carrier for a semiconductor package can be advantageously used in carriers such as a leadframe as well as for carriers such as a redistribution board. The provision of precursor bumps can, therefore, be advantageously used in all packages in which a ground bonding is desired and in which the semiconductor chip is attached to the carrier with die attach material.

Embodiments of the invention will now be described with reference to the figures.

Figure 1 shows a cross-sectional view of a section of a redistribution board according to a first embodiment of the invention,

Figure 2 illustrates the mounting of a semiconductor chip to the redistribution board of figure 1,

Figure 3 shows the formation of bond wires between the semiconductor chip and the redistribution board of figure 2,

Figure 4 illustrates a leadframe according to a second embodiment of the invention,

Figure 5 shows the formation of grounding wires between a semiconductor chip and the leadframe of figure 4, and

Figure 6 shows the semiconductor package including the leadframe of figure 5.

Figure 1 shows a cross-sectional view of a section of a redistribution board 2 which includes a plurality of package positions 1. One package position 1 can be seen in the view of
5 Figure 1. Each package position 1 of the redistribution board 2 is essentially the same. The plurality of package positions 1 is arranged in the redistribution board 2 in rows and columns in a regular grid array. Adjacent package positions 1 are separated by a singulation trench 27 which remains free of the
10 redistribution structure of each package position 1.

Each package position 1 of the redistribution board 2 includes a chip mounting area 3 located on the upper surface of the redistribution board. The chip mounting area 3 is located in approximately the lateral centre of each package position 1 of
15 the redistribution board 2. The chip mounting area 3 also includes a plurality of grounding areas 8. In this embodiment of the invention, the grounding areas 8 comprise a layer of silver. The grounding areas 8 are positioned towards the periphery of the chip mounting area 3. The area remaining in approximately the lateral centre of the chip mounting area 3 is
20 laterally larger than the semiconductor chip which is to be mounted in the chip mounting area 3. Therefore, the grounding pads 8 lie laterally outside of the area occupied by the semiconductor chip.
25

The chip mounting area 3 is laterally surrounded by a plurality of inner contact pads 4 which are also positioned on the upper surface of the redistribution board 2. The bottom surface of the redistribution board 2 includes outer contact pads
30 7. Each inner contact pad 4 is connected to an outer contact pad 7 by a conductor track 5 and a via 6. The inner contact

pads 4, conductor tracks 5, vias 6 and outer contact pads 7 provide the electrically conductive redistribution structure of the redistribution board 2. The body of the redistribution board 2 comprises an electrically insulating material such as
5 a dielectric, for example FR4 or BT.

The redistribution board 2 further includes a plurality of gold precursor bumps 9. A gold precursor bump 9 is positioned on each of the grounding areas 8 and on each of the inner con-
10 tact pads 4. As can be seen from figure 1, the precursor bumps 9 are formed on the redistribution board 2 before the semiconductor chip is attached to the chip mounting area 3.

The precursor bumps 9 are formed by a ball-bonding technique
15 in which a bump is subjected to a downwards force while being heated. Each precursor bump 9 has an approximate ovoid cross-section.

Figure 2 shows a cross-sectional view of the section of the
20 redistribution board 2 of figure 1. In this next stage of the process to assemble a semiconductor package 31 according to the invention, a semiconductor chip 10 is mounted in approximately the lateral centre of the chip mounting position 3. The semiconductor chip 10 has an active surface 11 including inte-
25 grated circuit devices and a plurality of chip contact areas 12. The chip contact areas 12 are arranged in a single row and are located towards the periphery of each of the four sides of the active surface 11 of the semiconductor chip 10.

30 The semiconductor chip 2 also has a passive surface 13 which is attached to the chip mounting area 3 by epoxy resin 14. The semiconductor chip 10 is laterally positioned on the chip

mounting area 3 between the grounding areas 8, a precursor bump 9 being positioned on each of the grounding areas 8. The semiconductor chip 10 is, therefore, laterally positioned between the precursor bumps 9. Typically, the epoxy resin 14
5 spreads laterally outwards from the interface between the passive surface 13 of the semiconductor chip 10 and the upper surface of the chip mounting position 3.

Since the redistribution board 2 includes the precursor bumps
10 9, which were formed on the grounding areas 8 and as well as on the inner contact pads 4 before the semiconductor chip 10 was mounted onto the chip mounting area 3, the interfaces between the precursor bumps 9 and the grounding areas 8 and the inner contact pads 4 remains uncontaminated by the epoxy resin
15 14. A low contact resistance between the precursor bumps 9 and the grounding pads 8 and between the precursor bumps 9 and the inner contact pads 4 is, therefore, provided.

Figure 3 shows the next step in the method to the assemble a
20 semiconductor package 31 using the redistribution board of figure 1. After, as shown in figure 2, the passive surface 13 of the semiconductor chip 10 is mounted to the chip mounting area 3, electrical connections are made between the semiconductor chip 10 and the redistribution board 2. As can be seen
25 in figure 3, the electrical connections are made by two pluralities of bond wires 15,16.

A first plurality of bond wires 15 is formed by firstly attaching a wire to a chip contact pad 12 by a ball-bond. The
30 ball bond is distinguished by the ovoid head 25 which is attached to, and in electrical contact with, the chip contact pad 12. The wire 15 is spooled out and connected to a precursor

sor bump 9 positioned on a grounding pad 8 where it is mechanically and electrically joined by a wedge bond 26 to the precursor bump 9. The wedge-bond 26 is formed while pressing the wire 15 while it is heated onto the surface of the precursor bump 9. The plurality of first bond wires 15 are grounding bond wires. The wire is then cut to form a grounding bond wire 15, the wire bonding tool is moved to the next chip pad 12 and a further wire bond formed in the same way.

10 In addition to the formation of a plurality of first wire bonds 15 between chip contact pads 12 and grounding areas 8, a second plurality of wire bonds 16 electrically connects the chip contact pads 12 to the precursor bumps 9 attached to the inner contact pads 4 of the redistribution structure of the redistribution board 2. The wire bonds 16 are produced using the same method as that for the first plurality of grounding bond wires 15.

The advantage of the redistribution board 2 including the precursor bumps 9 is clearly illustrated in the stage of the assembly process shown in figure 3. The interface between the precursor bump and the grounding pad remains free from the epoxy resin 14 and provides a high conductivity, low resistance interface. The second end 26 of each of the bond wires 15, 16 is attached to the upper surface of the precursor bumps 9. Since the precursor bumps 9 are provided on the redistribution board used in the assembly process before the semiconductor chip 10 is attached to the chip mounting area 3, the upper surface of the precursor bumps 9 is raised above the surface of the chip mounting area 3 and remains uncontaminated by any lateral spreading of the epoxy resin 14.

Also, since the precursor bumps 9 are formed on the grounding areas 8 and inner contact pads 4 of the carrier, the precursor bump 9 fabrication conditions can be optimised to provide a low resistance interface. If a diffusion bonding technique is used, intermetallic phases are formed at the interface between the precursor bump 9 and grounding area 8 and inner contact pads 4. This provides a clean, low resistance interface which remains uncontaminated from the epoxy resin 14.

10 The semiconductor chip 10, bond wires 15, 16, precursor bumps 9, chip mounting area 3 and inner contact pads 4 are then embedded in encapsulation or mold material 32. The mold material 32 also covers the upper surface of the redistribution board 2. The encapsulation may be carried out by over-molding each package position 1 individually and then singulating the individual packages 1 from the redistribution board 2 by cutting through the redistribution board along the singulation trenches 27.

20 Alternatively, all of the package positions 1 included on the redistribution board 2 may be embedded in a single mold mass to form a panel. Individual packages 31 are then singulated from the panel by cutting both the mold component and redistribution board along the singulation trenches 27 which separate adjacent package positions 1.

Figure 4 shows a carrier according to a second embodiment of the invention. In this embodiment, a leadframe strip provides the carrier. In the cross-sectional view of Figure 4, a single package position 28, which is part of a leadframe strip 29, is illustrated. The leadframe strip 29 includes a plurality of package positions 28 arranged in rows and columns. Each pack-

age position 28 is mechanically connected to its adjacent neighbours in the leadframe strip 29 by tie bars which cannot be seen in the figure and are not part of the leadframe 17 included in the semiconductor package 30.

5

Each package position 28 provides a leadframe 17 for a single semiconductor package 30. Each leadframe 17 includes a die paddle or die pad 18 located in approximately its lateral centre. The die pad 18 is surrounded by a plurality of lead-
10 fingers 19 which lie in essentially the same plane as the die pad 18. The inner portion of each leadfinger 19 includes an inner contact pad 12. The outer portion of each leadfinger 19 remains outside of the package encapsulation and provides the external contact areas of the package 30. The leadframe 17
15 further includes die pad leads 20 which protrude from the die pad 18 and extend outside of the package 30. The die pad leads 20 enable the die pad 18 to be grounded externally to the package 30.

20 A plurality of grounding pads 22 are provided on the die pad 18. The grounding pads 22 are located towards the periphery of the die pad 18 and are positioned outside of the area which will be occupied by the semiconductor chip.

25 The leadframe 17 further includes a gold precursor bump 23 located on each of the grounding pads 22. The precursor bump 23 is formed on the grounding pads 22 using a ball-bonding technique as previously described whereby intermetallic phases are formed at the interface between the precursor bump 23 and the
30 grounding pad 22.

Figure 5 illustrates the next stage of the assembly process of the second embodiment of figure 4. Similarly to the process shown in figures 2 and 3, a semiconductor chip 10 is mounted in approximately the lateral centre of the die pad 18 between the precursor bumps 23 located on the grounding pads 22. The passive surface 13 of the semiconductor chip 10 is mounted on the die pad 18 by epoxy resin 14. A first plurality of bond wires 15 are formed between the chip contact pads 12 and the precursor bumps 23 positioned on the grounding pads 22. A similar bond-wiring process is used as was described with reference to Figure 3.

Figure 6 shows the next stage in the assembly process. After the semiconductor chip 10 has been mounted on the die pad 18 and after the first plurality of grounding bond wires 15 has been formed, the second plurality of bond wires 16 is formed using a well-known wire-bonding technique. A gold bump 24 is formed on each of the inner contact pads 21 located on the inner portion of each of the leadfingers 19 using prior art formation conditions. The second bond wires 16 are then formed between the chip contact pads 12 and gold bumps 24 using a similar technique as that previously described. The semiconductor chip 10 is then electrically connected to the bumps 24 by the second plurality of bond wires 16.

The semiconductor chip 10, bond wires 15, 16 and inner portions of the leadfingers 19 including the inner contact pads 21 are encapsulated in mold material 32 to form a semiconductor package 30. The individual packages 30 are then singulated from the leadframe strip 29 by removing the tie bars by well-known cutting and stamping methods.

Reference numbers

1	first package position	28	second package position
2	redistribution board	29	leadframe strip
3	chip mounting area	30	second package
4	inner contact pad	31	first package
5	conductor track	32	mold material
6	via		
7	outer contact pad		
8	first grounding area		
9	first gold precursor bump		
10	semiconductor chip		
11	active surface of chip		
12	chip contact pad		
13	passive surface of chip		
14	epoxy resin		
15	grounding wire bond		
16	wire bond		
17	leadframe		
18	die pad		
19	leadfinger		
20	die pad lead		
21	second inner contact pad		
22	second grounding pad		
23	second gold precursor bump		
24	gold bump		
25	ball bond		
26	wedge bond		
27	singulation trench		

Patent Claims

1. A carrier for a semiconductor package (30; 31) comprising:
 - at least one package position (1; 28), each package position (1; 28) including a chip mounting area (3; 18),
5 at least one grounding area (8; 22) and an electrically conductive redistribution structure (2; 17) including inner contact pads (4; 21); and
 - at least one precursor bump (9; 23) disposed on the
10 carrier.
2. A carrier for a semiconductor package (30; 31) according to claim 1
characterised in that
15 the precursor bump (9; 23) is disposed on a grounding area (8; 22).
3. A carrier for a semiconductor package (30; 31) according to claim 1 or claim 2
20 characterised in that
the precursor bump (9) is disposed on an inner contact pad (4).
4. A carrier for a semiconductor package (30; 31) according to one of the previous claims
25 characterised in that
the redistribution structure is provided by a leadframe (17).
- 30 5. A carrier for a semiconductor package (30; 31) according to one of claims 1 to 3
characterised in that

the redistribution structure is provided by a redistribution board (2).

6. A carrier for a semiconductor package (30; 31) according
5 to one of the previous claims
characterised in that
the precursor bump (9; 23) comprises gold or a gold alloy.

7. A carrier for a semiconductor package (30; 31) according
10 to one of the previous claims
characterised in that
the carrier comprises a plurality of package positions (1;
28).

15 8. Method to assemble a carrier for a semiconductor package
(30; 31) comprising the steps of:
- providing a carrier comprising at least one package po-
sition (1; 28), each package position (1; 28) including
a chip mounting area (3; 18), at least one grounding
20 area (8; 22) and an electrically conductive redistribu-
tion structure (2; 17) including inner contact pads (4;
21); and
- forming at least one precursor bump (9; 23) on the car-
rier.

25

9. Method to assemble a carrier for a semiconductor package
(30; 31) according to claim 8
characterised in that
the precursor bump (9; 23) is formed on a grounding area
30 (8; 22).

10. Method to assemble a carrier for a semiconductor package (30; 31) according to claim 8 or claim 9 characterised in that the precursor bump (9) is formed on an inner contact pad (4).

11. Method to assemble a carrier for a semiconductor package (30; 31) according to one of claims 8 to 10 characterised in that the precursor bump (9; 23) is formed by a ball-bonding technique.

12. Method to assemble a semiconductor package (30; 31) comprising the steps of:

- providing the carrier of one of claims 1 to 6;
- providing a semiconductor chip (10) having an active surface (11) with chip contact pads (12) and a passive surface (13);
- attaching the passive surface (13) of the semiconductor chip (10) to the chip mounting area (3) by adhesive means (14);
- forming a plurality of first electrical connections (15) between the chip contact pads (12) and grounding areas (8; 22)
- forming a plurality of second electrical connections (16) between the chip contact pads (12) and inner contact pads (4; 21); and
- encapsulating at least the semiconductor chip (10), the plurality of first electrical connections (15) and the plurality of second electrical connections (16) in plastic material (32).

13. Method to assemble a semiconductor package (30; 31) according to claim 12 characterised in that the plurality of first electrical connections (15) and the plurality of second electrical connections (16) are formed by a wire-bonding technique.

14. Method to assemble a semiconductor package (30; 31) according to claim 12 or claim 13 characterised in that the plurality of first electrical connections (15) are formed between the chip contact pads (12) and precursor bumps (9; 23).

15. Method to assemble a semiconductor package (30; 31) according to one of claims 12 to claim 14 characterised in that the carrier includes a plurality of package positions (1; 28), and the individual semiconductor packages (30; 31) are singulated from the carrier.

16. Semiconductor package (30; 31) comprising:

- the carrier of one of claims 1 to 6;
- a semiconductor chip (10) having an active surface (11) with chip contact pads (12) and a passive surface (13), the passive surface (13) of the semiconductor chip (10) being attached to the chip mounting area (3; 18) by adhesive means (14);
- a plurality of first electrical connections (15) between the chip contact pads (12) and grounding areas (8; 23);

- a plurality of second electrical connections (16) between the chip contact pads (12) and inner contact pads (4; 21); and
- encapsulation material, encapsulating at least the semiconductor chip (10), the plurality of first electrical connections (15) and the plurality of second electrical connections (16).

17. Semiconductor package (30; 31) according to claim 16

characterised in that

at least one electrical connection (15) is positioned between a chip contact pad (12) and a precursor bump (9; 23).

18. Semiconductor package (30; 31) according to claim 16 or claim 17

characterised in that

the plurality of first electrical connections (15) and plurality of second electrical connections (16) are provided by bond wires.

FIG 1

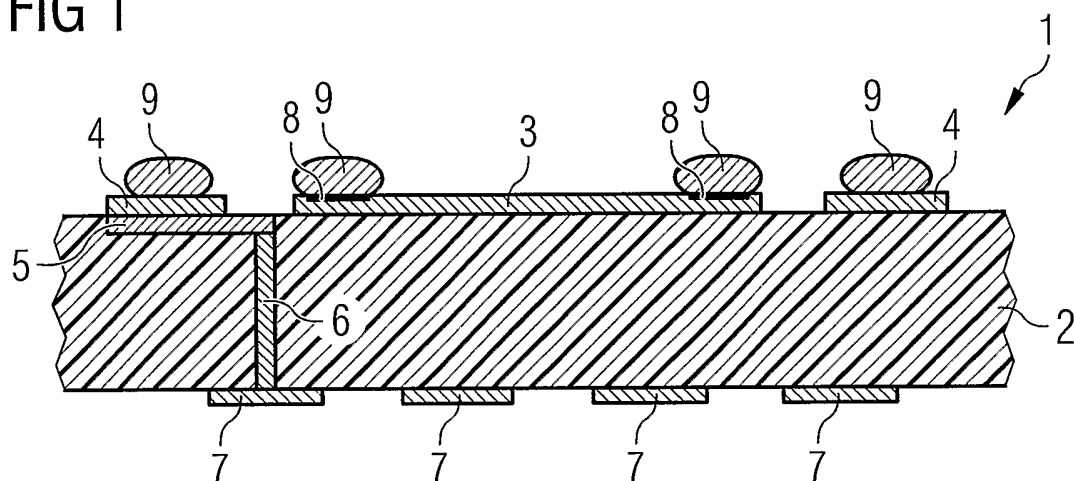


FIG 2

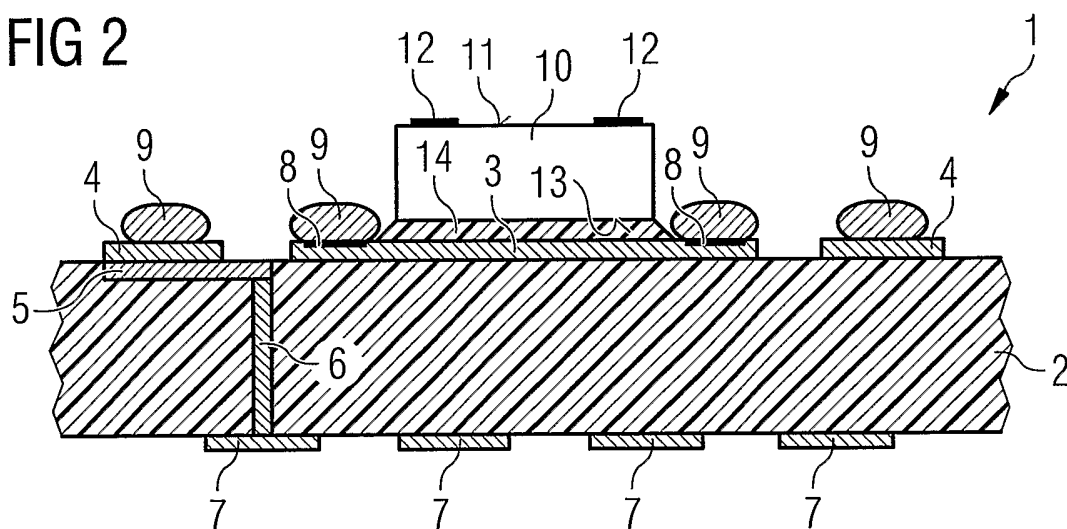


FIG 3

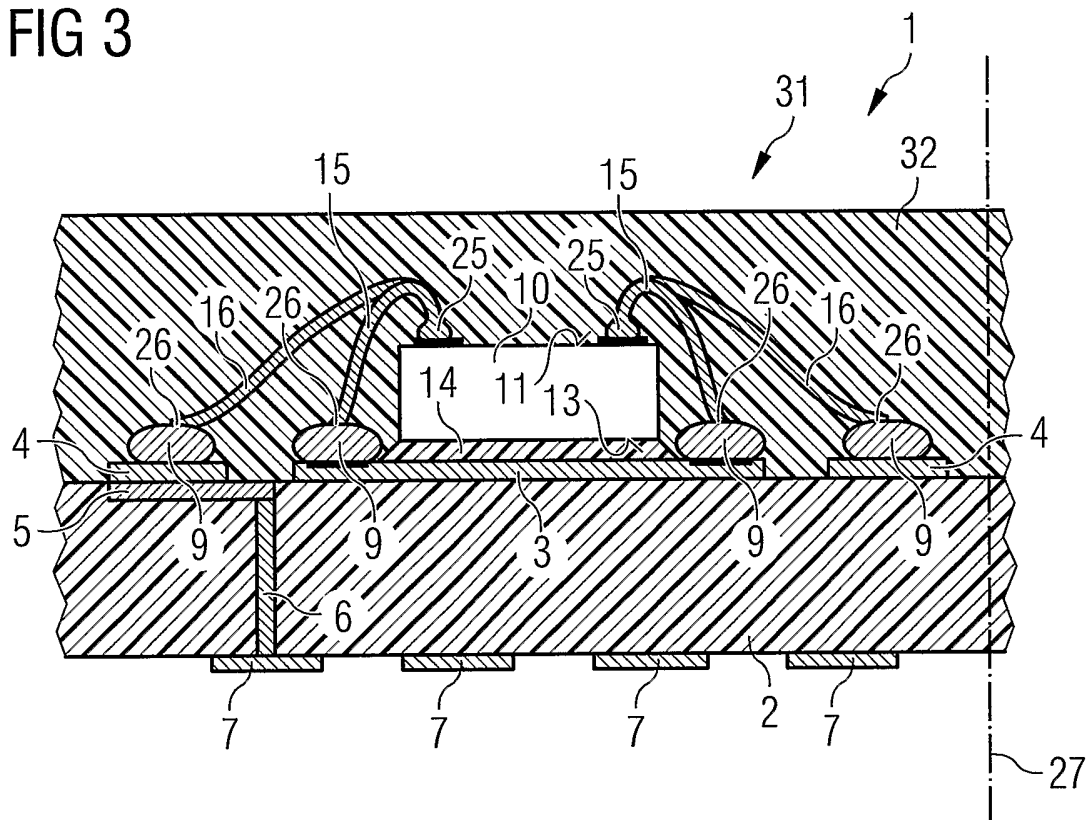


FIG 4

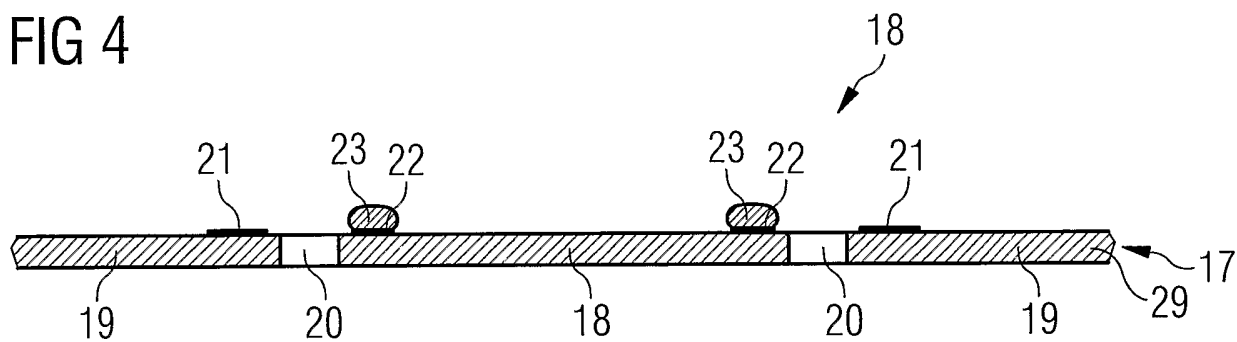


FIG 5

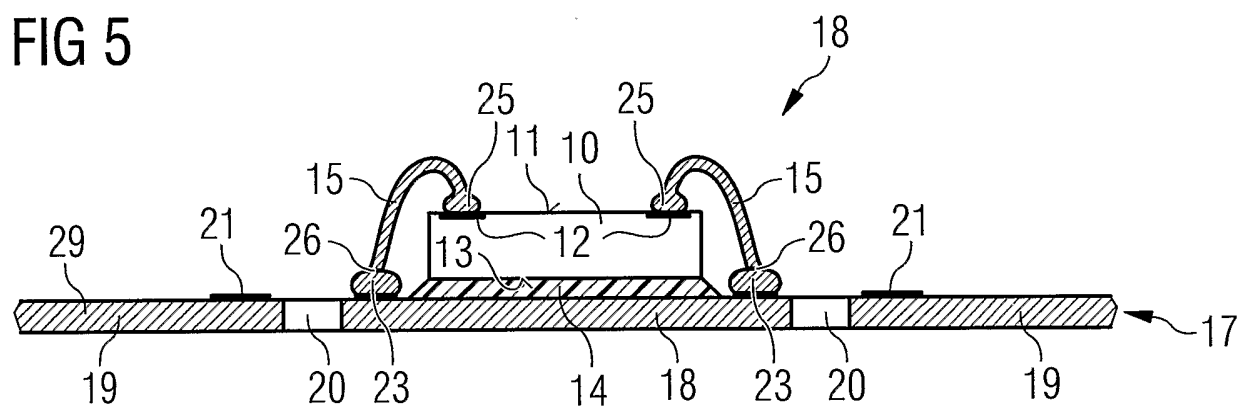
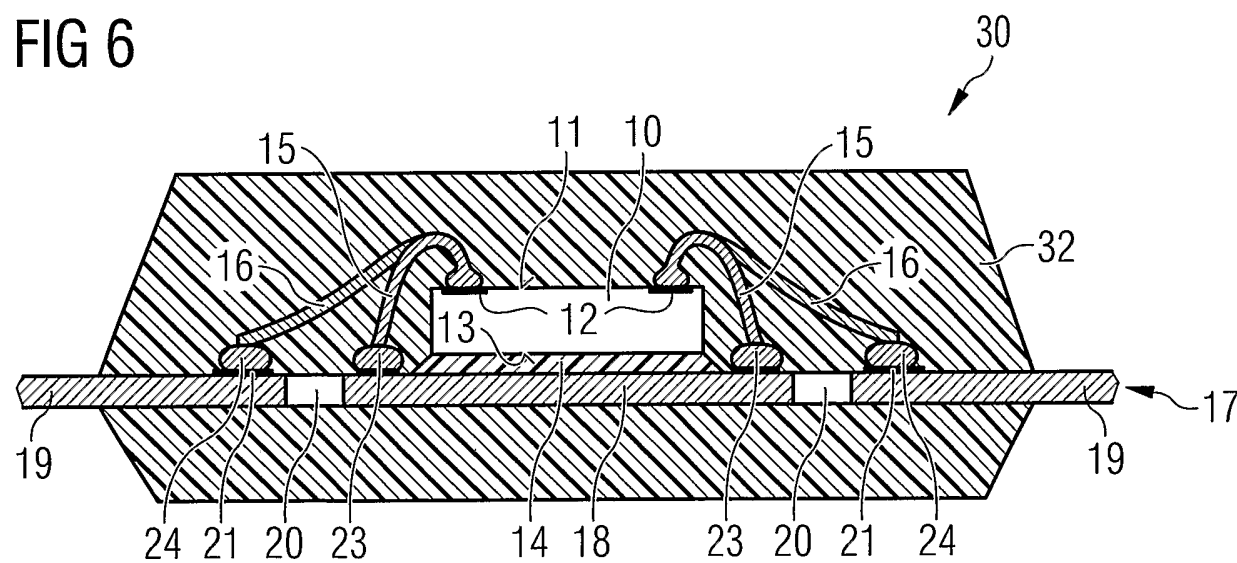


FIG 6



INTERNATIONAL SEARCH REPORT

Int. Patent Application No
PCT/IB2005/000200

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/498 H01L23/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/155332 A1 (PETTY-WEEKS SANDRA L ET AL) 12 August 2004 (2004-08-12)	1-3,5-11
Y	abstract; figures 3,4 paragraph '0039! - paragraph '0045!	12-18
X	US 6 025 640 A (YAGI ET AL) 15 February 2000 (2000-02-15)	1,4
Y	abstract; figures 1-16D column 2, line 9 - column 4, line 39	12-18
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	abstract; figure 4 paragraph '0039! - paragraph '0045!	
X	US 2002/084518 A1 (HASEBE HAJIME ET AL) 4 July 2002 (2002-07-04)	1,4
	abstract; figure 1	

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

24 August 2005

Date of mailing of the international search report

31/08/2005

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
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