



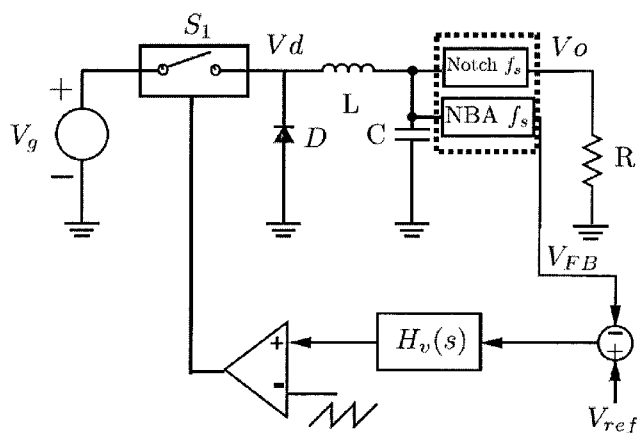
- (51) **International Patent Classification:** Not classified
- (21) **International Application Number:** PCT/IB2012/000147
- (22) **International Filing Date:** 31 January 2012 (31.01.2012)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:** E 11000854.7 3 February 2011 (03.02.2011) EP
- (71) **Applicants (for all designated States except US):** **UNIVERSITAT POLITECNICA DE CATALUNYA** [ES/ES]; c/ Jordi Girona, 31, E-08034 Barcelona (ES). **UNIVERSITAT ROVIRA I VIRGILI** [ES/ES]; c/ de l' Escorxador, s/n, E-43003 Tarragona (ES).
- (72) **Inventors; and**
- (75) **Inventors/Applicants (for US only):** **ALARCON COT, Eduard** [ES/ES]; c/ Auladell, 4, 1R 1A, E-08173 Sant Cugat del Vallès (ES). **RODRIGUEZ VILAMITJANA, Enric** [ES/ES]; c/ Orient 68, Sobreàtic 7, E-08172 Sant Cugat del Vallès (ES). **EL AROUDI CHAOUI, Abdelali** [ES/ES]; c/ Marcel·li Domingo, 5, 2N 3A, E-43007 Tarragona (ES).
- (74) **Agent:** **TORNER LASALLE, Elisabet**; Gran Via de les Corts Catalanes, 669 bis, 1r. 2a., 08013 Barcelona (ES).

- (81) **Designated States (unless otherwise indicated, for every kind of national protection available):** AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) **Designated States (unless otherwise indicated, for every kind of regional protection available):** ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- without international search report and to be republished upon receipt of that report (Rule 48.2(g))

(54) **Title:** A VOLTAGE-SENSING CIRCUIT STRUCTURE FOR A SWITCHING POWER CONVERTER AND METHOD FOR AN ENHANCED FAST-SCALE STABILITY MARGIN OF A SWITCHING POWER CONVERTER

**Figure 1**

(57) **Abstract:** The voltage-sensing circuit structure is intended to avoid fast-scale subharmonic instabilities in switching power converters, comprising a compact circuit structure to be connected at the output of a switching power converter, by means of which the sensed feedback voltage is altered with a double transfer function so that concurrently the ripple component is amplified to obtain an enhanced fast-scale stability margin while attenuating the converter output voltage ripple in the power path.

- 1 -

**A VOLTAGE-SENSING CIRCUIT STRUCTURE FOR A SWITCHING POWER
CONVERTER AND METHOD FOR AN ENHANCED FAST-SCALE STABILITY
MARGIN OF A SWITCHING POWER CONVERTER**

5 Technical field of the invention

The invention relates to controllers for avoiding fast-scale subharmonic instabilities in switching power converters or regulators, in which by means of a compact circuit structure the sensed feedback voltage is altered with a double transfer function so that concurrently the ripple component is amplified to obtain an enhanced fast- scale stability margin while attenuating the converter output voltage ripple in the power path.

The invention also provides a method to obtain an enhanced fast-scale stability margin of a switching power converter.

15 Background of the invention

Switching power converters are widely used in many applications due to their high efficiency, small size and low weight. However, the design- space when targeting miniaturization towards on- chip integration is technological limited by three performance metrics: area, efficiency and output ripple.

The area occupancy is mainly limited by the reactive components size; thus, reducing the inductor or capacitor values result in a decrease of the area, but also increases the natural frequency of the implicit low- pass filter of any DC- DC converter. The reduction of the ratio between the switching frequency and the natural frequency leads to high output voltage ripple. In order to increase such ratio and decrease ripple, the switching frequency is usually increased, but this implies increasing switching losses, hence in turn decreasing the overall converter efficiency. Therefore the desired low- area high- efficiency context, such as in miniaturized switching power converters, will upfront imply high output ripple.

However, the output voltage ripple size confronts a two-fold limitation: due to the strict specifications imposed by on-chip loads demanding tight regulation, but also because higher output voltage ripple makes the converter more prone to exhibit the so-called fast-scale subharmonic instabilities which can eventually result in chaotic oscillations.

Furthermore, these kinds of instabilities are also particularly common in peak current mode controlled converters, especially for duty cycles higher than 0.5 when the regulator is unconditionally unstable at the fast scale and requires of an additional

- 2 -

compensation ramp in order to be stabilized.

US 2009237060 discloses a frequency compensation method for voltage-mode switching regulators wherein a low pass filter and a band pass filter are employed in the two signal paths into the dual inputs of PWM comparators. In one embodiment, two
5 zeros are generated to compensate for the L-C output filter poles. Stable operation, low output voltage ripple and fast load transient response is achieved; while the power consumption of error amplifier and the area for implementing on-chip passive components are greatly reduced.

Redl, R. and Sun, J. "Ripple-based control of switching regulators. An
10 Overview", IEEE Transactions on power electronics, Volume 24, N° 12, 2009, discloses (see Fig. 21 and related description) the use of a ripple amplifier in a context of enhance control of switching regulators to eliminate fast scale stability. The article refers also to another document in the art of Redl, R "A new family of enhanced ripple regulators for power management applications" presented at PCIM, 2008, and where
15 referred ripple amplifies is further detailed.

However none of the quoted prior art documents explains to apply said ripple amplification based on a particular design criteria of a circuit intended to be connected at the output of a switching power regulator and taking into account the switching
20 frequency.

Brief summary of the invention

It is an object of this invention to concurrently address such both ripple-related constraints when high output ripple is a result because of low area or/and high efficiency requirements.

25 On the one hand, the invention aims to increase the fast- scale stability margin of the switching regulator and on the other hand the reduction of the output voltage ripple to fulfill load demands.

The invention in fact extends the possible solutions in the design space, and hence alternatively it can be considered allowing to reduce the reactive component
30 size, for better miniaturization, or to reduce switching frequency, for high efficiency, while enhancing stability.

The invention proposes a voltage-sensing single circuit structure for a switching power converter, SPC or power regulator, to be connected at the output of a SPC and with two enclosed functions, comprising:

- 35 - an attenuation filter part of the switching power converter output voltage ripple, having a first output; and

- 3 -

- an amplification part, amplifying the harmonic at the switching frequency with respect to the harmonic at half of the switching frequency, having a second output providing a feedback path for sensing the voltage entering to the feedback loop,

5 so that concurrently the ripple component is amplified obtaining an enhanced fast-scale stability margin while at the same time attenuating the converter output voltage ripple in the power path

As per an embodiment of the invention said attenuation filter part is a notch filter at the switching frequency.

10 The voltage-sensing single circuit structure of the invention comprises a compact structure including an inductor-capacitor series structure in which the inductor is connected to the output voltage of the SPC and the capacitor to ground; being a common node between both components the feedback control sensed voltage.

The invention also teaches a method to obtain an enhanced fast-scale stability margin of a switching power converter, implemented by the voltage-sensing single circuit structure disclosed, and comprising:

- filtering the switching power regulator output voltage ripple in order to obtain an attenuation thereof; and
- amplifying the harmonic at the switching frequency with respect to the harmonic at half of the switching frequency the output providing a sensed voltage entering the feedback loop, of the SPC ,

20 so that concurrently the ripple component is amplified to obtain an enhanced fast-scale stability margin while attenuating the converter output voltage ripple in the power path.

25 **Brief description of the drawings**

The invention is described in detail below through a representative non limitative example and with reference to the accompanying drawings, namely:

FIG. 1 is a block diagram illustrating the concept in which two transfer functions are applied at the output of switching power converter.

30 FIG. 2 is a preferred embodiment according to the invention for a buck converter, in which a compact LC circuit provides the required transfer functions in FIG 1.

FIG. 3 shows the input-to-output and input-to-feedback transfer functions of the buck converter, according to the invention and the proposed circuit in FIG. 2.

35 FIG. 4 shows relevant time-domain waveforms, of a buck converter including the invention, as illustrated in FIG. 2, and the ones obtained from the conventional buck

- 4 -

converter without including the invention, in the same design conditions save the inclusion of the LC compact voltage- sensing circuit.

FIG. 5 depicts the stability boundaries of a buck converter including the invention, compared to the ones obtained from the conventional buck converter.

5 FIG. 6 shows the peak ripple magnitude of a buck converter including the invention illustrated in FIG. 2, and the ripple obtained from the conventional buck converter without including the invention.

FIG. 7 is another example of the preferred embodiment in FIG 2 applied to a so-called peak- current- mode control with a voltage outer feedback loop.

10 FIG. 8 show the resulting time-domain waveforms of the converter illustrated in FIG. 6.

FIG. 9 depicts the stability boundaries of a current-mode buck converter including the invention as illustrated in FIG. 2, as a function of the duty cycle and proportional gain of the voltage feedback loop.

15

Detailed Description of the Embodiments

FIG. 1 illustrates an embodiment of a switching converter, utilizing a buck switching power topology with constant switching frequency PWM modulation, and the inventive principles of this patent disclosure. The voltage- mode controlled buck converter is used as an illustrative case, but the invention can be applied to any other switched topology.

From a feedback loop standpoint, the harmonic at the switching frequency must be amplified in order to improve the fast- scale stability boundary. Such amplification should amplify the harmonic at the switching frequency with respect to the harmonic at half of the switching frequency in order to obtain the desired fast- scale stability enhancement, and hence it is required to provide tuned narrow- band amplification (NBA).

On the other hand, the reduction of the converter output ripple has been usually tackled by relaxing circuit specifications (increase reactive components values or switching frequency), or by using more complex topologies such as multilevel converters [1], or by narrowband reactive filtering at the converter output [2]. However, in a close-loop configuration, the modification of the sensed output voltage ripple can lead the regulator to exhibit unstable fast- scale behavior.

FIG. 2 illustrates the preferred embodiment of a switching power regulator utilizing a representative voltage- mode controlled buck power converter with PI constant switching frequency control and an additional reactive circuit in the form of an

35

LC divider according to the inventive principles of this patent disclosure. The LC divider, in a compact structure, accomplishes the aim of reducing the output voltage ripple and at the same time narrowband amplifying the switching frequency harmonic in the feedback path. It is implemented as an inductor in series with a capacitor, whereby the
 5 inductor is connected to the output voltage node and the capacitor to ground; being the common node between both components the feedback control sensed voltage, in a similar way as in a simple voltage divider.

The patent disclosure embraces other combined or compact structures with the same functionality, but an LC divider is given as the preferred embodiment.

10 Consider a switching power converter example with parameters oriented to miniaturization, namely $V_g=6$, $V_{ref}=1.2$ V, $L=66$ nH, $C=20$ nH, $R=2.5$ Ω , $f_s=50$ MHz and $V_m=1$ V and being the PI controller $H_v(s)=k_p(s+w_{z1})/s$ with $k_p=3$ and $w_{z1}=1$ Mrad/s. The value of the structure reactive components are preferably chosen so that the resonant frequency is the same as the switching frequency $2\pi f_{cs}=(L_n C_n)^{(-1/2)}$, then $L_n=2$ nH
 15 $C_n=5$ nF.

The obtained magnitude of the input(V_d) - to- output(V_o) frequency response is illustrated in FIG. 3a, which shows that there is a rejection band tuned to the switching frequency that reduces the ripple component. The module of the input(V_d) - to- feedback(V_{FB}) frequency response is illustrated in FIG. 3b, which shows an
 20 amplification of the harmonic at the switching frequency with respect to the harmonic at half of the switching frequency, as needed for enhanced stability.

These advantages are illustrated in the simulated time- domain waveforms shown in FIG. 4a, in which the inductor current and output voltage are shown for a conventional voltage-mode buck converter exhibiting unstable fast-scale behavior. On
 25 the other hand, FIG. 4b illustrates the same waveforms under the same conditions as of FIG. 4a, but having a stable behavior due to the use of the preferred embodiment of the invention.

The benefits in terms of stability are shown in FIG. 5a in which it is shown the global stability boundary as a function of the PI controller parameters, namely the
 30 proportional gain k_p and the zero position w_{z1} , due to their capability to explore the complete stability design space. Note that the stability design space takes into account not only fast- scale instabilities but also the so- called low frequency slow scale Hopf instability, demonstrating the advantages of the proposed invention in terms of fast-scale stability improvement which is not detrimental to the Hopf instability boundary.

35 Furthermore, such benefits in terms of fast- scale stability conversely lead to the fact that the inductor and switching frequency can be reduced without losing stability.

- 6 -

The stability boundaries as a function of the duty cycle are compared for a conventional buck without using the LC divider as an implementation of the invention. FIG. 5b and FIG. 5c demonstrate the advantages resulting by the invention in terms of fast- scale stability, thereby allowing a reduction of the inductor or the switching frequency whilst
5 maintaining system stability.

Regarding the output voltage ripple, the ripple magnitudes obtained from the inclusion of the LC divider and from a conventional buck converter are compared in FIG. 6, showing the benefits of the invention in terms of output ripple, hence facilitating the reduction of reactive components or switching frequency, which along with the
10 aforementioned improvement upon stability, represents an overall improvement for miniaturized converters.

FIG. 7 illustrates the use of the invention in a peak- current- mode with a voltage feedback outer loop. A case example with the same parameters as in the previous case with only a voltage feedback loop but with $V_{ref}=1.5$ V and current gain $k_i=2$ is
15 considered to validate the use of the invention in this application.

In FIG. 8a it is shown the unstable behavior of a peak- current- mode buck converter under such parameters. The time- domain waveforms of the same converter but using the LC divider are shown in FIG. 8b, demonstrating its capability to control fast- scale instabilities. As a proof of the advantages of the invention, the design space
20 exploration has been extended to cover the duty cycle variation, since it is well known that fast- scale instabilities in peak- current- mode control strongly depend upon duty cycle. FIG. 9 shows that the controller turns the regulator to be unconditional stable for duty cycles below 0.5. For duty cycles above such 0.5 border, the regulator becomes stable by increasing the gain in the voltage feedback loop. Note that the use of the LC
25 divider avoids the use of an external ramp to control such instabilities.

References:

- [1] "Three-level buck converter for envelope tracking applications", Yousefzadeh, V.; Alarcon, E.; Maksimovic, D.; Power Electronics, IEEE Transactions on Issue Date:
30 March 2006 Volume: 21 Issue:2 pp. 549 - 552
- [2] Alarcon, E.; Villar, G.; Ferrandez, S.; Guinjoan, F. and Poveda, A. Ripple-reduction tuned filtering switching power converter topology, Power Electronics Specialists Conference, 2004. pag. 3739-3744 Vol.5
- [3] Redl, R. and Sun, J. " Ripple-based control of switching regulators. An Overview",
35 IEEE Transactions on power electronics, Volume 24, N° 12, 2009

- 7 -

[4] Redl, R. "A new family of enhanced ripple regulators for power management applications" presented at PCIM, 2008

CLAIMS

1.- A voltage-sensing circuit structure for a switching power converter to be connected at the output of a switching power regulator, comprising:

- 5 - an attenuation filter part of the switching power converter output voltage ripple, having a first output; and
- an amplification part, amplifying the harmonic at the switching frequency with respect to the harmonic at half of the switching frequency, having a second output providing a feedback path for sensing the voltage entering to the
- 10 feedback loop,

so that concurrently the ripple component is amplified to obtain an enhanced fast-scale stability margin while attenuating the converter output voltage ripple in the power path

2.- A circuit structure according to claim 1, characterized in that said attenuation filter part is a notch filter at the switching frequency.

- 15 3.- The circuit structure according to claim 1, wherein it comprises a compact structure including an inductor-capacitor series structure in which the inductor is connected to the output voltage of the switching power converter and the capacitor to ground, being a common node between both components the feedback control sensed voltage.

- 20 4.- Method to obtain an enhanced fast-scale stability margin of a switching power converter, comprising:

- filtering the switching power regulator output voltage ripple in order to obtain an attenuation thereof; and
- amplifying the harmonic at the switching frequency with respect to the
- 25 harmonic at half of the switching frequency the output providing a sensed voltage entering the feedback loop, of the SPC,

so that concurrently the ripple component is amplified to obtain an enhanced fast-scale stability margin while attenuating the converter output voltage ripple in the power path.

1/7

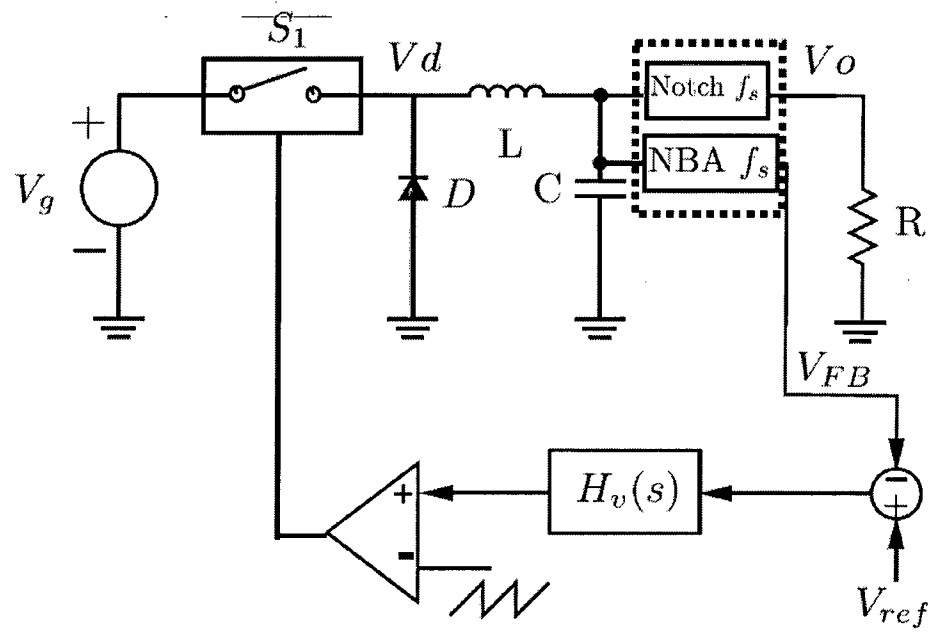


Figure 1

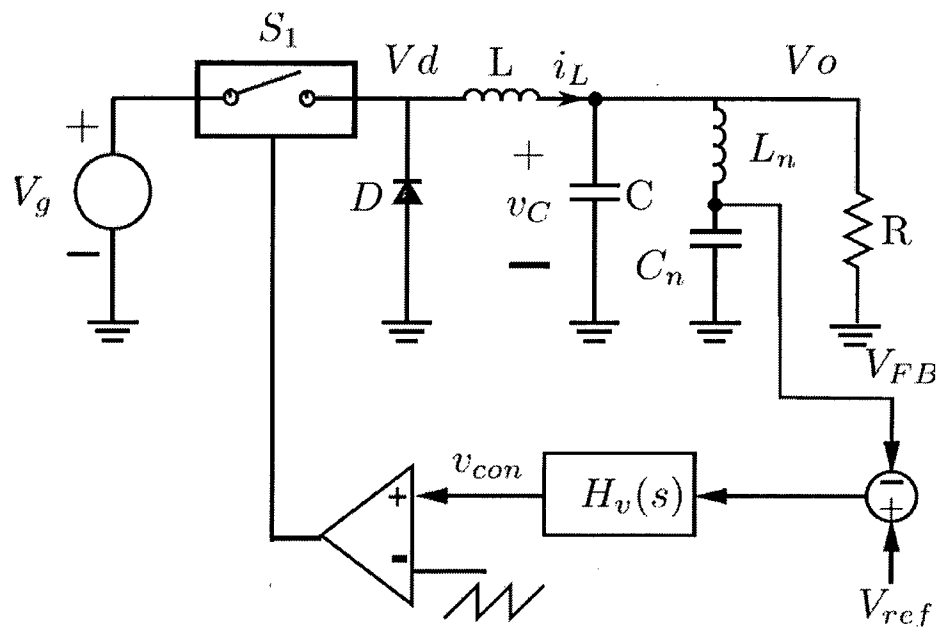


Figure 2

2/7

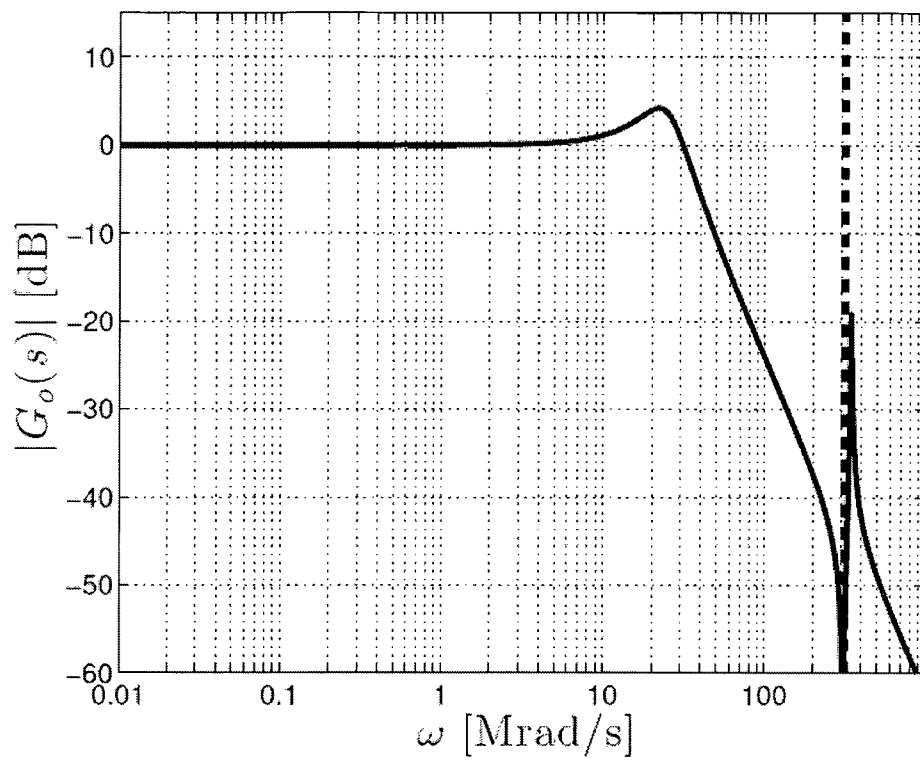


Figure 3a

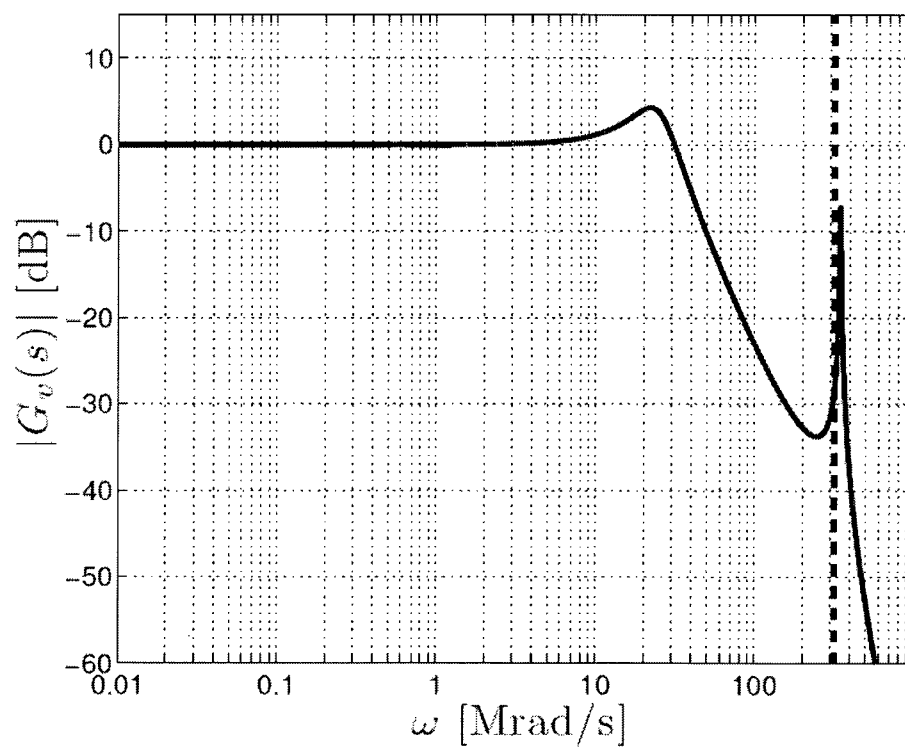


Figure 3b

3/7

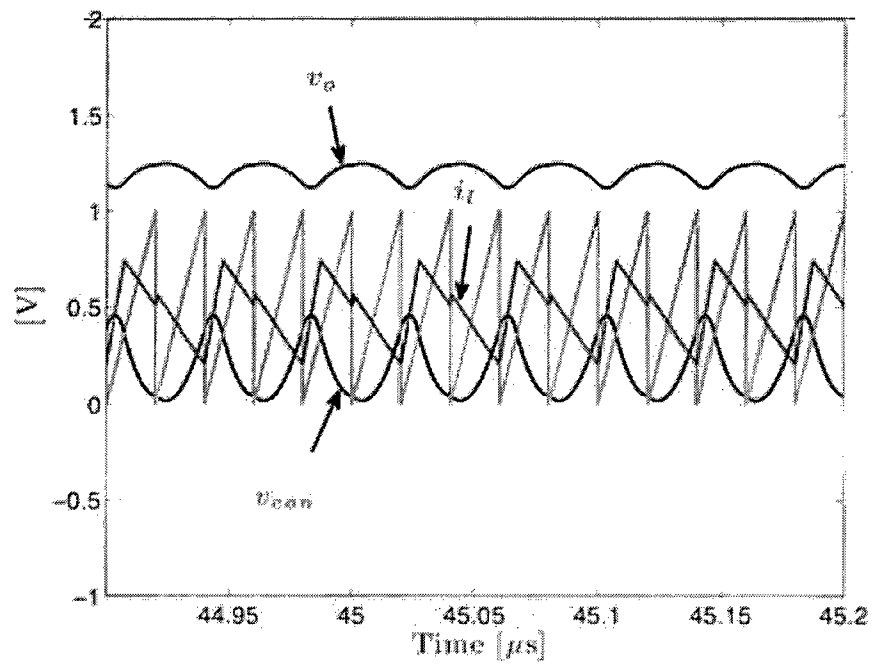


Figure 4a

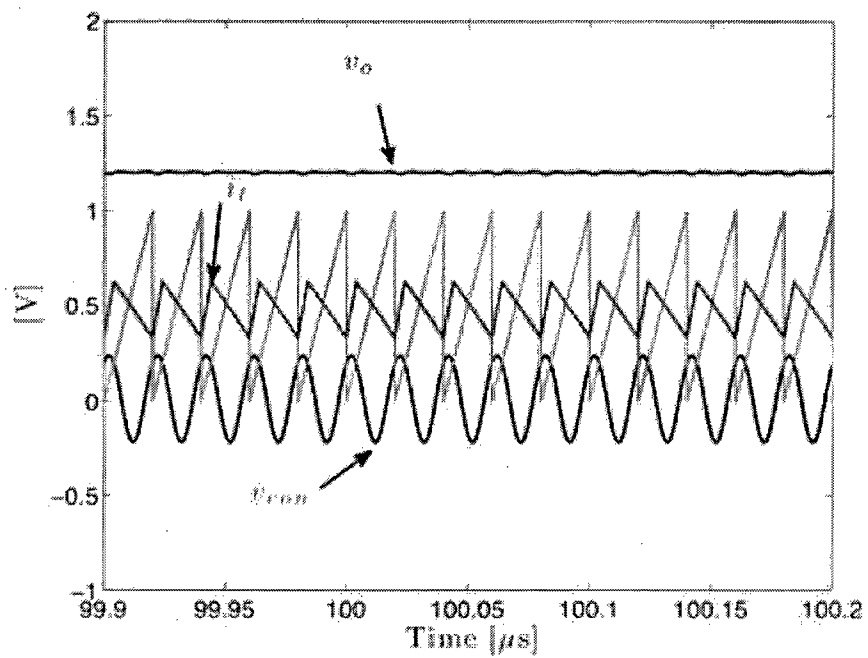


Figure 4b

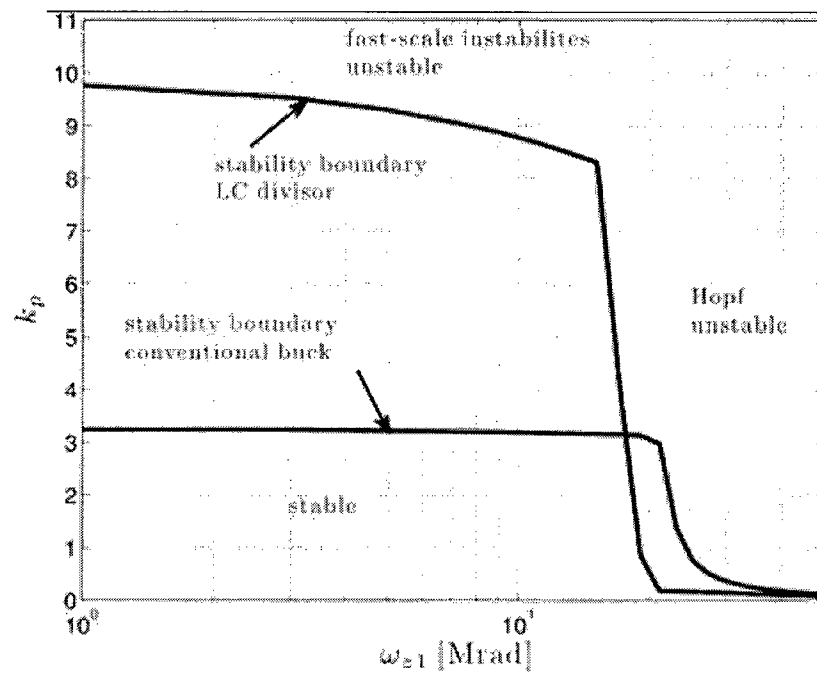


Figure 5a

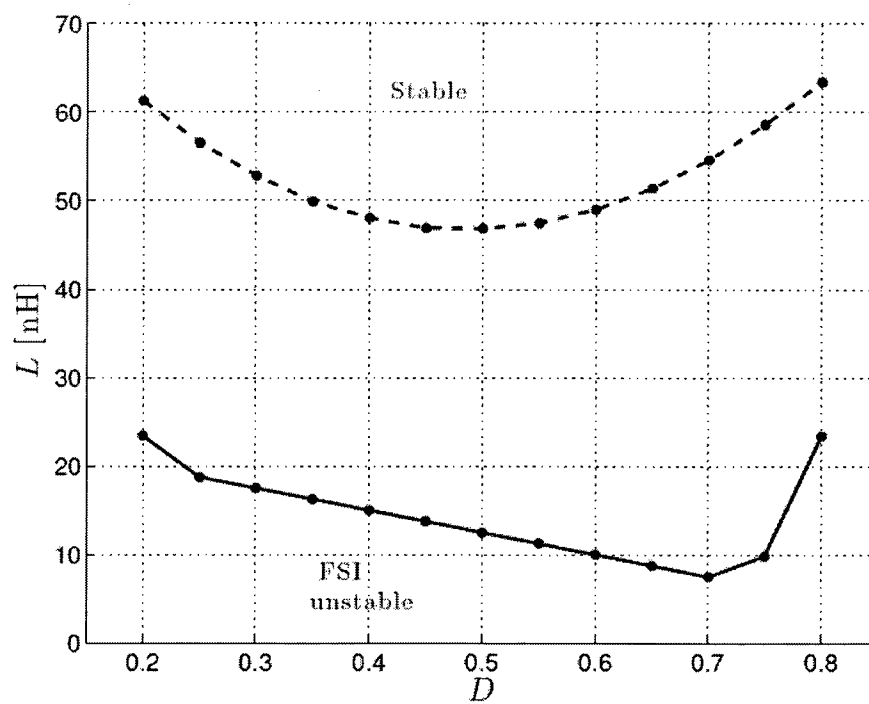


Figure 5b

5/7

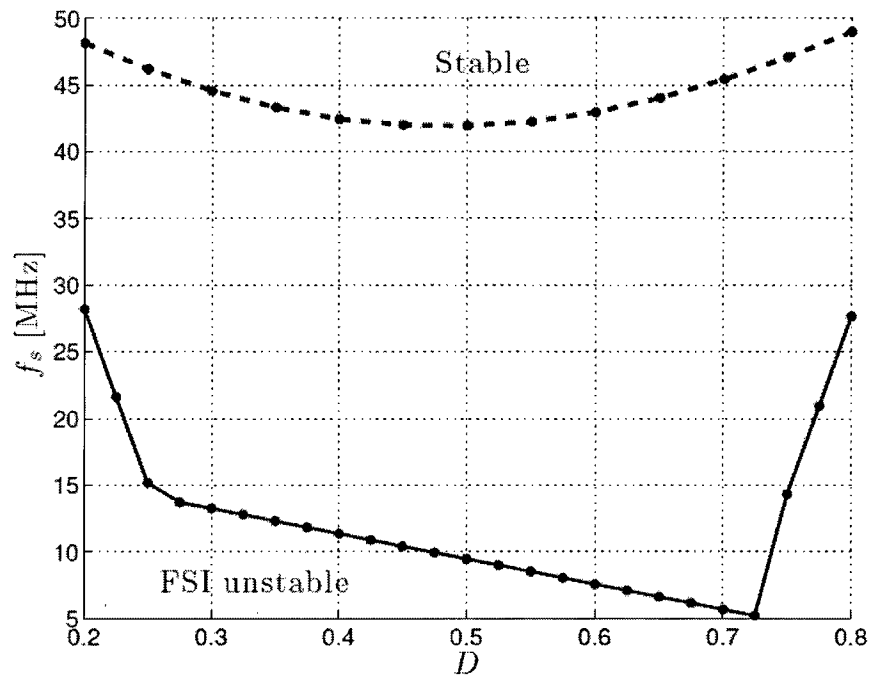


Figure 5c

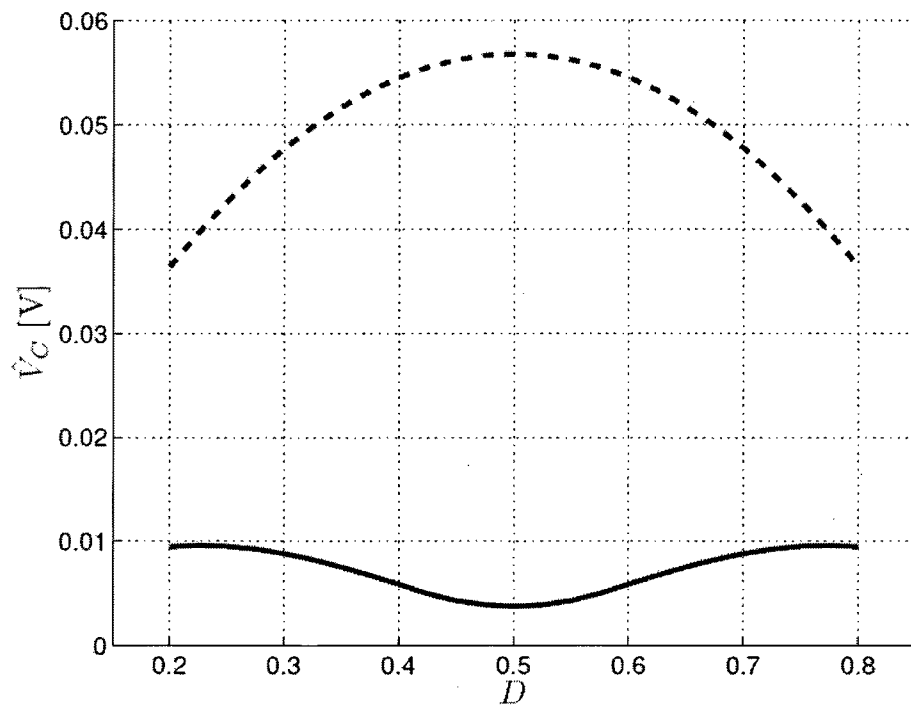


Figure 6

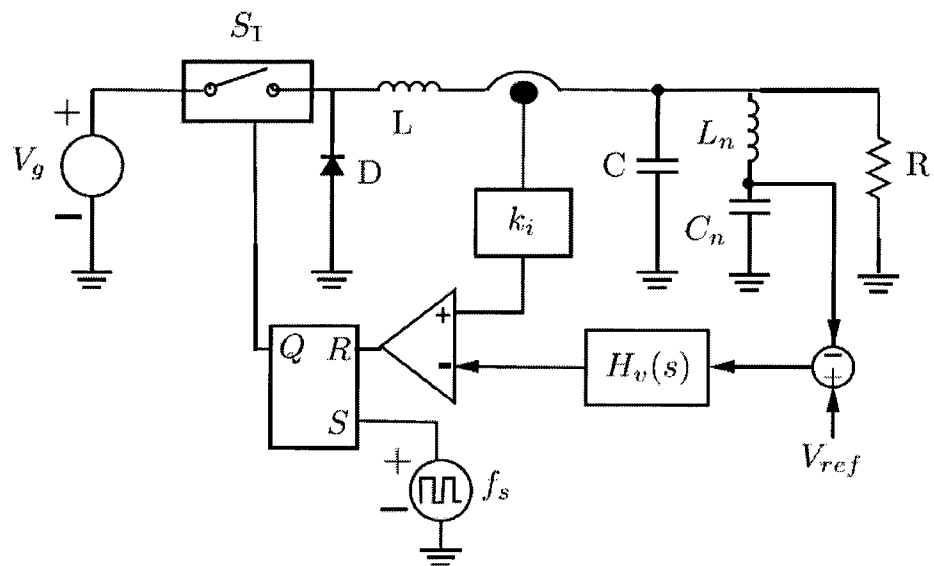


Figure 7

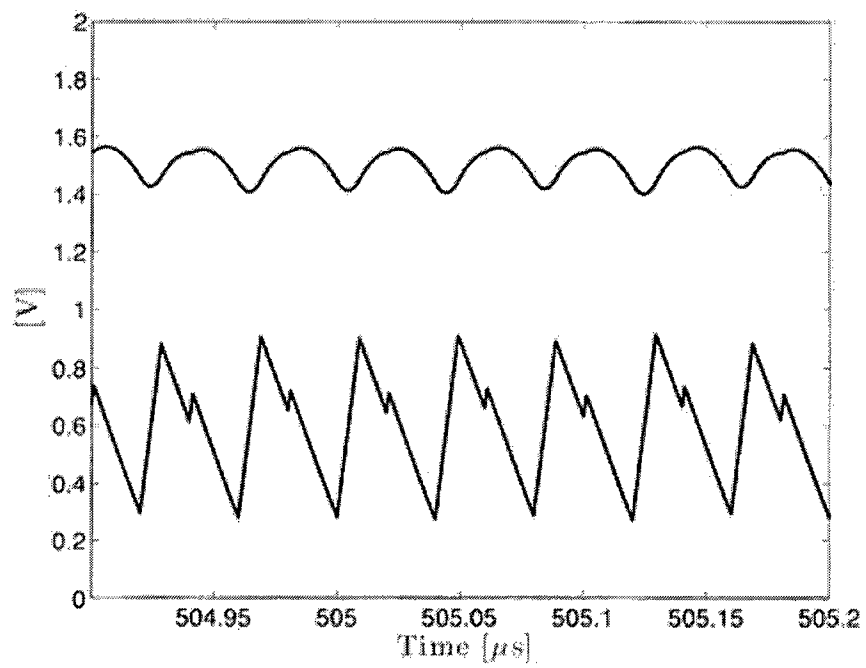


Figure 8a

7/7

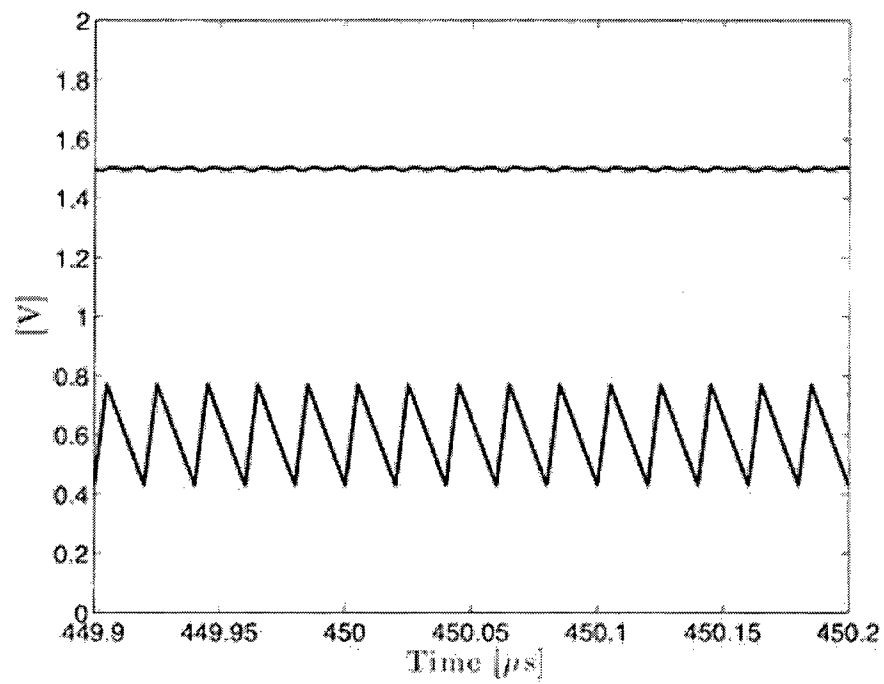


Figure 8b

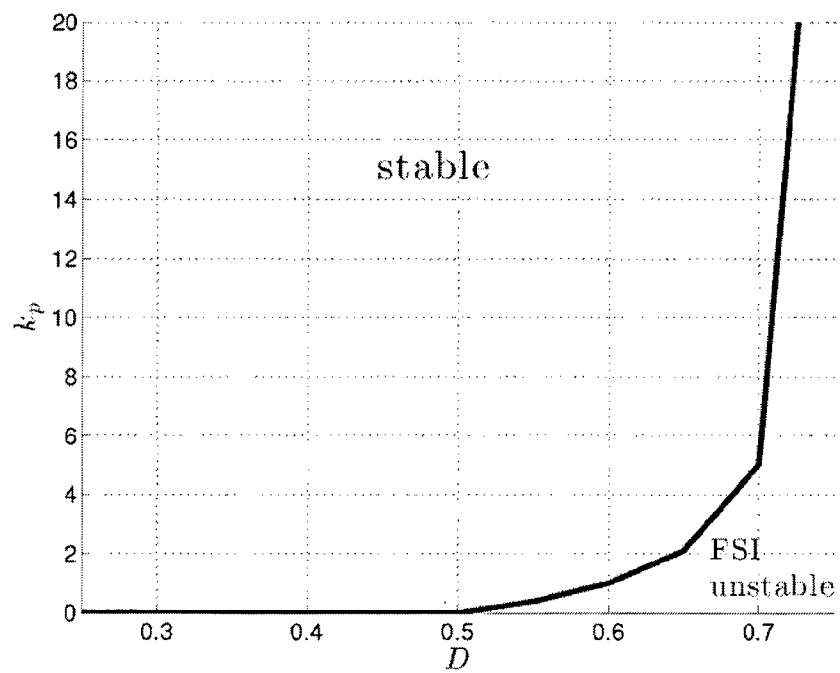


Figure 9