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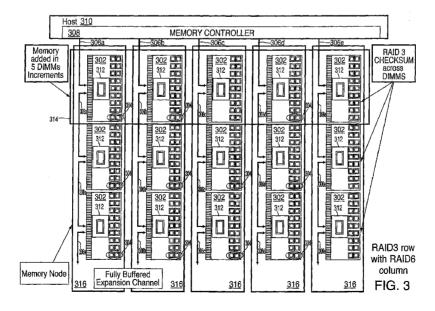
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(54) Title: SYSTEM AND METHOD FOR ERROR CORRECTION AND DETECTION IN A MEMORY SYSTEM



(57) Abstract: A system and method for error correction and detection in a memory system. The system includes a memory controller, a plurality of memory modules and a mechanism. The memory modules are in communication with the memory controller and with a plurality of memory devices. The mechanism detects that one of the memory modules has failed possibly coincident with a memory device failure on an other of the memory modules. The mechanism allows the memory system to continue to run unimpaired in the presence of the memory module failure and the memory device failure.

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	ata base consulted during the international search (name of data be	se and, where practical, search	terms used)	
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which citation "O" docume	ent which may throw doubts on priority claim(s) or is cited to establish the publication date of another n or other special reason (as specified) ent referring to an oral disclosure, use, exhibition or means	"Y" document of particular rele cannot be considered to in document is combined with	when the document is taken alone	
"P" docume	ent published prior to the international filing date but nan the priority date claimed	in the art. "&" document member of the s		
Date of the	actual completion of the International search	Date of mailing of the inter	national search report	
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Name and r	mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk	Authorized officer	-	
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