The invention provides apparatus and methods for detecting electromagnetic energy using an array of detectors arranged in at least one row and multiple columns. A single crystal body has multiple doped regions disposed therein. Each one of the detectors produces charge in a corresponding one of the doped regions in the body in response to electromagnetic energy impinging upon that detector. A first charge transfer device includes an output port and multiple serially coupled charge storage cells including multiple first charge transfer regions disposed in the body parallel to the row, or rows, of detectors. Multiple second charge transfer devices include multiple second charge transfer regions disposed in the body transverse to the row or rows, of detectors and the charge storage cells. Each one of the second charge transfer regions is adapted to charge transfer produced in a corresponding one of the doped regions to a corresponding one of the charge storage cells. Each one of the doped regions corresponding to one of the detectors has a doping profile adapted to produce an electric field in a direction from the doped region toward a corresponding one of the multiple second charge transfer regions. Such an arrangement allows dual polarization detection with little or no modification of the system configuration.
FIG. 4
FIG. 7B

VOLTS

1V

V

TIME

t

165
ELECTROMAGNETIC ENERGY DETECTION

BACKGROUND OF THE INVENTION

[0001] This invention relates generally to energy detection systems and more particularly to energy detection systems disposed on a single crystal substrate.

[0002] As is known in the art, electromagnetic energy detection systems have a wide range of application, e.g., from cameras to missile seekers. In such systems, electromagnetic energy, e.g., visible light or infrared energy, is focused by an optical system onto one, or more, electromagnetic energy detectors. Those detectors are often arranged in an array which is disposed at the focal plane of the optical system. The detector produces an indication of the detected energy by, for example, producing a corresponding electrical output signal. In one focal plane array, the detectors are semiconductor devices, such as HgCdTe or InSb, formed in different isolated regions of an upper surface of a single crystal semiconductor body. Thus, in response to light impinging upon the detector, charge is produced in the corresponding isolated region of the semiconductor body having the detector.

[0003] In one system, a read-out electronics (“ROE”), formed as an integrated circuit in a second semiconductor substrate, typically silicon, is mounted to a back surface of the first-mentioned substrate. The charge produced in the first-mentioned substrate passes to different isolated regions of the second-mentioned substrate through electrical contacts disposed therebetween. The read-out electronics provides clock signals to regulate the propagation of charge in the second-mentioned substrate to output signal processing circuitry. In order to transfer the charge produced in the first-mentioned substrate to the second substrate, a wire or other metal contacts are connected to ohmic contact diffusion regions in the semiconductor bodies to provide electrical contact. The ohmic contact regions result in the generation of generation-recombination (GR) noise. While this technique may be acceptable for some wavelengths of energy, the GR noise produced may create, in some applications, an unacceptably low signal to noise ratio (SNR) for some combinations of wavelength and substrate.

[0004] The use of a single silicon substrate for both the detectors and the read-out electronics has been suggested. However, with a silicon substrate, near infrared energy above about 8,000 Å passes readily through the substrate without generating sufficient charge for system SNR requirements. One technique has been presented in two articles, one entitled “Active-Pixel Image Sensor Integrated With Readout Circuits,” by Robert Nixon, Eric Fossum, and Sabrina Kemeny and the other entitled “CMOS Active-Pixel Image Sensor Containing Pinned Photodiodes,” by Eric R. Fossum both published in NASA Tech Briefs, October, 1996, from NASA’s Jet Propulsion Laboratory in Pasadena, Calif. In the articles, the authors describe an attempt at an image sensor including readout circuits and pinned diode detectors, for visible and ultraviolet light, on one chip. According to the second-mentioned article, however, the operation of the device has not been demonstrated.

SUMMARY OF THE INVENTION

[0005] In accordance with one feature of the invention, an electromagnetic energy detection system is provided having a plurality of detectors disposed in a single crystal body. Each one of the detectors is adapted to produce charge in a doped region disposed in the body in response to electromagnetic energy impinging upon such one of the detectors. A first charge transfer device (“CTD”) is provided having a plurality of first charge transfer regions disposed in the body and includes a plurality of serially coupled charge storage cells. A plurality of second charge transfer devices is provided for transferring the charge in a corresponding one of the doped regions to a corresponding one of the charge storage cells of the first charge transfer device.

[0006] With such an arrangement, ohmic contacts between each one of the detectors and the charge storage cells of the first charge transfer device are eliminated thereby reducing GR noise and improving the SNR performance of the detection system.

[0007] In accordance with another feature of the invention, an electromagnetic energy detection system is provided having a plurality of detectors disposed in a single crystal body. Each one of the detectors is adapted to produce charge in the body in response to electromagnetic energy impinging upon such one of the detectors. Read-out electronics is disposed on the body. The read-out electronics includes a first charge transfer device having a plurality of first charge transfer regions disposed in the body and includes a plurality of serially coupled charge storage cells. A last one of the cells is coupled to an output port. A charge coupling structure is disposed on the body to couple the charge produced by the detectors to the read-out electronics. The charge coupling structure includes a plurality of second charge transfer devices, including a plurality of second charge transfer regions, disposed in the body. Each one of the plurality of second charge transfer regions is adapted to transfer charge produced in a corresponding one of the detectors to a corresponding one of the plurality of charge storage cells. With such an arrangement, an effective electromagnetic energy detection system is provided wherein energy detectors, charge coupling structure and read-out electronics are formed on a single crystal substrate.

[0008] In a preferred embodiment of the invention, a shield is provided to reduce incident electromagnetic energy from impinging upon portions of the read-out electronics and portions of the charge coupling structure.

[0009] In accordance with still another feature of the invention, a detector is provided having a single crystal body with a doped region therein. Such detector is adapted to produce charge in the doped region in response to electromagnetic energy impinging upon such detector. A second region is disposed in the body and laterally displaced from the detector. The doped region has a doping profile selected to produce an electric field therein along a direction from the doped region toward the second region.

[0010] With such a structure, charge produced in the body is efficiently transferred from the doped region to a region displaced therefrom for processing by electronic circuitry also disposed on the body.

[0011] In a preferred embodiment, the body comprises silicon and the detector comprises a light detector.

[0012] In accordance with still another feature of the invention, apparatus is provided for reducing noise, e.g., transients, in an output of a charge transfer device formed in
a first region of a single crystal body. Such apparatus includes a transient suppression circuit. The circuit includes a pair of inputs; one of the inputs being coupled to the output of the charge transfer device and the other input being coupled to a second region of the body displaced from the first region. The circuit includes a differencing arrangement for subtracting signals at the pair of inputs to reduce noise components on at least one of such signals.

[0013] With such an arrangement, noise generated in the body is present at the output of the charge transfer device, along with a desired signal, and is also present in the second region of the body. Therefore, substantially the same noise is present at both of the inputs of the transient suppression circuit. The differencing arrangement combines the two signals at the two inputs to thereby cancel, or reduce, the noise present at the output of the charge transfer device thereby yielding the desired signal with a reduced noise component.

[0014] In accordance with another feature of the invention, an electromagnetic energy detection system is provided having a single crystal body. A detector is disposed in a first region the body. The detector produces charge in the body in response to electromagnetic energy impinging upon such detector. At least a portion of the produced charge passes through a second region of the body to an output port. A charge detector, disposed in the body, is coupled to the output port and produces a charge detector output signal indicative of detected charge. A sensor having an input port coupled to the body in a third region of the body produces a sensor output signal indicative of signals induced on the input port.

[0015] In a preferred embodiment, a differencing device is provided. The charge detector, the sensor, and the differencing device are arranged to provide an output indicative of detected energy. A first transfer device is provided to couple the produced charge from the detector to the output port. The charge detector is adapted to receive charges from the output port and to provide a charge detector signal. The sensor has an input coupled to the body in the third region of the body and is adapted to provide a sensor output signal. The differencing device is adapted to receive the charge detector signal and the sensor output signal to provide a difference output signal indicative of a difference of the sensor output signal and the charge detector signal. With such an arrangement, common mode noise is reduced, improving the dynamic range of the signal processing channel receiving the detected energy.

[0016] The invention provides numerous other advantages. For example, the invention provides a fully integrated system for real time image acquisition. Integrating multiphase clock generators, detectors, and read-out electronics on a single chip avoids a complex interface of wires and external electronics, allowing for simple and efficient system performance. Doping configurations and detector selection allow ±5V power supplies to operate the charge transfer devices, e.g., Buried Channel Charge Coupled Devices (BCCDs), and "pinned" diode detectors. By using buried channel charge coupled devices, extraneous wires are eliminated, reducing OR noise and improving SNR, and reducing stray inductance and capacitance and electromagnetic interference. The invention is easily adapted for multispectral (color) imaging to achieve multimegapixel color imaging, small package size, and low price, which is useful for applications such as scanning digital cameras. The invention is also suited for laser tomography.

BRIEF DESCRIPTION OF THE DRAWING

[0017] Other features and advantages of the invention, as well as the invention itself, will become more readily apparent when taken together with the following detailed description and the accompanying drawings, in which:

[0018] FIG. 1 is a diagrammatical layout of an electromagnetic energy detection system;

[0019] FIG. 2 is an enlarged view of a portion of the system of FIG. 1;

[0020] FIG. 3 is a simplified cross-sectional view of an electromagnetic detector and charge coupling structure, such cross-section being taken along line 3-3 in FIG. 2;

[0021] FIG. 4 is a plot of voltage as a function of vertical distance in the detector of FIG. 3;

[0022] FIG. 5A is cross-sectional view of an electromagnetic detector and charge coupling structure;

[0023] FIGS. 5B and 5C are plots of voltage gradients in the electromagnetic detector and charge coupling structure of FIG. 5A;

[0024] FIG. 6 is a cross-sectional view of charge transfer device read-out electronics, such cross-section being taken along the line 6-6 in FIG. 2;

[0025] FIG. 7A is a partially cross-sectional view and a partially schematic diagram of an output portion of the system of FIG. 1;

[0026] FIG. 7B is a voltage diagram of an output signal of a buffer amplifier of FIG. 7A;

[0027] FIG. 8 is an operational flow diagram of the system of FIG. 1;

[0028] FIG. 9 is a diagrammatical side view of a filter arrangement for the system of FIG. 1;

[0029] FIG. 10 is a side view of a gimbal scanning arrangement for the system of FIG. 1;

[0030] FIG. 11 is a side view of an aperture scanning arrangement for the system of FIG. 1; and

[0031] FIG. 12 is a schematic diagram of a Brewer detector arrangement.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

GENERAL

[0032] In FIG. 1, an electromagnetic energy detection system 10 is shown. The system 10 is formed on a single crystal semiconductor chip, or body 12, here having a p-type conductive silicon substrate 13. The detection system 10 is arranged in four similarly-structured quadrants 14a-14d. Each one of the quadrants 14a-14d includes an array of detectors 16-16, a charge transfer device read-out electronics (CTD ROE) 18 coupled to a read-out electronics driver section 20, a charge coupling structure 22 coupled to a charge coupling structure driver section 24, and a transient...
signal suppression circuit 26, all arranged as shown. The system 10 further includes a control circuit 27 disposed at one end of the body 12 as shown. The CTD ROE 18 and portions of the charge coupling structure 22, as described below, are charge transfer devices, preferably buried channel charge coupled devices. Connections from the control circuit 27 to the driver sections 20 and 24, and from the driver sections 20 and 24 to the charge transfer device read-out electronics 18 and to the charge coupling structures 22, respectively, are bus connections. The body 12 includes a plurality of interface pins 15. An n-type guarding 93 is implanted (e.g., doped with Phosphorous) in the substrate 13 surrounding the detectors 16, charge coupling structures 22, charge transfer device read-out electronics 18, and transient suppression circuits 26, and is biased, e.g., to 5V. The guarding 93 transfers spurious noise charges away from the detectors 16, 16, and the charge transfer device read-out electronics 18 to help preserve the SNR of the system 10.

[0033] Referring now also to FIG. 2, an exemplary one of the quadrants 14a-14d, here quadrant 14d is shown. The quadrant 14d includes a linear array 17 of the detectors 16, 16. Each one of the detectors 16, 16, is here a pin diode detector to be described in detail in connection with FIG. 3. Suffice it to say here, however, that each one of the detectors 16, 16, produces charge in body 12 in response to electromagnetic energy impinging upon such one of the detectors 16, 16. The charge transfer device read-out electronics 18 includes a plurality of serially coupled charge storage cells 28, 28. Each one of charge storage cells 28, 28, corresponds to one of the detectors 16, 16. The charge coupling structure 22 includes a plurality of charge transfer devices 30, 30, each one being between a corresponding one of the detectors 16, 16, and a corresponding one of the charge storage cells 28, 28.

[0034] The charge transfer devices 30, 30, are controlled by signals received from the charge coupling structure driver section 24 for transferring the charge in a corresponding one of the of the detectors 16, 16, through the substrate 13 to a corresponding one of the charge storage cells 28, 28, of the charge transfer device read-out electronics 18 as indicated by direction lines 31, 31a.

[0035] The charge transfer device read-out electronics 18 is controlled by signals received from the read-out electronics driver section 20 for transferring charge received from the charge transfer devices 30, 30, through the substrate 13 to an output port 32 as indicated by direction line 34. More particularly, the read-out charge transfer device 18 includes the output port 32 which is fed by the last one of the serially coupled charge storage cells 28, 28, i.e., by 28. The output port 32 is coupled to the transient signal suppression circuit 26. It is noted that the read-out electronics charge transfer device 18 is disposed parallel to the rows of detectors 16, 16. Each one of the charge transfer devices 30, 30, is disposed in the body 12 transverse to the linear array 17 of detectors 16, 16, and the charge storage cells 28, 28.

DETECTORS 16, 16

[0036] Referring now to FIG. 3, an exemplary one of the detectors 16, 16, here 16, along with the corresponding charge transfer device 30, of the charge coupling structure 22, and the corresponding charge storage cell 28, of the read-out electronics charge transfer device 18, are shown. The detector 16, is bordered on one end by a silicon dioxide insulator 42 and on the other end by the charge storage cell 28, of the charge transfer device read-out electronics 18. Such detector 16, includes a p-type anode 44 (e.g., doped with Boron), a cathode 45 provided by an undoped portion 47 of the substrate 13 (i.e., not altered from the original doping of the substrate 13), an n-type modulating layer 48, and an n-type Buried Channel Charge Coupled Device (BCCD) layer 50, all arranged as shown. The modulating layer 48 and the BCCD layer 50 are used to charge transfer produced by the detector 16, through the substrate 13 to the corresponding charge storage cell 28, of the charge transfer device read-out electronics 18 as indicated by directional arrow 31a. The cathode 45 is biased to the same potential as the anode 44, making the detector 16, a “pinned” diode (i.e., the anode 44 and cathode 45 are pinned to the same potential). The detector 16, is low lag pinned diode with potentials of the anode 44 and the substrate 13 set to ~5V.

[0037] To help collect produced charge, the anode 44, cathode 45, modulating layer 48, and BCCD layer 50 are arranged to have a doping profile to produce a voltage distribution along a vertical axis x of the detector 16. Referring also to FIG. 4, the voltage at a surface 54 of the anode 44 along axis x is biased to a voltage Vb. The voltage level increases from top to bottom in FIG. 4. The anode 44, modulating layer 48, BCCD layer 50, and substrate 13 have doping concentrations that produce voltage levels that, when moving away from the surface 54 along axis x into the detector 16, initially increase, reaching a maximum of Vm volts at a distance x<sub>m</sub> into the detector 16, and then gradually return to Vb approximately reaching Vb at distance x<sub>b</sub> into the detector 16. The thicknesses and doping concentrations are configured to produce a maximum voltage at a desired level and at a desired distance into the detector 16, in order to collect sufficient charge produced in the detector 16, to achieve an acceptable SNR. Typically, the anode 44 and modulating layer 48 are implanted less than several microns, but are capable of influencing the voltage levels further into the detector 16.

[0038] For example, the anode 44 can implanted to a depth of about 0.2 µm with an average carrier concentration of 10<sup>20</sup>/cm<sup>2</sup>, and the modulating layer 48 implanted to an effective depth of 0.4 µm, and Vb set to ~5V. With appropriate doping concentrations, Vm can be varied as desired, with x<sub>m</sub> being about 0.7 µm, and x<sub>b</sub> being about 4.5 µm.

[0039] To further help collect produced charge, the anode 44, cathode 45, modulating layer 48, and BCCD layer 50 are arranged to produce a voltage distribution along a horizontal axis y of the detector 16. The modulating layer 48 lies under a portion of the anode 44 close to the charge transfer device 30. The BCCD layer 50 lies under the entire modulating layer 48, plus an additional portion of the anode 44, but does not reach the insulator 42. The detector is thus asymmetrical about a centerline 149 of the detector 16, due to this asymmetrical arrangement and the doping of the layers along axis y (i.e., when moving along axis y from x<sub>y</sub> toward the charge transfer device 30), the voltage monotonically varies as a function of distance x<sub>y</sub> as will be described more fully in connection with FIGS. 5A-5C.

[0040] The voltage distributions produced by the layers produce electric fields in the detector 16, help collect charges produced in the detector 16. When electromagnetic
energy, e.g., light or infrared energy as indicated by arrow 51, impinges upon the detector 16, charges, e.g., charges 52a-52c, are produced in the detector 16. The voltage distributions discussed above produce electromagnetic fields, e.g., as indicated by vectors E1, E2, and E3, that urge the produced charges 52a-52c toward the potential minimum x0 (see FIG. 4) and toward the charge transfer device 30, as indicated by arrows 55a-55c. Thus, if energy with a wavelength, e.g., 8,100 Å, at which the silicon substrate 13 is substantially transparent (i.e., few charges are produced in the substrate 13 near the surface 54) is impinged upon the detector 16, then the voltage distributions improve the collection of produced charges from within the substrate 13 and urge them toward the charge transfer device 30, as further illustrated in FIG. 5A-5C and described below. For example, Schottky-barrier-diode detectors, e.g., PtSi detectors, can be used to detect Yttrium-Aluminum-Garnet (YAG) laser radiation. Frequency response of PtSi detectors reaches into the megahertz region.

CHARGE COUPLING STRUCTURE

[0041] Referring to FIG. 3, an exemplary one of the charge transfer devices 30-30, here 30, is shown. Such charge transfer device 30 includes: two gates 56 and 60, coupled to the charge coupling structure driver section 24 by lines 62 and 66 respectively, an oxide layer 68, a portion of the BCCD layer 50, and more of the undoped portion 47 of the substrate 13. The gates 56 and 60 overlap the oxide layer 68, such oxide layer 68 being formed on the surface 54 of the substrate 13. Beneath the oxide layer 68 is another portion of the BCCD layer 50, which overlies the undoped portion 47 of the substrate 13.

[0042] Charge transfer regions 70 and 74, are disposed beneath each of the gates 56 and 60 respectively, near to, but beneath, the surface 54. The oxide layer 68, BCCD layer 50, and substrate 13 are configured such that a "potential well" that collects charges will form in one of the charge transfer regions 70 or 74 by applying an appropriate bias potential on a corresponding one of the gates 56 or 60. Square wave clock signals swinging between two bias voltage levels VD and VDlow are supplied to gates 56 and 60 by one of the charge coupling structure driver sections 24 (using, e.g., CMOS inverter drivers) through lines 62 and 66, respectively. Coulombic forces produced by the clock signals supplied to gates 56 and 60 will dominate electron propagation in the charge transfer regions 70 and 74 if the gates have widths Wg less than about 10 μm. With widths Wg above about 10 μm, diffusion dominates the electron propagation. Because electron propagation by diffusion is much slower than when coulombic forces dominate, the gates preferably have widths Wg less than about 10 μm.

[0043] The detectors 16-16c, charge transfer devices 30-30c, and charge transfer device read-out electronics 18, are configured to facilitate charge transfer from the detectors 16-16c to the charge storage cells 28-28c and to isolate the charge detectors 16-16c from the charge storage cells 28-28c. The detector 16c and the charge transfer device 30c are disposed such that charges produced and collected in the detector 16c will be attracted to the potential well in charge transfer region 70 formed due to an appropriate bias on gate 56. The number of gates in the charge transfer device 16c and their widths Wg are selected, and the detector 16c, the charge transfer device 30c, and the charge transfer device read-out electronics 18 are disposed, such that the charge storage cell 28c is isolated from the energy impinging on the detector 16c. The charge transfer device 30 and the charge storage cell 28, are also disposed such that charges collected in the potential well in region 74 can be transferred to a potential well in a charge transfer region 76c in the charge storage cell 28c.

[0044] FIG. 5A shows a preferred arrangement for the detector 16c, the charge transfer device 30c, and the charge storage cell 28c, shown in FIG. 3. As shown in FIG. 5A, the modulating layer 48 of the detector has four regions 48a, 48b, 48c, and 48d. Region 48a is less heavily doped n-type than region 48b, which is less heavily doped n-type than region 48c, which is less heavily doped n-type than region 48d. The doping of the regions 48a, 48b, 48c and 48d creates a monotonic variance in the potential in these regions in the y direction (i.e., from the detector 16c toward the charge storage cell 28c). The charge transfer device 30c includes three gate regions 200, 200 and 200 each region having two gates 202 and 203. For example, gate region 200 has gates 202 and 203, coupled to the charge coupling structure driver section 24 through a conductor 204, and gate region 200, has gates 202 and 203, coupled to the charge coupling structure driver section 24 through a conductor 204. Doped regions 206 and 208, are disposed beneath gate 203, and doped regions 206 and 208 are disposed beneath gate 203. Regions 206 and 208 are more heavily doped n-type than the substrate 13, but less heavily doped n-type than regions 208. Regions 206 and 208 have widths W206 and W208 that are less than about 10 μm. The doping of the regions 206 and 208 creates a monotonic variance in the potential in these regions in the y direction (i.e., from the detector 16c toward the charge storage cell 28c).

[0045] The BCCD layer 50 and the doped regions 48a, 48b, 48c, 48d, 206 and 208 are formed by one or more of up to five implants. Each of the five implants are formed by implanting, e.g., Phosphorous or Arsenic, to form an n-type implant region having a selected average concentration in a selected implant depth (x), examples of which are shown in TABLE 1. The values shown in TABLE 1 are the parameters of each implant independent of any other implant.

<table>
<thead>
<tr>
<th>Implant</th>
<th>Average Concentration in Carriers/cm²</th>
<th>Depth (x) in μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5 x 10^19</td>
<td>3.0</td>
</tr>
<tr>
<td>2</td>
<td>2 x 10^19</td>
<td>0.2</td>
</tr>
<tr>
<td>3</td>
<td>5 x 10^21</td>
<td>0.3</td>
</tr>
<tr>
<td>4</td>
<td>2.5 x 10^12</td>
<td>0.4</td>
</tr>
<tr>
<td>5</td>
<td>5.5 x 10^10</td>
<td>0.4</td>
</tr>
</tbody>
</table>

The BCCD layer 50 is formed by implant 1. Region 48a is a combination of implants 1, 2, 3 and 5. Region 48b is a combination of implants 1, 2, 3, 4 and 5. The implants can be formed in any order to yield the desired combinations.

[0046] FIGS. 5B and 5C show how the potentials vary under the detector 16c, and the gate regions 200 and 200, at a depth x of about 0.5-0.7 μm (FIG. 4) under two bias conditions for the exemplary doping configuration of the regions 48a, 48b, 48c, 48d, 206 and 208 described above. FIG. 5B shows that when the charge coupling structure driver section applies zero volts on conductor 204, and -5
volts on conductor 204_y, the potential along axis y monotonically increases in regions 220, 221, 222, 223, 224, 225, and 226, and decreases between regions 226 and 227, producing a potential gradient that collects (i.e., integrates) charges 209 produced in the detector 16, under the doped region 208. FIG. 5C shows that when the charge coupling structure driver section 24 applies ~5 volts to the conductor 204_y and zero volts to conductor 204_x, the potential along axis x monotonically increases in regions 220, 221, 222, and 223, decreases between regions 223 and 224, and monotonically increases in regions 224, 225, 226, 227, 228, and 229, causing the charges 209 previously collected under region 208, to transfer and be collected under region 208. A gate 210 is coupled to the charge coupling driver section 24 by a conductor 212, and regulates the transfer of charge collected under region 208, to the charge storage cell 28. The dopings are configured to produce potential gradients to guard against charges flowing in a direction from the charge storage cell 28, toward the detector 16.

**CHARGE TRANSFER DEVICE READ-OUT ELECTRONICS**

[0047] FIG. 6 shows two exemplary ones of the charge storage cells 28, 28a, here cells 28, and 28b. The charge storage cell 28, and 28c include: six gates 78a-f, and 78a-f, respectively, coupled to the read-out electronics driver section 20 through line networks 80, 82a, 82b, and 82c; a portion of the BCCD layer 50; and a portion of the undoped portion 47 of the substrate 13. As shown, the charge storage cells 28, and 28c, are two-phase cells, one phase driving gates 78a, 78b, and 78a, 78b, and another phase driving gates 78d, 78e, and 78d, 78e. As shown in FIG. 6, the charge transfer device read-out electronics 18 is a two-phase buried channel charge coupled device.

[0048] The gates 78a-f, and 78a-f, are disposed above a portion of oxide layer 68. Beneath the oxide layer 68 is a portion of BCCD layer 50 that overlays a portion of undoped portion 47 of the substrate 13. Voltage profiles in the charge storage cells 28, 28a, beneath gates 78a, 78b, 78a, 78b, and 78d, are similar to that shown in FIG. 4, except that the voltage at a surface 84 is higher than V_d because the surface 84 is not pinned to the same voltage as the substrate 13. Also, under gates 78b, 78c, 78b, 78c, and 78d are gate doped regions 88a, 88c, 88a, 88c, and 88d, respectively. The gate doped regions 88a, 88c, 88a, 88c, and 88d, are more heavily doped n-type than gate doped regions 88a, 88c, 88a, 88c, and 88d, respectively. The gate doped regions 88b, 88a, 88b, and 88a, which are more heavily doped p-type than BCCD layer 50. For example, the gate doped regions 88b, 88a, and 88c, are formed using a combination of implants 1 and 2 (TABLE 1), and the gate doped regions 88c are formed using a combination of implants 1, 2, and 3 (TABLE 1). This doping profile is configured such that magnitudes of the potential wells in charge transfer regions 76a-f, and 76a-f, will vary monotonically along axis z (i.e., in a direction from charge storage cell 28, to charge storage cell 28a.) when appropriate bias potentials are applied to the gates 78a-f, and 78a-f. Thus, charge is collected in the potential wells in charge transfer regions 76f, and 76f, under one bias condition, and in charge transfer regions 76c, and 76c, in another bias condition.

[0049] The gates 78a-c, and 78a-c, are coupled through line networks 80, and 82, to read-out electronics drivers 92a, and 92a, respectively, and the gates 78d-f, and 78d-f, are coupled through similar line networks 80, and 82, to read-out electronics drivers 92d, and 92d, respectively. The read-out electronics drivers 92a-b, 92a-b, are CMOS inverter drivers, with sources of p-channel drivers bussed in common and sources of n-channel drivers bussed in common, and are disposed in the read-out electronics driver section 20. The read-out electronics drivers 92a-b, and 92a-b, supply phase clocks (i.e., a square wave swing between two bias voltages H_D low, and H_D high provided to the system 10) to the gates 78d-f, and 78d-f, and, as diagrammatically shown in FIG. 6, are distributed over the body 12 in the read-out electronics driver section 20, to among other things, help dissipate heat.

[0050] The gates 78a-f, 78a-f, are dimensioned and disposed to facilitate charge transfer as indicated by directional line 34. As with the gates 56 and 60 of the charge transfer devices 30, 30a, the gates 78a-f, 78a-f, preferably have widths W_s of less than about 10 μm to help ensure that electron propagation in transfer regions 76a-f, 76a-f, occurs due to coulombic forces and not diffusion. Thus, the configuration shown in FIG. 6 works well with charge storage cell widths W_s up to about 60 μm of gate width plus some distance for the spaces between the gates. The charge storage cells 28, and 28c, are disposed such that charges collected in a potential well in charge transfer region 76f, in charge storage cell 28, can be transferred to a potential well in charge transfer region 76a in charge storage cell 28c. The dopings of the charge storage cells 28 are configured to produce potential gradients to guard against charges flowing in a direction opposite directional line 34.

**TRANSIENT SUPPRESSION CIRCUIT**

[0051] As shown in FIG. 7A, an output port 94 of each of the quadrants 14a-14d, here quadrant 14d, includes a transient suppression circuit 26 having an input port 100 coupled to the output port 32 of a buffer stage 126 of the charge transfer device read-out electronics 18, and having an input port 102 coupled to a region 106 of the substrate 13 in a transient coupling region 300. An output port region 104 of the buffer stage 126 is coupled to the last charge storage cell 28a, and region 106 is displaced from, but in close proximity to, region 104.

[0052] More particularly, buffer stage 126 includes an output gate 130 and a reset transistor 137. The output gate 130 overlays a portion of the oxide layer 68. Layer 68 overlays a portion of the BCCD layer 50 which overlays more of the undoped portion 47 of the substrate 13. The output gate 130 is biased by a constant voltage V_d and is disposed proximate to the gate 78f, of the last charge storage cell 28a. Charges are transferred between the charge transfer region 76f, in the charge storage cell 28, to a charge transfer region 128 under the output gate 130 as indicated by directional line 34. As further indicated by directional line 34, a heavily doped n-type diffusion region 132, disposed in the output port region 104 of the substrate 13, attracts the charges from the charge transfer region 128. A line 134 (see also FIGS. 1 and 2) couples the diffusion region 132 to the output port 32 of the charge transfer device read-out electronics 18. The reset transistor 137 includes the diffusion region 132, a reset gate 133 and a diffusion region 135. The reset gate 133 is coupled to the control circuit 27 and is disposed on the surface 54 of the substrate 13 in close
proximity to the diffusion region 132. The diffusion layer 135 is heavily doped n-type and is disposed adjacent to the reset gate 133. The diffusion layer 135 is biased by a DC voltage $V_r$ that is at a higher level than the well potential in charge transfer region 76c. A pulsed voltage on the reset gate 133 causes the diffusion layer to be reset to the DC voltage $V_r$.

[0053] The transient coupling region 300 includes a reset transistor 140 similar to reset transistor 137, a pseudo charge storage cell 28x, and a gate 302. The reset transistor 140 includes a diffusion layer 120 disposed in region 106 of the substrate 13, a reset gate 142 coupled to the control circuit 27, and a diffusion region 144 biased to DC voltage $V_r$. Portions of transient signals travelling through the body 12 due to, e.g., edges of clocking signals such as a frame sync signal or a pixel clock signal discussed below, are coupled through the diffusion region 120. The diffusion region 120 is displaced from the diffusion region 132 far enough that the diffusion region 120 will not attract charges from the charge transfer region 128, but is disposed near enough to the diffusion region 132 such that the diffusion region 120 receives substantially the same transient signals as the diffusion region 132 does. The gate 302 is biased to voltage $V_r$ and couples the region 106 to the pseudo charge storage cell 28x. The pseudo charge storage cell 28x, shown in simplified fashion, is configured the same as charge storage cells 28-28, except that it is isolated from other charge storage cells 28 and from the charge transfer devices 30. Thus, as shown, the BCCD layer 50 has an edge 304 disposed proximate to an edge 306 of the pseudo charge storage cell 28x.

[0054] The transient suppression circuit 26 includes a main signal buffer amplifier 146 coupled to the input port 100, a pseudo signal buffer amplifier 162 coupled to the input port 102, and a differentiating amplifier 150 for subtracting signals at the pair of input ports 100 and 102 to reduce transient signal components of the signal on input port 100. The main signal buffer amplifier 146 is coupled to the output port 32 and includes a main signal output port 122. The pseudo signal buffer amplifier is connected to a diffusion region 120 of the body 12 and provides a pseudo signal output port 124.

[0055] The main signal buffer amplifier 146 processes charges received from the output port 32. The diffusion region 132 of the reset transistor 137 serves as a floating diffusion charge detector. Detected charges are coupled through a line 134 to the output port 32 of the charge transfer device read-out electronics 18. Line 134 (FIGS. 1 and 2) couples charges from the output port 32 through the input port 100 to the main signal buffer amplifier 146, inducing a corresponding current signal at the main signal output port 122. Port 122 is coupled through a line 148 to the differentiating amplifier 150. Alternatively, port 122 may be coupled, e.g., to one of the pins 15 (FIG. 1) on the periphery of the body 12.

[0056] The pseudo signal buffer amplifier 162 processes signals present in the body 12. Charges due to transient signals are coupled from the diffusion region 120, which serves as a transient signal sensor, by a line 152 (FIGS. 1 and 2) through the input port 102 to the pseudo signal buffer amplifier 162. The sensed transient signals on line 152 induce a corresponding sensor output current signal at the pseudo signal output port 124. Port 124 is coupled through a line 164 to the differentiating amplifier 150. As with port 122, port 124 may be coupled, e.g., to one of the pins 15 (see FIG. 1) on the periphery of the body 12.

[0057] The differentiating amplifier 150 is configured to remove the signal on line 164 (i.e., the output of amplifier 162) from the signal on line 148 (i.e., the output of amplifier 146). The output of the amplifier 146 is a boxcar signal as shown in FIG. 7B, having a DC bias of about +1V, having a period matching the period of the charge transfer device read-out electronics 18, and having heights of signal portions 165 representative of energy detected by the detectors 16-16, (i.e., the output of the amplifier 146 is an analog signal digitally controlled). This signal also includes transients from the system 10 that are not representative of energy detected by the detectors 16-16. The output of the amplifier 162 is also a boxcar signal that is representative of the transients in the system 10 but not of the energy detected by the detectors 16-16. Thus, by matching and subtracting the signal on line 164 from the signal on line 148, the differentiating amplifier 150 performs common mode rejection, yielding a signal on line 166 (see also FIGS. 1 and 2) representative of detected energy and little, if any, stray energy. “Matching” means that the signals on lines 148 and 164 are amplified so that the transients present in both signals are substantially equal in magnitude. The signal on line 166 facilitates analog to digital conversion for, e.g., image processing.

CONTROL CIRCUIT

[0058] The control circuit 27 is shown in FIG. 8 to provide control signals to each of the read-out electronics driver sections 20, and to each of the charge coupling structure driver sections 24 (it being noted that, for clarity, only the read-out electronics driver section 20 and the charge coupling structure driver section 24 for quadrant 14d are shown) to control energy detection and readout from the detectors 16-16. Clock bias signals CLCBIAS, a ground potential GND, and bias potentials $V_{DDP}$, $V_{SSP}$, $V_{DDP}$, $V_{DDH}$, and $V_{DDH}$, are supplied to the system 10 through the pins 15 (FIG. 1). Due to the doping profiles and configurations discussed above, $V_{DDH}$ and $V_{DDH}$ are $+5V$ and $V_{DDP}$ and $V_{DDP}$ are $-5V$. A pixel clock signal 168 and a frame sync signal 170 are supplied to the system 10 through the pins 15 to the control circuit 27. The control circuit 27 processes the pixel clock and frame sync signals in on-chip multiphase clock generation circuitry to produce charge coupling structure clock signals (i.e., vertical clock signals) $V_{CH}$, $V_{CH}$, and charge transfer device read-out electronics clock signals (i.e., horizontal clock signals) $H_{CH}$ and $H_{CH}$.

[0059] The charge coupling structure driver section 24 processes the vertical clock signals $V_{CH}$, $V_{CH}$ to produce vertical driver signals $V_{DS}$, $V_{DS}$. These clock signals are square waves swinging between two bias voltages, $V_{DD}$ and $V_{DD}$, and are coupled to the charge transfer devices 30-30, (i.e., vertical CTDs) in parallel.

[0060] The read-out electronics driver section 20 processes the horizontal clock signals $H_{CH}$ and $H_{CH}$ to produce horizontal driver signals $H_{DS}$ and $H_{DS}$ for the charge transfer device read-out electronics 18 (i.e., the horizontal CTD 18). The horizontal driver signals $H_{DS}$ and $H_{DS}$ are
square waves swinging between two bias voltages, \(H_{\text{high}}\) and \(H_{\text{low}}\), and are coupled to the gates, e.g., to gates 78a, 78b, 78c, and 78d, respectively (see FIG. 6), of the charge storage cells 28a, 28b.

[0062] The control circuit 27 also regulates the charge detector 137. A pulsed voltage reset signal RST is sent from the control circuit 27 to the reset transistors 137 and 140 just before the read-out electronics begins serially transferring charges from the n charge storage cells 28a, 28b.

[0063] As shown in FIG. 9, a filter subsystem 171 including a wavelength filter 172, a polarization separator 174, (e.g., a birefringent wedge), a shield 175, and a polarizer 176, are arranged to pass copolarized radiation to one row of detectors 16a and crosspolarized radiation to another row of detectors 16b. The filter 172 is disposed above the body 12 to intercept radiation as indicated by rays \(R_1\), \(R_2\) and \(R_3\), which have wavelengths \(\lambda_1\), \(\lambda_2\), and \(\lambda_3\), respectively. The filter 172 inhibits radiation, e.g., ray \(R_3\), having a wavelength outside a desired range from passing through the filter 172. Radiation, e.g., rays \(R_1\), and \(R_2\), having wavelengths within the desired range is allowed to pass through the filter 172 to the separator 174.

[0064] The separator 174 separates incident radiation into orthogonal polarizations, sending copolarized radiation \(R_{1\text{co}}\) of ray \(R_1\) toward the first row of detectors 16a and crosspolarized radiation \(R_{1\text{x}}\) of ray \(R_1\) toward the second row of detectors 16b. To separate the orthogonal polarizations of radiation, the separator 174 affects the phasing of the two polarizations differently. However, because the two rays \(R_1\) and \(R_2\) are incident from different areas, and therefore have different incident angles with respect to the separator 174, some of the crosspolarized radiation \(R_{1\text{x}}\) of ray \(R_1\) is directed by the separator 174 toward the first row of detectors 16a.

[0065] The shield 175 allows radiation, whether copolarized or crosspolarized, to impinge on the rows of detectors 16a and 16b while inhibiting the radiation from impinging upon other portions of the system 10. Radiation is permitted to pass through openings 177 and 179 in the shield 175 to the polarizer 176. The openings 177 and 179 have sizes substantially matched to sizes of the arrays 17.

[0066] The polarizer 176 helps ensure that only copolarized radiation reaches the first row of detectors 16a and only crosspolarized radiation reaches the second row of detectors 16b, which are separated by an insulator 178. Portions 176a and 176b only allow copolarized and crosspolarized radiation, respectively, to pass through them. Therefore, the crosspolarized radiation \(R_{1\text{x}}\) is not allowed to reach detectors 14a.

[0067] As shown in FIG. 10, the detection system 10 may be scanned using a gimbal arrangement 180. The gimbal arrangement 180 includes a motor/base 182, a bottom member 184, and a top member 186 attached to the bottom of system 10. The motor 182 cyclically drives the top member 186 to pivot with respect to the bottom member 184 about a pin 188, causing a field of view of the detectors 16 to be scanned as indicated by arc 190. Thus, the field of view of the detectors 16 is directed at different portions of the arc 190 at different times during a cycle of the motor 182.

OPERATION

[0068] In operation, electromagnetic energy is impinged upon the system 10 by directing the system 10, and filtering and separating the impinging energy, as desired using, e.g., the apparatus of FIGS. 9-10. For example, laser energy is directed at a target and the system 10 is directed to receive the laser energy reflected from the target. More particularly, the system 10 can detect YAG laser radiation if PSI detectors are used for the detectors 16.

[0069] By controlling the timing and amplitudes of the vertical driver signals VDS1, VDS2, and the horizontal driver signals HDS1, HDS2, the control circuit 27 regulates the transfer of charge from the detectors 16b to 16e, in each of the quadrants 14a-d to the output port 32. Beginning at the first rising edge of the pixel clock signal 168 after the frame sync signal 170 changes to its active state, the control circuit 27 sequentially actuates gates 56a, 56b, in parallel and 60a, 60b, (see FIG. 3) in parallel. Potential wells are sequentially produced similar to those shown in FIGS. 5B and 5C to charge transfer charge produced in the detectors 16b, 16e, to charge transfer regions 74a, 74b, where the charges are then ready to be transferred to the charge storage cells 28a, 28b, of the charge transfer device read-out electronics 18. Gate 210 (FIG. 5A) is then activated while HDS1 and HDS2 are set to fixed levels, thus allowing charge to flow into the charge storage cells 28a, 28b. Gate 210 is then deactivated. The control circuit 27 then actuates the gates 78a, 78b, 78c, to produce potential gradients, similar to those shown in FIGS. 5B and 5C, to serially move the charges to the output port 32.

[0070] It is noted that charges produced in the detectors 16b, 16e, are inhibited from passing through any diffusion regions or ohmic contacts between the detectors 16b, 16e, and the end of the charge transfer device read-out electronics 18. The charges produced in the detectors 16b, 16e, are transferred within (i.e., remain in) the substrate 13 until read out through the diffusion region 132 to the output port 32. This helps reduce noise and improve SNR, helping detection of near-infrared radiation that is substantially transparent to the substrate 13.

[0071] While the charges from the detectors 16b, 16e, are integrated and transferred in parallel through the charge transfer devices 30, 30, to the charge storage cells 28a, 28b, of the charge transfer device read-out electronics 18, earlier produced charges are serially transferred to, and read out from, the output port 32.

[0072] As the charges are received by the output port 32, signals are induced in the main signal circuit 116 and the pseudo signal circuit 118. These induced signals are amplified in buffer amplifiers 146 and 162. The amplified signals are coupled to the differentiating amplifier 150 which rejects
common modes of the outputs of the buffer amplifiers 146 and 162, yielding a signal that is substantially free of information unrelated to the detected energy from the detectors 160, 161. Alternatively, the amplified signals can be coupled to pins 15 for processing external to the system 10.

[0073] Other embodiments are within the spirit and scope of the appended claims. For example, instead of using the gimbal arrangement of FIG. 10, as shown in FIG. 11 the system 10 could be scanned using a moving window 192 having an aperture 194. The aperture 194 permits energy within a field of view 196 to reach the row of detectors 16a. By moving the window 192, the field of view 196 shifts, thereby exposing the detectors 16 to energy from different areas. Alternatively, the window 192 could be configured to be stationary, with the aperture 194 moving within the window 192. Also, the system 10 can include appropriate internal clock generators to produce the frame sync signal 170 and the pixel clock signal 168. Thus, those signals do not need to be brought in from outside of the system 10 through the pins 15.

[0074] Furthermore, a Brewer detector can be coupled to the end of the charge transfer device read-out electronics 18 to eliminate the diffusion region 132 (FIG. 7A). A Brewer detector arrangement 400 is shown schematically in FIG. 12. A PMOS transistor 402 has its drain 404 coupled to the substrate 13 in the output port region 104. The drain 404 is further coupled to a gate 406 of the transistor 402 and biased to a fixed DC voltage $V_{bias1}$. A source 408 of the transistor 402 is coupled through line 410 to a buffer amplifier 412. The line 410 is also coupled to a fixed DC voltage $V_{bias2}$ (e.g., +5V) through a current source $I_{bias}$. The presence of a buried channel charge packet 414 is detected as a difference in the voltage at the source 408. The buffer amplifier 412 provides the main signal output port 122 (FIG. 7A). For more information about Brewer detectors, reference is made to “The Low Light Level Potential of a CCD Imaging Array” by R. J. Brewer, IEEE Transactions on Electron Devices, Vol. ED-27, No. 2, February, 1980.

What is claimed is:

1. An electromagnetic energy detection system, comprising:
   a single crystal body;
   a plurality of detectors, each one thereof producing charge in the body in response to electromagnetic energy impinging upon such one of the plurality of detectors;
   a first charge transfer device having a plurality of first charge transfer regions disposed in the body and including a plurality of serially coupled charge storage cells;
   a plurality of second charge transfer devices including a plurality of second charge transfer regions disposed in the body, each one of the plurality of second charge transfer regions being adapted to transfer charge produced in a corresponding one of the detectors to a corresponding one of the plurality of charge storage cells; and
   an output port coupled to a last one of the plurality of charge storage cells.

3. The system recited in claim 2 wherein the first charge transfer device and the plurality of second charge transfer devices are buried channel charged coupled devices.

4. The system recited in claim 3 wherein the plurality of charge storage cells include first gates disposed above the first charge transfer regions, the system further comprising a plurality of first charge transfer device drivers distributed on the body and coupled to corresponding charge storage cells for supplying bias voltages to the first gates.

5. The system recited in claim 3 wherein a cell of the first charge transfer device comprises two sets of gates, each set coupled to a separate potential bias source and including three gates disposed above the first charge transfer regions, and wherein the first charge transfer regions beneath each of the three gates in each set have different doping configurations.

6. The system recited in claim 5 wherein the doping configurations beneath each of the three gates in each set vary monotonically in a direction of charge flow in the charge transfer device.

7. The system recited in claim 2 wherein the plurality of detectors are diodes having an upper doped region disposed in the body, the upper layer being biased to substantially the same potential as the body.

8. The system recited in claim 2 further comprising a guarding disposed and configured to inhibit electromagnetic energy from impinging upon portions of the first charge transfer device and portions of the plurality of second charge transfer devices.

9. The system recited in claim 2 further comprising clock circuitry coupled to the first and second charge transfer devices and adapted to provide first clock signals to the first charge transfer device and second clock signals to the plurality of second charge transfer devices.

10. The system recited in claim 2 further comprising a charge detector coupled to the first charge transfer device and adapted to receive charges from the first charge transfer device and to provide a charge detector output.

11. The system recited in claim 10 further comprising:
   a detector having an input coupled to the body in a region of the body substantially isolated from the plurality of detectors and adapted to provide a detector output; and
   a differentiating device adapted to receive the charge detector output and the detector output and to provide a differentiating output indicative of a difference of the detector output and the charge detector output.

12. A detection system, comprising:
   a single crystal body having a plurality of doped regions disposed therein;
an array of detectors arranged in at least one row and a plurality of columns, each one of the detectors producing charge in a corresponding one of the doped regions in the body in response to electromagnetic energy impinging upon such one of the detectors;

a first charge transfer device including a first plurality of charge transfer regions disposed in the body and a plurality of serially coupled charge storage cells disposed parallel to the at least one row of detectors; and

a plurality of second charge transfer devices including a second plurality of charge transfer regions disposed in the body, each one of the plurality of second charge transfer devices being disposed transverse to the at least one row of detectors and the first charge transfer device, each one of the second plurality of charge transfer regions being adapted to transfer charge produced in a corresponding one of the detectors to a corresponding one of the plurality of charge storage cells.

13. The system recited in claim 12 including an optical system for scanning a field of view of the array of detectors.

14. The system recited in claim 12 further comprising a control system for transferring charge from each one of the doped regions corresponding to one of the detectors to a corresponding one of the charge storage cells through a corresponding one of the second charge transfer devices in parallel and for serially coupling the charge in each of the charge storage cells to an output of the of the first charge transfer device.

15. A detection system, comprising:

a single crystal body having a plurality of doped regions disposed therein;

an array of detectors arranged in at least one row and a plurality of columns, each one of the detectors producing charge in a corresponding one of the doped regions in the body in response to electromagnetic energy impinging upon such one of the detectors;

a first charge transfer device including an output port and a plurality of serially coupled charge storage cells including a plurality of first charge transfer regions disposed in the body parallel to the at least one row of detectors;

a plurality of second charge transfer devices including a plurality of second charge transfer regions disposed in the body, each one of the plurality of second charge transfer devices being disposed transverse to the at least one row of detectors and the first charge transfer device, each one of the plurality of second charge transfer regions being adapted to transfer charge produced in a corresponding one of the doped regions to a corresponding one of the plurality of charge storage cells;

a controller coupled to the first charge transfer device and the plurality of second charge transfer devices, the controller adapted to regulate the transfer of charge from the doped regions corresponding to the detectors to the output port; and

wherein each one of the doped regions corresponding to one of the detectors has a doping profile adapted to produce an electric field in a direction from the doped region toward a corresponding one of the plurality of second charge transfer regions.

16. In combination:

a single crystal body;

da detector having a doped region disposed in the body, such detector being adapted to produce charge in the doped region in response to electromagnetic energy impinging upon such detector;

a second region disposed in the body and displaced from the detector; and

wherein the doped region has a doping profile selected to produce an electric field therein in a direction from the doped region toward the second region.

17. The combination recited in claim 16 wherein the single crystal body comprises silicon.

18. The combination recited in claim 16 wherein the detector comprises a light detector.

19. The combination recited in claim 16 further comprising a buried channel charge coupled device disposed in the second region.

20. An electromagnetic energy detection system comprising:

a single crystal body;

da detector, disposed in a first region of the body, for producing charge in the body in response to electromagnetic energy impinging upon such detector, and for providing at least a portion of the produced charge through a second region of the body to an output port;

a charge detector coupled to the output port and producing a charge detector output signal indicative of detected charges; and

a sensor having an input port coupled to the body in a third region of the body and producing a sensor output signal indicative of signals induced on the input port.

21. The system recited in claim 20 further comprising a differencing device coupled to the charge detector and the sensor, the differencing device adapted to produce a differencing device output indicative of a comparison of the sensor output signal and the charge detector output signal.

22. In a system including a charge transfer device formed in a first region of a single crystal body, an apparatus comprising:

a first input coupled to an output of the charge transfer device;

a second input coupled to a second region of the body displaced from the first region; and

a differencing arrangement coupled to the first and second inputs and adapted to subtract a second signal present at the second input from a first signal present at the first input.

23. A method comprising steps of:

impinging electromagnetic energy upon a plurality of detectors to produce charges in a first portions of a single crystal body;

transferring at least portions of the charges in the first portions of the body to a plurality of cells corresponding to the plurality of detectors, the plurality of cells being disposed in second portions of the body; and
transferring at least portions of the charges between the plurality of cells toward a first output port coupled to the plurality of cells.

24. The method recited in claim 23 wherein the second portions of the body are substantially isolated from the electromagnetic energy impinged upon the first portions of the body.

25. The method recited in claim 23 further comprising:
   - detecting the charges received by the first output port and providing a first signal indicative of the detected charges;
   - sensing signals present in a region of the body substantially isolated from the first portions of the body and providing a second signal indicative of the sensed signals; and
   - comparing the first signal with the second signal.

26. The method recited in claim 23 wherein the step of transferring at least portions of the charges to the plurality of cells comprises selectively biasing portions of the body between the plurality of detectors and the plurality of cells.

27. The method recited in claim 23 wherein the step of transferring at least portions of the charges between the plurality of cells comprises selectively biasing portions of the body between the plurality of cells.

28. The method recited in claim 23,
   - wherein the step of transferring at least portions of the charges between the plurality of cells comprises serially transferring between the cells charges that were produced in a first time period;
   - wherein the step of transferring at least portions of the charges produced in the first portions of the body to the plurality of cells comprises transferring in parallel charges that were produced in the first portions of the body in a second time period, after the first time period; and
   - wherein the two transferring steps occur substantially simultaneously.

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May 31, 2001