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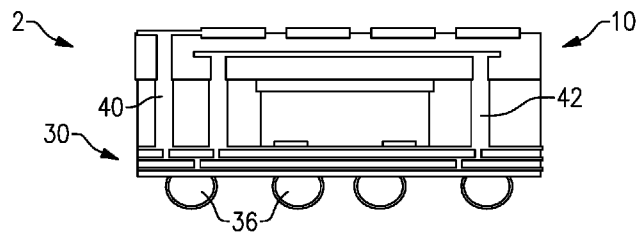


FIG. 2D

(57) Abstract: An integrated device package is disclosed. The integrated device package can include an antenna structure and an integrated device die electrically coupled to the antenna structure. The antenna structure can be formed with a system board or separated from the system board. When the antenna structure is formed with the system board, the integrated device package can include a redistribution layer having conductive routing traces such that the integrated device die is disposed between the system board and the redistribution layer, and the integrated device die is electrically coupled to the antenna structure at least partially through one or more of the conductive routing traces of the redistribution layer. When the antenna structure is separated from the system board, the integrated device die can be positioned between the antenna structure and the system board, and the integrated device die can be electrically coupled to the antenna structure at least partially through one or more of conductive routing traces of the system board and conductive wire of an interconnect structure between the system board and the antenna structure.



RADIO FREQUENCY DEVICE PACKAGES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Patent Application No. 63/271,042, filed October 22, 2021, titled “RADIO FREQUENCY DEVICE PACKAGES,” and U.S. Provisional Patent Application No. 63/343,325, filed May 18, 2022, titled “RADIO FREQUENCY DEVICE PACKAGES,” the entire contents of each of which are hereby incorporated herein by reference.

BACKGROUND

Field

[0002] The field generally relates to integrated device packages, and in particular, to radio frequency (RF) packages.

Description of the Related Art

[0003] High performance radio frequency (RF) devices are in high demand today. The performance of an RF device can be based on, for example, its gain, bandwidth, directivity, etc. The RF device can include an antenna structure and a die (e.g., radio frequency integrated circuit (RFIC), transceiver die, etc.). The manner in which the antenna structure and the die are packaged can affect the performance of the RF device. Efficiently designed Antenna in Package (AiP) or Antenna on Package (AoP) structures may simplify the module complexities while providing a performance boost for the evolving wireless technology landscape. It can be difficult to manufacture high performance RF devices that are compact and reliable. Accordingly, there remains a continuing need for improved RF device packages.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The detailed description is set forth with reference to the accompanying figures. The use of the same reference numbers in different figures indicates similar or identical items.

[0005] For this discussion, the devices and systems illustrated in the figures are shown as having a multiplicity of components. Various implementations of devices and/or

systems, as described herein, may include fewer components and remain within the scope of the disclosure. Alternatively, other implementations of devices and/or systems may include additional components, or various combinations of the described components, and remain within the scope of the disclosure.

[0006] Figures 1A-1F show steps in a method of manufacturing an integrated device package, according to one embodiment.

[0007] Figures 2A-2D show steps in a method of manufacturing an integrated device package, according to another embodiment.

[0008] Figures 2E-2H show steps in a method of manufacturing an integrated device package, according to another embodiment.

[0009] Figures 3A-3F show steps in a method of manufacturing an integrated device package, according to another embodiment.

[0010] Figures 4A-4E show steps in a method of manufacturing an integrated device package, according to another embodiment.

[0011] Figures 5A-5E show steps in a method of manufacturing an integrated device package, according to another embodiment.

[0012] Figures 6A-6E show steps in a method of manufacturing an integrated device package, according to another embodiment.

[0013] Figures 7A-7E show steps in a method of manufacturing an integrated device package, according to another embodiment.

[0014] Figure 8 is a schematic cross sectional side view of an integrated device package according to an embodiment.

[0015] Figure 9A is a schematic cross sectional side view of the integrated device package 7 according to an embodiment.

[0016] Figure 9B is a schematic top plan view of the integrated device package of Figure 9A.

[0017] Figure 9C is a schematic cross sectional side view of the integrated device package according to another embodiment.

[0018] Figure 9D is a schematic top plan view of the integrated device package of Figure 9C.

[0019] Figure 9E is a schematic cross sectional side view of the integrated device package according to another embodiment.

[0020] Figure 9F is a schematic cross sectional side view of the integrated device package according to another embodiment.

[0021] Figure 9G is a schematic cross sectional side view of the integrated device package according to another embodiment.

DETAILED DESCRIPTION

[0022] In various technologies such as wireless communications technologies, communication frequency has been increasing and likely will continue to increase. For example, in a typical cellular network, frequencies can be on the order of at least a few GHz. With new standards (e.g., a 5G standard), frequencies can be substantially higher, for example, at least 25 GHz, at least 50 GHz, at least 75 GHz, at least 94 GHz, at least 160 GHz, at least 300 GHz etc. Unlike systems compatible with a 4G standard, systems (e.g., millimeter wave (mmWave) systems) compatible with the 5G standard incorporate phased-array antennas, which include an array of antennas with individual radiating elements. A phased-array antenna can electrically steer a beam in multiple directions using beamforming techniques.

[0023] An antenna structure can be placed on a board that is separate from a radio frequency integrated circuit (RFIC) chipset. This approach is known as a discrete antenna approach. An antenna structure and the RFIC can also be integrated into a single package. Such integrated structure can be referred as an antenna-in-package (AiP). The AiP can make the distance between the antenna structure and the RFIC closer, which can contribute to improving transmitter efficiency and receiver noise as compared to the discrete antenna approach. The RFIC chipset may include transceiver ICs, power amplifier (PA), low-noise amplifier (LNA), switch, etc.

[0024] A connection between an RF system-in-package (SiP), such as the RFIC, and the antenna structure in the AiP, preferably has a relatively low insertion loss and good impedance matching, while the antenna structure placement may be controlled for improved radiation performance. There are tradeoffs in designing the AiP. For example, electrical

performance, thermomechanical reliability, compactness, manufacturability, and cost can be affected by a choice of the design of the AiP.

[0025] Various embodiments disclosed herein relate to an integrated device package that includes an antenna structure and an integrated device die (e.g., radio frequency integrated circuit (RFIC)) chipset coupled to the antenna structure. Various embodiments disclosed herein can enable a distance between the antenna structure and the die to be relatively short, thereby improving a transmitter efficiency and/or a receiver noise figure. The integrated device die can be mounted on a carrier such as a printed circuit board (PCB). In some embodiments, the antenna structure can be formed with a redistribution layer that is coupled to the carrier. The redistribution layer and the carrier can be electrically connected through an interconnect structure. The interconnect structure can comprise a standing bond wire, such as an array of standing bond wires (e.g., a bond via array (BVA[®])) or a conductive post, such as an array of conductive post. The BVA can comprise an array of bond wires that extend from conductive portions of the carrier. Connecting the element to the redistribution layer through the BVA can beneficially enable the integrated device package to improve its performance while reducing its manufacturing cost. The BVA can be structured so as to provide a shielding function. For example, the BVA can be formed with a pitch narrower than an operating frequency of the antenna structure to shield the integrated device die from the radio frequency having the operating frequency. Additional example BVA structures and implementations may be found throughout U.S. Patent No. 10,559,537, the entire contents of which are incorporated by reference herein in their entirety and for all purposes. The interconnected structure can comprise a electroplated conductive post or pillar. The interconnect structure can be formed using any other suitable technique.

[0026] In some other embodiments, the antenna structure can be formed with an element on a carrier, such as a system board (e.g., a printed circuit board (PCB)). The integrated device package can include a redistribution layer (RDL) that is coupled to the element. The element and the RDL can be connected through an interconnect structure (e.g., the BVA).

[0027] Figures 1A to 1F show various steps in a method of manufacturing an integrated device package 1. Figure 1A is a schematic cross sectional side view of an element 10 having an antenna structure 12. The element 10 can comprise a system board

such as a printed circuit board (PCB). In the illustrated embodiment, the laminate system board can serve as a package substrate for the package 1. The PCB can comprise an FR-4 board that includes conductive traces embedded in a reinforced epoxy laminate sheet reinforced, for example, by glass. The PCB can comprise a polytetrafluoroethylene (PTFE) PCB, a prepreg, a ceramic PCB, a polyimide PCB, or any other materials that may be implemented to manufacture a PCB. The antenna structure 12 can comprise one or more radiating elements 12a and an antenna ground 12b. The antenna structure 12 can comprise metallization layers formed in and/or on an insulating material 13. As illustrated in Figure 1A, the radiating element 12a can be disposed on a first side 10a of the element 10, and the antenna ground 12b can be at least partially embedded in the insulating material 13 of the element 10. For example, the antenna ground 12b can be completely embedded in the insulating material 13, and the radiating element 12a can be partially embedded in the insulating material 13 and exposed on the first side 10a. The antenna structure 12 can comprise a patch antenna, a grid antenna, Yagi-Uda, or any other type of antenna structure. The element 10 can include vias 14, 16. The via 14 can be connected to the one or more radiating elements 12a and extend at least partially through a thickness of the element 10 (*e.g.*, completely through the insulating material 13) from the second side 10a. The vias 16 can be connected to the radiating element 12b and extend at least partially through a thickness of the element 10 (*e.g.*, partially through the insulating material 13) from the second side 10a. Although the radiating elements 12a are shown in only one metal layer of the PCB or substrate in Figure 1A, the radiating elements 12a may be formed on two or more metal layers. An air pocket or cavity may be disposed between the radiating element 12a and the antenna ground 12b to help improve bandwidth and radiation efficiency and suppress the surface waves.

[0028] Figure 1B is a schematic cross sectional side view of the element 10 and conductive wires 18, 20. The conductive wires 18, 20 are an example of an interconnect structure. The conductive wires 18, 20 can define a bond via array (BVA). The conductive wire 18 can be connected to the via 14 by way of a wire bonding process, and the conductive wires 20 can be connected to the vias 16 by way of a wire bonding process. The conductive wires 18, 20 can extend generally vertically in a direction generally perpendicular to the second side 10b of the element 10. Although the conductive wires 18, 20 are shown to be

directly connected to the vias 16 and 14 in Figure 1B, in some other instances, the conductive wires 18, 20 may be connected using one or more metal layers or conductive wiring in the PCB. In some other embodiments, the conductive wires 18, 20 can comprise conductive posts or conductive pillar. The conductive wires 18, 20 can be formed by way of via electroplating or any other suitable post or pillar formation techniques.

[0029] One or more passive devices (e.g., capacitors, inductors) may be formed or embedded (e.g. integrated passive devices or IPDs) in other areas of the PCB. In another example, one or more microelectronic devices, e.g., a voltage regulator or any other integrated circuit die, may also be embedded in the PCB.

[0030] Figure 1C is a schematic cross sectional side view of the element 10 and an integrated device die 22 mounted to the second side 10b of the element 10. The integrated device die 22 can be a radio frequency (RF) die that includes RF circuitry. For example, the integrated device die 22 can comprise a radio frequency integrated circuit (RFIC), or a monolithic microwave IC (MMIC). The integrated device die 22 has a first side 22a and a second side 22b opposite the first side, and the first side 22a can be mounted to the element 10 by way of a die attach material 24. Operation frequency of the RF die can be, for example, at least 1 GHz, at least 5 GHz, at least 10 GHz, at least 25 GHz, at least 50 GHz, at least 75 GHz, at least 94 GHz, at least 160 GHz, at least 300 GHz etc. Additional electronic elements (not shown) can be mounted to the second side 10b of the element 10.

[0031] Figure 1D is a schematic cross sectional side view of the element 10 and the integrated device die 22 embedded in a molding material 26. The molding material 26 can be applied about the integrated device die 22 and the conductive wires 18, 20 and onto the element 10. The second side 22b of the integrated device die 22 can be embedded in the molding material 26 as shown in Figure 1D. In other embodiments, however, the second side 22b of the integrated device die 22 can be exposed through the molding compound 26 by polishing or otherwise removing portions of the molding material 26 that overlie the die 22. For example, a surface of the molding material 26 and the second side 22b of the integrated device die 22 can be generally flush with one another. In other embodiments, the second side 22 of the die 22 can be embedded in the molding material 26, and holes can be formed through the overlying portions of molding material 26 to provide electrical communication to bond pads of the die 22. A plate (not shown) can be provided over the second side 22b of the

integrated device die 22, and the molding material 26 can be flowed between the plate and the element 10, such that the molding material 26 underfills spaces or gaps between the plate and the element 10. The molding material 26 can be deposited and a portion of the molding material 26 over the second side 22b of the integrated device die 22 can be removed (e.g., polished).

[0032] In another example, conductive posts or pads (not shown) can be formed on the second side 22b of the integrated device die 22 and ends of conductive posts and conductive wires 18 and 20 can extend above the second side 22b of the integrated device die 22. The molding material 26 can be deposited around and over the conductive posts, the conductive wires 18, 20, and the integrated die 22, and a portion of the molding material 26 can be removed (e.g., polished) to expose the ends of the conductive wires 18, 20 and the conductive posts on the integrated device die 22, while second surface 22b is still under the molding material 26.

[0033] Figure 1E is a schematic cross sectional side view of the integrated device package 1 that includes the element 10, the integrated device die 22, and a redistribution layer (RDL) 30. The RDL 30 can comprise conductive traces 32 that extend laterally and conductive vias 34 that extend vertically within the RDL 30. The RDL 30 can be electrically connected to the conductive wires 18 20, and the integrated device die 22. In another example, conductive posts (not shown) can be formed on the integrated device die 22, and the integrated device die 22 and the RDL 30 can be electrically connected through the conductive posts on the integrated device die 22. The antenna structure 12 of the element 10 can be electrically coupled with the integrated device die 22 through the vias 14, 16, the conductive wires 18, 20, laterally through conductive traces of the RDL 30, and vertically through the conductive posts or pads formed on the integrated device die 22. The orientation of the antenna structure 12, the integrated device die 22, and the RDL 30 can enable relatively short electrical path between the antenna structure 12 and the integrated device die 22. Using the conductive wires 18, 20 for electrically connecting the structure 12 and the RDL 30 can enable a relatively low cost manufacture of the integrated device package 1, especially considering the relatively low number of such conductive wires 18, 20 used to make the electrical connections between the antenna structure 12 and the RDL 30. Forming the antenna structure 12 on a substrate or board such as a PCB, instead of forming the

antenna structure 12 with additional RDL layers, can improve the manufacturability and reduce the manufacturing cost.

[0034] As described above, the BVA can be structured so as to provide a shielding (e.g., electromagnetic shielding) function. For example, the BVA can be formed with a pitch narrower than an operating frequency of the antenna structure to shield the integrated device die from the radio frequency having the operating frequency. For example, the pitch of the BVA can be at least 150-200 microns. In some examples, the antenna ground 12b of the antenna structure 12 may be part of the shield. In some other examples, a separate ground layer may be provided to form a shield. In some examples, the BVA can be formed so as to shield one area within the integrated device package 1 from another area within the integrated device package 1. For example, one area of the integrated device package 1 can have the integrated device die 22 and the other area of the integrated device package 1 can include an electronic component (e.g., an integrated device die).

[0035] At Figure 1F, solder balls 36 can be provided on a surface of the RDL 30 for an input/output (I/O) connection. The integrated device package 1 can be mounted on a larger system or device through the solder balls 36. For example, the integrated device package 1 can be implemented in a motherboard of a device such as a cellular phone device.

[0036] Figures 2A to 2D show various steps in a method of manufacturing an integrated device package 2. Unless otherwise noted, the components of Figures 2A to 2D may be the same as or generally similar to like components of Figures 1A to 1F.

[0037] Figure 2A is a schematic cross sectional side view of an element 10 having an antenna structure 12. The element 10 can comprise a system board such as a printed circuit board (PCB). In the illustrated embodiment, the laminate system board can serve as a package substrate for the package 1. The antenna structure 12 can comprise a radiating element 12a (e.g., a patch antenna) and an antenna ground 12b. As illustrated in Figure 2A, the radiating element 12a can be disposed on a first side 10a of the element 10, and the antenna ground 12b can be at least partially embedded in the element 10. The element 10 can include vias 14, 16. The via 14 can be connected to the radiating element 12a and extend at least partially through a thickness of the element 10 from the second side 10a. The vias 16 can be connected to the antenna ground 12b and extend at least partially through a thickness of the element 10 from the second side 10a.

[0038] Figure 2B is a schematic cross sectional side view of the element 10 and an integrated device die 22 mounted to the second side 10b of the element 10. The integrated device die 22 can be a radio frequency (RF) die that includes RF circuitry. For example, the integrated device die 22 can be a radio frequency integrated circuit (RFIC), or a monolithic microwave IC (MMIC). The integrated device die 22 has a first side 22a and a second side 22b opposite the first side, and the first side 22a can be mounted to the element 10 by way of a die attach material 24.

[0039] Figure 2C is a schematic cross sectional side view of the element 10 and the integrated device die 22 embedded in a molding material 26. The molding material 26 can be applied about the integrated device die 22. The second side 22b of the integrated device die 22 can be embedded in the molding material 26. The second side 22b of the integrated device die 22 can be exposed, for example, by way of a polishing or other material removal process to remove portions of the molding compound 26 that overlies the die 22. For example, a surface of the molding material 26 and the second side 22b of the integrated device die 22 can be generally flush with one another. In other embodiments, the second side 22 of the die 22 can be embedded in the molding material 26, and holes can be formed through the overlying portions of molding material 26 to provide electrical communication to bond pads of the die 22.

[0040] Figure 2D is a schematic cross sectional side view of the integrated device package 2. At Figure 2D, conductive posts 40, 42 are formed. The conductive posts 40, 42 can be formed by drilling through mold vias in the molding material 26 and filling the vias with a conductive material. In some other examples, the conductive posts 40, 42 can be formed before mounting the integrated device die 22 on the second side 10b of the element 10 or providing the molding material 26. Also, at Figure 2D, an RDL 30 can be provided. The conductive posts 40, 42 can be similar to the conductive wires 18, 20 functionally. The RDL 30 can comprise conductive traces 32 that extend laterally and conductive vias 34 that extend vertically within the RDL 30. The RDL 30 can be electrically connected to the conductive wires 28, 20, and the integrated device die 22. The antenna structure 12 of the element 10 can be electrically coupled with the integrated device die 22 through the vias 14, 16, the conductive wires 18, 20, and through the RDL 30. The orientation of the antenna structure 12, the integrated device die 22, and the RDL 30 can enable a relatively short

electrical path between the antenna structure 12 and the integrated device die 22. Using the conductive wires 18, 20 for electrically connecting the structure 12 and the RDL 30 can enable a relatively low cost manufacture of the integrated device package 1. Also, at Figure 2D, solder balls 36 can be provided on a surface of the RDL 30 for an input/output (I/O) connection. The integrated device package 1 can be mounted on a larger system or device through the solder balls 36. For example, the integrated device package 1 can be implemented in a motherboard of a device such as cellular phone device.

[0041] Figures 2E to 2H show various steps in another method of manufacturing the integrated device package 2. Unless otherwise noted, the components of Figures 2E to 2H may be the same as or generally similar to like components of Figures 1A to 2D. The manufacturing process shown in Figures 2E to 2H are generally similar to the manufacturing process shown in Figures 2A to 2D, except that the conductive posts 40, 42 in the manufacturing process of Figures 2E to 2H are formed prior to providing the molding material 26.

[0042] Figures 3A to 3F show various steps in another method of manufacturing an integrated device package 9. Unless otherwise noted, the components of Figures 3A to 3F may be the same as or generally similar to like components of Figures 1A to 2H. In Figure 3A, conductive posts 40, 42 can be formed on a carrier 43. The conductive posts 40, 42 can comprise plated posts, and/or BVA. In some embodiments, a resist layer can be patterned and pillars can be electroplated to form the conductive posts 40, 42. In Figure 3B, an integrated device die 22 can be mounted on the carrier 43. The integrated device die 22 can be attached to the carrier 43 by way of a die attach material 24. The integrated device die 22 can comprise posts 45. In some embodiments, the integrated device die 22 can omit the posts 45 and terminals (not shown) can be exposed for electrical connection. In Figure 3C, a molding material 26 can be provided. In Figure 3D, at least a portion of the molding material 26 can be removed to reveal the conductive posts 40, 42 and the posts 45. In Figure 3E, an RDL 30 can be provided and electrically connected with the conductive posts 40, 42 and the posts 45. In Figure 3F, the carrier 43 can be removed and an element 10 can be provided and electrically connected with the conductive posts 40, 42. In some embodiments, the element 10 can be electrically connected to the conductive posts 40, 42 by way of, for example, a ball grid array (BGA) 47.

[0043] Figures 4A to 4E show various steps in a method of manufacturing an integrated device package 3. Unless otherwise noted, the components of Figures 4A to 4E may be the same as or generally similar to like components of Figures 1A to 3F. The integrated device package 3 is generally similar to the integrated device package 1 illustrated in Figure 1E and 1F, except that the antenna ground 12b of the integrated device package 3 is formed at (*e.g.*, exposed at) the second side 10b of the element 10. The integrated device package can omit the via 16 that is shown in some other embodiments disclosed herein. In Figures 4A-4E, the antenna ground 12b can also serve as an electrical ground connection for the die 22 in some embodiments.

[0044] Figures 5A to 5E show various steps in a method of manufacturing an integrated device package 4. Unless otherwise noted, the components of Figures 5A to 5E may be the same as or generally similar to like components of Figures 1A to 4E. The integrated device package 4 is generally similar to the integrated device package 3 illustrated in Figure 4E, except that the integrated device die 22 of the integrated device package 4 is electrically connected to the RDL 30 by way of conductive wires 44 that extend at least partially through a thickness of the molding material 26 between pads on the upper surface of the die 22 and the RDL 30. In some embodiments, the conductive wires 44 can be formed at the same time or after conductive wires 20 and 18 are formed. In some other embodiments, the conductive wires 44 can be replaced with conductive posts or conductive bumps.

[0045] Figures 6A to 6E show various steps in a method of manufacturing an integrated device package 5. Unless otherwise noted, the components of Figures 6A to 6E may be the same as or generally similar to like components of Figures 1A to 5E. The integrated device package 5 is generally similar to the integrated device package 1 illustrated in Figure 1E and 1F, except that the vias 14, 16 are omitted from the integrated device package 3 and the conductive wires 18, 20 are directly in contact with the antenna structure 12. As shown in Figures 6B-6E, for example, end portions of the wires 18, 20 can be embedded in the insulating material 13. Conductive wires 18, 20 can be formed on pads that are exposed for the conductive wires to enable wire bond. In some embodiments, portions of the conductive wires 18, 20 can be covered by the insulating material 13. In some other embodiments, for example, openings can be formed in the insulating material 13, and the wires 18, 20 can be connected within the openings to the antenna structure 12.

[0046] Figures 7A to 7E show various steps in a method of manufacturing an integrated device package 6. Unless otherwise noted, the components of Figures 7A to 7E may be the same as or generally similar to like components of Figures 1A to 6E. The integrated device package 6 is generally similar to the integrated device package 3 illustrated in Figure 4E. Unlike the integrated device package 3, the integrated device package 6 of Figures 7A-7E does not include the RDL 30. The integrated device package 6 can include solder balls 50 for an input/output (I/O) connection to an external device or external motherboard. The integrated device package 6 can include a horizontal interconnect 52. The horizontal interconnect 52 can connect the conductive wires 20 to the integrated device die 22. The horizontal interconnect 52 can function as a radiation shield in various embodiments.

[0047] Figure 8 is a schematic cross sectional side view of an integrated device package 7 according to an embodiment. Unless otherwise noted, the components of Figure 8 may be the same as or generally similar to like components of Figures 1A to 7E. The integrated device package 7 can include an element 10 that includes an antenna structure 12, a redistribution layer (RDL) 30, and an integrated device die 22. The integrated device die 22 can be embedded in a molding material 26. In the illustrated embodiment shown in Figure 8, the antenna structure 12 of the element 10 and the RDL 30 are on the same side of the integrated device die 22.

[0048] Figures 9A-9G show integrated device packages 7, 7', 8, 8', 8'' according to various embodiments. Any suitable principles and advantages discussed herein can be implemented and/or applied to the integrated device packages 7, 7', 8, 8', 8''. For example, any processes and/or combinations of processes disclosed herein can be applied to forming at least a portion of the integrated device packages 7, 7', 8, 8', 8''.

[0049] Figure 9A is a cross sectional side view of the integrated device package 7 according to an embodiment. Figure 9B is a top plan view of the integrated device package 7. The integrated device package 7 can include a carrier 100, an integrated device die 102 mounted on the carrier 100, an antenna structure 104 that includes a radiating element 106 and an antenna ground 108, an electromagnetic compatible (EMC) layer 110, and a molding material 112 disposed between the carrier 100 and the EMC layer 110. The EMC layer 110 can comprise an RDL material. In some embodiments, two or more antenna structures (not

shown) can be included in the integrated device package 7. For example, the two or more antenna structures can be formed on, in, or with the EMC layer 110. The RDL material can comprise a material such as, for example, polyimide (PI), polybenzoxazoles (PBO), etc., and be spin coated, laminated, or printed on the molding material 112. The antenna structure 104 can be electrically connected to the carrier 100 through an interconnect structure 114. The interconnect structure 114 can include conductive wires 116, 118. The conductive wires 116, 118 can define a bond via array (BVA), and can extend upwardly through the molding material from the carrier 100. For example, the carrier 100 and the radiating element 106 can be electrically connected through the conductive wire 116, and the carrier 100 and the antenna ground 108 can be electrically connected through the conductive wire 118. The conductive wire 118 can comprise a ground wire and provide ground connection to the antenna ground 108. In some embodiments, the conductive wire 116 that connects the radiating element 106 and the carrier 100 can be positioned laterally between the conductive wires 118 that connects the antenna ground 108 and the carrier 100, as shown in Figure 9A. In such embodiments, the conductive wire 116 can be positioned in a shielded region 119. As shown, the die 102 can also be positioned within the shielded region 119, which can be at least partially defined by the ground wires 118 that are disposed about a periphery of the die 102. In some other embodiments, the conductive wire 116 can be positioned laterally outside of the conductive wires 118, as shown in Figure 9B. In such embodiments, the conductive wire 116 can be positioned outside the shielded region 119.

[0050] The carrier 100 can comprise any suitable type of carrier or substrate in various embodiments. In some embodiments, the carrier 100 can comprise a system board such as a printed circuit board (PCB), which can serve as a package substrate for the package 7. The PCB can comprise an FR-4 board that includes conductive traces embedded in a reinforced epoxy laminate sheet reinforced, for example, by glass. The PCB can comprise a polytetrafluoroethylene (PTFE) PCB, a prepreg, a ceramic PCB, a polyimide PCB, or any other materials traditionally implemented to manufacture a PCB. In other embodiments, the carrier 100 can comprise a ceramic substrate, an interposer, or any suitable substrate or support. In some embodiments, the carrier can include conductive traces that extend laterally to provide electrical communication between the die 102 and the wires 116, 118.

[0051] The integrated device die 102 can be a radio frequency (RF) die that includes RF circuitry. For example, the integrated device die 102 can comprise a radio frequency integrated circuit (RFIC), or a monolithic microwave IC (MMIC). In some embodiments, the integrated device die 102 can be flip-chip mounted on the carrier 100. For example, the integrated device die 102 can be mounted on the carrier 100 by way of solder balls. In other embodiments, the integrated device die 102 can be wire bonded to the carrier 100. In such embodiments, a die attach material may be disposed between the carrier 100 and the integrated device die 102.

[0052] The antenna structure 104 can comprise one or more radiating elements 106 and an antenna ground 108. The antenna structure 104 can comprise a patch antenna, a grid antenna, Yagi-Uda, or any other type of antenna structure. In some embodiments, the antenna structure 104 can be formed with the EMC layer 110. For example, the radiating element 106 can be formed on a portion of an upper side 110a (e.g., an upper surface) of the EMC layer 110, and the antenna ground 108 can be formed on a portion of a lower side 110b (e.g., a lower surface) of the EMC layer 110.

[0053] In some embodiments, the EMC layer 110 can comprise a redistribution layer (RDL). The EMC layer 110 can comprise a via 120 that can extend at least partially through a thickness of the EMC layer 110. The via 120 can be provided in an opening formed in the EMC layer 110. The via 120 can comprise a filled via as shown in Figure 9A, or a conformal via as shown in Figure 9B. The via 120 can provide an electrical connection between the conductive wire 116 and the radiating element 106.

[0054] In some embodiments, the molding material 112 can comprise an electromagnetic compatible material. In some embodiments, the molding material 112 and the EMC layer 110 can comprise the same material. The integrated device die 102 and the conductive wires 116, 118 can be embedded in the molding material 112.

[0055] In some embodiments, the conductive wire 116, 118 can comprise a first portion 116a, 118a in contact with the carrier 100 and a second portion 116b, 118b extending non-parallel to (e.g., generally perpendicular to) a surface of the carrier 100 to which the integrated device die 102 is mounted. In some embodiments, the interconnect structure 114 can comprise a bond via array (BVA). In such embodiments, the first portion 116a, 118a can include a width wider than a width of the second portion 116b, 118b indicative of a wire

bond via formation process. For example, the first portion 116a, 118a and the second portion 116b, 118b can form a continuous, seamless, or uniform structure. In some embodiments, the BVA can be arranged to shield the integrated device die 102 from electromagnetic radiation. For example, the BVA can be formed around a periphery of the die 102 with a pitch between adjacent wires narrower than an operating frequency of the antenna structure 104 so as to shield the integrated device die 102 from the radio frequency having the operating frequency. In some embodiments, the BVA is not deposited (e.g., electroplated) as conformal layers over a portion of the package 7 such as the carrier 100 or the molding material 112. Rather, the BVA is formed by a wire bonding process.

[0056] Figure 9C is a cross sectional side view of the integrated device package 7' according to an embodiment. Figure 9D is a top plan view of the integrated device package 7'. Unless otherwise noted, the components of Figures 9C and 9D may be the same as or generally similar to like components of Figures 9A and 9B. Unlike the integrated device package 7 of Figures 9A and 9B, the via 120 in the integrated device package 7' of Figures 9C and 9D comprises a conformal via. Also, in the integrated device package 7' of Figure 9C, locations of the conductive wires 116, 118 of the interconnect structure 114, as well as locations of the corresponding conductive wires 116, 118, are different from those shown in Figure 9A. In some embodiments, the locations of the conductive wires 116, 118 in Figure 9C provide different shielding properties for the integrated device die 102 than the conductive wires 116, 118 in Figure 9A. The wire 116 can feed signals to the radiating element 106 from the integrated device die 102. The wires 118 can provide ground connection to the antenna ground 108.

[0057] Figure 9E is a cross sectional side view of the integrated device package 8 according to an embodiment. Unless otherwise noted, the components of Figure 9C may be the same as or generally similar to like components of Figures 9A to 9D. In the integrated device package 8 of Figure 9E, the antenna structure 104 can be formed on the molding material. In some embodiments, the EMC layer 110 is omitted. The radiating element 106 and the antenna ground 108 of the antenna structure 104 in the integrated device package 8 can be disposed on the molding material 112. The radiating element 106 can be laterally offset from the integrated device die 102, and can be disposed outside the electromagnetic shield (e.g., the shielded region 119). In some embodiments, the antenna ground 108 and the

conductive wires 118 can provide shielding for the integrated device die 102. The antenna ground 108 can comprise a continuous layer as shown in Figure 9E.

[0058] Figure 9F is a cross sectional side view of the integrated device package 8' according to an embodiment. Unless otherwise noted, the components of Figure 9F may be the same as or generally similar to like components of Figures 9A to 9E. The antenna ground 108 can comprise one or more openings through a sheet of conductive material, or a plurality of portions that are spaced apart by a gap. In Figure 9F, for example, the radiating element 106 and the ground element(s) (e.g., antenna ground 108) are disposed atop the molding material 112. The radiating element 106 can be positioned within the opening or gap between portions of the antenna ground 108. In Figure 9F, therefore, the wires 116 connected to the radiating element 106 can be disposed within the shielded region 119.

[0059] Figure 9G is a cross sectional side view of the integrated device package 8'' according to an embodiment. Unless otherwise noted, the components of Figure 9G may be the same as or generally similar to like components of Figures 9A to 9F. Unlike the radiating element 106 of the integrated device packages 8, 8' that is disposed on the molding material 112, the radiating element 106 of the integrated device package 8'' is disposed on a portion of the carrier 100. In various embodiments, the radiating element 106 can be deposited or patterned in the carrier 100, adhered to the carrier 100, or otherwise provided on the carrier 100. The conductive wire 116 can be omitted from the integrated device package 8''. In some embodiments, the radiating element 106 can be at least partially embedded in the molding material 112. For example, the radiating element 106 can be fully embedded in the molding material 112. In some embodiments, the carrier 100 can include conductive traces that extend laterally to provide electrical communication between the die 102 and the wires 118 or the radiating element 106.

[0060] Although Figures 9A-9G, depict integrated device packages 7, 7', 8, 8', 8'' that includes one ground layer (e.g., the antenna ground 108) and one antenna layer (e.g., the radiating element 106), two or more layers ground layers and/or two or more antenna layers may be formed. Although a separate RDL layer is not shown, it is assumed that metallization is achieved by redistribution layer formation or any suitable technique may be used to form those metal layers for antenna and ground.

[0061] The integrated device die disclosed herein (e.g., the integrated device die 22, 102) can be bonded to a carrier (e.g., the redistribution layer 30 or carrier 100) in any suitable manner. In some embodiments, the integrated device die disclosed herein (e.g., the integrated device die 22) can be directly bonded to a carrier (e.g., the redistribution layer 30) without an intervening adhesive. Bonding surfaces of the integrated device die and the redistribution layer 30 can be prepared for direct bonding prior to contacting the surfaces. In some embodiments, a nonconductive region (e.g., a semiconductor or an inorganic dielectric) of the integrated device die can be directly bonded to a nonconductive region (e.g., a semiconductor or an inorganic dielectric) of the redistribution layer 30, and a conductive feature of the integrated device die can be directly bonded to a conductive feature of the carrier.

[0062] In one aspect, an integrated device package is disclosed. The integrated device package can include a system board that has an antenna structure, a redistribution layer that has conductive routing traces, and an integrated device die that is disposed between the system board and the redistribution layer. The integrated device die is electrically coupled to the antenna structure at least partially through one or more of the conductive routing traces of the redistribution layer.

[0063] In one embodiment, the system board includes a printed circuit board (PCB).

[0064] In one embodiment, the antenna structure includes a patch antenna and an antenna ground between the patch antenna and the integrated device die. The patch antenna can be exposed on a surface of the system board and the antenna ground is embedded in the system board.

[0065] In one embodiment, the system board is electrically coupled by the redistribution layer through an interconnect structure. The interconnect structure can include a conductive wire. The interconnect structure can include a bond via array (BVA). At least a portion of the BVA can define a radiation shield. The interconnect structure can include a conductive post. The integrated device package can further include a molding material that is disposed between the system board and the redistribution layer. The integrated device die can be at least partially embedded in the molding material. The interconnect structure can be at least partially embedded in the molding material.

[0066] In one embodiment, the integrated device die is attached to the system board by way of a die attach material.

[0067] In one embodiment, the integrated device die includes radio-frequency (RF) circuitry.

[0068] In one embodiment, the integrated device die is electrically connected to the redistribution layer through a conductive wire.

[0069] In one embodiment, the integrated device die is directly bonded to the redistribution layer without an intervening adhesive. A nonconductive region of the integrated device die can be directly bonded to a nonconductive region of the redistribution layer, and a conductive feature of the integrated device die can be directly bonded to a conductive feature of the redistribution layer.

[0070] In one aspect, an integrated device package is disclosed. The integrated device package can include an element that has an antenna structure, a redistribution layer that has conductive routing traces, and an integrated device die that is at least partially embedded in a molding material and disposed between the element and the redistribution layer. The integrated device die is electrically coupled to the antenna structure at least partially through one or more of the conductive routing traces of the redistribution layer. The redistribution layer is electrically coupled to the element through an interconnect structure comprising one or more conductive wires or posts formed through the molding material.

[0071] In one embodiment, the element includes a printed circuit board (PCB).

[0072] In one embodiment, the antenna structure includes an antenna and an antenna ground between the antenna and the integrated device die. The antenna can be exposed on a surface of the element and the antenna ground is embedded in the element.

[0073] In one embodiment, the interconnect structure includes the one or more of conductive wires of a bond via array (BVA).

[0074] In one embodiment, the integrated device die includes radio-frequency (RF) circuitry.

[0075] In one embodiment, solder balls are disposed on a surface of the integrated device die that faces away the element.

[0076] In one aspect, a method of manufacturing an integrated device package is disclosed. The method includes providing an element having an antenna structure. The

element has a first side and a second side opposite the first side. The method can include mounting an integrated device die to the second side of the element, forming an interconnect structure extending from the second side, and providing a molding material around the integrated device die. The interconnect structure is at least partially embedded in the molding material. The method can include electrically coupling the antenna structure and a redistribution layer through the interconnect structure.

[0077] In one embodiment, the element includes a printed circuit board (PCB).

[0078] In one embodiment, the interconnect structure includes a bond via array or a conductive post.

[0079] In one embodiment, the integrated device die is disposed between the element and the redistribution layer.

[0080] In one embodiment, the antenna structure is formed on the first side of the element.

[0081] In one embodiment, the antenna structure is at least partially embedded in the element.

[0082] In one aspect, an integrated device package is disclosed. The integrated device package can include a system board that has an antenna structure, a redistribution layer that has conductive routing traces, and an integrated device die that is disposed between the system board and the redistribution layer. The integrated device die is electrically coupled to the redistribution layer .

[0083] In one embodiment, the integrated device die is at least partially embedded in a molding material.

[0084] In one embodiment, the system board and the redistribution are electrically connected through a bond via array (BVA).

[0085] In one embodiment, the integrated device die is a radio frequency (RF) die.

[0086] In one aspect, an integrated device package is disclosed. The integrated device package can include a system board, an antenna structure, a redistribution layer that has conductive routing traces, and an integrated device die that is disposed between the system board and the redistribution layer. The integrated device die is electrically coupled to

the antenna structure at least partially through one or more of the conductive routing traces of the redistribution layer.

[0087] In one embodiment, the system board includes a printed circuit board (PCB).

[0088] In one embodiment, the antenna structure is formed with the system board.

[0089] In one embodiment, the system board and the redistribution are electrically connected through a bond via array (BVA).

[0090] In one embodiment, the integrated device die is a radio frequency (RF) die.

[0091] In one aspect, an integrated device package is disclosed. The integrated device package can include an antenna structure, a carrier that includes one or more routing traces and electrically coupled to the antenna structure through a conductive wire of an interconnect structure, and an integrated device die that is attached to the carrier and disposed between the carrier and at least a portion of the antenna structure. The integrated device die is electrically coupled to the antenna structure at least partially through the one or more of conductive routing traces of the carrier and the conductive wire.

[0092] In one embodiment, the integrated device die is attached to the carrier with an adhesive.

[0093] In one embodiment, the conductive wire includes a first portion in contact with the carrier and a second portion extending non-parallel to a surface of the carrier to which the integrated device die is mounted. The first portion can have a width wider than a width of the second portion indicative of a bond wire formation. The first portion and the second portion of the conductive wire can include a seamless uniform structure.

[0094] In one embodiment, the interconnect structure includes an array of standing bond wires. The array of standing bond wires can be arranged to at least partially form an electromagnetic shield region configured to shield the integrated device die. The array of standing bond wires can include a plurality of ground wires that are arranged with a pitch narrower than an operating frequency of the antenna structure.

[0095] In one embodiment, the integrated device package further includes an electromagnetic compatible layer comprising the antenna structure. The electromagnetic compatible layer can include a redistribution layer that includes one or more of traces that

extend laterally. The electromagnetic compatible layer can further include a second antenna structure that is electrically connected to the one or more of traces. The electromagnetic compatible layer can include polyimide or polybenzoxazoles.

[0096] In one embodiment, the carrier includes a printed circuit board (PCB).

[0097] In one embodiment, the antenna structure includes a radiating element and an antenna ground. The antenna ground can be disposed between the radiating element and the integrated device die. The antenna ground can be formed on a first side of an electromagnetic compatible layer and the radiating element can be formed on a second side of the electromagnetic compatible layer opposite the first side. The electromagnetic compatible layer can include a via at least partially through a thickness of the electromagnetic compatible layer that electrically couples the conductive wire and the electromagnetic compatible layer. The via can include a filled via or a conformal via. The antenna ground can include a shielding layer that is configured to shield the integrated device die from a radio frequency. The radiating element can be exposed on a surface of the integrated device package. The antenna ground can be exposed on a surface of the integrated device package. The antenna ground can be formed on the carrier.

[0098] In one embodiment, the integrated device package further includes a molding material that is disposed between the carrier and the portion of the antenna structure. The integrated device die can be at least partially embedded in the molding material. The interconnect structure can be at least partially embedded in the molding material. The antenna structure can be formed on a surface of the molding material.

[0099] In one embodiment, the integrated device die is flip-chip mounted to the carrier.

[0100] In one embodiment, the integrated device die includes radio-frequency (RF) circuitry.

[0101] In one aspect, an integrated device package is disclosed. The integrated device package can include an electromagnetic compatible layer that has an antenna structure, a carrier that has one or more routing traces that are electrically coupled to the antenna structure through a conductive wire of an interconnect structure, and an integrated device die that is mounted on the carrier and disposed between the carrier and the

electromagnetic compatible layer. The integrated device die is electrically coupled to the antenna structure at least partially through the conductive wire.

[0102] In one embodiment, the interconnect structure can include an array of standing bond wires. The array of standing bond wires can be arranged to shield the integrated device die from a radio frequency. The array of standing bond wires can be formed with a pitch narrower than an operating frequency of the antenna structure.

[0103] In one embodiment, the antenna structure includes a radiating element and an antenna ground. The antenna ground can be formed on a first side of the electromagnetic compatible layer and the radiating element can be formed on a second side of the electromagnetic compatible layer opposite the first side. The electromagnetic compatible layer can include a via at least partially through a thickness of the electromagnetic compatible layer that electrically couples the conductive wire and the radiating element. The via can include a filled via or a conformal via.

[0104] In one aspect, an integrated device package is disclosed. The integrated device package can include an antenna structure. The integrated device package can include a carrier that includes one or more of routing traces and is electrically coupled to the antenna structure through a conductive wire of an interconnect structure. The integrated device package can include an integrated device die that is mounted on the carrier and disposed between the carrier and at least a portion of the antenna structure. The integrated device die is electrically coupled to the antenna structure at least partially through the conductive wire. The integrated device package includes a molding material that is disposed between the carrier and the portion of the antenna structure. The integrated device die is at least partially embedded in the molding material. The interconnect structure is at least partially embedded in the molding material. The portion of the antenna structure is formed on a surface of the molding material.

[0105] In one embodiment, the interconnect structure includes an array of standing bond wires. The array of standing bond wires can be arranged to shield the integrated device die from a radio frequency. The array of standing bond wires can be formed with a pitch narrower than an operating frequency of the antenna structure so as to shield the integrated device die from the radio frequency having the operating frequency.

[0106] In one embodiment, the antenna structure comprises a radiating element and an antenna ground, the radiating element is formed on a portion of a surface of the molding material. The antenna ground can be formed on a second portion of the surface of the molding material. The antenna ground can be formed on a surface of the carrier.

[0107] Unless the context clearly requires otherwise, throughout the description and the claims, the words “comprise,” “comprising,” “include,” “including” and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of “including, but not limited to.” The word “coupled”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Likewise, the word “connected”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words “herein,” “above,” “below,” and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word “or” in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0108] Moreover, conditional language used herein, such as, among others, “can,” “could,” “might,” “may,” “e.g.,” “for example,” “such as” and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments.

[0109] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel apparatus, methods, and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without

departing from the spirit of the disclosure. For example, while blocks are presented in a given arrangement, alternative embodiments may perform similar functionalities with different components and/or circuit topologies, and some blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these blocks may be implemented in a variety of different ways. Any suitable combination of the elements and acts of the various embodiments described above can be combined to provide further embodiments. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

WHAT IS CLAIMED IS:

1. An integrated device package comprising:
a system board comprising an antenna structure;
a redistribution layer having conductive routing traces; and
an integrated device die disposed between the system board and the redistribution layer, the integrated device die electrically coupled to the antenna structure at least partially through one or more of the conductive routing traces of the redistribution layer.
2. The integrated device package of Claim 1, wherein the system board comprises a printed circuit board (PCB).
3. The integrated device package of Claim 1, wherein the antenna structure comprises a patch antenna and an antenna ground between the patch antenna and the integrated device die.
4. The integrated device package of Claim 3, wherein the patch antenna is exposed on a surface of the system board and the antenna ground is embedded in the system board.
5. The integrated device package of Claim 1, wherein the system board is electrically coupled by the redistribution layer through an interconnect structure.
6. The integrated device package of Claim 5, wherein the interconnect structure comprises a conductive wire.
7. The integrated device package of Claim 6, wherein the interconnect structure comprises a bond via array (BVA).
8. The integrated device package of Claim 7, wherein at least a portion of the BVA defines a radiation shield.

9. The integrated device package of Claim 5, wherein the interconnect structure comprises a conductive post.

10. The integrated device package of Claim 5, further comprising a molding material disposed between the system board and the redistribution layer, the integrated device die is at least partially embedded in the molding material, the interconnect structure is at least partially embedded in the molding material.

11. The integrated device package of Claim 1, wherein the integrated device die is attached to the system board by way of a die attach material.

12. The integrated device package of Claim 1, wherein the integrated device die comprises radio-frequency (RF) circuitry.

13. The integrated device package of Claim 1, wherein the integrated device die is electrically connected to the redistribution layer through a conductive wire.

14. The integrated device package of Claim 1, wherein the integrated device die is directly bonded to the redistribution layer without an intervening adhesive.

15. The integrated device package of Claim 14, wherein a nonconductive region of the integrated device die is directly bonded to a nonconductive region of the redistribution layer, and a conductive feature of the integrated device die is directly bonded to a conductive feature of the redistribution layer.

16. An integrated device package comprising:
an element comprising an antenna structure;
a redistribution layer having conductive routing traces; and
an integrated device die at least partially embedded in a molding material and disposed between the element and the redistribution layer, the integrated device die electrically coupled to the antenna structure at least partially through one or more of the conductive routing traces of the redistribution layer,

wherein the redistribution layer is electrically coupled to the element through an interconnect structure comprising one or more conductive wires or posts formed through the molding material.

17. The integrated device package of Claim 16, wherein the element comprises a printed circuit board (PCB).

18. The integrated device package of Claim 16, wherein the antenna structure comprises an antenna and an antenna ground between the antenna and the integrated device die.

19. The integrated device package of Claim 18, wherein the antenna is exposed on a surface of the element and the antenna ground is embedded in the element.

20. The integrated device package of Claim 16, wherein the interconnect structure comprises the one or more of conductive wires of a bond via array (BVA).

21. The integrated device package of Claim 16, wherein the integrated device die comprises radio-frequency (RF) circuitry.

22. The integrated device package of Claim 16, wherein solder balls are disposed on a surface of the integrated device die that faces away the element.

23. A method of manufacturing an integrated device package, the method comprising:

providing an element having an antenna structure, the element having a first side and a second side opposite the first side;

mounting an integrated device die to the second side of the element;

forming an interconnect structure extending from the second side;

providing a molding material around the integrated device die, the interconnect structure at least partially embedded in the molding material; and

electrically coupling the antenna structure and a redistribution layer through the interconnect structure.

24. The method of Claim 23, wherein the element comprises a printed circuit board (PCB).

25. The method of Claim 23, wherein the interconnect structure comprises a bond via array or a conductive post.

26. The method of Claim 23, wherein the integrated device die is disposed between the element and the redistribution layer.

27. The method of Claim 23, wherein the antenna structure is formed on the first side of the element.

28. The method of Claim 23, wherein the antenna structure is at least partially embedded in the element.

29. An integrated device package comprising:
a system board having an antenna structure;
a redistribution layer having conductive routing traces; and
an integrated device die disposed between the system board and the redistribution layer, the integrated device die electrically coupled to the redistribution layer .

30. The integrated device package of Claim 29, wherein the integrated device die is at least partially embedded in a molding material.

31. The integrated device package of Claim 29, wherein the system board and the redistribution are electrically connected through a bond via array (BVA).

32. The integrated device package of Claim 29, wherein the integrated device die is a radio frequency (RF) die.

33. An integrated device package comprising:
a system board;

an antenna structure;
a redistribution layer having conductive routing traces; and
an integrated device die disposed between the system board and the redistribution layer, the integrated device die electrically coupled to the antenna structure at least partially through one or more of the conductive routing traces of the redistribution layer.

34. The integrated device package of Claim 33, wherein the system board comprises a printed circuit board (PCB).

35. The integrated device package of Claim 33, wherein the antenna structure is formed with the system board.

36. The integrated device package of Claim 33, wherein the system board and the redistribution are electrically connected through a bond via array (BVA).

37. The integrated device package of Claim 33, wherein the integrated device die is a radio frequency (RF) die.

38. An integrated device package comprising:
an antenna structure;
a carrier comprising one or more routing traces and electrically coupled to the antenna structure through a conductive wire of an interconnect structure; and
an integrated device die attached to the carrier and disposed between the carrier and at least a portion of the antenna structure, the integrated device die electrically coupled to the antenna structure at least partially through the one or more of conductive routing traces of the carrier and the conductive wire.

39. The integrated device package of Claim 38, wherein the integrated device die is attached to the carrier with an adhesive.

40. The integrated device package of Claim 38, wherein the conductive wire comprises a first portion in contact with the carrier and a second portion extending non-parallel to a surface of the carrier to which the integrated device die is mounted, the first portion has a width wider than a width of the second portion indicative of a bond wire formation.

41. The integrated device package of Claim 40, wherein the first portion and the second portion of the conductive wire comprises a seamless uniform structure.

42. The integrated device package of Claim 38, wherein the interconnect structure comprises an array of standing bond wires.

43. The integrated device package of Claim 42, wherein the array of standing bond wires is arranged to at least partially form an electromagnetic shield region configured to shield the integrated device die.

44. The integrated device package of Claim 43, wherein the array of standing bond wires comprises a plurality of ground wires that are arranged with a pitch narrower than an operating frequency of the antenna structure.

45. The integrated device package of Claim 38, further comprising an electromagnetic compatible layer comprising the antenna structure.

46. The integrated device package of Claim 45, wherein the electromagnetic compatible layer comprises a redistribution layer that includes one or more of traces that extend laterally.

47. The integrated device package of Claim 46, wherein the electromagnetic compatible layer further comprises a second antenna structure that is electrically connected to the one or more of traces.

48. The integrated device package of Claim 45, wherein the electromagnetic compatible layer comprises polyimide or polybenzoxazoles.

49. The integrated device package of Claim 38, wherein the carrier comprises a printed circuit board (PCB).

50. The integrated device package of Claim 38, wherein the antenna structure comprises a radiating element and an antenna ground.

51. The integrated device package of Claim 50, wherein the antenna ground is disposed between the radiating element and the integrated device die.

52. The integrated device package of Claim 51, wherein the antenna ground is formed on a first side of an electromagnetic compatible layer and the radiating element is formed on a second side of the electromagnetic compatible layer opposite the first side.

53. The integrated device package of Claim 52, wherein the electromagnetic compatible layer comprises a via at least partially through a thickness of the electromagnetic compatible layer that electrically couples the conductive wire and the electromagnetic compatible layer.

54. The integrated device package of Claim 53, wherein the via comprises a filled via or a conformal via.

55. The integrated device package of Claim 50, wherein the antenna ground comprises a shielding layer configured to shield the integrated device die from a radio frequency.

56. The integrated device package of Claim 50, wherein the radiating element is exposed on a surface of the integrated device package.

57. The integrated device package of Claim 56, wherein the antenna ground is exposed on a surface of the integrated device package.

58. The integrated device package of Claim 50, wherein the antenna ground is formed on the carrier.

59. The integrated device package of Claim 38, further comprising a molding material disposed between the carrier and the portion of the antenna structure, the integrated device die is at least partially embedded in the molding material, the interconnect structure is at least partially embedded in the molding material.

60. The integrated device package of Claim 59, wherein the antenna structure is formed on a surface of the molding material.

61. The integrated device package of Claim 38, wherein the integrated device die is flip-chip mounted to the carrier.

62. The integrated device package of Claim 38, wherein the integrated device die comprises radio-frequency (RF) circuitry.

63. An integrated device package comprising:
an electromagnetic compatible layer including an antenna structure;
a carrier comprising one or more routing traces electrically coupled to the antenna structure through a conductive wire of an interconnect structure; and
an integrated device die mounted on the carrier and disposed between the carrier and the electromagnetic compatible layer, the integrated device die electrically coupled to the antenna structure at least partially through the conductive wire.

64. The integrated device package of Claim 63, wherein the interconnect structure comprises an array of standing bond wires.

65. The integrated device package of Claim 64, wherein the array of standing bond wires is arranged to shield the integrated device die from a radio frequency.

66. The integrated device package of Claim 65, wherein the array of standing bond wires is formed with a pitch narrower than an operating frequency of the antenna structure.

67. The integrated device package of Claim 63, wherein the antenna structure comprises a radiating element and an antenna ground, the antenna ground is formed on a first side of the electromagnetic compatible layer and the radiating element is formed on a second side of the electromagnetic compatible layer opposite the first side.

68. The integrated device package of Claim 67, wherein the electromagnetic compatible layer comprises a via at least partially through a thickness of the electromagnetic compatible layer that electrically couples the conductive wire and the radiating element.

69. The integrated device package of Claim 68, wherein the via comprises a filled via or a conformal via.

70. An integrated device package comprising:
an antenna structure;
a carrier comprising one or more of routing traces and electrically coupled to the antenna structure through a conductive wire of an interconnect structure;
an integrated device die mounted on the carrier and disposed between the carrier and at least a portion of the antenna structure, the integrated device die electrically coupled to the antenna structure at least partially through the conductive wire; and
a molding material disposed between the carrier and the portion of the antenna structure, the integrated device die is at least partially embedded in the molding material, the interconnect structure is at least partially embedded in the molding material,
wherein the portion of the antenna structure is formed on a surface of the molding material.

71. The integrated device package of Claim 70, wherein the interconnect structure comprises an array of standing bond wires.

72. The integrated device package of Claim 71, wherein the array of standing bond wires is arranged to shield the integrated device die from a radio frequency.

73. The integrated device package of Claim 72, wherein the array of standing bond wires is formed with a pitch narrower than an operating frequency of the antenna structure so as to shield the integrated device die from the radio frequency having the operating frequency.

74. The integrated device package of Claim 70, wherein the antenna structure comprises a radiating element and an antenna ground, the radiating element is formed on a portion of a surface of the molding material.

75. The integrated device package of Claim 74, wherein the antenna ground is formed on a second portion of the surface of the molding material.

76. The integrated device package of Claim 74, wherein the antenna ground is formed on a surface of the carrier.

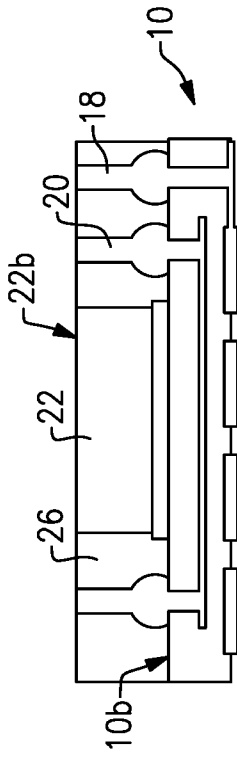


FIG. 1D

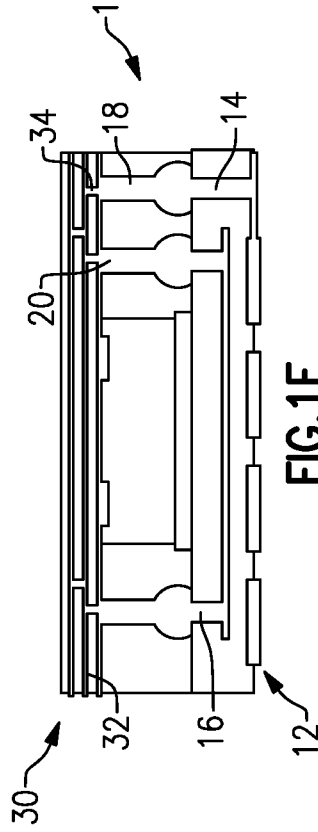


FIG. 1E

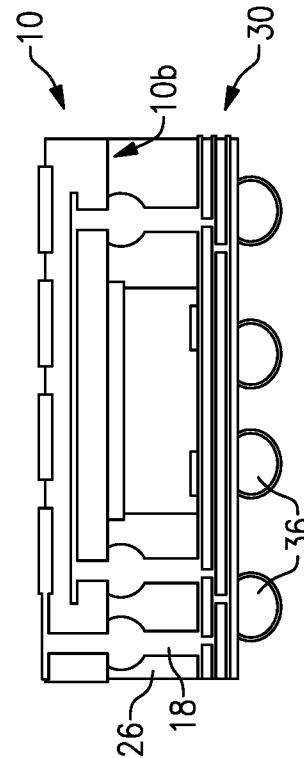


FIG. 1F

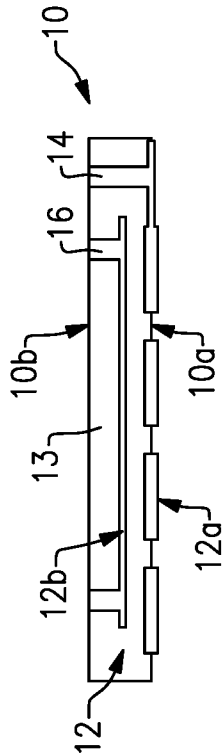


FIG. 1A

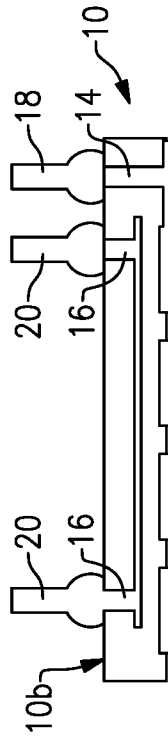


FIG. 1B

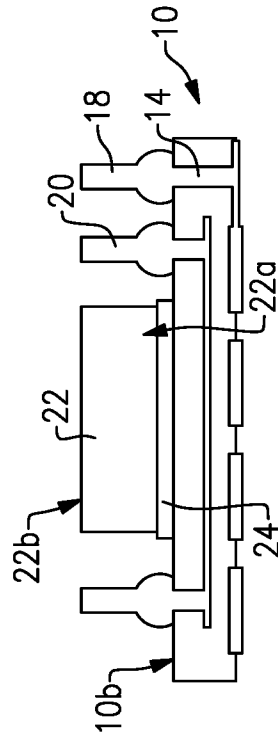


FIG. 1C

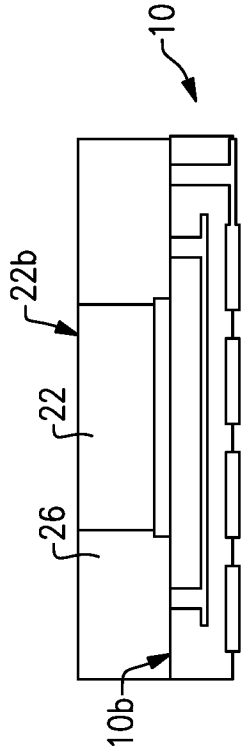


FIG. 2C

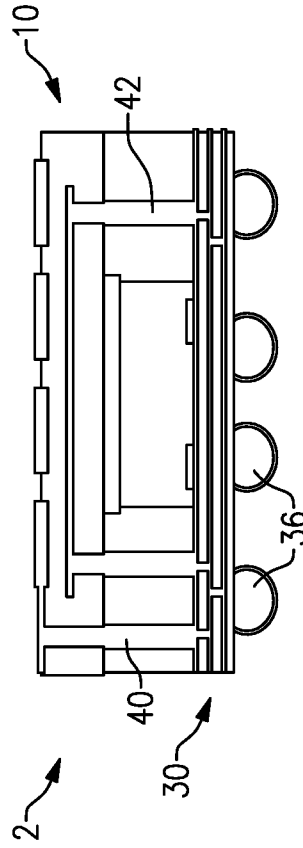


FIG. 2D

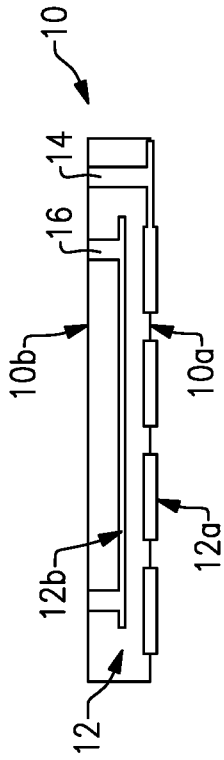


FIG. 2A

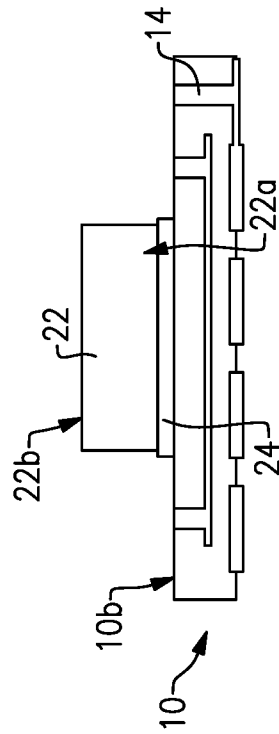


FIG. 2B

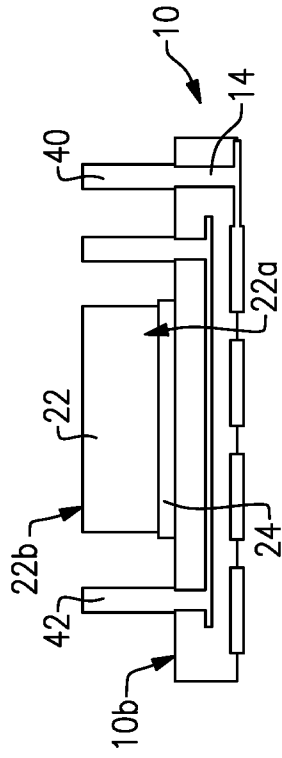


FIG. 2G

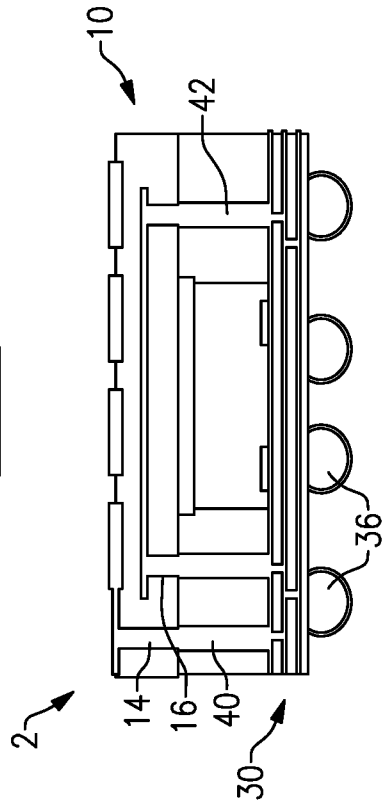


FIG. 2H

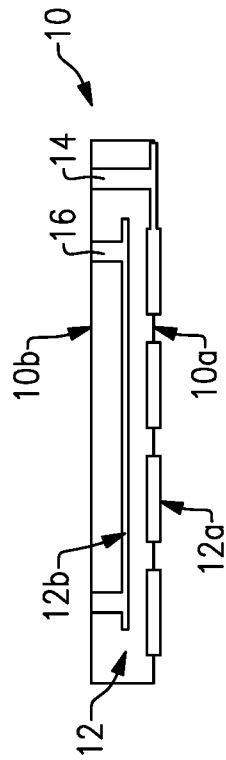


FIG. 2E

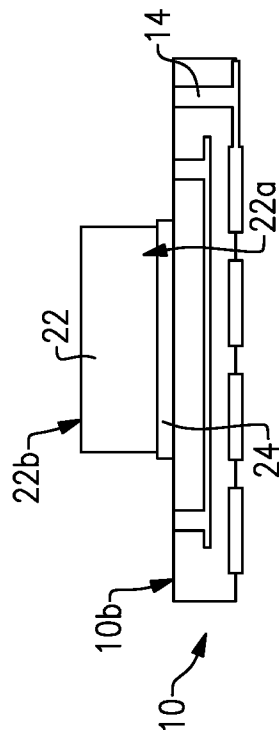


FIG. 2F

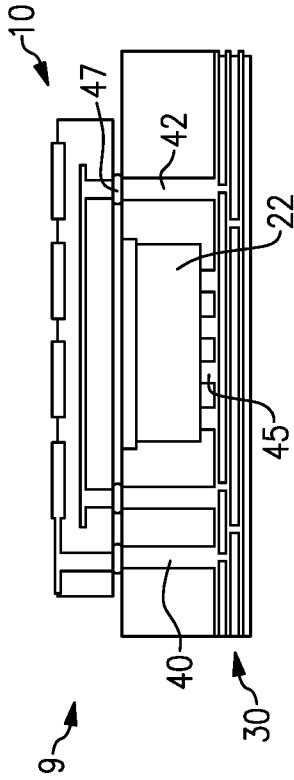


FIG. 3F

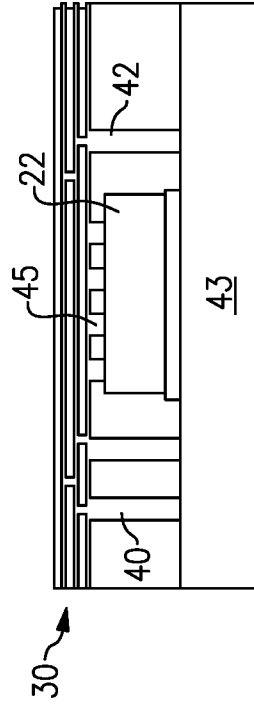


FIG. 3E

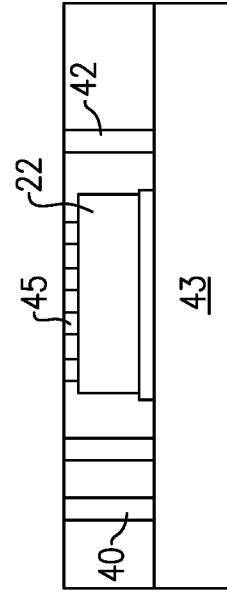


FIG. 3D

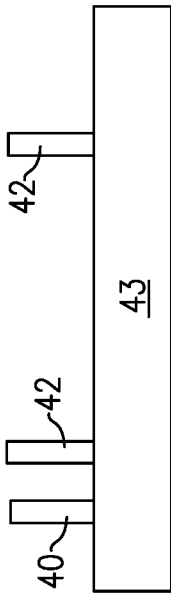


FIG. 3A

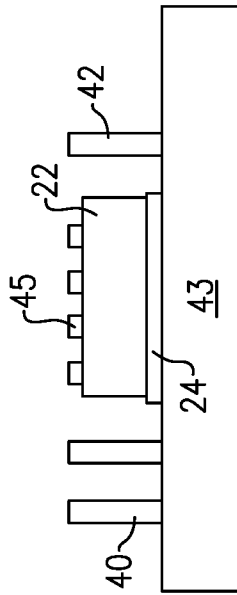


FIG. 3B

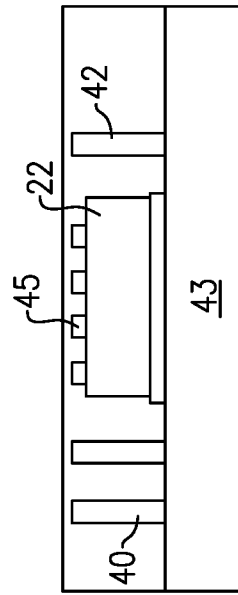


FIG. 3C

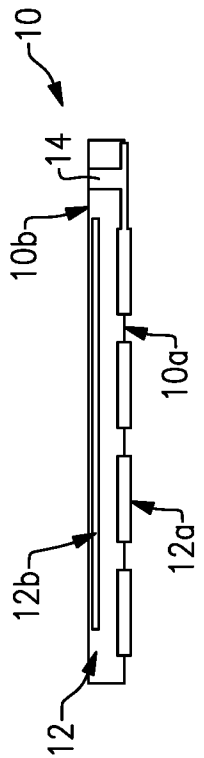


FIG. 4A

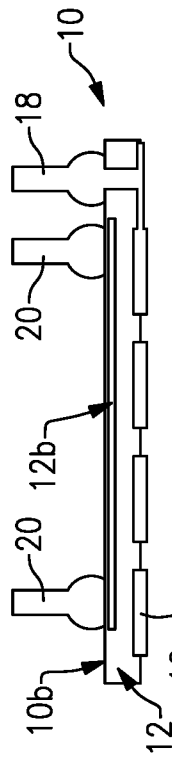


FIG. 4B

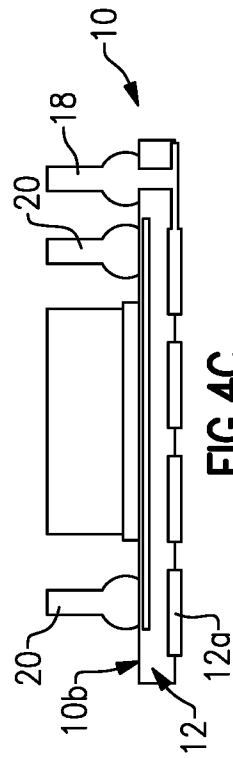


FIG. 4C

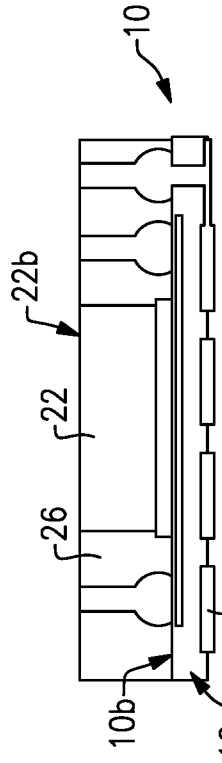


FIG. 4D

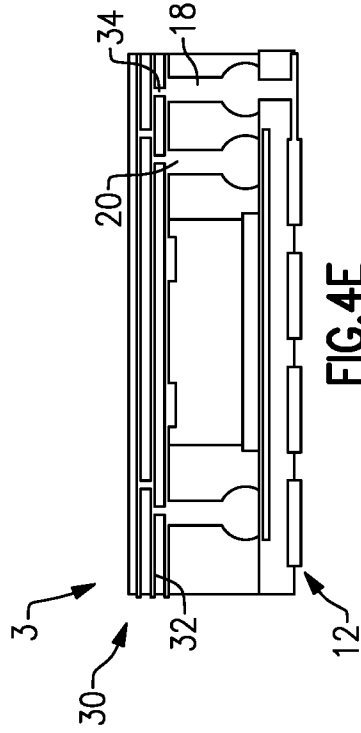


FIG. 4E

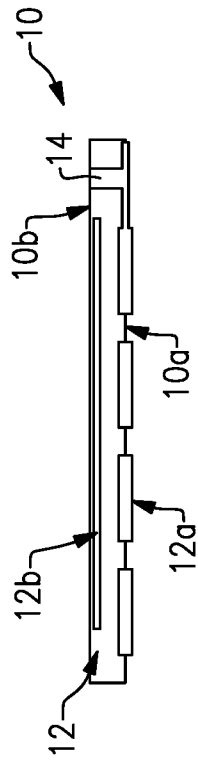


FIG. 5A

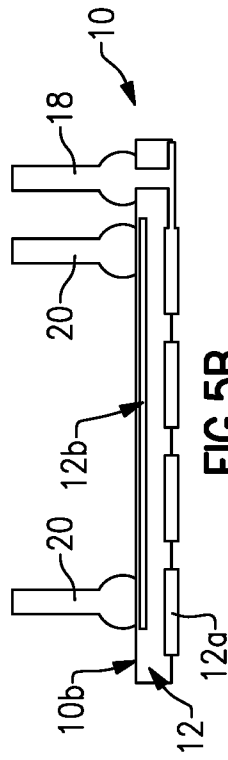


FIG. 5B

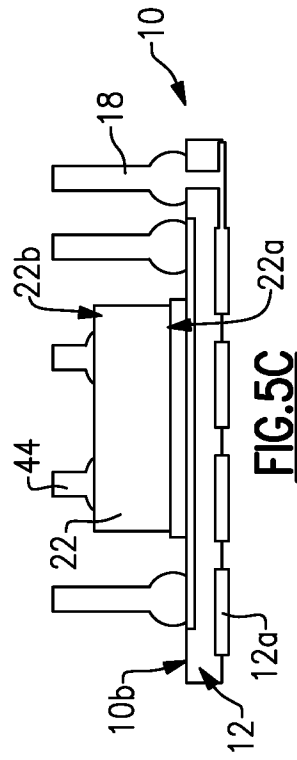


FIG. 5C

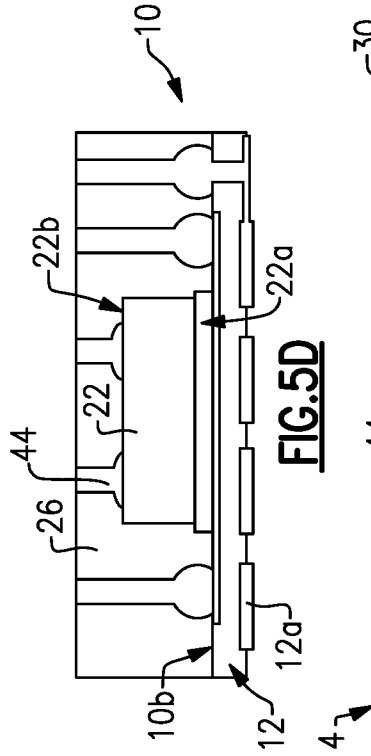


FIG. 5D

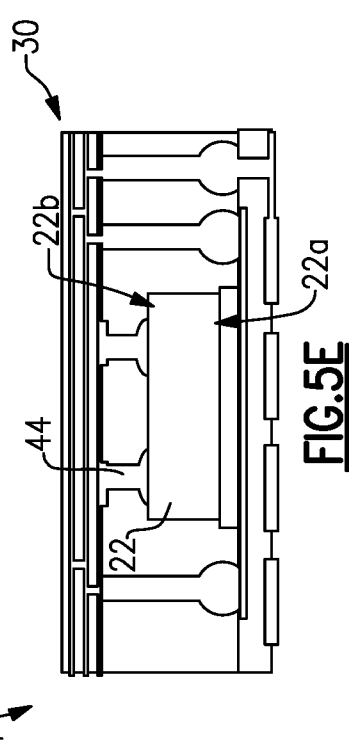


FIG. 5E

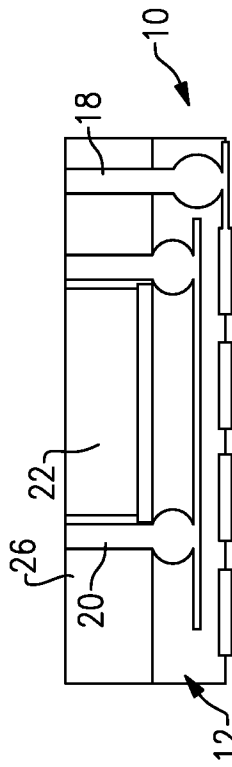
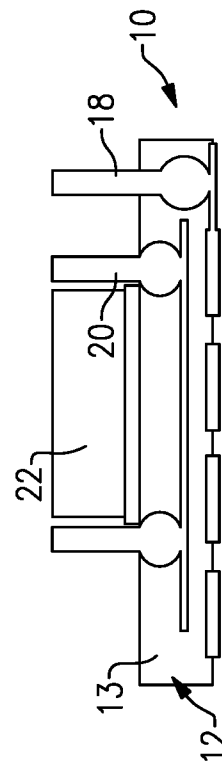
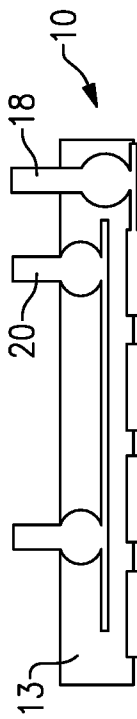
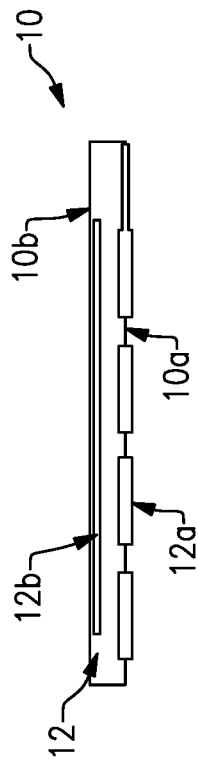


FIG. 6D

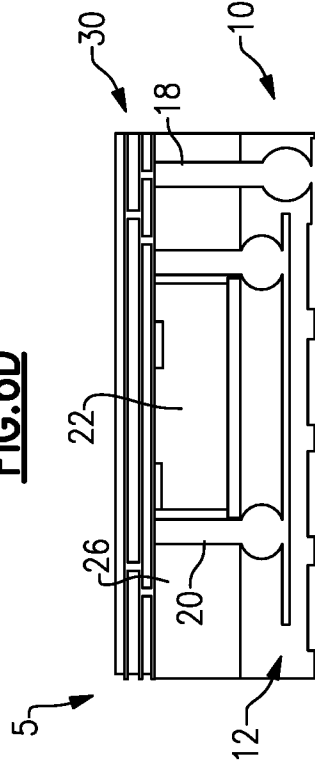


FIG. 6E

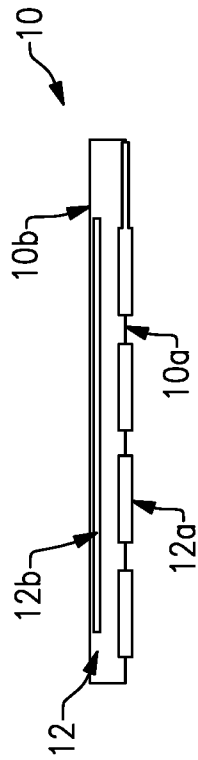


FIG. 7A

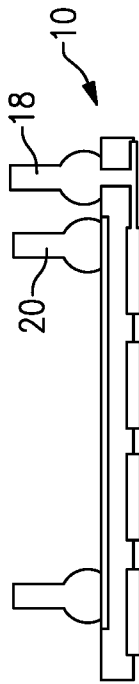


FIG. 7B

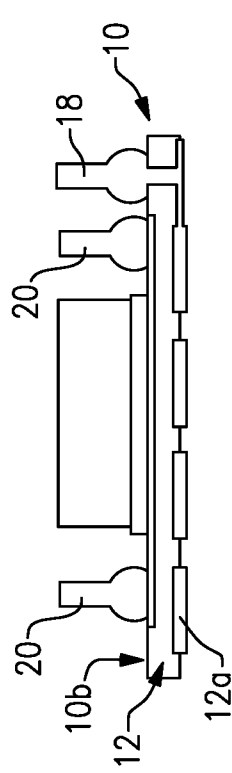


FIG. 7C

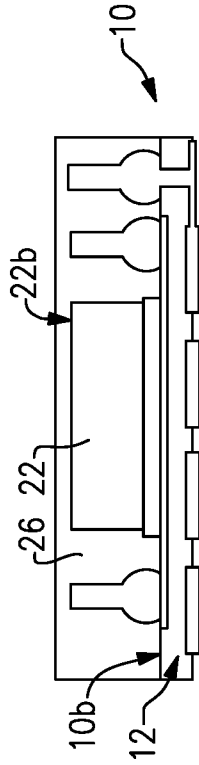


FIG. 7D

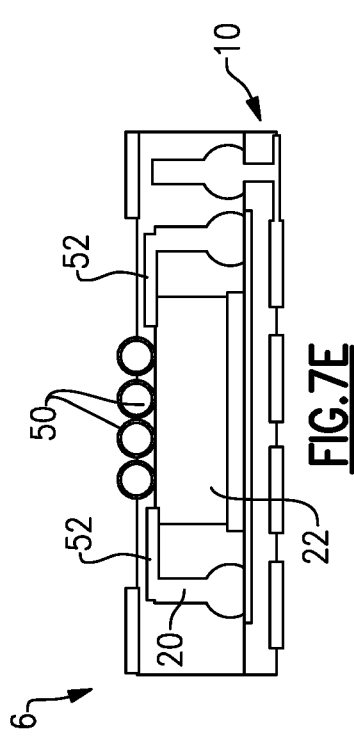


FIG. 7E

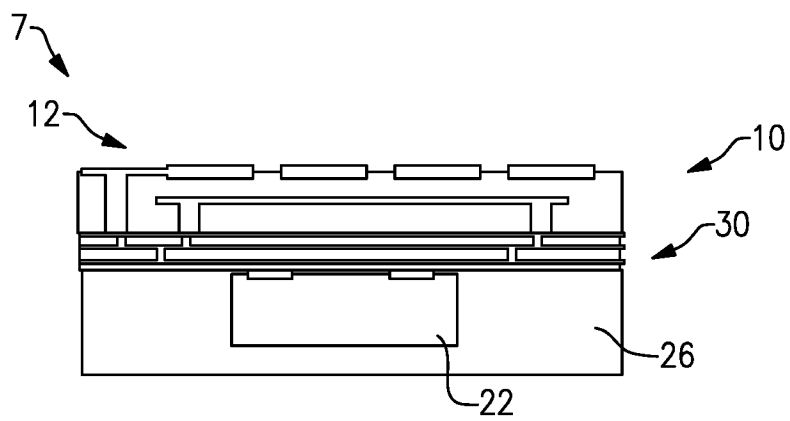


FIG.8

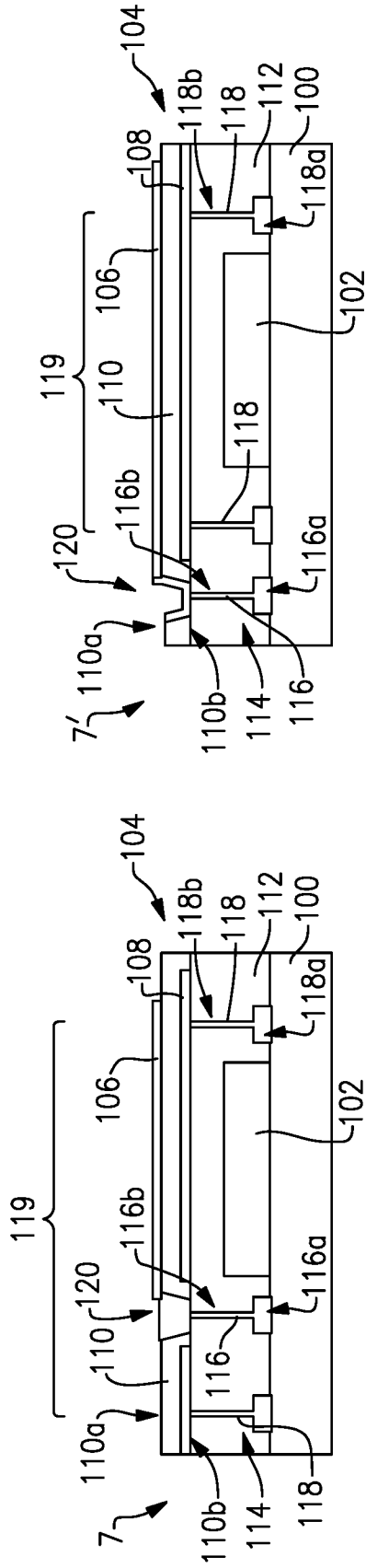


FIG. 9A

FIG. 9C

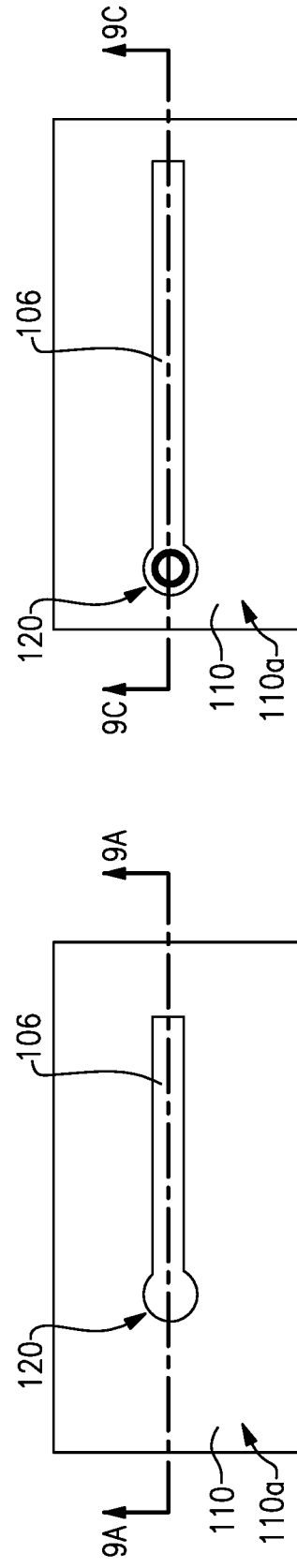


FIG. 9B

FIG. 9D

11/11

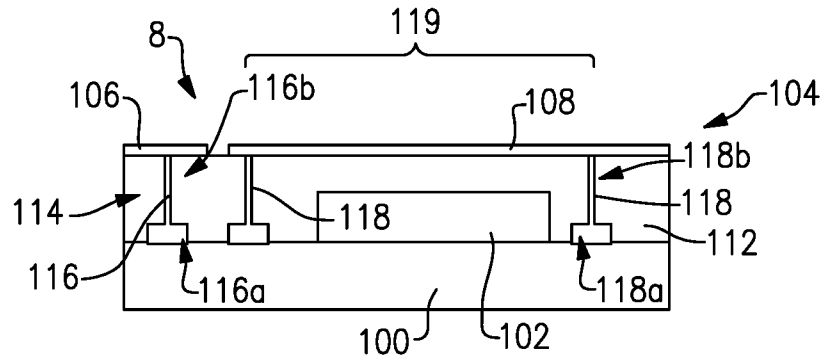


FIG. 9E

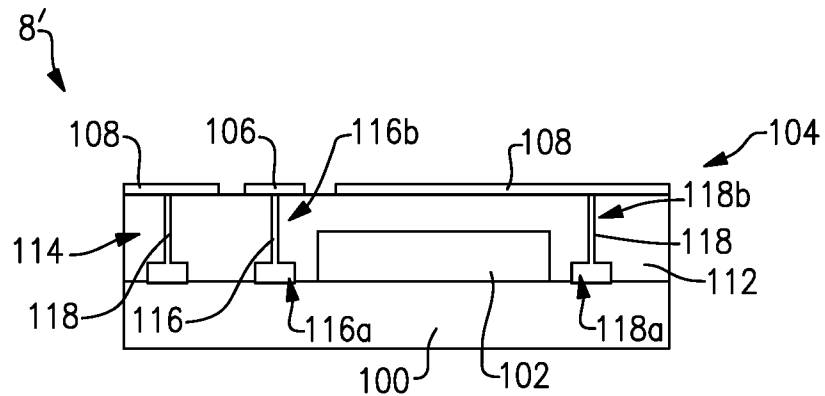


FIG. 9F

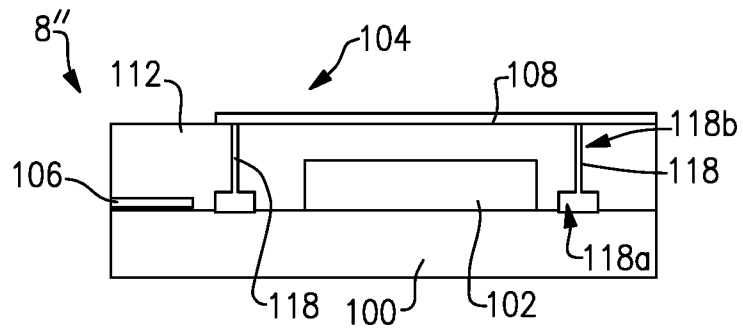


FIG. 9G

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2022/078431

A. CLASSIFICATION OF SUBJECT MATTER		
H01Q 1/38(2006.01)i; H01Q 1/22(2006.01)i; H01Q 1/52(2006.01)i; H01Q 9/04(2006.01)i		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) H01Q 1/38(2006.01); H01L 21/48(2006.01); H01L 21/60(2006.01); H01L 23/00(2006.01); H01L 23/498(2006.01); H01L 23/552(2006.01); H01L 23/66(2006.01); H01Q 1/22(2006.01)		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: antenna, package, molding, material, board, redistribution, layer, via, conductive, wire		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 111446175 A (NATIONAL CENTER FOR ADVANCED PACKAGING CO., LTD. (NCAP CHINA)) 24 July 2020 (2020-07-24) paragraphs [0065]-[0086], claim 4 and figures 1-10	1-2,5-6,9-10,12-17, 21-30,32-35,37-41, 45-49,59-63,70,74-76
Y		3-4,7-8,11,18-2 0,31,36,42-44,5 0-58,64-69,71-73
Y	US 2021-0257716 A1 (INFINEON TECHNOLOGIES AG) 19 August 2021 (2021-08-19) paragraphs [0022]-[0059] and figures 2-24	3-4,11,18-19, 50-58,67-69
DY	US 2017-0117231 A1 (INVENSAS CORPORATION) 27 April 2017 (2017-04-27) paragraphs [0060]-[0088] and figures 3A-8	7-8,20,31,36,42 -44,64-66,71-73
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "D" document cited by the applicant in the international application "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 20 February 2023		Date of mailing of the international search report 20 February 2023
Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon 35208, Republic of Korea Facsimile No. +82-42-481-8578		Authorized officer KIM, Yeon Kyung Telephone No. +82-42-481-3325

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2022/078431

C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013-0292808 A1 (HAN-CHEE YEN et al.) 07 November 2013 (2013-11-07) claims 1-6 and figures 1-38C	1-76
A	US 2020-0075513 A1 (GLOBALFOUNDRIES INC.) 05 March 2020 (2020-03-05) claims 1-6 and figures 1-4E	1-76

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/US2022/078431

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				EP 3866194 A1	18 August 2021
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				US 10580745 B1	03 March 2020