AUTO-TRANSFORMER COUPLED HYBRID CIRCUITS FOR TRANSISTOR AMPLIFIER STAGES

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References Cited
UNITED STATES PATENTS

2,932,800 4/1960 Bereskg ......................... 330/15 X

3,230,467 1/1966 Atherton et al .................. 330/15
2,860,192 11/1958 McIntosh ....................... 330/119 X
2,654,058 9/1953 McIntosh ....................... 317/220

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ABSTRACT

This invention pertains to an auto-transformer coupled output stage for transistor amplifiers, which utilizes a specially designed auto-transformer with split primary and secondary windings, bi-filarly wound, and input windings, incorporated in a push-pull circuit so as to minimize leakage inductance, phase shift, resistance losses, and capacitive coupling. The circuit is suited to Class A, AB, B, or C type operation. Three designs of transformers are described.

5 Claims, 5 Drawing Figures
AUTO-TRANSFORMER COUPLED HYBRID CIRCUITS FOR TRANSISTOR AMPLIFIER STAGES

SUMMARY

The transformer used in this circuit consists of two identical coils, each coil containing one-half the primary winding and one-half the secondary winding, wound bi-filarly, and an input winding, the two identical coils being placed on a common magnetic core, in such relative positions that the polarity of one coil is opposite that of the other, in reference to the beginnings and endings of the coils. Preferably, all windings are of the same number of turns. Other turns ratios may be used, but the advantages of this circuit will be diminished rapidly as the turns ratio varies from unity. The starting ends of the two primary windings are connected together and to one polarity of the d-c power source, and the starting ends of the two secondary windings are connected together, and to the other polarity of the d-c power source. The free end of the secondary winding of the first coil is connected to the emitter of a first transistor, and the free end of the primary winding is connected to the collector of a second transistor; one end of the input winding of the first coil, of the same polarity as the free end of the secondary winding, is connected to the base of the first transistor. Similarly, the free ends of the secondary and primary windings of the second coil are connected to the emitter of the second transistor and to the collector, respectively, of the first transistor, and the end of the second input winding, of like polarity, is connected to the base of the second transistor. The load is connected to the emitters of the two transistors, and the input is connected to the free ends of the two input windings, with an appropriate base to emitter biasing circuit.

In this circuit, the input windings provide an input voltage equal to that of the secondary windings, so that the circuit functions as a common emitter circuit. The signal currents in the bi-filarly wound primary and secondary windings are always in opposite directions, and equal when the primary and secondary have equal number of turns; the signal voltages in each pair of bi-filar windings are equal, or very nearly so, and in the same direction. These factors contribute to high power gain, minimum leakage reactance, phase shift, and capacitive effects, and improved uniformity of response.

DRAWINGS

All the drawings are schematic and functional only. No actual circuitry design is intended, except as it relates to the functioning of this invention. In the interest of brevity, FIGS. 1, 2, and 3 show the feedback version of the three types of circuits. For the non-feedback version, the transformer windings in the base legs of the circuits is deleted. NPN transistors are shown, but PNP would be equally suitable. No d-c values are shown, since they are unnecessary to the description. For convenience, bias voltage sources are shown as batteries, but they can be the usual rectified supply. The + and − symbols represent the assumed instantaneous polarity (or dε/dt) of the signal voltage vector, while, in A, etc., with the accompanying arrows, indicate the assumed positive directions of the signal current vectors (or dI/dt). For increased clarity, the conventional sym-
This compensating voltage accomplishes two purposes. The first is that it boosts the input voltage so that the gain of the stage approaches unity without feedback, or $N_z / (N_y - N_z)$ with feedback. The second is that it supplies a reactive component opposite in phase to the reactive current from base to emitter.

If $N_x = N_z$, then $i_b = 2i_z$, and $i_c = i_b$. The current gain of the stage is twice the current gain of the transistor. The load voltage will be half the collector to emitter voltage, so that the effective transistor load impedance will be four times the load impedance. As another example, if $N_z = 2N_x$, $i_e$ becomes equal to $\frac{1}{2} i_z$ and $i_b = 3/2 i_z$. The load voltage will be equal to $2/3$ the collector to emitter voltage, so that the effective transistor load impedance will be $2 \frac{1}{4}$ times the actual load impedance. In this case, the secondary can be wound bifilar in two halves, concurrently with the primary for minimum leakage reactance.

It is obvious that the output can be taken from the collector leg of the transformer instead of the emitter leg. In this case, a voltage gain of $N_1/N_2$ times the common collector voltage will be realized. The current in the collector leg will be reversed, and the uncompensating effect of the resistance drop, will not occur. Furthermore, the output will be at the collector bias voltage, so that the usefulness of this arrangement is limited, and it appears that additional voltage gain can be better obtained by the feedback circuit illustrated.

The circuit in FIG. 1, either with or without feedback offers a wide selection of choices of voltage gain, current gain, and load ratio, making it useful as an input, intermediate driver or output stage. When $N_1 = N_2$ optimum reduction in leakage reduction will be obtained. There will be capacitive coupling between the two windings, but this should not be a serious deficiency, since this type of stage would be used at low power levels in high fidelity equipment, or at higher power levels, in other than high fidelity applications.

In FIG. 2 the following relationships exist:

$$i_1 = i_2 = i_c = i_b = (N_1 + N_2)/2N_2.$$

Substituting (2) in (1):

$$i_1 N_1 = i_2 N_2 = i_c = i_b = i_0 N_x.$$

or

$$i_0 = i_b = (N_1 + N_2)/2N_2.$$

From (3) it will be seen that, if $N_x = N_z$, $i_b = i_z$ and $i_c = 0$. If $N_1 = 2N_x$, $i_b = 3/2 i_z$, and $i_c = \frac{1}{2} i_z$. When $N_2 = 2N_x$, $i_b = \frac{1}{4} i_z$ and $i_c = -\frac{1}{4} i_z$ (or downward in the schematic). Taking the case of $N_1 = N_2$ as the most favorable, if windings 1–2 and 5–6 of the auto-transformer are wound bifilar, with 1 and 5 as the beginning of the windings, the signal currents are equal and opposite, the ground end of the windings, with respect to the signal voltage, are next to the core, and the two conductors are at the same potential throughout their length, so that there will be minimum leakage reactance and capacitive effects to ground and between the windings. Windings 7–8, if used, will wound separately from 1–2 and 5–6, and either separately or bifilar with respect to 3–4. $N_3$ must be smaller than $N_x$.

In the case of FIG. 2, with $N_1 = N_2$ the load current and the collector current are equal, and the load voltage and the collector-emitter voltage are equal, so that the load transformation ratio is unity. The current gain is equal to the transistor gain, while the voltage gain is approximately, but less than, 2. Since $i_b$ is zero, the gain and phase correction effect mentioned in par. 7 will not occur. This circuit is believed to be well suited for use as a direct-coupled driver for a push-pull stage, or for a single-ended output stage. Compared to FIG. 3, it has the disadvantage of greater d-c core saturation.

An alternate circuit to FIG. 2, especially for an output stage, would be to remove windings 5–6 from windings 3–4, and connect terminal 6 to terminal 1 of the collector leg, with the bias voltage at the mid-tap, and connecting the load across winding terminals 5–2. With $N_1 = N_2$, then $i_1 = i_2 = -\frac{1}{2} i_2$, and the three windings would be wound trifilar. In this case, $i_2$ is the collector current. The voltage gain would be something less than 2, and the current gain would be half the transistor gain. Since the load current is half the collector current, and the output voltage equals the collector-emitter voltage, the effective transistor load impedance will be $\frac{1}{4}$ the actual load impedance. This arrangement would have the disadvantage that the load is at full d-c collector voltage.

The circuit of FIG. 3, as a Class A amplifier, with $N_1 = N_2$ combines all the previously mentioned features of minimum leakage reactance, capacitive effects, and phase shift. The two transistors are connected in push-pull and are coupled to a bifilar wound transformer. The input coils $N_z$ are connected, respectively, between the two input terminals and the bases of said transistors. The secondary windings $N_y$ are connected in series with the ends 6 and 7 connected as a common junction. The other ends of the said secondary windings 5, 8 being connected, respectively, to the emitters of said transistors. One end of each of the primary windings $N_1$ (1 and 4) is connected, respectively, to the collector of said transistors, the other terminals 2, 3 are connected together to form a juncture. A potentiometer is connected between the two input ends 9 and 11 of the input windings $N_y$. A source of potential is connected between the movable tap of the potentiometer and the juncture of the two secondary windings. A second potential source of opposite polarity is connected between the juncture of the primary and secondary windings $N_1$ and $N_2$. The load is taken from the emitters of the transistors. As a Class B or C amplifier, with $N_1 = N_2$, the first two advantages are obtained but the phase shift correction does not occur. Either of two methods of winding the auto-transformer, as shown in FIGS. 4 and 5 may be used, and it may be well to discuss these first.

FIG. 4 is a shell type auto-transformer. Windings 1–2 and 5–6 are wound bifilar as are coil, and windings 3–4 and 7–8 as another identical coil, placed on the core with one end turned end for end with respect to the other. If terminals 2, 3, 6, and 7 are the beginning of each winding, and the transformer connected as shown in FIG. 3, the ground end of each winding will be next the core, and each winding will be at the same potential across one interface between turns, and at a potential of one turn across the other interface. If the conductors are transposed at the beginning of each new layer, so that the same conductor leads throughout the winding, the same polarity is maintained across the interfaces. If they are not transposed, the polarity is reversed in each successive layer. In either case, the capacitive effect between windings is small. An alternate method winding would be to start the two conductors 180° apart, and transpose them at the beginning of each layer. In this case, each conductor is at a potential midway between the adjacent turns of the other conductor, so that
the capacitive coupling between windings will be essentially zero, except for that between layers of the winding. Also from Fig. 3, it will be noted that the currents in each pair of conductors are in opposite directions. When \( N_1 \) and \( N_2 \) of Fig. 3 are equal the currents in each pair of conductors are equal, so that the leakage inductance of the windings will be low. If \( N_1 \) and \( N_2 \) are unequal, one winding will be shorter, and the current in it larger, so that there will be less reduction of leakage inductance than in the former case. If the ratio of \( N_1 \) to \( N_2 \) is an integral number, then the longer winding can be divided into multiples of the shorter and all wound concentrically, or multifilar. Here, again, leakage inductance will be somewhat greater than in the first case, since the individual conductors will not be as tightly coupled, and, in addition, there will be voltage differences between windings, and, as a result, some capacitive coupling between windings. Within limits, however, it appears that better characteristics and performance can be achieved than with conventional transformers. For clarity, feedback windings 9–10 and 11–12 are omitted from the figure. These would be small conductor windings, wound either independently of each other, or bifilar, either under or over the main windings, and of fewer turns than \( N_2 \).

FIG. 5 is a core type transformer. Here the two coils are wound identical to each other, as in Fig. 4, but are placed on the core with the same ends up. The reverse direction of flux in the core accomplishes the same result as the reverse positions of the coils did in the case of Fig. 4. Here again the feedback coils are omitted. They can be wound independently, one on each leg of the core, or co-axially, half of each winding on each leg. The rest of the comments for the shell type transformer also apply here.

In most transformer applications, the shell type transformer is preferred because of its lower leakage inductance. However, in this case, since the windings are split, and because the construction minimizes leakage inductance, the core type transformer offers considerable advantage over the shell type, since it inherently permits more copper on the same amount of iron, especially more so here because of the split windings. It will also have a smaller mean length of turn.

Returning to Fig. 3, and considering Class A operation first, the following signal current relations obtain:

1. \( N_1 (i_1 + i_2) = N_2 (i_3 + i_4) \)
2. \( i_0 = i_1 + i_3 \)
3. \( i_0 = i_2 + i_4 \)
4. \( i_1 = i_2 \)
5. \( i_3 = i_4 \)

Substituting (4) and (5) in (1):

\( N_1 (2i_0 - i_0) = N_2 (2i_0 - i_0) \)

or

\( 6, N_1 i_1 - N_2 i_4 = i_0 (N_1 - N_2) / 2 \)

The left hand term represents the difference in amperes turns in the two bifilar windings 3–4 and 7–8, and is thus a measure of increase in leakage inductance due to the unbalanced current \( i_3 \). The right hand term shows that the effect of unbalanced operation increases as the turns ratio increases. As an example, if we assume that \( N_1 = 2N_2 \) and that \( i_0 = 10 \) percent of \( i_1 \), the right hand term becomes \( N_1 i_0 / 40 \) or about 2-1/2 percent less effective leakage reactance reduction. If \( N_2 = 2N_1 \), the figure becomes 5 percent. Thus it can be concluded that ordinary imbalance in the circuit will not affect the leakage reactance seriously. If \( N_1 = N_2 \), then no unbalance occurs between the two windings for any degree of current unbalance.

Continuing, combining (2) and (3) in par. 16, gives

7. \( i_0 = \frac{1}{2} (i_1 + i_2 + i_3 + i_4) \)

from (1)

8. \( i_0 + i_2 = N_1 (i_1 + i_2) / N_2 \)

Substituting (8) in (7):

9. \( i_0 = \frac{1}{2} (i_1 + i_2) (N_1 + N_2) / N_2 \)

The term \( \frac{1}{2} (i_1 + i_2) \) is, of course, the average collector current and no significant error is introduced by substituting either \( i_1 \) or \( i_2 \) for it.

Taking the special case of \( N_1 = N_2 \), \( i_0 = 2i_1 = 2i_2 \). The voltage across the load is equal to the collector to emitter voltage of each transistor, so that the effective load impedance of each transistor is twice that of the actual load. The current gain of the stage is twice the transistor gain, while the voltage gain without feedback is nearly unity, and with feedback, nearly \( N_2 / (N_2 - N_3) \).

The stage of Fig. 3, in Class A, operation appears to be well suited for input, intermediate, driver and output stages in high fidelity applications. The prototype constructed by the applicant consists of one input-driver stage identical to Fig. 3 without feedback, using two Sylvania ECG 123 A transistors, direct coupled to an output stage using 2 Sylvania ECG 152 transistors, with a feedback ratio of \( N_3 / N_2 = 0.88 \). For both transistors a ratio of \( N_1 = N_2 \) was used, with an overall feedback loop of about 10 percent of output voltage. No formal tests have been made on this unit, but an input estimated at 1-2 volts from a small FM table set gave good quality reproduction on a Jensen 15-inch co-axial speaker, and was able to drive the speaker to overload, which would indicate that this analysis is sufficiently accurate for design purposes.

The Class A operation of Fig. 3 as an output stage has several points of superiority over Class AB, B, or C. First, the auto-transformer is smaller. When the ratio is \( N_1 = N_2 \), the design current is only one half the requirements for Class AB, B, or C. In addition the quality of performance will be superior, although this advantage can be largely overcome by overall negative feedback.

The disadvantage of Class A operation for larger capacity amplifiers is, of course, that transistor dissipation is highest at zero and output, and the power consumption is constant at all loads. Thus, for small amplifiers or for larger amplifiers operating at fairly high power levels continuously, Class A operation would be preferred. Most amplifier duty is at a small fraction of full output, and Class AB, B or C is usually preferred, since both power consumption and transistor dissipation are about proportional to the output.

For Class B or C operation, Fig. 3 will apply to the half-cycle when the upper transistor is conducting. Corresponding relationships will obtain, of course on the alternate half-cycle when the lower transistor is conducting and the upper transistor cut off. For the conditions indicated in Fig. 3, for Class B operation, \( i_0 = 0 \), \( i_4 = i_6 \), and \( i_6 = i_1 \), and the following relations are established:

1. \( N_1 i_1 = N_2 i_3 + N_2 i_6 \)
2. \( i_0 - i_1 + i_3 \)

Substituting (2) in (1)

3. \( i_0 = i_1 (N_1 + N_2) / 2 N_2 \)
4. \( i_1 = i_2 (N_1 + N_2) / 2 N_2 \)

If \( N_1 = 2N_2 \), \( i_0 = 3/2 i_1 \) and \( i_3 = 1/2 i_3 \). The effective transistor load impedance will be 3/2 the actual load, the
current gain 3/2 the transistor gain, the voltage gain about unity, without feedback, or about $N_2 / (N_2 - N_1)$ with feedback. $N_2 i_2 = \frac{3}{2} N_1 i_1$, so that less than optimum reduction of leakage impedance will occur. Also, since $i_2 = 0$, $N_2$ will have no opposing ampere turns. Thus, although an appreciable reduction in leakage reactance occurs it will be considerably less than optimum. Similarly, if $N_3 = 2N_2$, then $i_3 = \frac{3}{2} i_2$, and the effective transistor load impedance becomes $\frac{9}{4} i_2$. Here again, less than maximum reduction of leakage induction is obtained. The current gain is $\frac{3}{4}$ the transistor gain and the voltage gain about unity without feedback, or about $N_2 / (N_2 - N_3)$ with feedback.

When $N_i = N_2$, in Class B or C operation, $i_0 = i_i$, and $i_3$ becomes zero, so that minimum leakage reactance occurs. All the gain and load transformation ratios becomes unity, except that, with feedback, the voltage gain is nearly $N_i / (N_2 - N_2)$. Capacitive coupling between windings is a minimum.

In the circuit of FIG. 3 the load can, of course, be connected to the collector leg of the transformer. The relationships in this case can be easily established, and it appears unnecessary for the purpose of this description to treat them in detail.

In this discussion, emphasis has been placed on the case of unity transformation ratio, because of the superior characteristics of the circuit at this value. It appears that in many cases it would be advantageous to accept something less than optimum transformer ratios for these advantages. It has not been the intention to preclude the usefulness of other transformer ratios, since, in some cases, especially for output stages, the load transformation ratio may be a prime consideration.

Some of the advantages of the circuits, aside from expected high performance will be simplification, easy servicing and improved reliability of amplifiers using these circuits. Because of the low d-c and signal voltages, and relatively high currents, the transformers will be fairly rugged and essentially failure-proof. In the case of the output transformer, a fuse in the primary power circuit or d-c supply will protect it from other circuit failures. For other stages, the voltage dropping resistors usually will limit fault currents to safe values in the transformers.

As an example of circuit simplification, an amplifier can be constructed using an output stage, either Class A, AB, C or D, based on FIG. 3, direct coupled to a driver stage based on FIG. 3 or FIG. 2, and, if necessary, an input stage based on FIG. 1, direct coupled to the driver stage. The high efficiency of energy transfer between stages will minimize the number of stages required. The only capacitors and resistors required would be associated with the amplifier input, the d-c bias supplies, and, usually, an overall feedback loop. Even the latter can be replaced by a small additional winding on the output transformer.

The features which the applicant believes to be novel, and of his invention, are:

1. A push-pull transistor amplifier circuit suitable for amplifier, driver or output stages in audio frequency or ultrasonic frequency ranges, comprising:

   an auto-transformer having a first and a second primary winding, and a first and a second secondary winding, and a first and a second input winding,

   said first primary and first secondary windings consisting of single insulated conductors wound bi-filarly, starting and ending either simultaneously, or one-half turn apart, and being transposed at the beginning of each successive layer, so that the same conductor leads the other, throughout the course of the winding, said first feed-back winding of equal, or nearly equal number of turns being wound either over or under the first primary and secondary windings, the three windings forming a first coil of the transformer, the second primary, secondary and feedback windings being wound in the same fashion to form an identical second coil, and the two coils being placed on a magnetic core, in opposite relative positions on a shell-type core, or in the same relative position for a core-type core, so that the induced voltages in the two coils are in opposite phase relation; and

   a first transistor, the emitter being connected to the end of the first secondary winding, the collector being connected to a end of the second primary winding, and the base being connected to one end of the first input winding of the same relative polarity as the emitter; a second transistor, the emitter being connected to the end of the second secondary winding, the collector to the end of the first primary winding, and the base to one end of a second input winding, of the same relative polarity as the emitter; the unconnected ends of the first and second primary windings being connected together, and to one end of the direct current power source, the unconnected ends of the first and second secondary windings being connected together, and to the other end of the direct current power source, the load being connected to the emitters of the first and second transistors, and the transistor bias and input signal being applied to the ends of the first and second input windings, opposite the ends connected to the transistor bases.

2. An output stage for transistor amplifiers consisting of a first transistor and a second transistor of like conductivity, and a transformer having a first input winding, a first primary winding wound bi-filarly with a second primary winding, a second input winding, a second primary winding wound bi-filarly with a second secondary winding, one terminal, of a first polarity, of said first input winding being connected to the base of the first transistor and one terminal, of a second polarity, of said second input winding being connected to the base of the second transistor, the free ends of said first and second input windings being connected to an input signal source, with appropriate bias, one terminal, of the first polarity, of said first secondary winding being connected to the emitter of the first transistor, one terminal, of the second polarity of said second secondary winding being connected to the emitter of the second transistor, the free ends of said first and second secondary windings being connected together, one terminal, of the first polarity, of said first primary winding being connected to the collector of the second transistor, one terminal, of the second polarity, of said second primary winding being connected to the collector of the first transistor, and the free ends of said primary windings being connected together, a source of direct-current bias being connected between the common connections of said primary and secondary windings, and the output load being connected between the emitters of the first and second transistors.
3. A transformer as set forth in claim 2 comprising a magnetic core, two input windings, two primary windings and two secondary windings, said windings consisting of two identical coils, each coil containing a separately wound input coil, and a primary and a secondary coil, bi-filarly wound, with two insulated wires, each winding starting 180° from, and outside, the other, so that the first half-turn of each winding is on the outer end of the first layer, said wires being transposed at the beginning of each subsequent layer, so that the same conductor leads during the entire winding process, and said two identical coils being placed on said magnetic core in such relative positions that the beginning of one coil is of a polarity opposite to that of the other.

4. A transformer as set forth in claim 2 comprising a magnetic core, two input windings, two primary windings and two secondary windings, said windings consisting of two identical coils, each wound with seven strands of insulated wire, in the standard seven-wire twisted cable configuration, the central wire of each cable comprising one input winding, and each three alternate outer wires of each cable being connected together at the ends to form one primary and one secondary winding, said two identical coils being placed on said magnetic core in such relative positions that the beginning of one coil is of a polarity opposite that of the other.

5. A transformer as set forth in claim 2 comprising a magnetic core, two input windings, two primary windings and two secondary windings, said windings consisting of two identical coils, each coil containing a separately wound input winding and a primary and a secondary coil wound together bi-filarly and spirally with two insulated tape or ribbon conductors, one conductor, being started 180° ahead of the other, and each conductor being started beneath the other, so that the first half turn of each conductor occupies the inner surface of the coil, said two identical coils being placed on said magnetic core in such relative positions that the beginning of one coil is of a polarity opposite that of the other coil.

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