United States Patent

[11] 3,619,741

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[54] **METHOD OF PROVIDING INTEGRATED DIFFUSED EMITTER BALLAST RESISTORS FOR IMPROVED POWER CAPABILITIES OF SEMICONDUCTOR DEVICES**
7 Claims, 14 Drawing Figs.

[52] **U.S. Cl.** ..... **317/235 R,**
317/235 (29) Q, 317/235 (40.13) Z
[51] **Int. Cl.** **H011 11/06**
[50] **Field of Search** 317/235
(40.1), 235 (40.13)

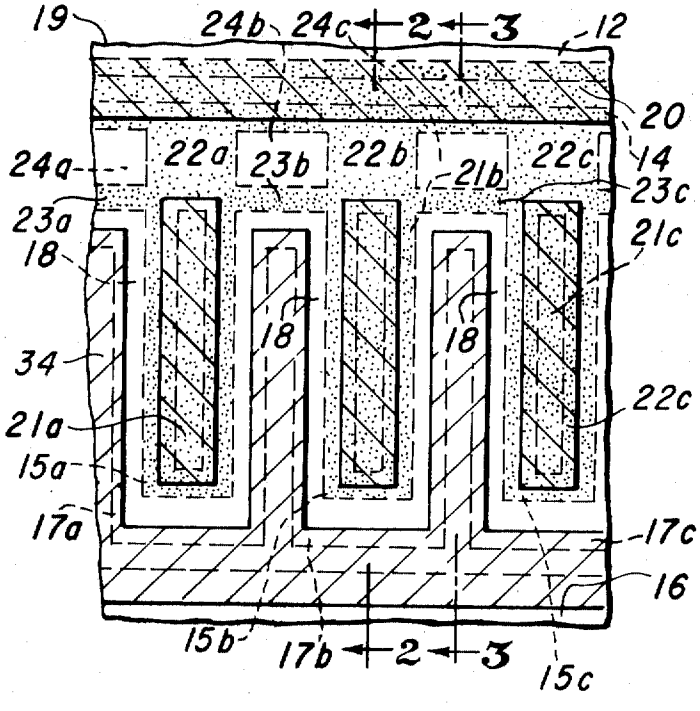
[56] **References Cited**

UNITED STATES PATENTS

3,225,261	12/1965	Wolf	317/235
3,358,197	12/1967	Scarlett	317/235
3,444,443	5/1969	Moroshima	217/235

Primary Examiner—Jerry D. Craig
Attorneys—James O. Dixon, Andrew M. Hassell, Mel Sharp, Harold Levine, John E. Vandigriff, Henry T. Olsen, Michael A. Sileo, Jr. and Gary C. Honeycutt

ABSTRACT: The disclosure is directed to planar transistors which include an emitter region disposed in a base region, the emitter region comprising an elongated spine from which spaced parallel emitter stripes project. The emitter electrode comprises a spine contact and individual electrode strips extending from the distal ends of the emitter fingers to locations spaced apart from the spine contact leaving discontinuities in the emitter electrode such that the sheet resistance of the emitter fingers underlying the discontinuities is utilized to form electrical ballast resistances in the emitter contact sufficient to prevent localized thermal runaway during operation of the transistor. The base contact has contact strips interdigitating with the emitter contact strips and extending from a common base electrode portion. Adjacent the discontinuities in the emitter contact, webs of emitter region material extend across the ends of the base contact strips and join adjacent ones of the emitter fingers to prevent deleterious localized current injection during operation of the transistor. An embodiment is also described in which the emitter region does not have a spine but consists of a series of spaced-apart, parallel extending fingers.



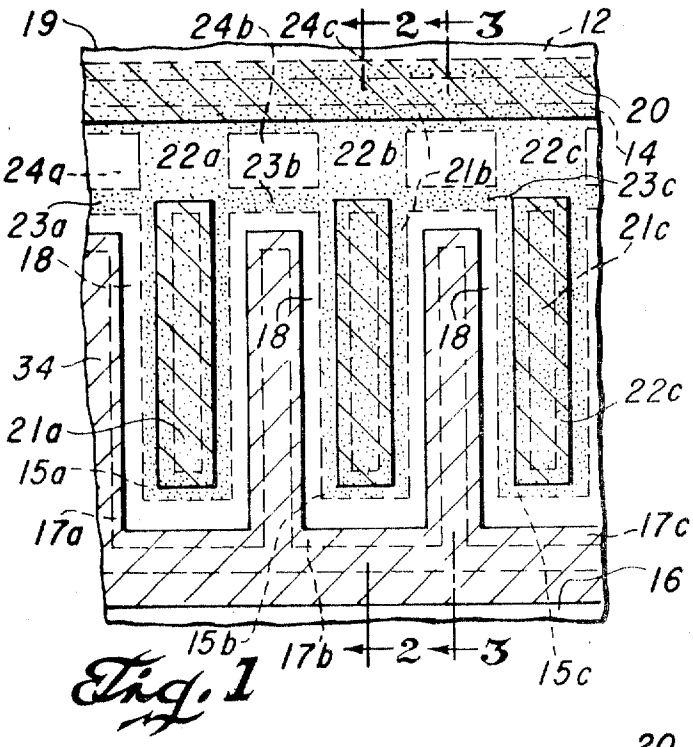


Fig. 1

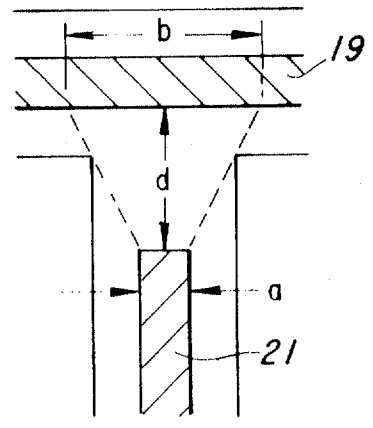


Fig. 4

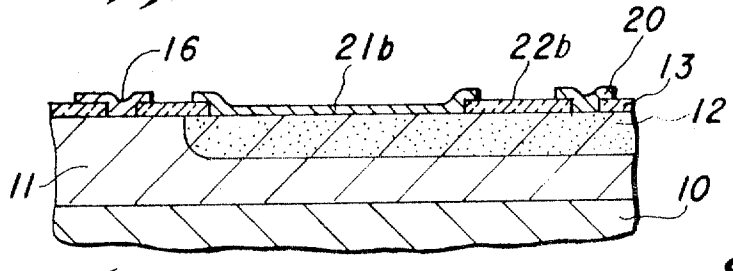


Fig. 2

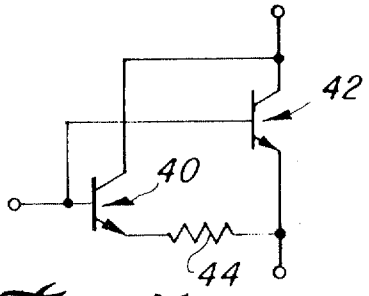


Fig. 5

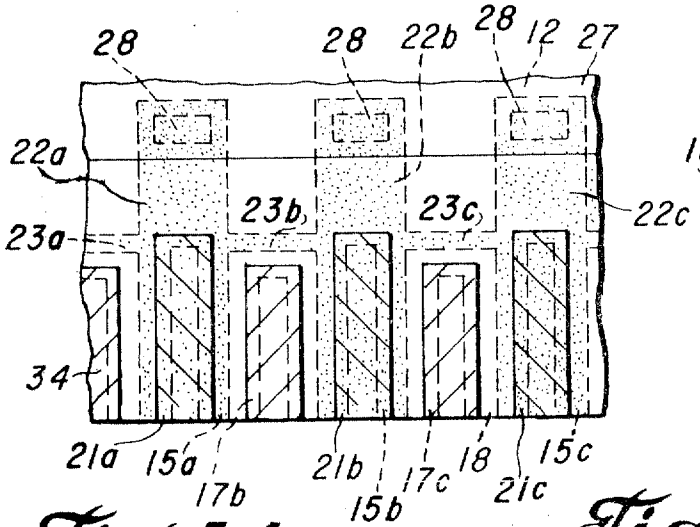


Fig. 14

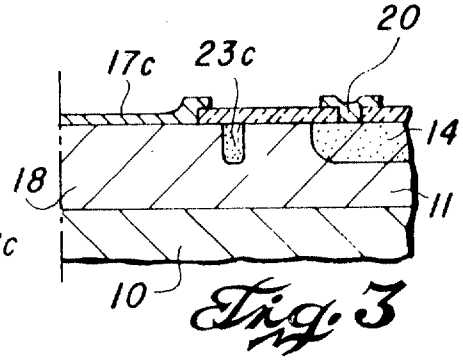


Fig. 3

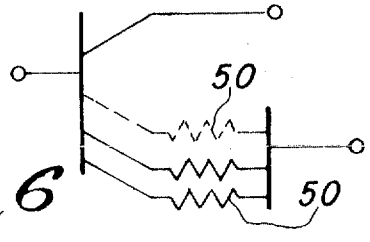


Fig. 6

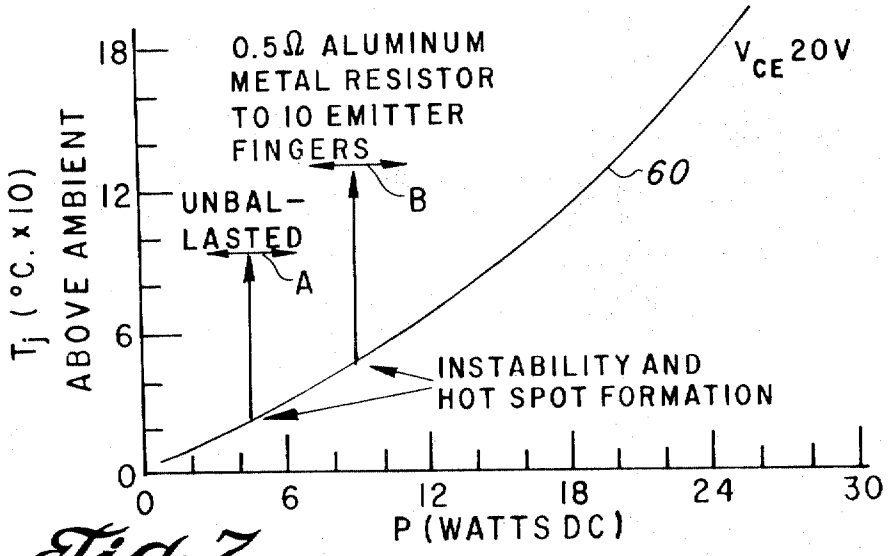


Fig. 7

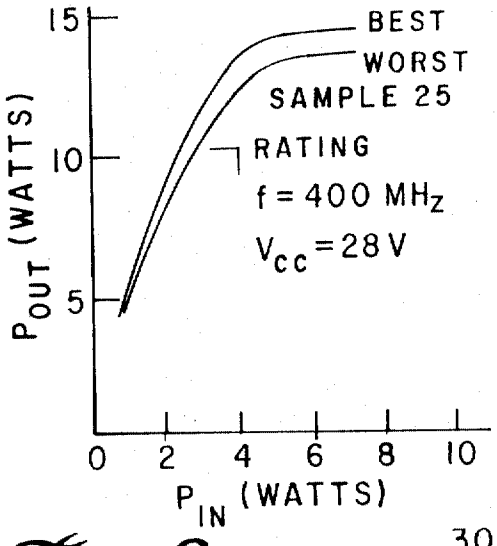


Fig. 8

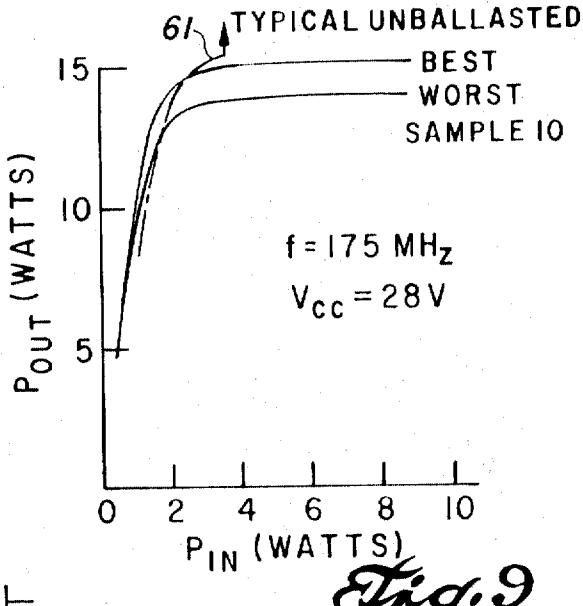


Fig. 9

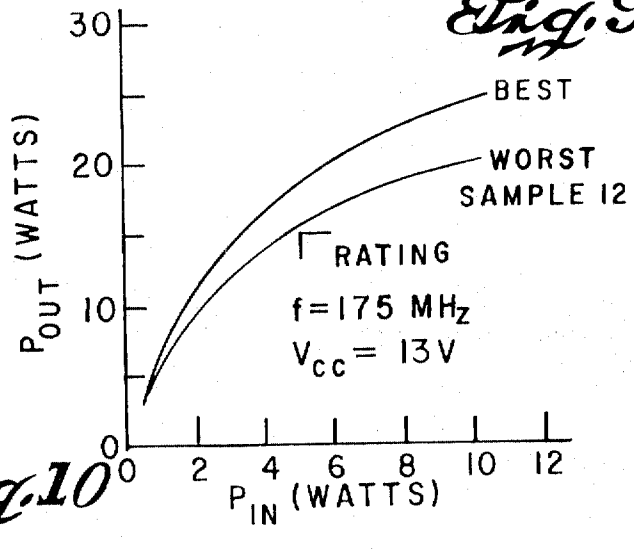


Fig. 10

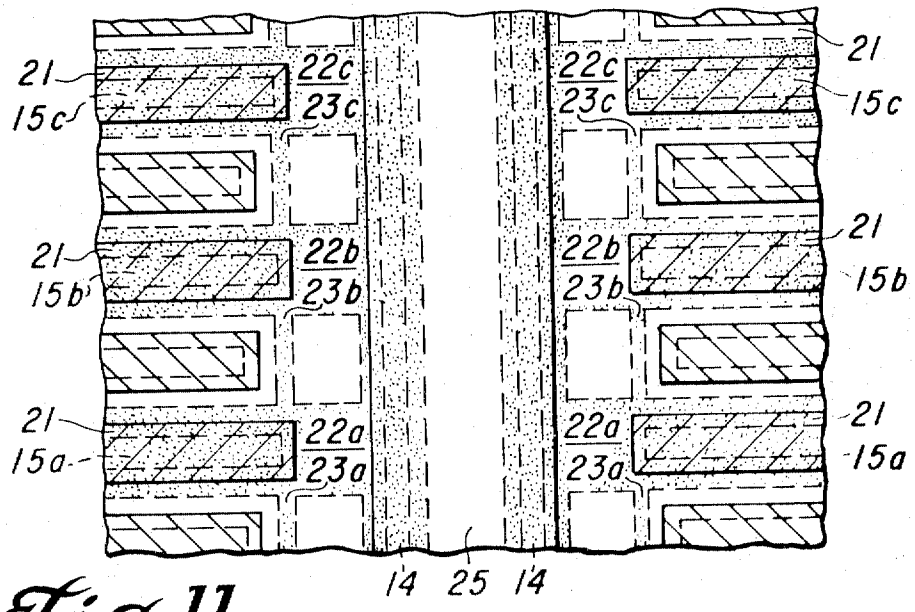


Fig. 11

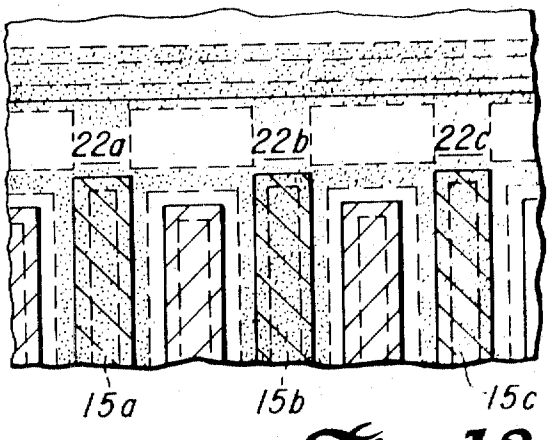
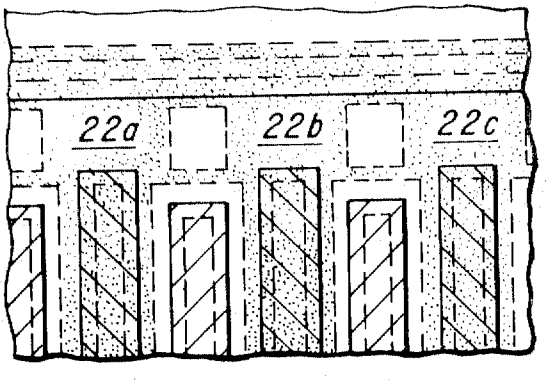


Fig. 12

Fig. 13



METHOD OF PROVIDING INTEGRATED DIFFUSED EMITTER BALLAST RESISTORS FOR IMPROVED POWER CAPABILITIES OF SEMICONDUCTOR DEVICES

This invention relates to semiconductor devices, and more particularly, to transistors suitable for high power operations whilst remaining thermally stable, for example, as RF amplifiers or oscillators or current-switching devices. The invention is applicable both to discrete semiconductor devices as well as to semiconductor devices which are formed as elements of an integrated circuit, monolithic or hybrid.

Limitations have heretofore existed in the power-handling capabilities of transistors and in particular, the capabilities of power transistors used at radio frequencies, wherein mismatch on tuning must be withstood. A substantial amount of these limitations have been due to secondary breakdown caused by lateral thermal instability resulting from localized thermal runaway. This thermal instability has been caused by large positive temperature coefficient of current flow in the transistor, wherein any slight nonuniformity of the transistor tends to cause a nonuniform thermal distribution across the transistor upon the application of substantial power. Increased current flow through the transistor then tends to take place in the hottest region of the transistor, thereby causing further localized heating. A regenerative effect, termed localized thermal runaway in this description, may thus occur, leading to catastrophic failure of the transistor.

It has heretofore been proposed to utilize a resistance having a positive temperature coefficient between the emitter contact and the emitter region of a transistor in order to thermally stabilize the transistor and to reduce the tendency to lateral thermal instability of the transistor. For example, U.S. Pat. No. 3,286,138 issued Nov. 15, 1966 to W. Shockley, discloses the provision of a layer of resistive metal between the emitter region of a transistor and the metal emitter contact to thermally stabilize the transistor. This technique has provided improved thermal stability for transistors but has been found to require a substantial amount of extra metallization, thereby resulting in increased production costs and sometimes presenting yield problems due to scratches and imperfections in the additional metallization layer. Moreover, such techniques have not been generally satisfactory for use with transistors employing interdigitated geometry and intended for operation at high input frequencies. Techniques have also been proposed for increasing the power handling capability of interdigitated transistors by controlling the contact geometry upon the emitter fingers but problems such as voltage differences along the finger lengths have rendered such techniques generally impracticable. Another proposal has been the formation of resistive elements from contact metallization or by an additional metallization upon interdigitated transistors by forming a number of thin film resistors connected in series to groups of emitter fingers, but problems have arisen due to lack of adequate control of the metallization thickness and geometry as well as due to such phenomena as electromigration.

U.S. Pat. No. 3,358,197 issued Dec. 12, 1967 to M. Scarlett, discloses a transistor having an emitter region comprising a plurality of fingers extending from a common emitter portion, the emitter being formed in a base region which has an area of increased depth underlying the common emitter portion. The emitter contact system comprises metallization strips overlying the outer portions of the emitter fingers and spaced from a contact portion to the common emitter portion so that the sheet resistance of the emitter region in the said spaces effectively introduce series resistors between the emitter contact strips and the common emitter contact portion. This approach offers the prospect of advantages over the techniques discussed above but is liable to suffer from deleterious localized current injection from the emitter region wherein the resistive element is formed and from that part of the emitter region to which external contact is made. The formation of the base region with a portion of increased depth may also give rise to production yield problems and although this relatively deep portion of the base region is stated to provide a relatively inactive portion of the emitter base junction, the result is effectively that of a low gain transistor permanently in parallel with the transistor incorporating the active regions of the emitter-base junctions.

The present invention constitutes an improvement over the above described prior proposals and provides a transistor device including an emitter region disposed in a base region, the emitter region having individual spaced-apart portions with portions of said base region interposed therebetween. An emitter electrode system is ohmically connected to and distributed over the said emitter region and includes a portion common to all said individual emitter portions and discontinuities formed in the electrode system over areas of the individual emitter portions to form electrical resistances sufficient to stabilize the current density of the device, thereby to prevent localized thermal runaway. The device also includes means for reducing localized current injection from parts of the emitter region adjacent said common portion of the emitter contact means into the base region. Preferably, the said electrical resistances are formed by the sheet resistance of the emitter region underlying the said discontinuities. In particular, the means for reducing localized current injection comprises webs of emitter region material extending between and connecting adjacent ones of the individual emitter portions in the regions of the said discontinuities, the said webs extending across the ends of base contact fingers located between the individual emitter portions. Such webs prevent localized current injection from undesired regions and suppress any possible undesirable secondary transistor action. By employment of the invention, practicable transistors can be realized which are capable of operation at high frequencies and with enhanced freedom from thermal runaway, without employment of additional or modified diffusion processes during fabrication of such transistors.

For a more complete understanding of the present invention and for further objects and advantages thereof, reference is now to the following description taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a top view of an embodiment of a transistor according to the invention;

FIG. 2 is a cross-sectional view taken generally along the section lines 2—2 of FIG. 1;

FIG. 3 is a cross-sectional view taken generally along the section lines 3—3 of FIG. 1;

FIG. 4 is a diagrammatic illustration of the geometry of a portion of the device shown in FIG. 1;

FIGS. 5 and 6 are schematic diagrams of equivalent circuits of transistor constructions illustrating the improvements provided by the present invention;

FIGS. 7–10 are graphs illustrating various operating parameters of transistors embodying the invention; and

FIGS. 11–14 illustrate modifications of the transistor structure shown in FIG. 1.

FIGS. 1–3 show portions of a planar transistor employing a suitable semiconductor material, e.g. silicon or germanium, and embodying the present invention. The construction of an NPN-transistor will be described by way of example and it will be understood the PNP-transistors embodying the invention also may be constructed.

The transistor illustrated comprises a semiconductor body having an N-type collector region **10** formed therein. The collector region may, for example, be a diffused region or an epitaxial region e.g. an N-type epitaxial layer on an N+ type substrate. Using oxide masking and diffusion techniques, a P-type base region **11** of uniform depth or thickness is inset in the collector region and an N-type emitter region **12** is inset in the base region. The base-collector and base-emitter junctions extend to a common surface of the semiconductor body and are there covered by a protective passivating layer **13**, e.g. a silicon oxide. The emitter region **12** is comblike in structure and comprises an elongated spine portion **14** having a plurality of spaced apart, parallel emitter stripes, such as **15**.4–c, projecting transversely therefrom.

An ohmic contact to the base region comprises a base contact spine **16** parallel to the emitter spine **14** and spaced from the distal ends of the emitter stripes **15** with base contact fingers such as **17***a–c* extending from the spine **16** between the emitter stripes **15** towards the emitter spine **14** and in ohmic contact with underlying stripes **18** of the base region. It is to be noted that the base contact fingers **17** terminate well short of the junction between the base region stripes **18** and the emitter spine **14** to reduce localized injection.

An emitter contact system **19** has an emitter contact spine **20** extending along and in ohmic contact with the emitter spine **14** and emitter contact fingers such as **21***a–c* overlying and in ohmic contact with portions of the emitter stripes **15***a–c*. The emitter contact fingers **21***A–c* extend from the distal ends of the emitter stripes **15***a–c* towards the emitter contact spine **20**, interdigitating with the base contact fingers **17***a–c*, and an important feature of the invention is spaces or discontinuities **22***a–c* in the emitter contact system between the emitter contact spine and the contact fingers.

The emitter and base contacts ohmically contact the respective emitter and base regions through appropriate apertures in the oxide layer **13** and preferably, as shown in FIGS. **2** and **3**, extend out from the apertures over part of the oxide layer. These ohmic contacts can be formed by selectively etching a metallization layer formed on the oxide layer. This layer may comprise a single metallurgical component e.g. aluminum or may be of multiple layer metallurgy having two or more components e.g. molybdenum overlaid by gold or aluminum; or gold sandwiched between layers of molybdenum and in such cases the underlying layer of molybdenum may itself be attached to the semiconductor by an by an interposed thin layer of aluminum. An ohmic contact (not shown) to the collector region **10** may be formed in like manner.

As noted above, an important feature of the invention is the formation of the discontinuities **22***a–c* in the emitter contact system whereby the areas of semiconductor material of the emitter region underlying the discontinuities, provide sheet resistances of sufficient magnitude to impart thermal stability to the transistor during operation thereof. Electrically these resistances are in series between the emitter contact spine **20** and the emitter contact fingers **21***a–c* and current between the contact spine **20** and the fingers **21***a–c* flows through the sheet resistances provided by areas of the emitter stripes **15** underlying the discontinuities. It may be noted that:

$$I_E = I_S \exp (V_{BE})/kTq \qquad (1)$$

wherein

I_E = emitter current

I_S = reverse saturation current

V_{BE} = applied base-emitter bias (minus the bandgap potential

q/kT = constant.

Thus, the voltage drop across a resistive element caused by the flow of emitter current provides a debiassing action, as shown by:

$$I_E = I_S \exp \frac{(V_{BE} - I_E R)_q}{kT} \qquad (2)$$

wherein,

R = the value of the resistive element.

The interdigitated transistor of FIGS. **1—3** provides advantages in the ratio of emitter periphery to base area, which is a major factor in governing current handling capability, particularly when utilized in RF environments. Reduced capacitance values are also provided by the interdigitated transistor. The resistive areas formed by the discontinuities **22***a–c* may be very accurately defined by the conventional photomasking techniques.

The use of an emitter spine results in improved yield and reliability since, by comparison with construction not using such a spine, the current density within the emitter contact **19** is reduced on crossing the discontinuity, formed at the edge of the contact aperture, to the semiconductor material.

FIG. **4** diagrammatically illustrates the geometry for the computation of the resistance formed by one of the discontinuities **22** in the metal emitter electrode. The resistance may be defined as follows:

$$R = \rho SE^d \frac{\left(\ln \frac{b}{a}\right)}{b-a} \qquad (3)$$

wherein,

ρSE = the sheet resistance of the diffused emitter region,

d = the distance between the end of an emitter finger contact **21** and the emitter spine contact **19**,

a = the width of the emitter finger contact **21**,

b = the width of the base of a trapezoid drawn from the corners of the emitter finger contact **21** to the emitter spine contact **19** and passing through the corners of the junction between the emitter stripe **15** and the emitter spine **14**.

It will thus be seen that the resistance formed between each of the emitter contact fingers **21***a–c* and the emitter contact spine **19** comprises a trapezoidal spreading resistance. Spreading resistances may thus be very accurately determined for a given value of emitter sheet resistance by suitably controlling the geometric parameters *a*, *b*, and *d* according to Equation **3**. In practice, the resistance defined in Equation **3** may be slightly lower than the defined trapezoidal value, due to spreading in the diffused emitter sheet.

The use of an emitter spine and the consequent trapezoidal spreading resistance results in less variation in resistance value due to geometric variance in processing than can be achieved in a construction not incorporating such a spine and having a rectalinear spreading resistance.

In practical embodiments of the present interdigitated transistor, a sheet resistance value of about 5 ohms formed by a discontinuity in each emitter contact strip has been found to work well, but of course, such resistances may be widely varied for different applications. In practical manufacture of the devices, some variances in the photoresist techniques may cause slight variations in the specified geometry of the discontinuities. However, such variations have not been found to substantially affect the operation of the transistors, due to the fact that the variances in the final sheet resistance are generally negligible.

The present invention not only provides operational advantages due to the ballasting of individual emitter fingers, but also enables wafer sizes to be reduced by as much as about one-third. The present invention thus makes it possible to increase the overload capability for an interdigitated transistor, in addition to increasing the collector efficiency and increasing the power gain at high input powers.

As a result of the manner of geometric delineation of the resistive element in each emitter finger, the resistor value may be readily increased such that improved resistance to thermal instability is obtained at the expense of power gain, which is then lowered due to degeneration as a result of increasing the total resistance in the emitter terminal.

The transistor shown in FIGS. **1–3** also includes diffused webs, or false spines, **23***a–c* of emitter semiconductor material which are formed across the ends of the base contact fingers **18***a–c* adjacent the ends of the emitter contact fingers **21***a–c*, to reduce localized current injection due to the proximity of the base contact fingers to the emitter spine **14**. Portions **24***a–c* of base region semiconductor material are thus interposed between the webs **23***a–c* and the emitter spine **14**. The ends of the webs **23***a–c* are integral with and connect adjacent ones of the emitter fingers **15***a–c*. The oxide layer **13** covers the upper surfaces of the webs **23***a–c* and the base portions **24***a–c* as shown in FIG. **3**. The emitter webs **23***a–c* are preferably of narrower width than the width of the emitter fingers and, as shown in FIG. **3**, are not necessarily contacted by the emitter stripe metallization.

In operation of a particular embodiment of the transistor described with reference to FIGS. 1–3, but in the absence of the emitter webs 23*a–c*, voltage drops of about 100–300 millivolts typically may occur across the emitter ballast resistors provided by the regions 22*a–c*. Due to the relationship shown by equation 1, localized current injection may take place from the emitter spine directly opposite the ends of the base contact fingers. This localized injection may lead to possible failure of the transistor, or of degradation of current dependent operating parameters such as h_{FE} or h_{fe}.

This problem may be further understood by reference to FIG. 5 wherein an equivalent circuit approximating a transistor as shown in FIGS. 1–3, but not incorporating the emitter webs 23*a–c*, is illustrated. A large area transistor designated generally by the reference 40 represents the ballasted emitter fingers with a small area transistor designated generally by the reference 42 representing the regions opposite the ends of the base contact finger capable of operating with high bias V_{BE}. The emitters of transistors 40 and 42 are connected to a resistance 44, which is representative of the magnitude of the resistances formed by the sheet resistance of the portions 22*a–c* of the diffused emitter regions. The bases and collectors of transistors 40 and 42 are commonly connected. It will thus be understood that the properties of the transistors 40 and 42 primarily depend upon the value of current flowing through the small area transistor 42.

In operation of the transistor described with reference to FIGS. 1–3, and which does include the emitter web portions 23*a–c*, the emitter webs are at the same potential as the adjacent ends of the emitter stripes i.e. the potential at the "active" or emitter stripe ends of the ballast resistors. The emitter spine edge is at a higher potential than that at the "active" ends of the ballast resistors and since the high potential emitter spine edge is essentially screened by the webs 23*a–c*, the current injection from the spine due to the base contact finger ends, and the secondary low gain transistor action from the spine region, are eliminated. The screening action is caused at a normal current level due to the fact that current crowding causes the injected emitter current to be localized at the web edge adjacent the ends of the base contact fingers 17. This injected emitter current effectively forms a recombination barrier that prevents base current from reaching the high potential emitter spine edge. Essentially, a controlled amount of current injection is thus caused immediately adjacent the base contact finger ends, thereby preventing interaction with the higher potential region of the emitter spine contact.

The schematic equivalent circuit of the transistor is then changed from the parallel transistor combination shown in FIG. 5 to the multiemitter single transistor configuration indicated in FIG. 6. Although a resistance 50 of about 5 ohms may be inserted in each emitter contact finger, FIG. 6 indicates that the total resistance in the emitter lead liable to cause degradation of power gain is inversely proportional to the number of emitter stripes incorporated in the transistor.

FIG. 7 is a plot of the active region temperature Tj (as measured at the emitter-base junction) above ambient against DC power dissipation P and illustrates the improved power capacity of a typical transistor embodying the invention. Curve 60 illustrates a capacity approximating 30 watts of DC power over a temperature range of 200° C. above ambient temperature without failure of the transistor. As shown in this graph, this performance is superior to that of various otherwise comparable, conventional unballasted transistors, the limits of operation of which (indicated by instability and hot-spot formation) fall over the indicated range A. This performance is also superior to that of otherwise comparable transistors having aluminum metal resistors each in series with a group of emitters; in the example illustrated, 0.5 ohm resistors in series with 10 emitter contact fingers, wherein the maximum power dissipation at the limits of operation fall over the range B i.e. a maximum power dissipation of about 10 watts.

FIGS. 8–10 illustrate the power gain of typical interdigitated transistors embodying the present invention. FIG. 8 is a plot of output power versus input power and shows the performance spread of a batch of 25 transistors operated at about 400 MHz with a V_{cc} of 28 volts. FIG. 9 is a plot of output power versus input power and shows the performance spread of a batch of 10 transistors operated at about 175 MHz and with a V_{cc} of about 28 volts, while FIG. 10 shows the performance spread of a batch of 12 transistors operated at the same frequency with a V_{cc} of 13 volts. In FIG. 9, the broken line 61 indicates the input and output powers at which a batch otherwise comparable, typical conventional unballasted transistors were subject to catastrophic failure due to thermal instability. In FIGS. 8–10, it may be seen that the best and worst cases of the transistor groups, embodying the invention, are extremely closely spaced, thereby illustrating not only the excellent performance of the present transistors but also the manufacturing reliability possible of the result of this invention.

The improved power dissipation properties of transistors embodying the invention indicate that a large degree of mismatch under operational conditions may be tolerated with impunity.

Although the present invention has been described with reference to specific embodiments thereof, it will be understood that various changes and modifications may become apparent to one skilled in the art, examples of some possible modifications being illustrated in FIGS. 11–14.

FIG. 11 illustrates a transistor having a base region in which are inset two spaced emitter spines 14, each having emitter fingers such as 15*a–c* extending transversely therefrom, the emitter spines extending parallel to one another and being disposed back-to-back. The formation of the emitter contact fingers 21, the discontinuities 22*a–c* and the emitter webs 23*a–c* is identical in each case to that described with reference to FIGS. 1–3. However, both sets of emitter contact fingers 21, are associated with a common emitter contact spine 25.

In FIG. 12, there is shown a modification of the structure of FIGS. 1–3, suitable for use in transistors intended for low-frequency operation. In low-frequency transistors, the sheet resistance of the emitter region, used in accordance with the invention to provide the emitter ballast resistors, may be relatively low and in order to maintain tolerance compatibility, the width of the regions 22 of the emitter stripes 15 is reduced as compared with the width of the remainder of the emitter stripes, in order to provide the required resistance value.

When transistor intended for operation is in the region of the upper limit of high frequency that can be attained at the present state of the art, the emitter region has a high sheet resistance and, again in order to maintain tolerance compatibility, the width of the regions 22 may be increased compared to the width of the remainder of the emitter stripes to obtain the required resistance value, as illustrated in FIG. 13.

Apart from the changes described, the structures of the embodiments illustrated by FIGS. 12 and 13 is the same as that described with reference to FIGS. 1–3 and like references have been used where appropriate.

In all the above described embodiments of the invention, the emitter region of the transistor is comprised of spaced fingers projecting from an emitter spine to form a comblike structure. However, it will be appreciated that other geometries e.g. a rib and spine or star-shaped, also may be employed. Further, it is not an essential feature of the invention that an emitter spine or common portion be employed and embodiments of the invention may be instructed incorporating discrete, spaced emitter regions. One such embodiment is shown in FIG. 14, the laterally spaced emitter fingers 15*a–c* being joined towards one end thereof by transversely extending emitter webs 23*a–c*. At that end of the emitter stripes, an elongated metal contact pad 27 extends parallel to, and spaced from, the emitter webs 23*a–c* over the emitter fingers, making ohmic contact with each of them through apertures 28 in the oxide layer. Alternatively, the contact pad may be on the oxide over the collector region and metal fingers projecting from the contact pad extend over the oxide step at the base-collector junction to contact the emitter fingers through

the apertures **28**. The emitter stripes **15***a–c* have respective contact fingers **21***a–c* which terminate adjacent the emitter webs **23***a–c* so that, as in the previously described embodiments, the sheet resistance of the emitter regions at the discontinuities **22***a–c* form resistances in series between each emitter contact finger and the contact pad **27**. In other respects, the structure of the embodiment shown in FIG. **14** remains unchanged from that described with reference to FIGS. 1–3.

The features of the above described embodiments of the invention may be utilized in the manufacture of discrete devices and also of transistors formed as circuit elements in monolithic and hybrid integrated circuits.

What is claimed is:

1. A planar transistor including a base region of one conductivity type and an emitter region of opposite type inset in the base region, the emitter region comprising a common portion having spaced elongated portions projecting therefrom, a base electrode comprising electrode strips extending between said elongated emitter portions from a common base electrode portion, an emitter electrode system comprising an electrode portion on the said common emitter portion and electrode strips on the respective elongated emitter portions terminating short of the common emitter electrode portion whereby the sheet resistance of the elongated emitter portions not overlaid by said electrode strips provide series resistances between said common emitter electrode portions and said emitter electrode strips, and wherein webs of emitter material extend between and interconnect adjacent elongated emitter portions, the said webs being located between the ends of the base electrode strips and said common emitter portion in the vicinities of the ends of the emitter electrode strips adjacent the common emitter portion.

2. The planar transistor of claim **1**, wherein the emitter region comprises an elongated common spine portion and spaced parallel emitter stripes projecting therefrom.

3. A planar transistor including a base region of one conductivity type and discrete, spaced elongated emitter portions of opposite conductivity type inset in the base region, a base electrode having electrode strips extending between the said emitter portions from a common base contact portion, an emitter electrode system comprising a common portion ohmically connected to each of said emitter portions and emitter electrode strips overlying parts of the respective emitter portions and extending towards but spaced from the said common emitter electrode portion to leave an area of each emitter portion disposed between the electrode strip of that emitter portion and the common emitter electrode portion whereby the emitter electrode strips are effectively electrically connected to the said common emitter electrode portion by series resistances formed by the sheet resistance of the said areas of the emitter portions, and wherein webs of emitter material extend between and interconnect adjacent emitter portions, the said webs being located between the ends of the base electrode strips and the common emitter contact portion in the vicinities of the terminations of the emitter electrode strips at said areas of the emitter portions.

4. the planar transistor of claim **3**, wherein the emitter portions are parallel, spaced elongated portions ohmically interconnected at one end by a transversely extending common emitter electrode portion, wherein said emitter electrode strips extend from the opposite ends of said emitter portions to locations in the vicinity of said webs of emitter material.

5. A transistor device including emitter and base regions with a PN-junction therebetween, said emitter region including a common region from which individual spaced-apart portions project, said spaced-apart portions being disposed in the base region so that portions of the base region are interposed between said individual emitter portions; emitter electrode means ohmically connected to and distributed over said emitter regions, a portion of said electrode means being common to all said individual emitter portions, with discontinuities formed in said electrode means over areas of the said individual emitter portions to form electrical resistances sufficient to stabilize the current density of the device, thereby to prevent localized thermal runaway; and webs of material of said emitter region extending between and joining adjacent ones of said spaced emitter portions for screening said interposed portions of said base region from electrical potential appearing on said common emitter portion, whereby localized current injection is reduced from parts of said emitter region adjacent said common portion of the emitter contact means into said interposed portions of said base region.

6. The transistor device of claim **5**, wherein said webs are disposed adjacent the junctures of said discontinuities and the electrode means overlying said individual emitter portions.

7. The transistor device of claim **5**, wherein said common emitter portion is an elongated spine and said individual emitter portions are outwardly projecting stripes spaced along the length of said spine, said discontinuities being formed in the area of the juncture of said spine and said emitter stripes such that the sheet resistances of portions of said emitter stripes underlying the discontinuities form said electrical resistances.

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