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(71) Applicant: INDIAN INSTITUTE OF TECHNOLOGY

MADRAS (IIT MADRAS) [IN/IN]; The Dean, Industrial Consultancy & Sponsored Research [IC&SR], Indian Institute of Technology Madras, Sardar Patel Road, IIT P.O., Chennai 600036 (IN).

(72) Inventors: SAXENA, Saurabh;

Department of Electrical Engineering, Indian Institute of Technology Madras, IIT P.O., Chennai 600036 (IN). **R, Gautam**; Department of Electrical Engineering, Indian Institute of Technology Madras, IIT P.O., Chennai 600036 (IN). **BANDARUPALI, Jaya Deepthi**; Department of Electrical Engineering, Indian Institute of Technology Madras, IIT P.O., Chennai 600036 (IN).

(74) Agent: RANJNA, Mehta-dutt et al.;

Remfry & Sagar, Attorneys-at-law, Remfry House At The Millenium Plaza, Sector 27, Gurgaon - 122 009, New Delhi Capital Region (IN).

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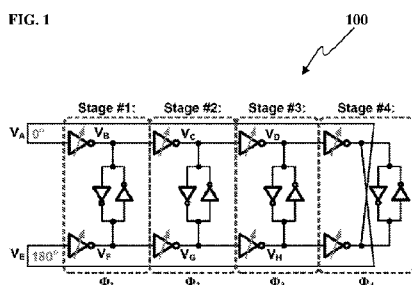
- as to the identity of the inventor (Rule 4.17(i))
- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

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(54) Title: INJECTION LOCKED CLOCK MULTIPLIER WITH EMBEDDED PHASE INTERPOLATOR

FIG. 1



(57) **Abstract:** Injection locked clock multiplier with an embedded phase interpolator and 2X frequency range. A wide range (2X) injection locked clock multiplier (ILCM) with an embedded phase interpolator multiplies a low-frequency clock to generate a high-frequency output wherein the phase is shifted as desired during the clock generation itself. The ILCM retains the low output clock jitter across (340-550fs_{rms}) and a good PI resolution (1.5°-2°) across the phase interpolation range by eliminating the multiphase high-frequency clock distribution during phase interpolation.

DESCRIPTION**INJECTION LOCKED CLOCK MULTIPLIER WITH EMBEDDED
PHASE INTERPOLATOR****TECHNICAL FIELD**

[0001] Embodiments are generally related to analog and digital communication systems and methods. Embodiments are further related to phase interpolators. Embodiments are also related to injection locked clock multipliers with embedded phase interpolators. Embodiments are particularly related to an injection locked clock multiplier with 2X frequency range and resolution (1.5^0 - 2^0) for embedded phase interpolator.

BACKGROUND OF THE INVENTION

[0002] In general, phase interpolators are used to shift the output phase of a clock in a wide range of communication systems including, but not limited to wireline and wireless communication systems. Such phase interpolators require a multiphase clock, such as for example, a four phase ($0^0/90^0/180^0/270^0$) high frequency clock with low jitter and accurate phase-shifting capability. In such conventional systems, phase interpolation can add to the clock jitter and degrade the output clock. The multiphase high-frequency clock distribution requires to have precise matching which adds to the power consumption of the system. Furthermore, it can be beneficial to minimize the power consumption of the clock generator and phase interpolator combined, while eliminating the need for a separate high frequency clock distribution.

[0003] The prior art solutions are unable to provide an effective solution to achieve low jitter and good PI resolution across the wide frequency range. Furthermore, the prior art systems require multiphase high-frequency clock distribution, clock skewing circuit, and fine current/voltage DAC, traditionally required for phase interpolation.

[0004] Based on the foregoing a need therefore exists for a low-jitter ($340\text{-}550f_{\text{S}_{\text{rms}}}$) clock multiplier, and a good PI resolution ($1.5^{\circ}\text{-}2^{\circ}$) across the frequency range without the need of multiphase high-frequency clock distribution, clock skewing circuit, and fine current/voltage DAC for phase interpolation. Also, a need exists for a clock multiplier with wide frequency range ($2X$ frequency) and resolution ($1.5^{\circ}\text{-}2^{\circ}$) for embedded phase interpolator, as discussed in greater detail herein.

SUMMARY OF THE INVENTION

[0005] The following summary is provided to facilitate a clear understanding of the new features in the disclosed embodiment, and it is not intended to be a full, detailed description. A detailed description of all the aspects of the disclosed invention can be understood by reviewing the full specification, the drawing and the claims and the abstract, as a whole.

[0006] One objective of the present invention is to provide an injection locked clock multiplier with an embedded phase interpolator to achieve a low jitter ($340\text{-}550f_{\text{S}_{\text{rms}}}$) and a good PI resolution ($1.5^{\circ}\text{-}2^{\circ}$) across the frequency range without

the need of multiphase high-frequency clock distribution, clock skewing circuit, and fine current/voltage DAC for phase interpolation.

[0007] Further objective of the present invention is to provide an injection locked clock multiplier with $2X$ frequency range and 1.5° - 2° phase resolution for the embedded phase interpolator across the $2X$ frequency range.

[0008] The aforementioned aspects along with the objectives and the advantages can be achieved as described herein. An injection locked clock multiplier with $2X$ frequency range and 1.5° - 2° phase resolution for the embedded phase interpolator, is disclosed herein. A wide range ($2X$) injection locked clock multiplier (ILCM) with an embedded phase interpolator (PI) multiplies a low-frequency clock to generate a high-frequency output wherein the phase is shifted as desired during the clock generation itself. The ILCM retains the low output clock jitter across $2X$ frequency range (340 - $550f_{s_{rms}}$) and a good PI resolution (1.5° - 2°) across the phase interpolation range while eliminating the multiphase high-frequency clock distribution during phase interpolation.

[0009] The ILCM-cum-PI disclosed herein realizes an intermediate output clock phase by digitally controlling delays for signals already present in a multiphase ring oscillator. The clock signals are manipulated in time-domain rather than voltage or current domain during phase interpolation. The proposed ILCM-cum-PI's output phase does not depend on the shape of the analog multiphase clock signals such as, sinusoidal, triangular, square wave, etc., otherwise used during summing with a different voltage or current weights.

Furthermore, the proposed ILCM-cum-PI does not need multiphase high-frequency clock distribution for phase interpolation, thereby saving power in high-frequency clock distribution and matching between multiple clock phases. The proposed ILCM-cum-PI's output phase is not restricted by the number of delay cells used to realize the ring oscillator wherein the ILCM-cum-PI has a linear change in the output phase with respect to the input digital control as delays or phases are directly manipulated. Unlike conventional phase interpolators, the random jitter is independent of the input code or number of stages.

[0010] In one embodiment of the proposed invention, the embedded phase interpolator interpolates clock phases within a ring oscillator (e.g., of a four-stage pseudo-differential ring oscillator (RO)) to generate intermediate clock phases. The four-stage pseudo-differential ring oscillator (RO) can be locked to the N^{th} harmonic of the reference frequency f_{ref} (i.e., $f_o = 1/T_{CCO} = Nf_{ref}$) wherein the total delay and phase across the four stages are $1/2f_o$ and 180° respectively for sustained oscillations. At the output of Stage-2, the output phase ϕ_{OUT} is

$$\phi_{OUT} = \phi_1 + \phi_2 = 180^\circ - \phi_3 - \phi_4$$

[0011] Where ϕ_1 , ϕ_2 , ϕ_3 , and ϕ_4 are phases added by the four stages, respectively. The change in the output phase ($\Delta\phi_{OUT}$) can be:

$$\Delta\phi_{OUT} = \Delta\phi_1 + \Delta\phi_2 = -\Delta\phi_3 - \Delta\phi_4.$$

[0012] A variation in the output phase is realized by varying delays of the four stages in a complimentary manner satisfying the below relation:

$$\Delta\phi_{OUT} = \frac{2\pi}{T_{CCO}}(\Delta t_{d1} + \Delta t_{d2}) = -\frac{2\pi}{T_{CCO}}(\Delta t_{d3} + \Delta t_{d4})$$

[0013] The tunable capacitor banks implement a variable delay in each stage, thereby producing a phase shift. At ϕ_{OUT} , a $\pm 22.5^\circ$ phase shift with 5-bit (PI_{LSB}) resolution is implemented by varying the phase contributions of the four delay stages. The tapped output nodes are varied from one stage to the other, and a $\pm 22.5^\circ$ phase shift can be realized at each tapped output. Shifting between different output stages is implemented so that the final output phase spans 0-360° with respect to a fixed output clock. The proposed phase interpolator implements a 45° phase shift at its output by locking the ring oscillator with a 45° phase-shifted reference clock, injecting the ring oscillator and tapping the ring oscillator at 45° phase-shifted nodes.

BRIEF DESCRIPTION OF DRAWINGS

[0014] The drawings shown here are for illustration purpose and the actual system will not be limited by the size, shape, and arrangement of components or number of components represented in the drawings.

[0015] FIG. 1 illustrates a block diagram (100) of a pseudo-differential ring oscillator (RO) implemented with an embedded phase interpolator for interpolating clock phases within the ring oscillator (RO) to generate intermediate clock phases, in accordance with the disclosed embodiments;

[0016] FIG. 2 illustrates a block diagram (200) of the ILCM with embedded phase interpolator (PI) with frequency range (2X frequency) and resolution (1.5° - 2°), in accordance with the disclosed embodiments;

[0017] FIG. 3 illustrates a timing diagram (300) of a single wave form for coarse phase step at its output, in accordance with the disclosed embodiments;

[0018] FIG. 4 illustrates a timing diagram (400) of a single waveform for a fine phase step at its output, in accordance with the disclosed embodiments.

[0019] FIG. 5 illustrates an operational block diagram (500) of the ILCM-cum-PI with tunable oscillator stages to embed the phase interpolation with a resolution (1.5° - 2°) across 2X frequency range, in accordance with the disclosed embodiments.

DETAILED DESCRIPTION

[0020] The principles of operation, design configurations and evaluation values in these non-limiting examples can be varied and are merely cited to illustrate at least one embodiment of the invention, without limiting the scope thereof.

[0021] The embodiments will be described in detail with corresponding marked references to the drawings, in which the illustrative components of the invention are outlined. The embodiments disclosed herein can be expressed in different forms and should not be considered as limited to the listed embodiments in the disclosed invention. The various embodiments outlined in the subsequent sections are construed such that it provides a complete and a thorough

understanding of the disclosed invention, by clearly describing the scope of the invention, for those skilled in the art.

[0022] An injection locked clock multiplier with 2X frequency range and 1.5° - 2° resolution for the embedded phase interpolator, is disclosed herein. A wide range (2X) injection locked clock multiplier (ILCM) with an embedded phase interpolator multiplies a low-frequency clock to generate a high-frequency output wherein the phase is shifted as desired during the clock generation itself. The ILCM retains the low output clock jitter across (340-550fs_{rms}) and a good PI resolution (1.5° - 2°) across the phase interpolation range by eliminating the multiphase high-frequency clock distribution during phase interpolation.

[0023] The ILCM-cum-PI disclosed herein realizes an intermediate output clock phase by digitally controlling delays for signals already present in a multiphase ring oscillator. The clock signals are manipulated in time-domain rather than voltage or current domain during phase interpolation. The proposed ILCM-cum-PI's output phase does not depend on the shape of the analog multiphase clock signals such as, sinusoidal, triangular, square wave, etc., otherwise used during summing with a different voltage or current weights. Furthermore, the proposed ILCM-cum-PI does not need multiphase high-frequency clock distribution for phase interpolation, thereby saving power in high-frequency clock distribution and matching between multiple clock phases. The proposed ILCM-cum-PI's output phase is not restricted by the number of delay cells used to realize the ring oscillator wherein the ILCM-cum-PI has a

linear change in the output phase with respect to the input digital control as delays or phases are directly manipulated. Unlike conventional phase interpolators, the random-jitter is independent of the input code or number of stages.

[0024] In one embodiment of the proposed invention, the embedded phase interpolator interpolates clock phases within a ring oscillator (e.g., of a four-stage pseudo-differential ring oscillator (RO)) to generate intermediate clock phases. FIG. 1 illustrates a block diagram (100) of a pseudo-differential ring oscillator (RO) (exemplary embodiment) implemented with an embedded phase interpolator for interpolating clock phases within the ring oscillator (RO) to generate intermediate clock phases, in accordance with the disclosed embodiments. The four-stage pseudo-differential ring oscillator (RO) can be locked to the N^{th} harmonic of the reference frequency (i.e., $f_o = 1/T_{CCO} = Nf_{ref}$) wherein the total delay and phase across the four stages are $1/2f_o$ and 180° respectively for sustained oscillations. At the output of Stage-2, the output phase ϕ_{OUT} can be:

$$\phi_{OUT} = \phi_1 + \phi_2 = 180^\circ - \phi_3 - \phi_4$$

[0025] Where ϕ_1 , ϕ_2 , ϕ_3 , and ϕ_4 are phases added by the four stages, respectively. The change in the output phase ($\Delta\phi_{OUT}$) can be:

$$\Delta\phi_{OUT} = \Delta\phi_1 + \Delta\phi_2 = -\Delta\phi_3 - \Delta\phi_4.$$

[0026] A variation in the output phase is realized by varying delays of the four stages in a complimentary manner satisfying the below relation:

$$\Delta\phi_{OUT} = \frac{2\pi}{T_{CCO}}(\Delta t_{d1} + \Delta t_{d2}) = -\frac{2\pi}{T_{CCO}}(\Delta t_{d3} + \Delta t_{d4})$$

[0027] The tunable capacitor banks implement a variable delay in each stage, thereby producing a phase shift. At ϕ_{OUT} , a $\pm 22.5^\circ$ phase shift with 5-bit (PI_{LSB}) resolution is implemented by varying the phase contributions of the four delay stages. The tapped output nodes are varied from one stage to the other, and a $\pm 22.5^\circ$ phase shift can be realized at each tapped output. Shifting between different output stages is implemented so that the final output phase spans $0-360^\circ$ with respect to a fixed output clock. The proposed phase interpolator implements a 45° phase shift at its output by locking the ring oscillator with a 45° phase-shifted reference clock, injecting the ring oscillator and tapping the ring oscillator at 45° phase-shifted nodes.

[0028] FIG. 2 illustrates a block diagram (200) of the ILCM with embedded phase interpolator (PI) with 2X frequency range and $1.5^\circ-2^\circ$ resolution, in accordance with the disclosed embodiments. FIG. 2 illustrates a block diagram (200) of the proposed 2.5-5.0GHz ILCM with an embedded phase interpolator consisting of a pseudo-differential current-controlled ring oscillator (RCCO), a NAND-based programmable injection pulse generation circuit, a digital-to-time converter (DTC), a 1:4 DMUX, an 8:1 differential MUX, and digitally controlled current-DACs (IDACs).

[0029] An IDAC with Coarse control is used to bring the ring oscillator within ± 400 ppm of the center frequency (2.5-5.0GHz). The reference clock REF is

delayed by the DTC and combined by the pulse generating logic to produce a short pulse for injecting in the ring oscillator. The output phase, Φ_{OUT} , is controlled in two steps by phase interpolation codes, PI_{MSB} and PI_{LSB} .

[0030] A 3-bit PI_{MSB} controls DTC's delay in steps of $T_{CCO}/8$, changes node of injection in the oscillator through 1:4 DMUX, and taps the desired clock output phase with 8:1 MUX. It results in a coarse change in phase by 45° at the output. A 5-bit PI_{LSB} regulates the delay of different delay cells used to realize the oscillator, thereby changing the output phase in 1.5° steps. During the output phase change by varying the delay of RCCO's delay cells, the oscillator is maintained to oscillate at the desired frequency. Any frequency perturbations at the output due to change in PI_{LSB} is compensated by current I_{fine1} .

[0031] FIG. 3 illustrates a timing diagram (300) of a single wave form for coarse phase step at its output, in accordance with the disclosed embodiments. FIG. 3 illustrates the change in control codes and output phase shifts where a coarse 45° phase step with phase selection in the ring oscillator is realized.

[0032] FIG. 4 illustrates a timing diagram (400) of a single waveform for fine phase step at its output, in accordance with the disclosed embodiments. FIG. 4 illustrates the change in control codes and output phase shifts where a fine 1.5° - 2° phase step is realised with 5-bit capacitor bank in each stage of the ring oscillator.

[0033] The proposed phase interpolator realizes the output phase at different frequencies by tuning the ring oscillator for the desired output frequencies. The

DTC gives the required delay in the reference clock path for injection. Hence, an output phase with less than 2° resolution is realized across a wide range of frequencies.

[0034] FIG. 5 illustrates an operational block diagram (500) of the ILCM-cum-PI with tunable oscillator stages to embed the phase interpolation in accordance with the disclosed embodiments. The delay setting in the digital-to-time converter (DTC) controls the delay of the injected pulse according to the node of injection. The capacitor banks in the oscillator stages are adjusted to embed the phase interpolation in the oscillator. For each node of injection, a $\pm 22.5^\circ$ phase shift or $\pm T_{CCO}/16$ delay is implemented at output node with 1.5° - 2° phase step resolution.

[0035] The different output phases at frequency f_o are realized digitally in two steps: The digital control bits PI_{MSB} are used to change the injection node in the ring oscillator and select the desired output phase using an 8:1 MUX. Hence, a coarse phase-step with 45° phase resolution is realized. Depending on the desired output phase ($n \times 45^\circ$), the delay of the pulse used for injection in the oscillator is varied by using a DTC. The latter provides $p/8f_o$ delay where $p \in \{0, 1, 2, 3\}$. A fine phase step with a 5-bit resolution around each coarse phase step is generated by digitally controlling each stage's delay within the four-stage ring oscillator. A 5-bit capacitor bank controls the delay of each stage at its output. The delays for different RO's stages have to be complimentary to retain the clock period.

[0036] It will be appreciated that variations of the above-disclosed and other features and functions, or alternatives thereof, may be desirably combined into

many other different systems or applications. Also, that various presently unforeseen or unanticipated alternatives, modifications, variations or improvements therein may be subsequently made by those skilled in the art which are also intended to be encompassed by the following claims.

CLAIMS:**I/We claim:**

1. An injection locked clock multiplier with embedded phase interpolator, comprising:

a wide range (2X) injection locked clock multiplier (ILCM) with an embedded phase interpolator (PI) multiplies a low-frequency clock to generate a high-frequency output wherein the phase is shifted as desired during the clock generation itself with 2X frequency range and 1.5° - 2° resolution.
2. The clock multiplier as claimed in claim 1 wherein the injection locked clock multiplier with embedded phase interpolator retains the low output clock jitter across $(340-550f_{s_{rms}})$ and a good PI resolution (1.5° - 2°) across the phase interpolation range by eliminating the multiphase high-frequency clock distribution during phase interpolation.
3. The clock multiplier as claimed in claim 1 wherein the ILCM-cum-PI realizes an intermediate output clock phase by digitally controlling delays for signals already present in a multiphase ring oscillator.
4. The clock multiplier as claimed in claim 1 wherein the clock signals are manipulated in time-domain.
5. The clock multiplier as claimed in claim 1 wherein the ILCM-cum-PI's output phase does not depend on the shape of the analog multiphase clock

signals otherwise used during summing with a different voltage or current weights.

6. The clock multiplier as claimed in claim 1 wherein the output phase of the ILCM-cum-PI has a linear change in the output phase with respect to the input digital control as delays or phases are directly manipulated and is not restricted by the number of delay cells used to realize the ring oscillator wherein the ILCM-cum-PI.

DRAWINGS

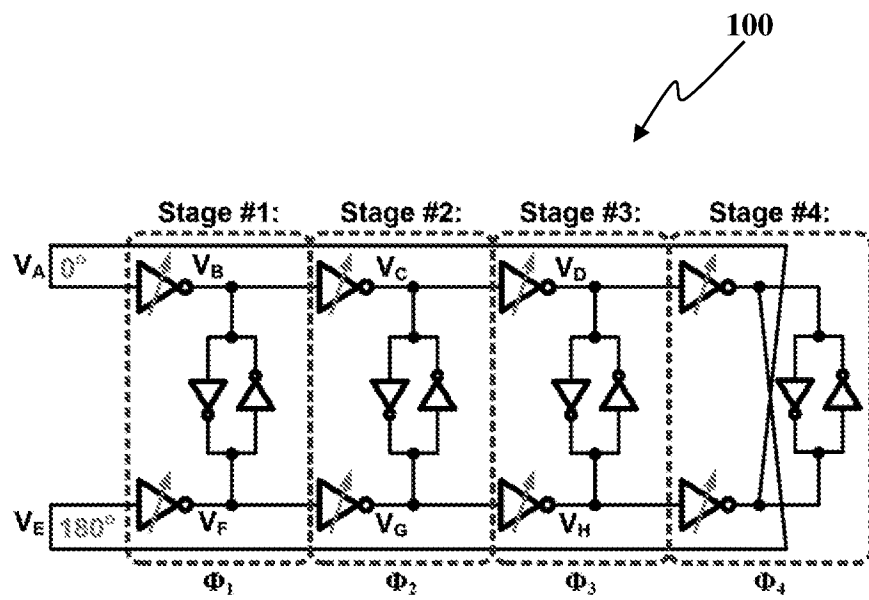


FIG. 1

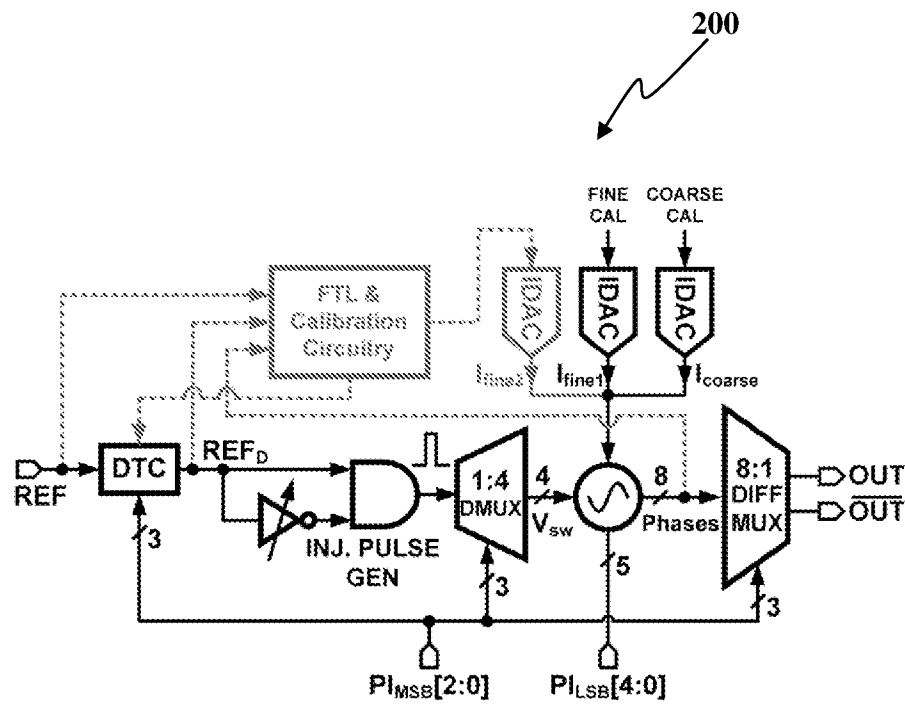


FIG. 2

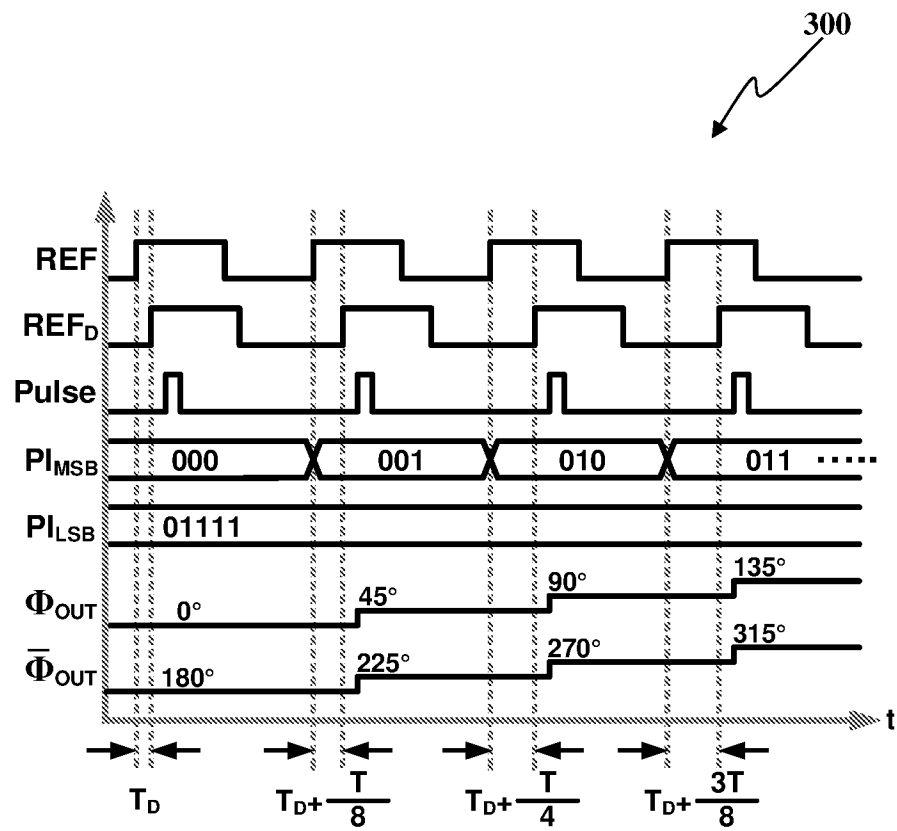


FIG. 3

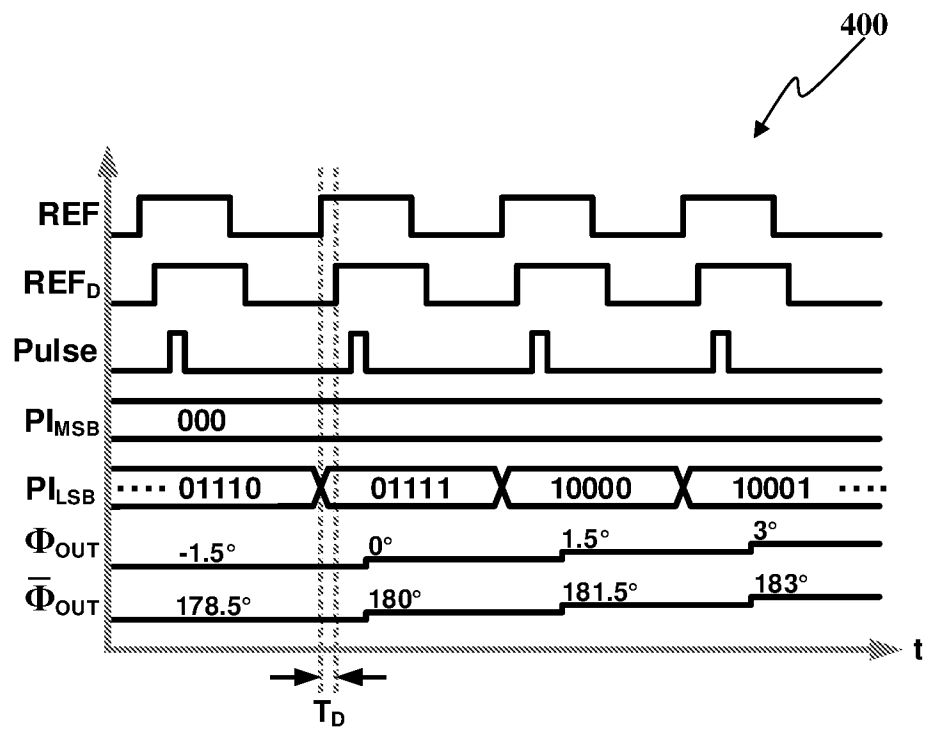


FIG. 4

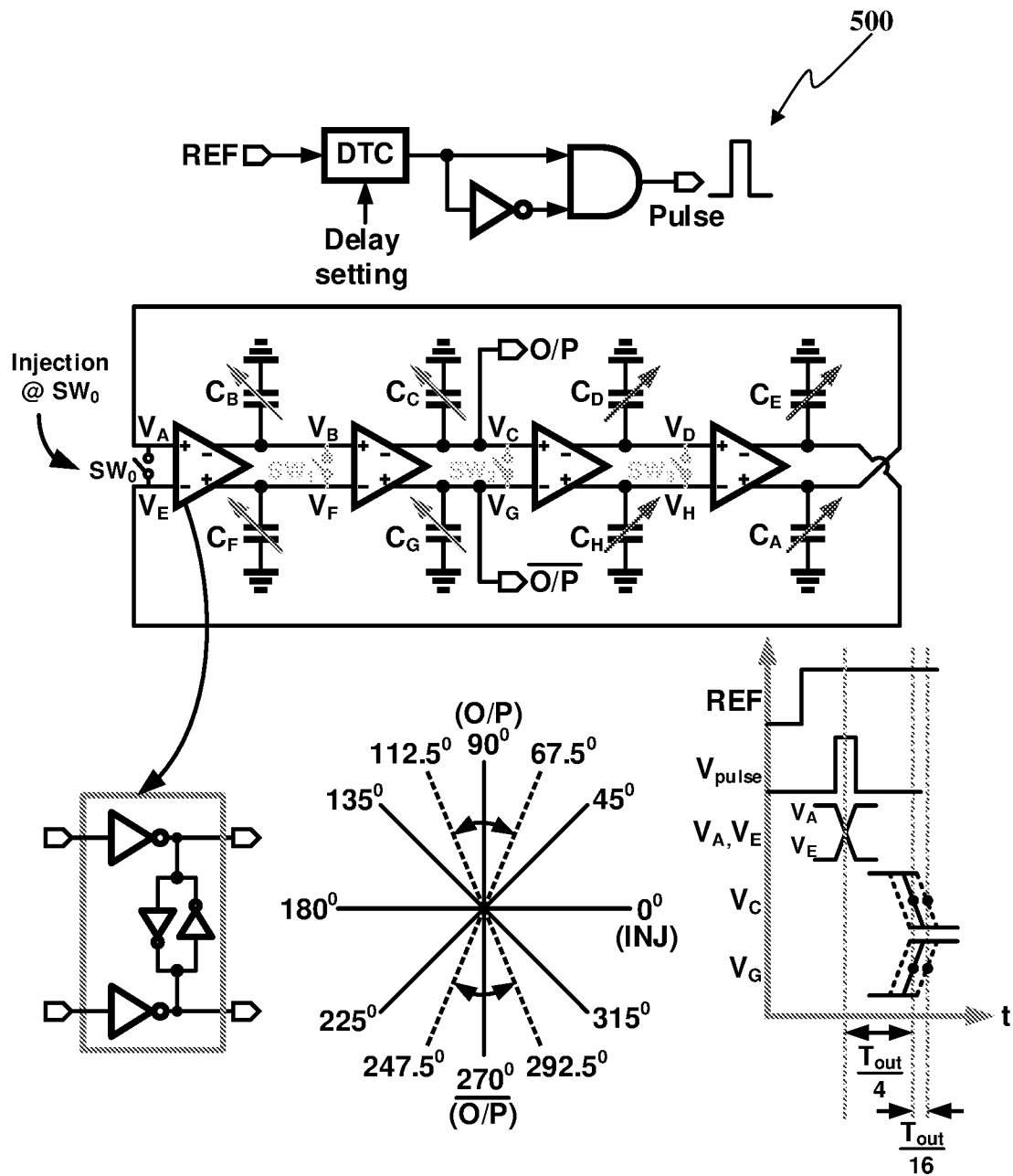


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER
H03L7/24, H03L7/083 Version=2022.01

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases - PatSeer, IPO Internal Database.

Searched Keywords - Phase Interpolator, Frequency Multiplier, Oscillator

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 20020113660 A1 (VELIO COMMUNICATIONS, INC), 22-08-2002 (22 August, 2002) Whole Document	1-6
Y	US 20100201418 A1 (PMC-SIERRA, INC.), 12-08-2010 (12 August, 2010). Whole Document	1-6
O	GAUTAM R. et. al, "A 2.5-5GHz Injection-Locked Clock Multiplier with Embedded Phase Interpolator in 65nm CMOS," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, pp. 1-5, doi: 10.1109/ISCAS45731.2020.9180829. 12-10-2020 (12 October, 2020) Whole Document	1-6

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Authorized officer

Gaurav Kumar Tomar

Telephone No. +91-1125300200