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 08106036.0 24 December 2008 (24.12.2008) EP</p> <p>(71) Applicant (<i>for all designated States except US</i>): NXP B.V. [NL/NL]; High Tech Campus 60, NL-5656 AG Eindhoven (NL).</p> <p>(72) Inventor; and</p> <p>(75) Inventor/Applicant (<i>for US only</i>): MEIJER, Rinze Ida Mechtildis Peter [NL/NL]; c/o NXP B.V., Intellectual Property & Licensing Department, High Tech Campus 32, NL-5656 AE Eindhoven (NL).</p> | <p>(74) Agents: KROTT, Michel Willy François Maria et al.; c/o NXP B.V, Intellectual Property & Licensing Department, High Tech Campus 32, NL-5656 AE Eindhoven (NL).</p> <p>(81) Designated States (<i>unless otherwise indicated, for every kind of national protection available</i>): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.</p> <p>(84) Designated States (<i>unless otherwise indicated, for every kind of regional protection available</i>): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,</p> |
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(54) Title: INTEGRATED CIRCUIT

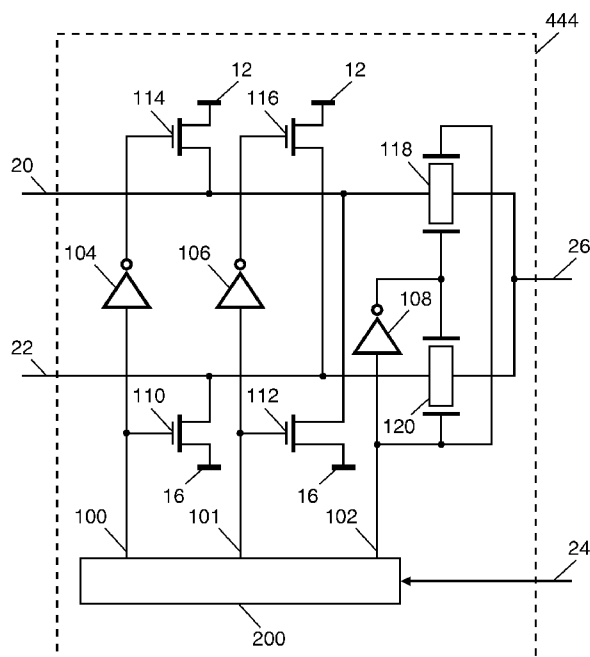


FIG. 5

(57) Abstract: A controller for controlling the body bias voltages in an integrated circuit, wherein the controller: receives a mode input; receives a reference voltage; outputs a first body bias voltage; and outputs a second body bias voltage. The first body bias voltage and the second body bias voltage may be dependent on the mode input and the reference voltage. The controller may comprise an arrangement of switches, each switch controlled by the mode input.



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DESCRIPTION

INTEGRATED CIRCUIT

The present invention relates to integrated circuits. The present invention is particularly suited to, but not limited to, low-power, low-voltage integrated circuits.

5

It is known to reduce active power consumption in integrated circuits by lowering V_{DD} . However, a disadvantage of reduced V_{DD} operation is that the circuit performance is degraded, because the reduced transistor switching speeds.

10

Transistor body biasing can effectively reduce the leakage power of the design (in the case of reverse body bias), or improve the circuit's performance (in the case of forward body bias). It is most effective when it is used in conjunction with V_{DD} scaling. A circuit's performance can be improved for a given power target through body bias (BB) control

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A number of BB controllers have been proposed. The majority of the published BB controllers require the generation and distribution of separate body bias voltage levels using global and local analog bias generation circuitry with external components.

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Nose, K., M. Hirabayashi, H. Kawaguchi, S. Lee and T. Sakurai " V_{TH} -Hopping Scheme to Reduce Subthreshold Leakage for Low-Power Processors" IEEE Journal of Solid-State Circuits, Vol.37, No.3, March 2002, p.413-419 discloses a scheme in which the body bias is dynamically controlled through software depending on the workload of a processor. This technique requires special externally generated BB voltages to which the transistors can be connected. However, only two BB voltages are supported.

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Ananthan, H., H. Kim, and K. Roy “*Larger-than-V_{DD} Forward Body Bias in Sub-0.5V Nanoscale CMOS*”, Proc. of ISLPED, August 2004, p.8-10 discloses scheme where V_{DD} is expected to scale below 0.5V [2]. The limitation of this technique is that it becomes energy-inefficient for V_{DD} 's higher than 0.6V due to the junction leakage. Therefore, it can only offer a good solution for low-voltage circuits. Furthermore, the scheme always enables FBB in active mode to achieve higher performance, and uses normal BB in standby mode to reduce leakage. This may not be a good choice if the higher performance is not required.

US 2005/0213370 A1 describes a means to provide forward body bias voltage to SRAM cell PMOS load transistors to improve cell read margin stability.

The present inventors have realised it would be desirable to provide a circuit with improved power-performance operation suitable for reduced supply voltage operation.

The present inventors have realised it would be desirable to provide a more efficient body bias controller offering plural distinct forward body-bias voltages.

The present inventors have realised it would be desirable for there to be no need for an active component for body bias control.

In a first aspect, the present invention provides a controller for controlling the body bias voltages in an integrated circuit, wherein the controller receives a mode input, receives a reference voltage, outputs a first body bias voltage, and outputs a second body bias voltage.

The first body bias voltage and the second body bias voltage may be dependent on the mode input and the reference voltage.

The controller may comprise an arrangement of switches, each switch controlled by the mode input.

The first body bias voltage may set an N-type transistor of the integrated circuit and the second body bias voltage may set a P-type transistor of the integrated circuit.

5 The mode input may be a mode signal indicative of an operating mode of the controller.

The reference voltage may set the first body bias voltage and the reference voltage may set the second body bias voltage.

The controller may be incorporated onto an integrated circuit chip.

The controller may be incorporated into an integrated circuit.

10 The integrated circuit may further comprise a power mode controller, a reference voltage generator, and a CMOS circuit; wherein the power mode controller generates the mode input, the reference voltage generator generates the reference voltage and the CMOS circuit receives the first body bias voltage and the second body bias voltage.

15 In a further aspect, the present invention provides a method of controlling the body bias voltages in an integrated circuit, the method comprising the steps of receiving a mode input, receiving a reference voltage, outputting a first body bias voltage and outputting a second body bias voltage.

20 The first body bias voltage and the second body bias voltage may be dependent on the mode input and the reference voltage.

The method may further comprise the steps of setting an N-type transistor of the integrated circuit based on the first body bias voltage and setting a P-type transistor of the integrated circuit based on the second body bias voltage.

25 The mode input may be a mode signal indicative of an operating mode of the controller.

The method may further comprise the steps setting the first body bias voltage based on the reference voltage and setting the second body bias voltage based on the reference voltage.

30 The controller may be incorporated onto a single chip.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic illustration of a circuit according to a first
5 embodiment of the present invention;

Figure 2 is a schematic illustration of the reference voltage generator of the circuit of Figure 1;

Figure 3 is a schematic illustration of the well controller of the circuit of Figure 1;

10 Figure 4 is a schematic illustration of an alternative embodiment of the well controller of the circuit of Figure 1; and

Figure 5 is a schematic illustration of a further alternative embodiment of the well controller of the circuit of Figure 1.

15

Figure 1 is a schematic illustration (not to scale) of an integrated circuit 1 according to a first embodiment of the present invention. The integrated
20 circuit 1 comprises a CMOS circuit 2, a well controller 4, a power mode controller 6 and a reference voltage generator 8.

The CMOS circuit 2 receives a first supply voltage 10. The CMOS circuit 2 receives a NWEELL voltage 20 and a PWEELL voltage 22. The CMOS circuit 2 outputs a first source voltage 14. The CMOS circuit 2 contains the
25 circuit parts for which the well bias is controlled. The CMOS circuit 2 contains digital circuits. The CMOS circuit is implemented in a triple-well chip technology. This allows the adaptation of both NWEELL and PWEELL voltages in which PMOS and NMOS transistors are laid out, respectively.

The NWEELL voltage 20 and a PWEELL voltage 22 are output from the
30 well controller.

The (single) well controller 4 is incorporated onto a single chip. The well controller 4 receives a second supply voltage 12. The well controller 4

receives a power mode signal 24. The well controller 4 receives a reference voltage 26. The well controller 4 outputs a second source voltage 16. The well controller sets selected well bias voltages at the NWELL voltage 20 and PWELL voltage 22 for the CMOS circuit 2. The applied well bias voltages
5 depend on the power mode signal 24 and the reference voltage 26.

The power mode signal 24 is output from the power mode controller 6.

The reference voltage 26 is output from the reference voltage generator
8.

The power mode controller 6 provides the operating mode of the well
10 controller 4 via the power mode signal 24. The power mode controller 6 is a digital synthesized circuit. The power mode controller 6 provides functionality to reprogram the operation modes depending on the needs of the user or software.

The reference voltage generator 8 is implemented centrally. The
15 reference voltage generator 8 is a circuit component that provides a given reference voltage 26. The reference voltage 26 equals the mid supply voltage level.

Figure 2 is a schematic illustration of the reference voltage generator 8
of Figure 1. The reference voltage generator 8 comprises a first resistor 32
20 and a second resistor 34. A first terminal of the first resistor 32 receives a third supply voltage 30. A second terminal of the first resistor 32 is connected to a first terminal of the second resistor 34. A second terminal of the second resistor 34 outputs a third source voltage 36. The reference voltage 26 is output from the second terminal of the first resistor 32.

25 The reference voltage generator 8 can be easily implemented on a chip. The reference voltage 26 is determined from the ratio between the resistances of the first resistor 32 and the second resistor 34. The first resistor 32 and the second resistor 34 have the same resistance. The third supply voltage is 0.8V. The reference voltage 26 is 0.4V.

30 Figure 3 is a schematic illustration of the well controller 4. The well controller receives a second supply voltage 12. The second supply voltage 12 is 0.8V.

The well controller 4 comprises a first switch 40, a second switch 42, a third switch 44 and a fourth switch 46. The switches 40, 42, 44, 46 are controlled by the power mode signal 24 to provide the desired well potentials 20, 22. An advantage of the well controller 4 over, for example, an operational amplifier, is that the well controller 4 does not need an active component to provide a well bias.

When the first switch 40 and the fourth switch 46 are set to a conducting position, the nominal well potentials are provided to the CMOS circuit 2. This operating mode (called the NORMAL mode) enables the nominal operation, i.e. a nominal well bias. The second switch 42 and the third switch 44 connect the reference voltage 26 as forward body-bias voltage to both PWELL 22 and NWELL 20 voltages. This operating mode (called the BOOST mode) boosts the circuit performance by providing forward body biasing to both the NWELL voltage 20 and the PWELL voltage 22.

An advantage of the above described integrated circuit 1 is that when providing a forward bias of the reference voltage 26 to both wells 20, 22 the reference voltage generator 8 does not need to provide the static well currents associated to the well bias applied. This eliminates the need for an active circuit component to be used to provide the well bias.

A further advantage is the fact that it eliminates latch-up which could take place when well bias is adapted in an improper way. For the BOOST mode, the NWELL voltage 20 and the PWELL voltage 22 are virtually shorted. Therefore the existing parasitic thyristor structure in the CMOS circuit 2 which may cause latch-up cannot become conductive. In prior art solutions, for supply voltages higher than 0.6V a latch-up state can be a possibility depending on the layout implementation of the design. Also, for the other two operating modes (NORMAL and MAXBOOST) latch-up due to well biasing cannot happen. This is because the applied well voltage is constrained to be less than the diode voltage. We conclude that the proposed approach is reliable and enables robust circuit operation.

An advantage of the above described circuit 1 is that it effects improved power-performance operation suitable for reduced supply voltage operation over previous systems.

5 A further advantage of the above described system is that it offers a more efficient body bias controller design offering a few distinct forward body-bias voltages.

The above described integrated circuit tends to be latch-up immune over the full supply voltage range.

10 The above described integrated circuit can operate at medium supply voltages.

The above described integrated circuit can be fully integrated on-chip.

The above described integrated circuit is modular.

The above described integrated circuit is fully scalable.

15 The above described integrated circuit constrains circuit over-dimensioning when utilizing performance boost for design area.

The above described integrated circuit increases circuit autonomy due to lower-power operation.

With the above described integrated circuit, full integration is possible; no external components are needed.

20 The well controller 4 can be implemented as a single IP next to the CMOS Circuit 2 for which the wells 20, 22 are controlled. Another implementation is to place the well controller 4 within the standard-cell rows, or at the edge of a standard-cell block. For this approach, it makes most sense to lay out the well controller 4 in a standard-cell fashion. Thus, a centralized well controller 4 and a distributed well controller 4 are possible.

25 In the above embodiment, the single well controller 4 is incorporated on a single chip. However, for example in multiple power domain chips, multiple well controllers can be used within the same chip. Each of those well controllers may be independently controlled by the power mode controller 6. In that way, one can further optimize the power-performance of individual chip parts, e.g. power domains or part of a power domain.

In the above embodiment, the reference voltage generator 8 is implemented centrally. However, in other embodiments, the reference voltage generator can be implemented differently, for example, in the case where multiple well controllers are used, reference voltages can be locally generated for each well controller.

In the above embodiment, the CMOS circuit 2 contains digital circuits. However, in other embodiments the CMOS circuit may contain other appropriate circuits, for example analog or mixed-signal circuits.

In the above embodiment, the CMOS circuit 2 is implemented in a triple-well chip technology. However, in other embodiments the CMOS circuit may be implemented using other alternative technologies, for example, twin-well chip technology. However, the use of twin-well chip technology means that only the NWell voltage 20 can be adapted.

In the above embodiment, the reference voltage generator 8 uses a resistive divider circuit for generating a reference voltage 26. However, in other embodiments different suitable methods may be used for generating a reference voltage.

In the above embodiment, the third supply voltage 30 of the reference voltage generator 8 is 0.8V. However, in other embodiments, the third supply voltage 30 may be a different suitable voltage.

In the above embodiment, the first resistor 32 and the second resistor 34 of the reference voltage generator 8 have the same resistance. However, in other embodiments the resistances of the first resistor 32 and the second resistor 34 may be different.

In the above embodiment, the reference voltage 26 supplied by the reference voltage generator 8 is 0.4V. However, in other embodiments the reference voltage may be a different suitable voltage. Different reference voltages may be used, for example, to help compensate the impact of unbalanced process corners, such as slowN-fastP and fastN-slowP corners. For example, in a different embodiment, the reference voltage 26 could be 0.2V. This could compensate a fastN-slowP process since the PWell voltage 22 is forward biased by 0.2V while the NWell voltage 20 is forward biased by

0.6V. This means that the PMOS transistors are made relatively faster than the NMOS transistors.

In the above embodiment the well controller 4 is supplied with a second supply voltage 12 of 0.8V. However, in other embodiments the second supply
5 12 voltage is a different alternative voltages, for example, the second supply 12 voltage is between 0.4V and 1.1V.

In the above embodiment the well controller 4 is provided by the system shown in Figure 3. However, in other embodiments, the well controller 4 may be provided by other appropriate systems.

10 For example, Figure 4 is a schematic illustration of an alternative embodiment 440 of the well controller 4. The same reference numerals as in Figure 3 have been used to identify the same elements. In addition to the common elements of Figure 3, the alternative well controller 440 comprises a fifth switch 50 and a sixth switch 52 which are controlled by the power mode
15 signal 24. The fifth switch 50 and the sixth switch 52 enable the connection of the PWELL 22 to the second supply voltage 12 and the NWELL 20 to second drain voltage 16. This increases the amount of forward BB applied. This operating mode (called the MAXBOOST mode) offers the same functionality as the 'Digital Body Biasing' as described in Ananthan, H., H. Kim, and K. Roy
20 "*Larger-than-Vdd Forward Body Bias in Sub-0.5V Nanoscale CMOS*", Proc. of ISLPED, August 2004, p.8-10. This mode makes most sense for low supply voltage points to constrain diode leakage of the forward-biased junctions. Typically, this means that the mode make only sense when used with supply voltages equal or lower than 0.6V.

25 Figure 5 is a schematic illustration of a further alternative embodiment 444 of the well controller 4. The same reference numerals as in Figure 3 have been used to identify the same elements. In addition to the common elements of Figure 3, the further alternative well controller 444 comprises a first inverter 104, a second inverter 106, a third inverter 108, a first pass-transistor switch 110, a second pass-transistor switch 112, a third pass-transistor switch 114, a
30 fourth pass-transistor switch 116, a first register 118, a second register 120 and a reference voltage receiver 200. The switch-matrix of the well controller 4

has been implemented using pass-transistor switches 110, 112, 114, 116. The inverters 104, 106, 108 and the registers 118, 120 are used to generate the switch control signals. The registers 118, 120 are optional. The further alternative well controller 444 comprises switch control lines 100, 101, 102.

5 The switch control lines 100, 101, 102 can also be routed as separate input pins, or alternatively, they can be provided from a 2input-to-3output decoder circuit.

The body bias generation of the above described integrated circuit derives a body bias value as referenced to the local V_{DD} and V_{SS} supplies.

10 Thus, the applied body bias value is always constant and independent of supply voltage variations or supply voltage settings.

The above described integrated circuit is compatible with any power supply scaling approach that is used to control power consumption and performance of the circuit part.

15 The above described integrated circuit controls the body bias voltages of PMOS and NMOS transistors within the circuit part.

The above described integrated circuit can select the PWELL and NWELL (body bias) voltages to be exactly the same. The PWELL and NWELL voltages can be provided through one shared body bias network which gives
20 lower area costs.

The control function of the above described integrated circuit can be integrated on-chip, and not done by external control. This enhances the modularity and enables dynamic power management.

It will be appreciated that, in the above embodiments, a circuit with a
25 capability for improved energy-efficient operation has been provided. This improved energy-efficient operation has been provided by the use of smart well bias control to boost circuit performance. A simple and low-cost programmable well controller element has been provided to effect the proper well bias voltages. The circuit provided uses the body bias approach through
30 the use of a programmable component to drive both wells using a single voltage value. Also, in addition to the advantages outlined above the provided circuit is particularly useful in ICs where multiple power domains have been

used and where low-power is a differentiator. The circuit is an enabler for performance-enhanced low-voltage circuit operation. Example applications are microcontrollers for health monitoring or hearing aids, wireless sensor networks, and mobile applications.

CLAIMS:

1. A controller for controlling the body bias voltages in an integrated circuit, wherein the controller:
 - receives a mode input;
 - receives a reference voltage;
 - 5 outputs a first body bias voltage; and
 - outputs a second body bias voltage.
2. A controller according to claim 1, wherein the first body bias voltage and the second body bias voltage are dependent on the mode input
10 and the reference voltage.
3. A controller according to any of claims 1 and 2, comprising an arrangement of switches, each switch controlled by the mode input.
- 15 4. A controller according to any of claims 1 to 3, wherein:
 - the first body bias voltage sets an N-type transistor of the integrated circuit; and
 - the second body bias voltage sets a P-type transistor of the integrated circuit.
20
5. A controller according to any of claims 1 to 4, wherein the mode input is a mode signal indicative of an operating mode of the controller.
- 25 6. A controller according to any of claims 1 to 5 wherein
 - the reference voltage sets the first body bias voltage; and
 - the reference voltage sets the second body bias voltage.

7. An integrated circuit chip comprising a controller according to any of claims 1 to 6.

5 8. An integrated circuit comprising a controller according to any of claims 1 to 7.

9. An integrated circuit according to claim 8, further comprising:

- a power mode controller;
- 10 - a reference voltage generator; and
- a CMOS circuit; wherein:
the power mode controller generates the mode input;
the reference voltage generator generates the reference voltage; and
the CMOS circuit receives the first body bias voltage and the second

15 body bias voltage.

10. A method of controlling the body bias voltages in an integrated circuit, the method comprising the steps of:

- receiving a mode input;
- 20 - receiving a reference voltage;
- outputting a first body bias voltage; and
- outputting a second body bias voltage.

11. A method according to claim 10, wherein the first body bias voltage and the second body bias voltage are dependent on the mode input and the reference voltage.

25

12. A method according to any of claims 10 or 11, further comprising the steps of:

- 30 - setting an N-type transistor of the integrated circuit based on the first body bias voltage; and

- setting a P-type transistor of the integrated circuit based on the second body bias voltage.

13. A method according to any of claims 10 to 12, wherein the mode
5 input is a mode signal indicative of an operating mode of the controller.

14. A method according to any of claims 10 to 13, further comprising the steps of:

- setting the first body bias voltage based on the reference voltage; and
- 10 - setting the second body bias voltage based on the reference voltage.

15. A method according to any of claims 10 to 14, wherein the controller is incorporated onto a single chip.

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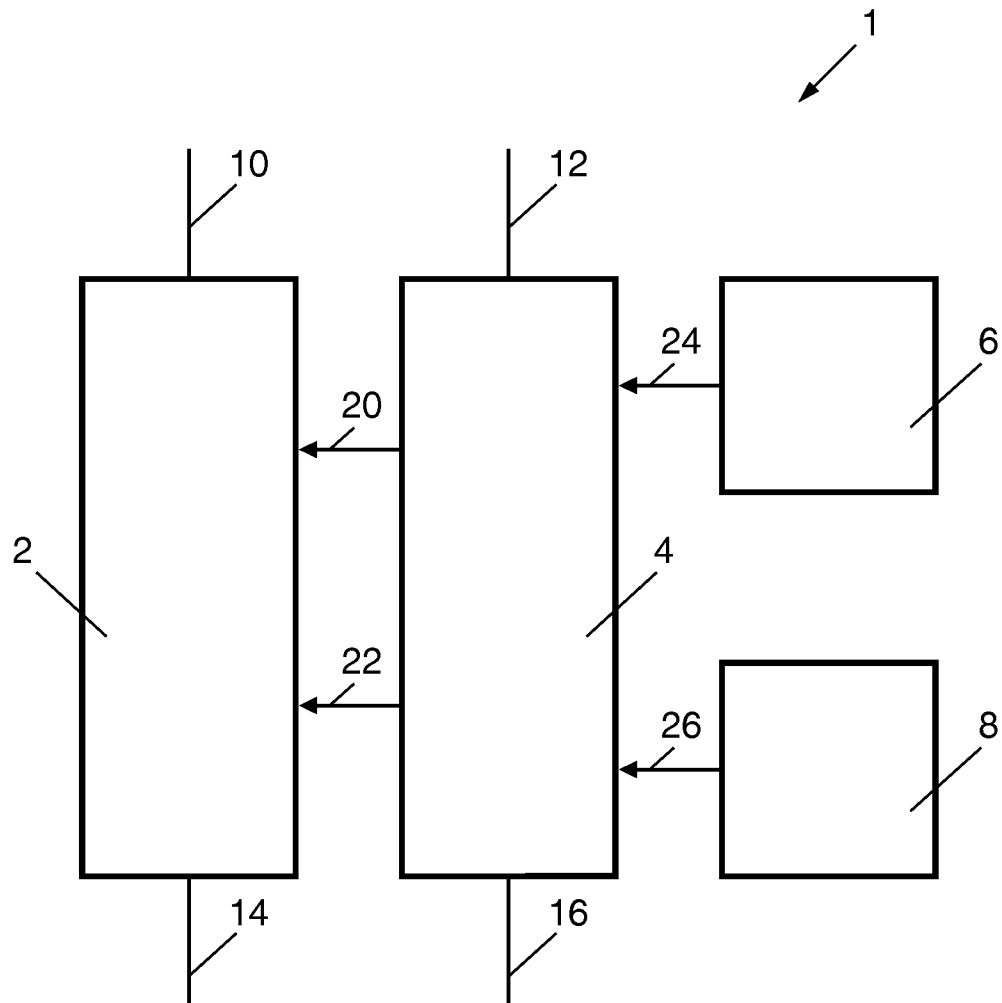


FIG. 1

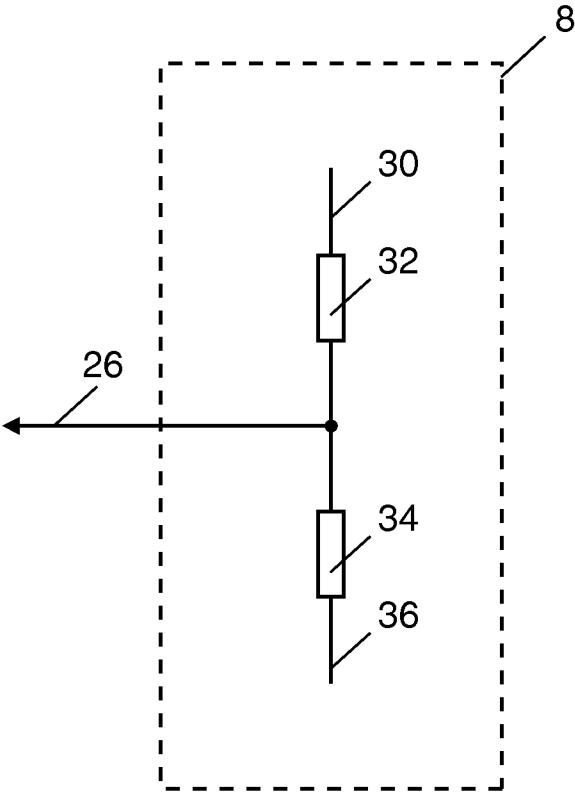


FIG. 2

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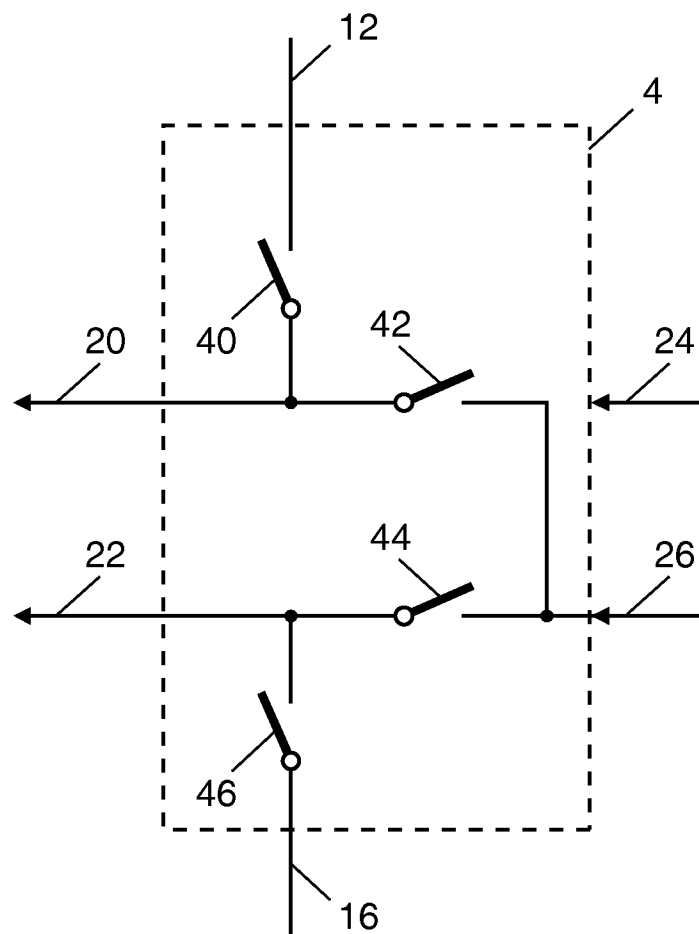


FIG. 3

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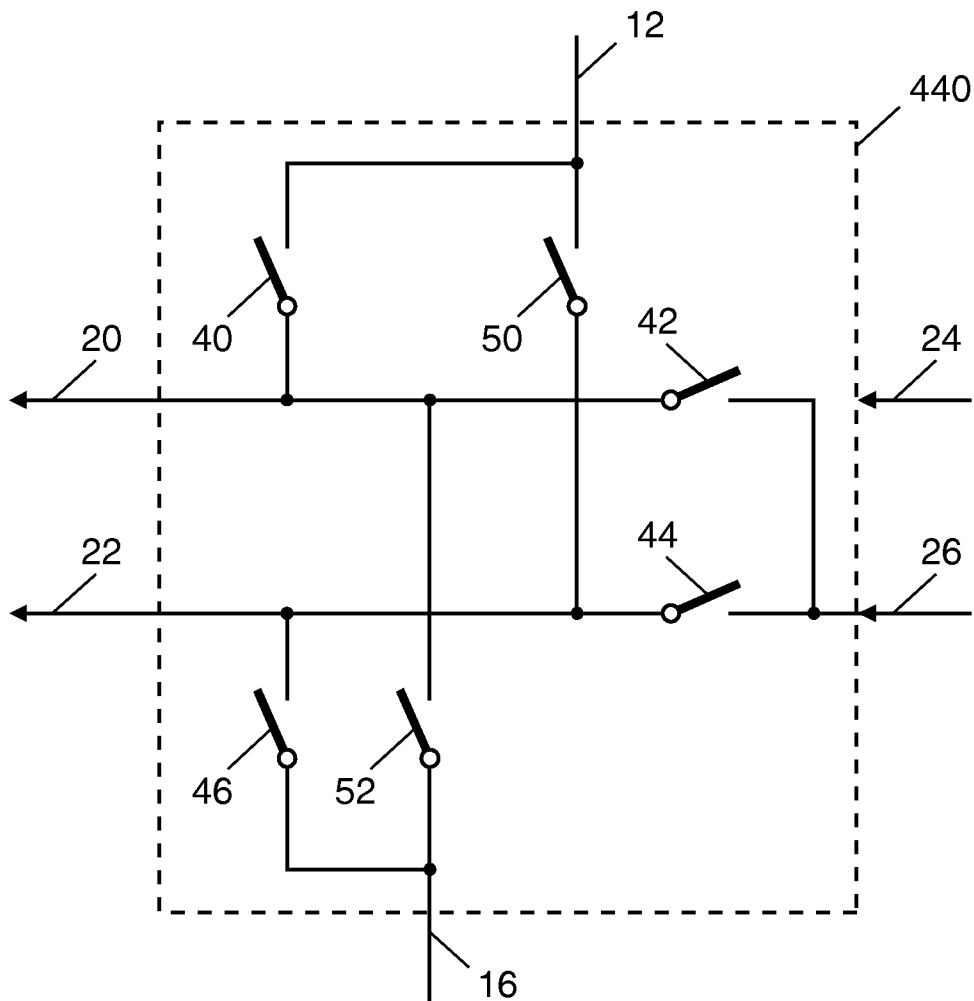


FIG. 4

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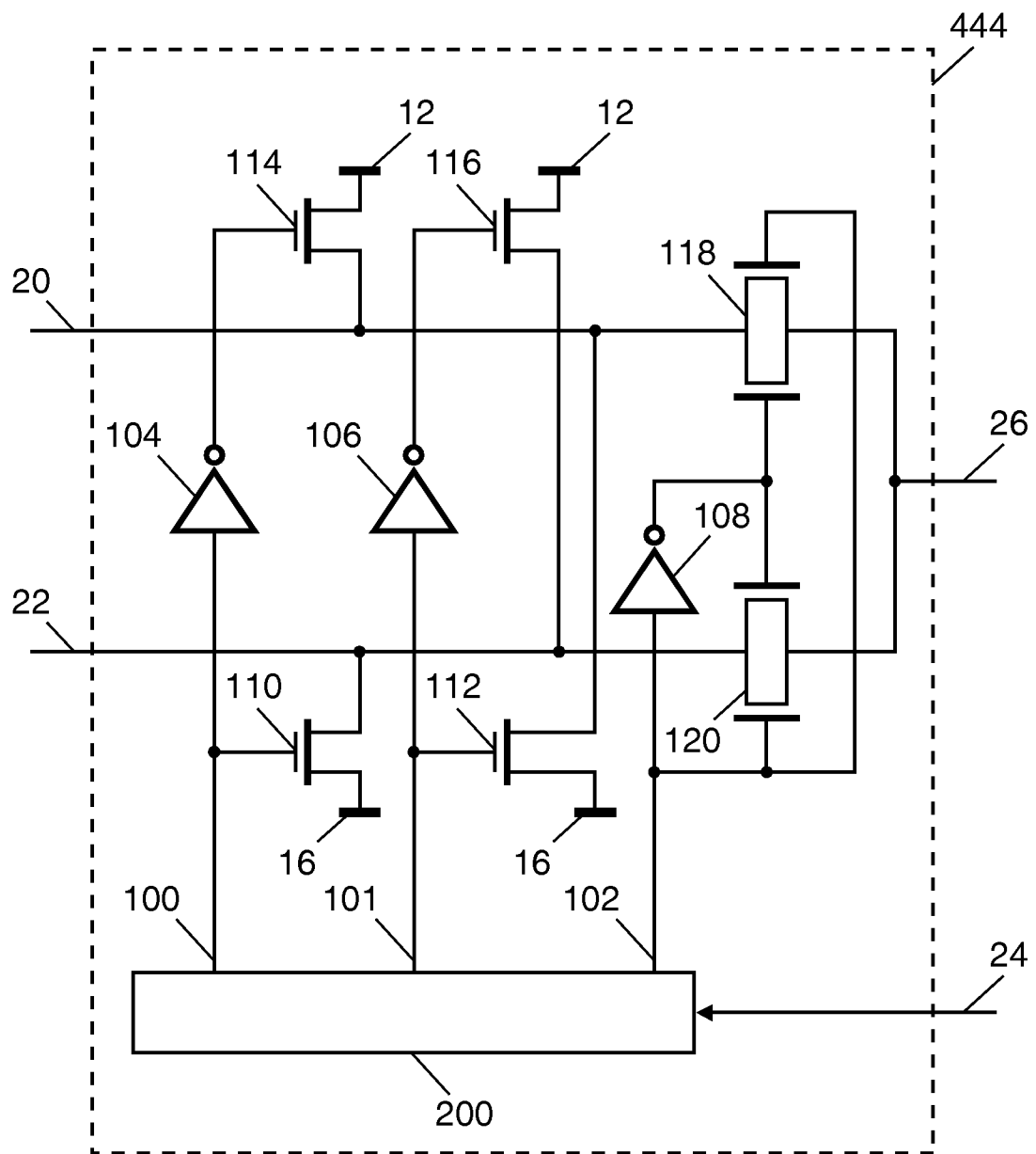


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2009/055580

A. CLASSIFICATION OF SUBJECT MATTER

INV. G11C11/413 H03K19/00

ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/030533 A1 (DE VIVEK K [US] ET AL) 14 March 2002 (2002-03-14) figures 7,8 paragraphs [0054] - [0055] -----	1-15
X	US 6 100 751 A (DE VIVEK K [US] ET AL) 8 August 2000 (2000-08-08) abstract figure 4 the whole document -----	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/IB2009/055580

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2002030533 A1	14-03-2002	NONE	
US 6100751 A	08-08-2000	US 6232827 B1	15-05-2001
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