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[54] **TIMER START-STOP APPARATUS**
**7 Claims, 2 Drawing Figs.**


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[56] **References Cited**
UNITED STATES PATENTS

3,363,243 1/1968 Morley ..... 340/232



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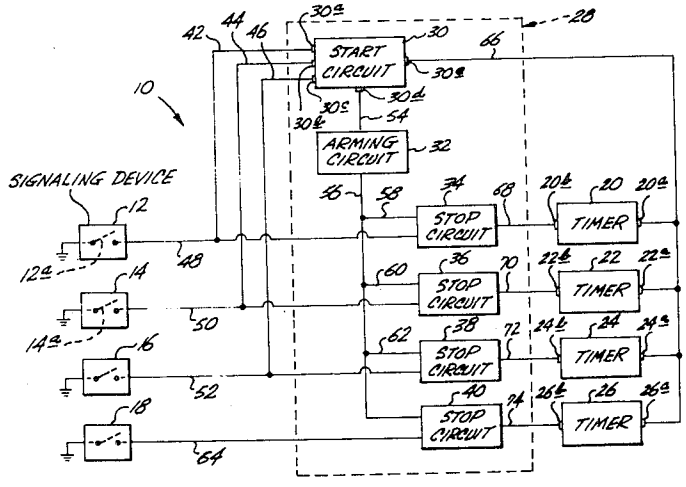
**ABSTRACT:** Electronic circuitry for controlling from the actions of one or more hand-operated signaling devices the starting and stopping of one or more electrical timers employed to time the performances of participants in sporting and like events. The circuitry employs a start circuit, and separate therefrom a different stop circuit for each participant. Interposed between the start and stop circuits is an arming circuit which prevents operation of the stop circuits until the elapse of a predetermined time after operation of the start circuit.

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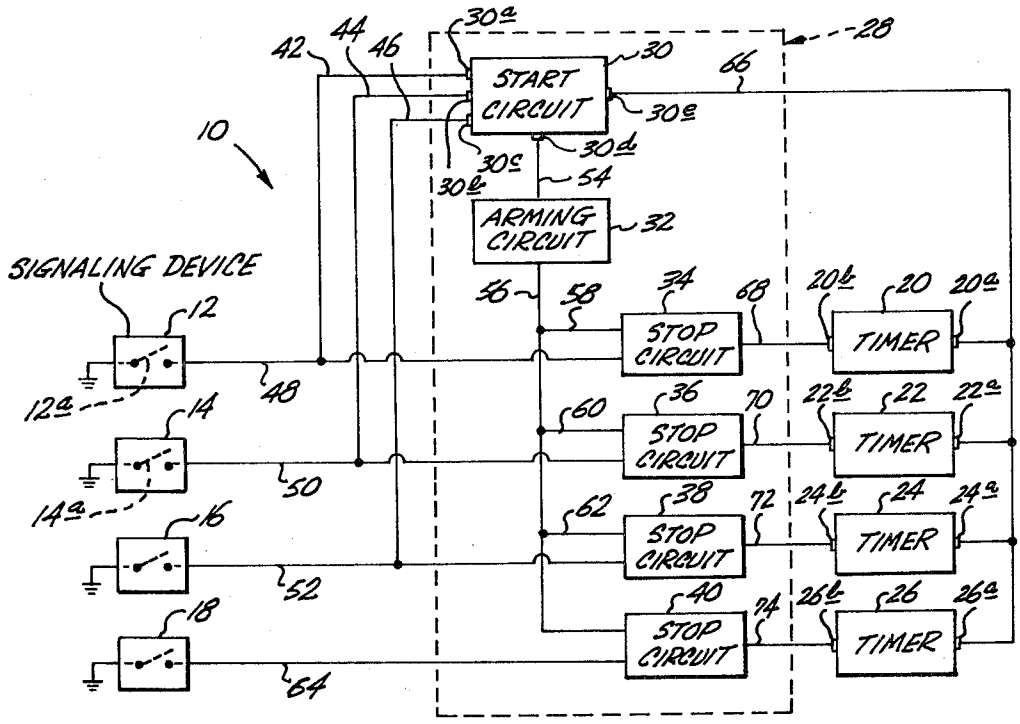


Fig. 1.

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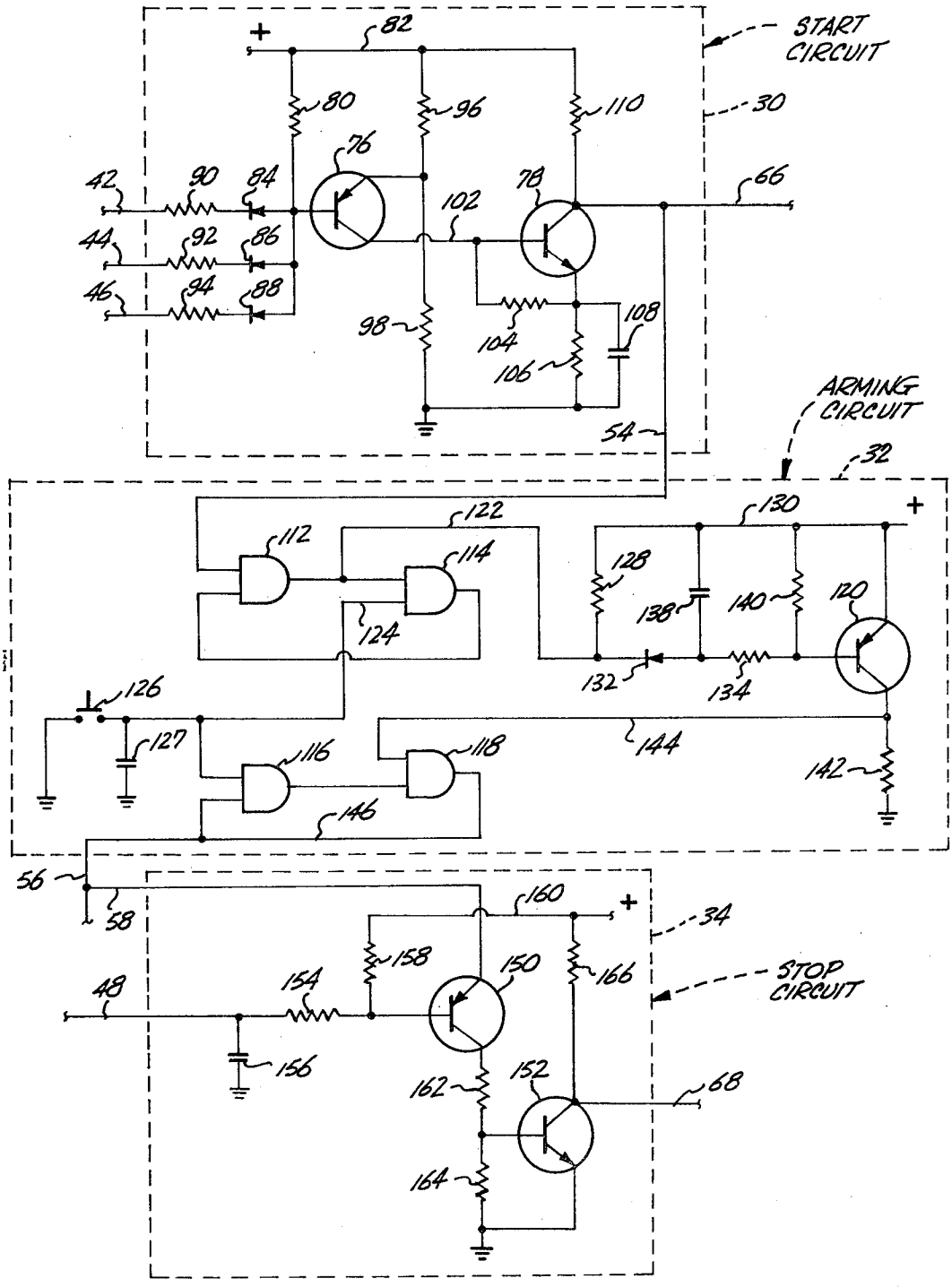


Fig. 2.

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# TIMER START-STOP APPARATUS

## BACKGROUND OF THE INVENTION

This invention pertains to circuitry for controlling the starting and stopping of one or more electrical timers employed for sporting and like events.

One of the important considerations in an event such as a swimming or track meet, is that the recorded times reflecting the performances of different participants, and especially those times reflecting the winning performances, be as accurate as possible. With conventional timing techniques, employing officials operating stop watches, good accuracy is not regularly obtainable. For example, at the start of a race, it is difficult for the officials operating the watches to anticipate exactly when the starting gun will fire. Experience has shown that the different reaction times of officials, particularly at the beginning of a race, is a primary contributing factor to inaccuracies.

To minimize such problems in the past, a group of three or more (although typically three) timing officials has been used for each "place" (i.e., first, second third, etc.) in a race where greater accuracy is desired. Normally, such a group is provided only to cover first place. At the end of a race, the recorded times of each official in a group are compared, and the mean (intermediate) time is selected and considered to be the correct time.

While this kind of practice has helped somewhat, there are still inaccuracies because of the impossibility of having all watches start at exactly the same time after firing of the starting gun. In addition, considerable time is consumed in selecting and recording the mean times.

## SUMMARY OF THE INVENTION

A general object of the present invention, therefore, is to provide novel apparatus for obtaining times in an event of the type generally indicated above which greatly minimizes inaccuracies encountered with present timing practices.

More specifically, an object of the invention is to provide such apparatus which greatly minimizes the effect which differences in different persons' reaction times has on the accuracy of times recorded for an event.

The proposed apparatus is adapted for use with an electrical timer which starts and stops, respectively, on receiving start and stop electrical signals. Accordingly, an object of the present invention is to provide novel start-stop circuitry employable with such a timer.

A related object is to provide such circuitry which may be used with multiple timers to provide a common start signal for all timers employed during an event, thus assuring that all timers begin operating at exactly the same moment.

Still another object of the invention is to provide such circuitry which includes a novel start circuit that is capable at the beginning of a race of selecting the means reaction time of three officials (who operate signaling devices connected to the circuit) as an indication of when to supply a start signal to a timer.

A further object of the invention is to provide circuitry of the type so far generally indicated which incorporates a stop circuit for each timer, and a novel delayed-biasing arming circuit interposed between the start and stop circuits which permits the same hand-operated signaling devices that are employed to begin the operations of timers also to be employed to stop their operations.

According to a preferred embodiment of the invention, the proposed circuitry includes a single start circuit, a single arming circuit, and one or more stop circuits depending on the number of timers to be controlled. A different stop circuit is provided for each timer. The start circuit has three inputs, each connected to a different one of three different hand-operated signaling devices. One signaling device is provided for each participant in a race, with each device connected to a different stop circuit.



In the particular embodiment shown herein, four participants can be taken care of. There are four timers, four signaling devices, and four stop circuits. Three of the signaling devices are connected to the start circuit and to three different stop circuits. The fourth signaling device is connected only to the fourth stop circuit.

At the beginning of a race, with overlapping actuations of any two of the three signaling devices connected to the start circuit, and only under such circumstances, the latter supplies a common start signal to all timers. Mean reaction time of the three officials operating these three timers is thus selected at the indicator to start the timers. Further, no timer gets a head-start. The stop circuits are initially in nonarmed states, and are nonresponsive to operations of the signaling devices.

A predetermined time interval after the production of a start signal, the arming circuit produces an arming signal which it supplies to each of the different stop circuits. On receipt of an arming signal, the stop circuits are placed in armed states wherein they are responsive to any subsequent actuations of their respective associated signaling devices. AS each individual participant finishes the race, and on actuation of the associated signaling device, the associated stop circuit supplies a stop signal to the proper timers. Individual performance times are immediately obtainable in the final indications of the timers.

## DESCRIPTION OF THE DRAWINGS

These and other objects and advantages attained by the invention will become more fully apparent as the description which follows is read in conjunction with the accompanying drawings, wherein:

FIG. 1 is a simplified block diagram illustrating a system employing apparatus constructed according to the present invention; and

FIG. 2 is a fragmentary circuit diagram illustrating details of the apparatus employed in the system of FIG. 1.

## DETAILED DESCRIPTION OF THE INVENTION

Turning now to the drawings, and referring first to FIG. 1 indicated generally at **10** is an electrical timing system employing an embodiment of the present invention. System **10** is of a type which might be used, for example, to time the performances of as many as four different swimmers in a swimming race.

Indicated generally in block form at **12, 14, 16, 18** are four hand-operated signaling devices—one for each possible participant in a race. These devices are operated by different officials during a race. Each signaling device includes a normally open switch, such as switches **12***a*, **14***a* in devices **12, 14**, respectively. These switches may be closed, selectively, momentarily through the operation of an externally accessible button or the like. Devices **12, 14, 16** may be thought of herein as primary devices, since it is their actuations which result in starting of timers in the system at the beginning of a race.

Indicated generally in block form at **20, 22, 24, 26** are four timers—one for each of the four possible participants. Timers **20, 22, 24, 26**, are associated with signaling devices **12, 14, 16, 18** respectively. Each timer includes a start and a stop input terminal bearing the same reference numeral as the timer, together with the suffixes *a*, *b*, respectively,. These timers may be of any suitable conventional type which start on receiving a substantially ground-level voltage pulse (start signal) at their start input terminals, and stop on receiving a similar pulse at their stop input terminals. Each timer is equipped with a suitable indicator which presents a running elapsed-time indication progressing from when the timer is started. The timers are provided with suitable conventional means for resetting them to present a zero elapsed-time indication after each timing operation.

Indicated generally within the dashed block designated **28** is apparatus constructed as contemplated herein. This apparatus

includes a start circuit 30, an arming circuit 32, and four stop circuits 34, 36, 38, 40. Circuits 34, 36, 38, 40 are associated, respectively, with signaling devices 12, 14, 16, 18 and timers 20, 22, 24, 26.

Start circuit 30 includes three input terminals 30*a*, 30*b*, 30*c*, and two output terminals 30*d*, 30*e*. Terminals 30*a*, 30*b*, 30*c* are connected through conductors 42, 44, 46 and conductors 48, 50, 52, respectively, to one set of sides of the switches in signaling devices 12, 14, 16, respectively. The other sides of these switches are grounded. Conductors 42, 44, 46 constitute input conductors herein. Conductors 48, 50, 52 also connect with one set of input terminals in stop circuits 34, 36, 38, respectively.

Output terminal 30*d* of circuit 30 is connected by a conductor 54 to the input terminal of arming circuit 32. The output terminal of the arming circuit is connected to another set of input terminals in stop circuits 34, 36, 38 through a conductor 56 and conductors 58, 60, 62 respectively. Conductor 56 also connects with one input terminal in stop circuit 40. A conductor 64 interconnects the other input terminal of circuit 40 with one side of the switch in signaling device 18. The other side of this switch is grounded.

Output terminal 30*e* is connected through a conductor 66 to the start input terminals of the four timers. The output terminals of circuits 34, 36, 38, 40 are connected through conductors 68, 70, 72, 74 to the stop input terminals of timers 20, 22, 24, 26, respectively.

Referring to FIG. 2, start circuit 30 includes a pair of transistors, or electronic switching devices, 76, 78. The base of transistor 76 is connected through a resistor 80 to a conductor 82 which is connected to the positive side of a suitable source of DC voltage. The base also is connected to conductors 42, 44, 46 through diodes 84, 86, 88 and resistors 90, 92, 94, respectively. Resistors 80, 90, 92, 94 form part of a voltage divider for the base. Resistors 90, 92, 94 have substantially the same resistance values. The particular one or ones of resistors 90, 92, 94 which affect the voltage on the base at a given time depends upon which of the switches in signaling devices 12, 14, 16, are closed. A resistor 96 connects the emitter of transistor 76 to conductor 82, and a resistor 98 connects the emitter to ground. The collector of transistor 76 is connected through a conductor 102 to the base of transistor 78.

Considering transistor 78, its emitter is connected to its base through a resistor 104, and is connected to ground through the parallel combination of a resistor 106 and a capacitor 108. A resistor 110 provides positive voltage from conductor 82 to the collector of transistor 78. In addition, this collector is connected to previously mentioned conductors 66, 54.

With two or more of the switches in devices 12, 14, 16 open, transistor 76, 78 are nonconductive. Under such circumstances, the voltage on conductors 54, 66 is substantially at the same positive level as the voltage on conductor 82. Such a voltage level is referred to herein as a "1" state voltage. And a conductor or terminal having this voltage on it is referred to as being in a "1" state, or as having a "1" state on it.

The moment that any two or more of the switches in devices 12, 14, 16 are closed, a sufficiently low bias voltage is provided the base of transistor 76 to cause it, and transistor 78, to conduct. It will be noted that closure of the switches in devices 12, 14, 16 grounds conductors 42, 44, 46, respectively. A ground-level or near ground-level voltage is referred to herein as a "0" state voltage. With conduction of transistors 76, 78, conductors 54, 66 are placed in "0" states. Such a condition lasts only so long as two or more of the three switches mentioned are closed.

Arming circuit 32 includes four conventional two-input NAND-gates 112, 114, 116, 118, and a transistor 120. EAch of these gates functions as follows: with a "0" state voltage on either input terminal (at the left sides of the gates in FIG. 2), the output terminal of the gate is held in a "1" state; with both input terminals in a "1" state, the output terminal is placed in a "0" state. With a "1" state on conductor 54, the output terminals of gates 112, 114, 116, 118 are normally in "0," "1," "1," "0," states, respectively.

Conductor 54 connects with the upper input terminal of gate 112. The lower input terminal of this gate is connected to the output terminal of gate 114. The output terminal of gate 112 is connected to the upper input terminal of gate 114, and also to a conductor 122. The lower input terminal of gate 114 is connected through a conductor 124 to one side of a normally open switch 126. The other side of switch 126 is grounded. A capacitor 127 bypasses conductor 124 to ground.

Conductor 122 is connected through a resistor 128 to a supply conductor 130 which is connected to the same voltage supply terminal as previously mentioned conductor 82. In addition, conductor 122 is connected to the base of transistor 120 through a diode 132 and a resistor 134. A capacitor 138 connects conductor 130 and the junction between diode 132 and resistor 134. A resistor 140 connects the base of transistor 120 to conductor 130. The emitter of transistor 120 is connected directly to conductor 130. The collector of transistor 120 is connected to ground through a resistor 142.

A conductor 144 connects the collector of transistor 120 to the upper input terminal of gate 118. The lower input terminal of gate 118 is connected to the output terminal of gate 116. The upper input terminal of gate 116 is connected to previously mentioned conductor 124. The output terminal of gate 118 is connected through a conductor 146 to the lower input terminal of gate 116. Previously mentioned conductor 56 is connected to conductor 146.

With the output terminals of the gates in the conditions mentioned above, transistor 120 conducts, and capacitor 138 is charged substantially to the same voltage existing between conductor 130 and ground.

These conditions remain until a "0" state voltage is placed on conductor 54. When this occurs, the voltage on the output terminal of gate 112 switches to a "1" state, and that on the output terminal of gate 114 switches to a "0" state. As a consequence of the state change mentioned on the output terminal of gate 112, sufficiently low bias voltage is not longer provided by conductor 122 to the base of transistor 120. With the state change mentioned on the output terminal of gate 114, gates 112, 114 become locked in their new conditions.

With the supply of base bias voltage via conductor 122 changed as indicated, capacitor 138 discharges through the base-emitter circuit of transistor 120, and through resistors 134, 140, to maintain the transistor in a conducting state for a short time. In the embodiment described herein, transistor 120 and resistors 134, 140 are chosen whereby this time interval is about 3 seconds. After this interval, referred to herein as a predetermined time interval, transistor 120 stops conducting, and the state of the voltage on conductor 144 changes from "1" to "0."

With conductor 144 in a "0" state, gate 118 switches to a condition with a "1" state voltage on its output terminal, and gate 116 switches to a condition with a "0" state voltage on its output terminal. As a result gates 116, 118 become locked in their new conditions.

This situation remains until reset switch 126 is momentarily closed to place a "0" state voltage on the lower input terminal of gate 114 and on the upper input terminal of gate 116. On such occurring, gates 112, 114, 116, 118 return to their initial conditions. Thereupon, transistor 120 starts conducting again, and capacitor 138 again becomes charged to the voltage previously mentioned.

Stop circuit 34 includes a pair of transistors 150, 152. The emitter of transistor 150 is connected to previously mentioned conductor 58. The base of this transistor is connected through a resistor 154 to previously mentioned conductor 48. A bypass capacitor 156 connects the junction of conductor 48 and resistor 154 to ground. The base of transistor 150 additionally is connected through a resistor 158 to a positive voltage supply conductor 160. Conductor 160 is connected to the same source of positive voltage provided for conductors 82, 130. The collector of transistor 150 is connected to ground through resistors 162, 164. Transistor 150 constitutes an electronic switching device herein.

Transistor 152 has its emitter connected directly to ground, and its base connected to the junction between resistors 162, 164. The collector of transistor 152 is connected to conductor 160 through a resistor 166, and in addition is connected directly to previously mentioned conductor 68.

Stop circuits 36, 38, 40 are constructed in substantially the same manner as circuit 34. Thus, only circuit 34 is described in detail, and shown in FIG. 2.

With a "0" state voltage on conductors 56, 58, sufficiently positive emitter bias voltage is lacking to permit transistor 150 to conduct. With transistor 150 nonconductive, so also is transistor 152. Under such circumstances, conductor 68 is in a "1" state. In this situation, circuit 34 is in what is referred to herein as a nonarmed state.

With a "1" state on conductors 56, 58, sufficient positive bias voltage is provided the emitter of transistor 150. This situation is referred to herein as an armed state for circuit 34. Under such conditions, with a "0" state voltage applied to conductor 48, transistor 150 conducts, and causes transistor 152 also to conduct. Conduction of transistor 152 places a "0" state on conductor 68. Transistors 150, 152 continue to conduct only so long as there is sufficient positive bias voltage provided the emitter of transistor 150, and a "0" state voltage exists on conductor 48.

Explaining now how the system described herein performs as a whole during an event such as a swimming race, the start circuit, arming circuit and stop circuits are initially in conditions awaiting closure of the switches in signaling devices 12, 14, 16, 18. More specifically: start circuit 30 is in a condition placing conductors 54, 66 in "1" states; arming circuit 32 is in a condition placing a "0" state on conductors 56, 58, 60, 62; and the stop circuits are in conditions (nonarmed states) placing "1" states on conductors 68, 70, 72, 74. Timers 20, 22, 24, 26, are stopped, and are in conditions indicating zero elapsed time.

Assuming a normal start to the race, subsequent to the firing of the starting gun the various officials operating signaling devices 12, 14, 16, 18 momentarily close the switches in their respective devices. This results in momentary "0" state voltages being applied to conductors 48, 50, 52, 64. Because arming circuit 32 is in a condition placing a "0" state on conductor 56, these momentary "0" state voltages on conductors 48, 50, 52, 64 effect no change in the conditions of the four stop circuits. This is because sufficiently positive emitter bias voltage is not available for transistor 150 in circuit 34, and for the corresponding transistors in circuits 36, 38, 40.

However, such momentary "0" state voltages on conductors 48, 50, 52 do effect a change in the condition of start circuit 30. More specifically, at the first moment that any two of the "0" state voltages on conductors 48, 50, 52 overlap in time, sufficiently low bias voltage is provided the base of transistor 76 to cause it and transistor 78 to conduct. When this occurs, and as previously explained, a "0" state is applied to conductors 54, 66. Such action, it will be noted, occurs at a time after firing of the starting gun corresponding to the means reaction times of the three officials operating the primary signaling devices (12, 14, 16). It occurs automatically and instantaneously.

The "0" state on conductor 66 is applied simultaneously to the start input terminals of all four timers in the system. Thus, and according to an important feature of the invention, at exactly the same moment in time, all timers for all of the swimmers in the race begin counting off elapsed times.

The "0" state applied to conductor 54 simultaneously with that applied to conductor 66 changes conditions in arming circuit 32. As was previously described, such action results in transistor 120 stopping conducting about 3 seconds after initiation of the state change on conductor 54 from "1" to "0." When transistor 120 stops conducting, a "1" state is applied to conductors 56, 58, 60, 62. As a consequence, the stop circuits are placed in their armed states. The three second delay in shutting off of transistor 120 is to assure ample time for the officials operating the signaling devices to reopen the switches in the devices before the stop circuits are placed in armed states.

These conditions remain until a switch in one of the signaling devices is again actuated.

When the winning swimmer finishes, and assuming that his performance is being followed by the official handling device 12, the official again momentarily closes the switch in the device. As a consequence, a momentary "0" state voltage is applied to conductor 48, and this causes transistors 150, 152 is stop circuit 34 momentarily to conduct. As a result, a momentary "0" state voltage is applied through conductor 68 to the stop input terminal of timer 20. Timer 20, alone, then stops.

Similar action occurs as each of the remaining swimmers in the race finishes. In other words, with the stop circuits in armed states, closure of the switch in a signaling device results in stopping of the timer associated with the device. When all swimmers have finished, reset switch 126 in the arming circuit may be closed momentarily to return the arming circuit to a condition placing a "0" state on conductors 56, 58, 60, 62. This action returns all of the stop circuits to nonarmed states.

One important feature of the apparatus just described is that it prevents starting of the timers in the event that one of the officials accidentally anticipates the starting gun. This is because it requires simultaneous (overlapping) operation of switches in at least two of the signaling devices before a start signal can be furnished the timers. It will be apparent, and experience has shown, that it is quite unlikely that two operators will simultaneously anticipate a starting gun.

Another important feature is that with placement of the stop circuits in their armed states delayed by arming circuit 32, the same switches in the same signaling devices which are used to start operation of timers, may also be used to stop the timers.

While a preferred embodiment of the invention has been described herein, it is appreciated that variations and modifications may be made without departing from the spirit of the invention.

It is claimed and desired to secure by Letters Patent:

1. In the electrical timing system including a timer having one input terminal adapted to receive a start signal which initiates operation of the timer and another input terminal adapted to receive a stop signal which terminates operation of the timer, and a signaling device operable to produce a control signal,

apparatus for utilizing a pair of time-spaced control signals from said signaling device to produce first a start signal and next a stop signal for said timer, said apparatus comprising

a start circuit operatively connected to said signaling device and to said timer's said one input terminal, adapted to receive a control signal from the signaling device, and operable on receiving such a signal to supply a start signal to said one input terminal,

an arming circuit operatively connected to said start circuit operable to produce an arming signal a predetermined time interval after said start circuit supplies a start signal, and

a stop circuit operatively connected to said signaling device, to said arming circuit, and to said timer's said other input terminal, adapted to receive a control signal from said signaling device and an arming signal from said arming circuit,

said stop circuit having a nonarmed state in which it is nonresponsive to a control signal from said signaling device, and on receiving an arming signal from said arming circuit being placeable in an armed state, and being operable while in its said armed state to supply a stop signal to said other input terminal on receiving a control signal from said signaling device.

2. The apparatus of claim 1, where in said stop circuit includes an electronic switching device having a terminal which must be biased a certain amount to place the stop circuit in its said armed state, and said arming circuit is operatively connected to said switching device's said terminal and biases the same by said certain amount said predetermined time interval after said start circuit supplies a start signal.

3. In an electrical timing system including timing means adapted to receive a start signal which initiates operation of timing means, and at least two signaling devices each operable to produce control signals,

apparatus interconnecting said signaling devices and said timing means utilizing control signals from the former to produce a start signal for the latter, said apparatus comprising

a pair of input conductors input conductors each connected to a different one of said signaling devices to receive control signals therefrom, and

a start circuit operatively connected to said input conductors and to said timing means operable to supply a start signal to the latter only under circumstances with each of said input conductors simultaneously in a condition receiving a control signal from its respective associated signaling device.

4. The apparatus of claim 3, wherein said timing means comprising a pair of timers whose operations are initiated simultaneously upon the supply of a start signal by said start circuit.

5. The apparatus of claim 3, wherein said start circuit comprises an electronic switching device having an input terminal, and a voltage divider for said device operatively connected to said input terminal for supplying voltage thereto, said voltage divider including a pair of resistors each connected between said input terminal and a different one of said input conductors.

6. In an electrical timing system including at least a pair of timers, each having one input terminal adapted to receive a start signal for initiating operation of the timer and another input terminal adapted to receive a stop signal for terminating operation of the timer, and at least a pair of signaling devices each operable to produce a control signal, circuit means comprising

a start circuit operatively connected to said signaling devices and to said timers' said one input terminals adapted to receive control signals from said signaling devices, and operable on receiving simultaneously a control signal from each signaling device to supply a start signal to both timers,

an arming circuit operatively connected to said start circuit operable to produce an arming signal a predetermined timer interval after said start circuit supplies a start signal to said timers, and

a pair of stop circuits, one for each timer, each operatively connected to a different one of said signaling devices, to said arming circuit, and to its respective associated timer, and adapted to receive control signals from its respective associated signaling device and an arming signal from said arming circuit,

each stop circuit having a nonarmed and an armed state and being placeable in the latter state on receiving an arming signal from said arming circuit, and each stop circuit when in its said armed state and on receiving a control signal from its respective associated signaling device supplying a stop signal to its respective associated timer.

7. For use with sporting event timing apparatus including timing means which is capable of producing a separate running elapsed-time indication for each of a certain number of participants in an event, and which includes a shared start input terminal adapted to receive a start signal for simultaneously initiating an elapsed-time indication for each participant, and a separate stop input terminal for each participant adapted to receive a stop signal for stopping the elapsed-time indication for that participant, and a signaling device for each participant operable to produce control signals associated with performance of the participant,

a start circuit adapted to be connected to said timing means and to said signaling devices, and adapted when so connected to receive control signal from the latter and to supply a start signal to said start input terminal under circumstances with at least two of said signaling devices simultaneously producing a control signal, and

for each participant, a stop circuit adapted to be connected to said timing means, to said start circuit, and to the signaling device associated with the participant, operable when so connected, and subsequent to operation of said start circuit, to supply a stop signal stopping the elapsed-time indication for the participant on receiving a control signal from its respective associated signaling device.

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