AMENDED

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P/00/001
Section 29

AUSTRALIA
PATENTS ACT 1990

PATENT REQUEST: STANDARD PATENT

WE, being the person identified below as the Applicant, request the grant of a patent to the person identified below as the Nominated Person, for an invention described in the accompanying standard complete specification.

Full application details follow:

[71]	**Applicant**	PHILIPS ELECTRONICS N.V. Groenewoudseweg 1, 5621 BA Eindhoven. The Netherlands.
[71]	**Nominated Person Address:**	PHILIPS ELECTRONICS N.V. Groenewoudseweg 1, 5621 BA Eindhoven. The Netherlands.
[54]	**Invention Title:**	DEVICE FOR ENCODING DIGITAL SIGNALS REPRESENTING TELEVISION PICTURES
[72]	**Name(s) of actual Inventor (s)**	Frederique GUEDE
[74]	**Address for service in Australia:**	F.B. Rice, Co Sydney NSW 2001 Patent & Trade Marks Division, Philips Electronics Australia Limited 16th Floor, The Philips Building, 15 Blue Street, North Sydney, N.S.W. 2060

ADDRESS FOR SERVICE ALTERED

Attorney Code PH

[BASIC CONVENTION APPLICATION(S) DETAILS

[60] Application No.	[33] Country	Country Code	32] Date of Applc.
9215504	FRANCE	FR	22.12.92

Drawing Number recommended to accompany the Abstract: FIG.3

For and on behalf of
PHILIPS ELECTRONICS N.V.

P.W. Mackenzie (Attorney)

15-11-96
Date

PHF92570
P/00/008
Section 29 (1)
Regulation 3.1 (2)

AUSTRALIA

PATENTS ACT 1990

NOTICE OF ENTITLEMENT

(TO BE FILED BEFORE ACCEPTANCE)

WE PHILIPS ELECTRONICS N.V.

of Groenewoudseweg 1, 5621 BA Eindhoven, The Netherlands

being the applicant in respect of Application No. state

the following:-

1. The person nominated for the grant of the patent has entitlement from the actual inventor/ by virtue of a mesne assignment.

2. The person nominated for the grant of the patent has entitlement from the applicant of the basic application/ listed on the Patent Request Form.

3. The basic applications listed on the Patent Request Form are the first applications made in a Convention country in respect of the invention.

For and on behalf of
PHILIPS ELECTRONICS N.V.

P.W. Mackenzie (Attorney)

21/12/93
Date

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(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 675808

(54) Title
DEVICE FOR ENCODING DIGITAL SIGNALS REPRESENTING TELEVISION PICTURES

International Patent Classification(s)
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(30) Priority Data

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92 15504	22.12.92	FR FRANCE

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(56) Prior Art Documents
US 5091782
EP 510972
EP 490799

(57) Claim

1. A device for encoding digital signals corresponding to interlaced-field pictures, comprising a first variable-length encoding channel (10), which channel comprises a series arrangement of a first section for compressing interlaced data and an encoding section, and, in parallel therewith, a second variable-length encoding channel (30), which channel comprises a series arrangement of a second section for compressing non-interlaced data and an encoding section, and a first channel (20) for prediction on the basis of output signals of said first section and, in parallel therewith, a second channel (40) for prediction on the basis of output signals of said second section, said second section including at its input side a circuit (31) for de-interlacing the fields and said second prediction channel including a circuit (45) for re-interlacing the fields, characterised in that the device also comprises a decision sub-assembly (50) comprising means for comparing the output signals of the first and second encoding channels and means for selecting the prediction and encoding channels in accordance with the result of said comparison.

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PATENTS ACT 1990

COMPLETE SPECIFICATION

FOR A STANDARD PATENT

O R I G I N A L

AUSTRALIAN PATENT OFFICE SEC. 104

Name of Applicant: Philips Electronics N.V.
~~PHILIPS ELECTRONICS N.V.~~
~~N.V. Philips' Gloeilampenfabrieken~~

AUSTRALIAN PATENT OFFICE SEC. 113

Actual Inventors: Frederique GUEDE

AUSTRALIAN PATENT OFFICE REG 22.10 (2)

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Invention Title: "DEVICE FOR ENCODING DIGITAL SIGNALS REPRESENTING TELEVISION PICTURES"

The following statement is a full description of this invention including the best method of performing it known to us.

Device for encoding digital signals representing television pictures.

FIELD OF THE INVENTION

The invention relates to a device for encoding digital signals corresponding to interlaced-field pictures, comprising a first variable-length encoding channel, which channel comprises a series arrangement of a first section for compressing interlaced data and an encoding section, and, in parallel therewith, a second variable-length encoding channel, which channel comprises a series arrangement of a second section for compressing non-interlaced data and an encoding section, and a first channel for prediction on the basis of output signals of said first section and, in parallel therewith, a second channel for prediction on the basis of output signals of said second section, said second section including at its input side a circuit for de-interlacing the fields and said second prediction channel including a circuit for re-interlacing the fields. This invention is particularly applicable for encoding television signals in accordance with the MPEG1 standard ("Moving Picture Expert Group" which is a work group in the International Standardization Organization dealing with the problem of encoding animated picture sequences).

BACKGROUND OF THE INVENTION

The specifications of the MPEG1 standard state that the treated pictures are necessarily in a sequential form. If the original pictures are television pictures, *i.e.* pictures having two interlaced fields, these two fields considered for MPEG encoding as information components taken at the same instant correspond, however, to a lesser extent to data which in reality are spaced apart by inter-field intervals of 20 ms. In picture sequences in which the motion is very rapid, such a significant inter-field motion contributes to picture faults, such as comb effects which are due to the appearance of parasitic frequencies in the blocks.

In accordance with the MPEG1 standard each picture is cut up into macroblocks of 16 x 16 pixels comprising four blocks of 8 x 8 pixels for the luminance and two blocks of 8 x 8 pixels for the chrominance. Fig. 1 shows in such a macroblock a vertical structure whose alignment is satisfactorily maintained in the absence of

motion, even if the lines of this macroblock alternately correspond to the one or the other of the two interlaced fields which are 20 ms apart. Fig. 2 shows the same vertical structure in the case where the inter-field motion is significant and where the comb effect appears due to time-shifting of the information components of the odd lines and those of the even lines of the macroblock.

United States Patent 5,091,782 describes a device for encoding digital video signals in which the two interlaced fields are treated in two distinct manners before encoding. On the one hand, the interlaced fields are separated and then subdivided into blocks which are subsequently each submitted to an orthogonal transform followed by a quantization, and on the other hand the blocks thus obtained and being in spatial conformity in the two fields are re-interlaced so as to be submitted to an orthogonal transform and a quantization. Error computations with respect to the signals before quantization are respectively effected on the two distinct sequences of signals thus quantized so that, in accordance with the motion in the original signals, the definitive selection of one of said two quantized signal sequences to be encoded can be made, *viz.* the sequence with which the smallest error is associated.

SUMMARY OF THE INVENTION

It is an object of the invention to propose an encoding device making use of another type of technical solution for compressing the data in a more efficient manner while taking the more or less great significance of motion in the pictures into account.

To this end the invention relates to an encoding device as described in the opening paragraph, which is characterized in that it also comprises a decision sub-assembly comprising means for comparing the output signals of the first and second encoding channels and means for selecting the encoding and prediction channels in accordance with the result of said comparison.

The structure thus proposed has the particular advantage of a greater simplicity of implementation in the sense that, in contrast to the device described above, it does not require any error computation with respect to the original signals but is based solely on a comparison of the number of bits after encoding.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 and 2 show the fault referred to as "comb structure" in a part of the picture which is a sub-assembly constituted by four luminance blocks, during significant movements in the picture;

Fig. 3 shows an embodiment of an encoding device according to the invention;

Figs. 4 and 5 show the same assembly of four picture blocks available before encoding in the first and second encoding channels, respectively;

Fig. 6 shows an embodiment of a decoding device which is suitable for processing encoded signals received from the encoding device according to the invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

The encoding device shown in Fig. 3 comprises a first variable-length-encoding channel 10 receiving the digital signals to be encoded, and an associated first channel 20 for prediction on the basis of signals available before coding. The encoding channel 10 comprises a series arrangement of an orthogonal transform circuit 12 (a discrete cosine transform in this embodiment), a quantizing circuit 13, a variable-length encoding circuit 14 and a buffer memory 15 (whose output S_1 constitutes that of the encoding device), as well as a return connection 16 between this buffer memory and the circuit 13 for adjusting the quantization step and thus the bit rate. The prediction channel 20 receives the signals before encoding and comprises, at the output of the circuit 13, a series arrangement of an inverse quantizing circuit 21 and an inverse orthogonal transform circuit 22 (an inverse discrete cosine transform in this case) ensuring the respective inverse transforms of those performed by the circuits 13 and 12. The output signals of the circuit 22 are applied to a first input of an adder 23 whose output signal is stored in a picture memory 24.

The output signal of the memory 24 is applied to a motion compensation stage 60 which comprises a motion estimation circuit 61 and a motion compensation circuit 62. A first input of the circuit 62 receives the output signal of the memory 24 and a second input receives that of the circuit 61. The circuit 61 receives the digital input signals of the encoding device and determines, for each picture block, a displacement vector which is representative of its motion with respect to the

corresponding block of a picture previously transmitted for encoding (this determination is known as block matching). The vector thus determined is applied to the second input of the motion compensation circuit 62. These displacement vectors are also supplied to the decoding device described hereinafter.

The circuit 62 supplies a predicted block whose difference with the preceding block is determined in a subtracter 25 which is arranged upstream of the orthogonal transform circuit 12. The predicted block is also applied to a second input of the adder 23. A first input of the subtracter 25 receives the output signal of a format conversion circuit 75 which receives the digital input signals of the device corresponding to the pictures to be presented at its output in the form of blocks. The digital signals at the input of the circuit 12 are thus signals representing the prediction error, *i.e.* the difference between each original picture block and the predicted block which is deducted therefrom after the operations performed in the prediction channel 20 between the input of the inverse quantizing circuit 21 and the output of the motion compensation circuit 62.

The device of Fig. 3 also comprises a second variable-length-encoding channel 30 with an associated second prediction channel 40, and a decision sub-assembly 50. The second encoding channel 30, arranged in parallel with the first encoding channel, comprises, at the output of the subtracter 25, a series arrangement of a circuit 31 for suppressing the field interlacing, a second orthogonal transform circuit 32, a second quantizing circuit 33 and a second variable-length encoding circuit 34. The channel 30 also includes the buffer memory 15, as well as a second return connection 36 connecting the buffer memory 15 to the circuit 33, as described hereinbefore, for adjusting the quantization step and the bit rate. Similarly as the first channel, the second prediction channel 40 associated with this channel 30 comprises a series arrangement of a second inverse quantizing circuit 41, a second inverse orthogonal transform circuit 42, a second adder 43, a second picture memory 44 and, in the motion compensation stage 60, a second motion compensation circuit 64. The channel 40 also comprises, in series between the circuits 42 and 43, a circuit for re-interlacing fields. The output of the channel 40, *i.e.* that of the circuit 64, is coupled to that of the first prediction channel 20 (*i.e.* that of the circuit 62) so as to be applied in common to the negative input of the subtracter 25. The second circuits 32, 33, 34, 41, 42, 43, 44, 64 are identical to the first circuits 12, 13, 14, 21, 22, 23, 24, 62, respectively.

The decision sub-assembly 50 comprises a comparison stage and a selection stage. The comparison stage comprises a first counter 51 for counting the number of bits at the output of the encoding circuit 14, a second counter 52 for counting the number of bits at the output of the encoding circuit 34 and a comparator 53 for comparing these two numbers. The selection stage, controlled by the output signal of the comparator 53, comprises a first switch 55 whose non-common terminals are connected to the outputs of the two encoding circuits 14 and 34, respectively and whose common terminal is connected to the input of the buffer memory 15 for applying the output signal of one of these circuits 14 and 24 to said buffer memory, and first and second switches 56 and 57 for connecting or not connecting each prediction channel at the output of the quantizing circuit of the associated encoding channel. A signal S_2 (constituted by a single bit in this case) is supplied by the decision sub-assembly 50 so as to be applied, after transmission, to the decoding device described hereinafter and to indicate whether the lines of the macroblock under consideration have been de-interlaced or not.

This device shown in Fig. 3 operates as follows. It is known that the digital input signals of the device correspond originally to television pictures composed of two interlaced fields, but for which this initial interlacing is converted, macroblock by macroblock, into a sequential arrangement. The above-described device according to the invention uses a given criterion, in this case the *a posteriori* evaluation of the number of bits provided by encoding, with and without interlacing of the lines of each macroblock thus obtained (*i.e.* having this sequential arrangement) for either encoding and prediction of the remaining signals as arranged in Fig. 4 where the lines of the macroblock correspond to the original interlaced fields, or, instead, of de-interlaced signals as shown in Fig. 5 where the eight lines of the odd field are, for example placed in the upper part of the macroblock and the eight lines of the even field are placed in the lower part. In the latter case, the fact that the macroblock is previously de-interlaced provides the possibility of performing the orthogonal transform, followed by quantization and encoding on the basis of coherent blocks. Fig. 2 makes it clear how this coherence is re-established if, in the vertical structure shown in this Fig. 2, the information components situated furthest to the left (lines of an odd field) and the information components situated furthest to the right (lines of the corresponding even field) are now regrouped into upper and lower parts, respectively, of this macroblock

after suppression of the macroblock interlacing.

Conversely, when digital signals originally corresponding to interlaced television pictures are treated, as described hereinbefore, in an encoding device of the type shown in Fig. 3, the signals thus encoded may be decoded in a decoding device of the type as shown in Fig. 6. This decoding device comprises a decoding channel 110 and a prediction sub-assembly 120, and, between this decoding channel and said prediction sub-assembly, a second decision sub-assembly 150.

The decoding channel 110 comprises a series arrangement of a buffer memory 111, a variable-length decoding circuit 112, an inverse quantizing circuit 113, an inverse orthogonal transform circuit 114 (here an inverse discrete cosine transform), as well as a complementary connection 115 between the circuits 112 and 113 intended to furnish the value of the quantization step for the inverse quantizing circuit from the assembly of encoded signals from the encoding device.

The prediction sub-assembly 120 comprises a series arrangement of a picture memory 121 furnishing the output signal of the decoding device, a circuit 122 for prediction on the basis of the contents of the picture memory 121 on the one hand and of each displacement vector also provided by the variable-length decoding circuit 112 on the other hand, (the displacement vectors are also transmitted in said assembly of encoded signals), and an adder 123 whose first input receives the output signal of the decoding channel 110 *via* the second decision sub-assembly 150 and whose second input receives the output signal of said prediction circuit 122. The output of this adder 123 constitutes the output of the decoding device.

The second decision sub-assembly 150 comprises two parallel paths 151 and 152 between the respective non-common terminals of the two switches 153 and 154. The common terminal of the switch 153 receives the output signal of the decoding channel 110 (*i.e.* that of the inverse orthogonal transform circuit 114), while the common terminal of the switch 154 constitutes the first input of the adder 123. The path 151 is a direct path for transmitting the output signal of the decoding channel 110 to the adder 123, while the path 151 ensures the same transmission, but this time *via* a circuit 155 for re-interlacing the fields of the pictures. The switches 153 and 154 are controlled in synchronism by the signal S_2 supplied in the encoding device by the first decision sub-assembly 50 and indicating whether in the encoding section the odd and even lines of the macroblock under consideration have been de-interlaced or not.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A device for encoding digital signals corresponding to interlaced-field pictures, comprising a first variable-length encoding channel (10), which channel comprises a series arrangement of a first section for compressing interlaced data and an encoding section, and, in parallel therewith, a second variable-length encoding channel (30), which channel comprises a series arrangement of a second section for compressing non-interlaced data and an encoding section, and a first channel (20) for prediction on the basis of output signals of said first section and, in parallel therewith, a second channel (40) for prediction on the basis of output signals of said second section, said second section including at its input side a circuit (31) for de-interlacing the fields and said second prediction channel including a circuit (45) for re-interlacing the fields, characterised in that the device also comprises a decision sub-assembly (50) comprising means for comparing the output signals of the first and second encoding channels and means for selecting the prediction and encoding channels in accordance with the result of said comparison.

2. An encoding device as claimed in Claim 1, in which the first variable-length encoding channel (10) comprises a series arrangement of a first orthogonal transform circuit (12) and a first quantizing circuit (13), as well as a first variable-length encoding circuit (14), a buffer memory (15) and a return connection (36) from said memory to the first quantizing circuit (13), in which the first prediction channel (20) comprises, at the output of said quantizing circuit, a series arrangement of an inverse quantizing circuit (21), an inverse orthogonal transform circuit (22), an adder (23), a picture memory (24) and a motion compensation circuit whose output also constitutes the second input of said adder, while the second variable-length encoding channel (30) comprises a series arrangement of a circuit (31) for suppressing the interlacing, a second orthogonal transform circuit (32) and a second quantizing circuit (33), as well as a second variable-length encoding circuit (34), the buffer memory (15) and a return connection 16 from said memory to the second quantizing circuit (33), and the second prediction channel (40) comprises a series arrangement of a second inverse quantizing circuit (41), a second orthogonal transform circuit (42), the circuit (45) for re-interlacing the fields, a second adder (43), a second picture memory (44) and a second motion compensation circuit whose output also constitutes the second input

AUSTRALIAN PATENT OFFICE

of said second adder, the output of said second prediction channel (40) being connected to that of the first prediction channel (2) so as to be applied in common to the negative input of a subtracter (25) arranged at the input side of the two encoding channels, and the positive input of the subtracter (25) receives the signals to be coded; characterised in that the decision sub-assembly (50) comprises a stage for comparing the number of bits provided by coding in the first and second encoding channels, and a stage for selecting the prediction and encoding channels corresponding to the lowest number, said comparison stage comprising counters (51, 52) for counting the number of bits at the output of the encoding circuits (14, 34) and a comparator (53) for comparing these two numbers of bits, and said selection stage comprising a switch (55) for selecting the encoding channel corresponding to that having the lowest of the two numbers of bits, and two switches (56, 57) for selecting the prediction channel corresponding to the encoding channel thus selected.

3. A device for encoding signals corresponding to interlaced-field pictures such as herein described with reference to the accompanying drawings.

Dated this 13th day of December 1996.

PHILIPS ELECTRONICS N V
Patent Attorneys for the Applicant:

F.B. RICE & CO.

AUSTRALIAN PATENT OFFICE

ABSTRACT:

Device for encoding digital signals representing television pictures

Device for encoding interlaced-field picture signals, comprising a first variable-length encoding channel (10) and an associated first prediction channel (20), as well as a second variable-length encoding channel (30), arranged in parallel with the first channel and including at its input side a circuit (31) for de-interlacing the fields, an associated second prediction channel (40) including a circuit (45) for re-interlacing the fields and a decision sub-assembly (50) for comparing the signals supplied by coding in the respective first and second encoding channels and selection of the prediction and encoding channels as a function of the result of said comparison.

Application: Transmission of television signals.

Reference: Fig. 3.

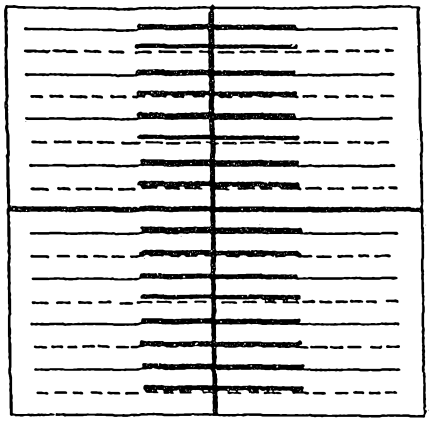

FIG. 1

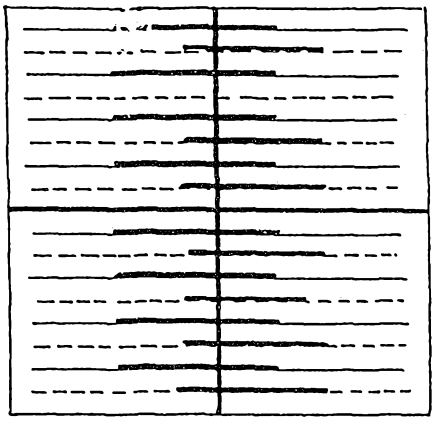

FIG. 2

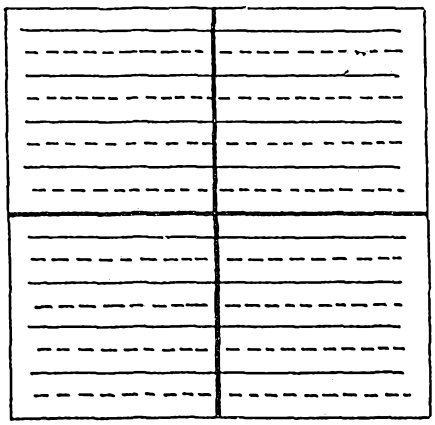

FIG. 4

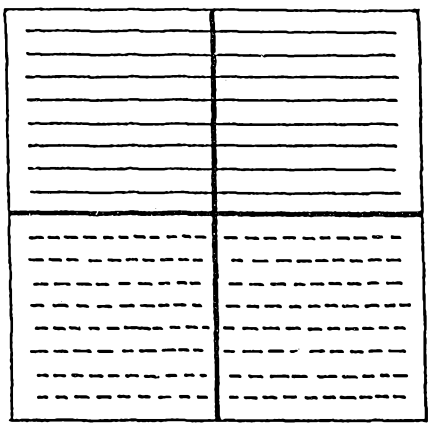

FIG. 5

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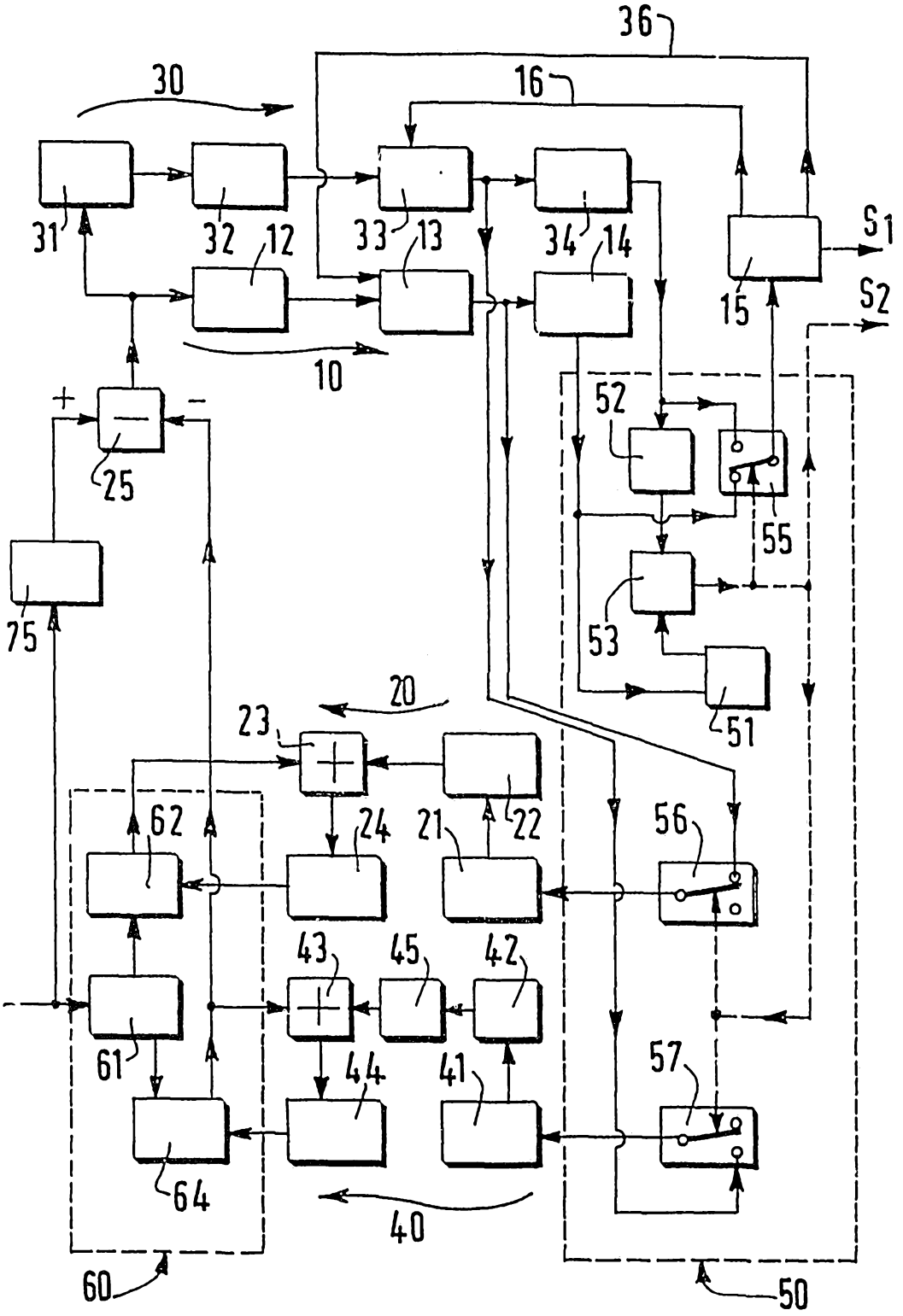
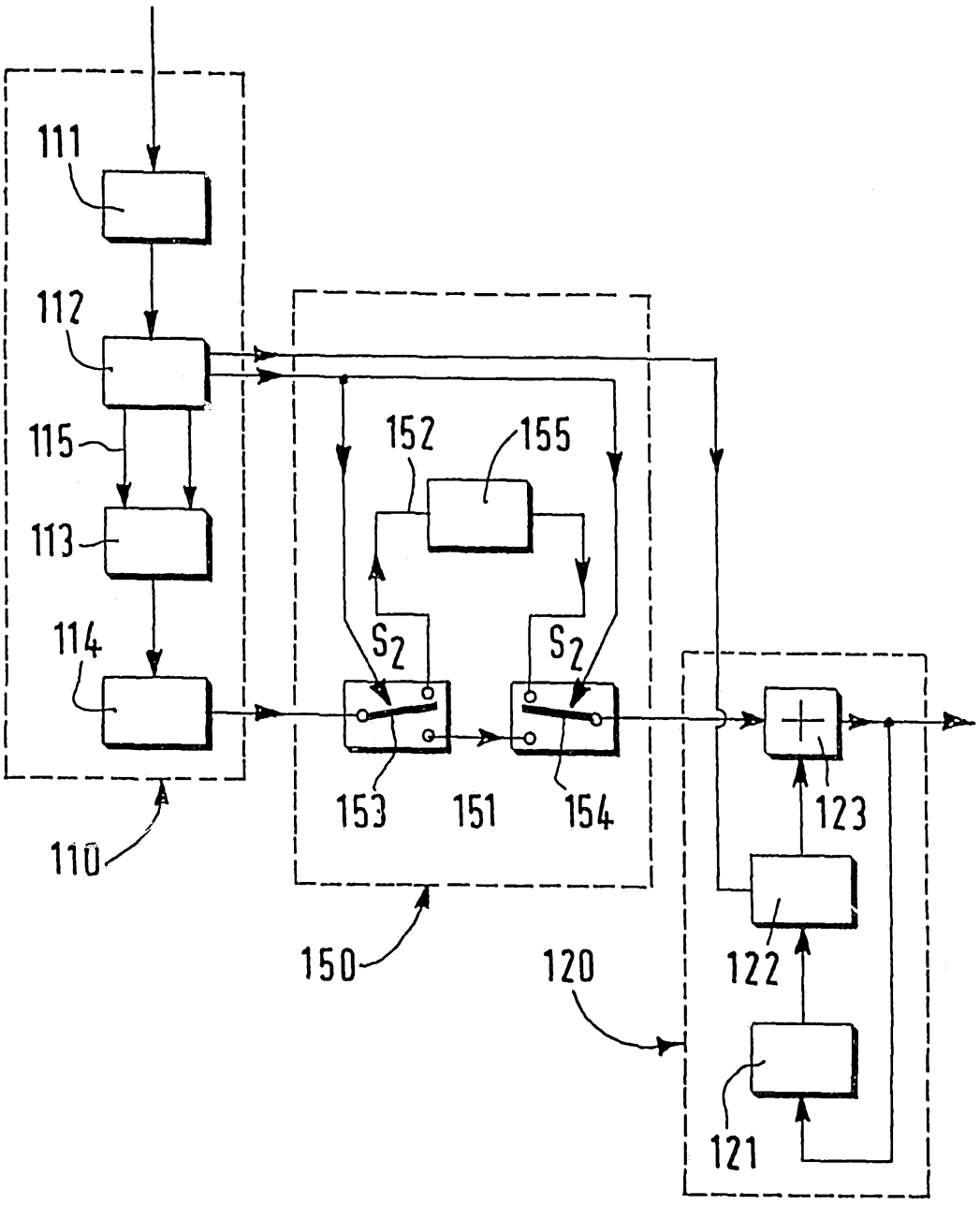


FIG. 3


111
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S_2
S_2
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122
121

FIG. 6