Nov. 20, 1951 G. W. HOBBS 2,575,916

ELECTRIC SELECTING MATRIX

Filed Nov. 30, 1949 2 SHEETS—SHEET 1

Fig. 1.

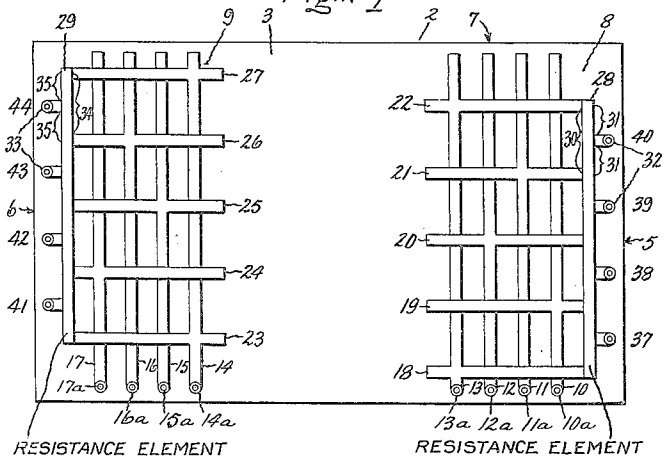


Fig. 3.

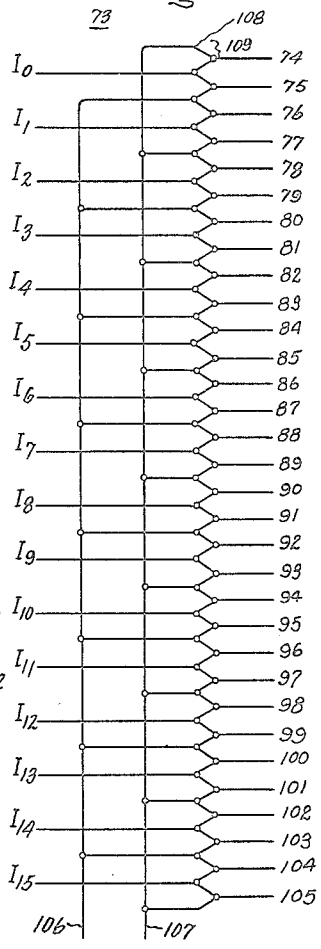
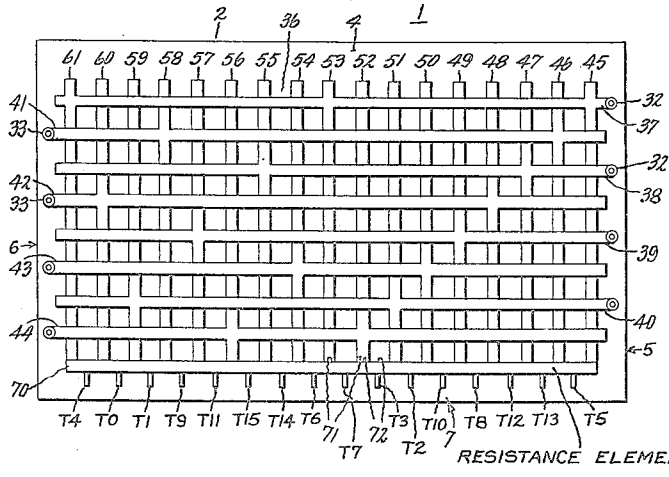


Fig. 1a.



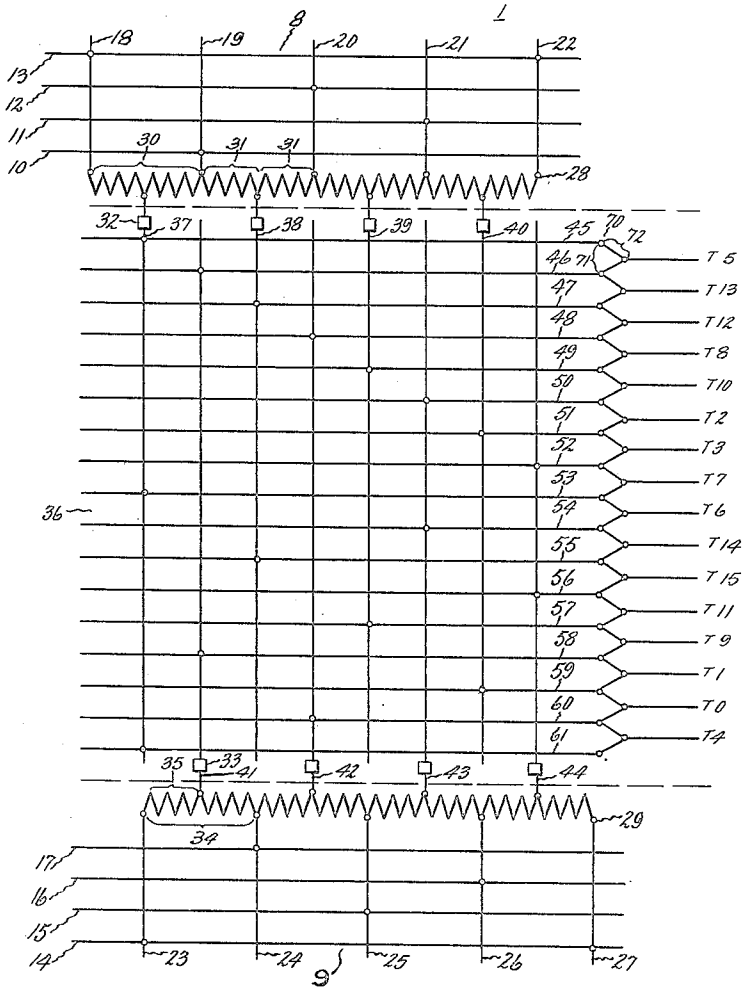
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ELECTRIC SELECTING MATRIX

Filed Nov. 30, 1949 2 SHEETS--SHEET 2

Fig. 2.



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Patented Nov. 20, 1951

2,575,916

UNITED STATES PATENT OFFICE

2,575,916

ELECTRIC SELECTING MATRIX

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Application November 30, 1949, Serial No. 130,144

8 Claims. (Cl. 177—353)

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This invention relates to electric selecting matrices and more particularly to a flat-coded electric selecting matrix.

Selecting matrices are of considerable use in digital calculating devices as well as in other systems in which multiple control of electric circuits is required. Matrices of this type are disclosed, for example, in U. S. Patents 2,428,811 and 2,428,812 to Rajchman.

In conventional selecting matrices, a plurality of input conductors are electrically connected in a predetermined order to a plurality of output conductors by individual resistor units of equal resistance value within restricted resistance tolerance limits. Moreover, where selecting matrices are of the flat-coded type, that is, where the conductors and resistors are of thin substantially linear physical form as is found for example in printed circuits and the like, particular difficulty is experienced in forming resistance units of equal resistance value.

It is an object of this invention to provide a selecting matrix in which the resistor units are more readily and easily formed and in which narrow resistance tolerance difficulties are avoided as compared to conventional selecting matrices.

A further object is to provide a simple reliable flat-coded selecting matrix readily adaptable to low cost manufacturing methods.

In general, my invention consists of a flat-coded selecting matrix comprising a plurality of simple two-family matrices electrically interconnected through common single line resistors tapped to provide segments and sub-segments of equal respective resistance values.

For a complete understanding of my invention reference should be had to the following specification and the accompanying drawings.

Figs. 1 and 1*a* are respectively plan and bottom views of a four pair input, sixteen conductor output, flat-coded selecting matrix illustrative of my invention, Fig. 2 is a diagrammatical view of the selecting matrix shown in Fig. 1 and Fig. 1*a*, and Fig. 3 is a diagrammatical view of a two family matrix having thirty-two outputs illustrative of a modification of my invention.

Referring to Figs. 1 and 1*a* of the drawings, I have shown therein a four pair input, sixteen conductor output flat-coded selecting matrix 1 illustrative of my invention. Selecting matrix 1 comprises a base 2 of any suitable insulation material such as steatite or plastic sheet having flat sides 3 and 4, opposite ends 5 and 6 and an

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edge 7. On side 3 of base 2 respectively adjacent ends 5 and 6 two two-family matrices 8 and 9 are flat-coded as by printing or other suitable process. The matrices 8 and 9 comprise respectively a plurality of spaced input conductors 10–13 and 14–17 having terminal means 10*a*–13*a* and 14*a*–17*a* supported by said base and a plurality of output conductors 18–22 and 23–27.

The conductors 10–27 are flat-coded by any suitable process such as the conventional silk screen process described in the National Bureau of Standards Circular 468 to electrically connect the output conductors of each matrix to its associated input conductors in a predetermined relation, as shown in Fig. 1. The paint used in such printing is a mixture of finely divided silver or copper particles with some binder and may be either air-dried or fired according to the fabricator's preference. Insulation and protection from moisture and short circuits is provided by covering the printed surface with lacquer or similar material. If desired, the lacquer can be applied in conjunction with a mask in order that certain points be left bare. Cross lines can thereafter be over printed with a good conductive bond assured at the required points.

A pair of flat-coded single-line resistors 28 and 29 comprising strips of resistance coating are painted or otherwise formed on the surface 3 of the base 2 adjacent the respective ends 5 and 6 thereof. The spaced output conductors 18–22 of matrix 8 are electrically connected to the resistor 28 at points dividing the resistor into a plurality of segments 30 of equal resistance value. The segments 30 are further divided into subsegments 31 of equal resistance value by a plurality of connectors 32 electrically connected to the resistor 28 at points substantially equidistant between adjacent of the conductors 18–22. The output conductors 23–27 and a plurality of connectors 33 are electrically connected to the resistance 29 in a similar manner, the conductors and connectors being spaced to divide the resistor 29 into segments 34 of equal resistance value and subsegments 35 of equal resistance value. The connectors 32 and 33 are through connectors penetrating through the base 2 and supported thereby.

A third two-family matrix 36 having a first and second plurality of interspaced input conductors 37–40 and 41–44 and a plurality of spaced output conductors 45–61 is printed or otherwise flat-coded, as described for matrices 2 and 3, on side 4 of base 2, as shown in Fig. 1*a*. The input conductors 37–40 and 41–44 are electrically

connected to the output conductors 45–61 in a predetermined relation, as shown in Fig. 1a as the conductors are printed. As seen in Fig. 1a the right hand ends of input conductors 37–40 are connected respectively to the connectors 32 and the left hand ends of the conductors 41–44 are connected respectively to the connectors 33. The output conductors 45–61 terminate at and are electrically connected to a flat-coded single-line resistor 70 formed on side 4 of the base 2 adjacent edge 7 thereof and are spaced to engage the resistor 70 at points dividing the resistor into a plurality of segments 71 of equal resistance value. A plurality of spaced output terminals T0–T15 are electrically connected to the resistor 70 at points intermediate of the output conductors 45–61, as shown in Fig. 1a, to divide each of the segments 71 into subsegments 72 of equal resistance value between each output conductor and its adjacent output terminals.

To show the operation of selective matrix 1 attention is referred to Fig. 2 in which a diagrammatical circuit of the matrix 1 of Fig. 1 is shown. Each of the elements of the matrix 1, shown in Fig. 1, is given the same character reference in Fig. 2. In considering the operation of the matrix 1, as diagrammatically shown in Fig. 2, assume that the input conductors 10–13 and 14–17 of respective matrices 8 and 9 are electrically connected to the outputs of a four stage binary counter (not shown), an example of which may be found in my copending application Serial No. 150,395, filed March 18, 1950, for an Electric Computer and assigned to the same assignee as this present application.

Those skilled in the art will understand that when the inputs 10–17 are connected to a binary counter (not shown), the polarity of the voltages, positive and negative, may be varied on the inputs 10–17 to represent therein the binary equivalents of the decimals 0–15. For example, assuming the voltage condition of inputs 14 and 15 to represent the first digit of a binary number, inputs 16 and 17 the second, 10 and 11 the third and 12 and 13 the fourth digit and further assuming the condition of input 15 positive and input 14 negative, input 17 positive and input 16 negative, input 11 positive and input 10 negative and input 13 positive and input 12 negative to represent the binary character zero in each pair of inputs and the reverse voltage condition to represent the binary character 1 in each pair of inputs, the following table then shows the relationship of voltages on the inputs 10–17 required for the binary equivalents of the decimals 0–15.

Decimal System	Binary Equivalent	Input Voltage Relation							
		13	12	11	10	17	16	15	14
0	0000	+	−	+	−	+	−	+	−
1	0001	+	−	+	−	+	−	−	+
2	0010	+	−	+	−	−	+	+	−
3	0011	+	−	+	−	−	+	−	+
4	0100	+	−	−	+	+	−	+	−
5	0101	+	−	−	+	+	−	−	+
6	0110	+	−	−	+	−	+	+	−
7	0111	+	−	−	+	−	+	−	+
8	1000	−	+	+	−	+	−	+	−
9	1001	−	+	+	−	+	−	−	+
10	1010	−	+	+	−	−	+	+	−
11	1011	−	+	+	−	−	+	−	+
12	1100	−	+	−	+	+	−	+	−
13	1101	−	+	−	+	+	−	−	+
14	1110	−	+	−	+	−	+	+	−
15	1111	−	+	−	+	−	+	−	+

Applying to input conductors 10–17 shown in Fig. 2 the voltage polarity relations produced in accordance with the above table by such a device as a binary counter, it may be seen that multiple switching in a predetermined order is provided by the selective matrix 1 and each of the output terminals T0–T15 are excited with positive voltage in accordance with the operation of the binary counter (not shown). For example, assume that the binary equivalent of the decimal 0 is stored in the binary counter. In this case, the binary equivalent of the decimal 0 being 0000 the voltage relation of input conductors 10–17 as shown in the first line of the above table prevails. Thus, input conductors 13, 11, 17 and 15 are impressed with positive voltage and negative voltage is applied to input conductors 12, 10, 16 and 14. The voltage relation thus established on input conductors 10–17 causes the particular output terminal T0 to be excited. In considering the operation of the matrix 1 producing this result it is seen that conductors 13 and 11 are electrically connected respectively to output conductors 22 and 21 of matrix 8, thus applying a positive voltage to each of the adjacent subsegments 31 of the resistor 28 between the output conductors 21 and 22 of matrix 8. By applying a positive voltage to each of the subsegments 31 of resistor 28 between the conductors 21 and 22 a positive voltage is applied to input conductor 40 of matrix 36 which in turn applies a positive voltage to output conductors 51 and 59 electrically connected thereto. In a similar manner input conductors 17 and 15 of matrix 9 being positive in accordance with the first line of the above table, a positive voltage is applied to output conductors 48 and 60 of matrix 36 through input conductor 42 of matrix 36 and subsegments 35 of resistor 29 between the output conductors 24 and 25 of matrix 9 which are respectively electrically connected to the input conductors 17 and 15. Thus adjacent output conductors 59 and 60 of matrix 36 are each impressed with positive voltage which is applied therethrough to the subsegments 72 of the resistor 70 adjacent the output terminal T0 to produce a predetermined positive output voltage thereon indicating the storage of the binary 0000 in the binary counter. It will be noted that under the assumed voltage relation of input conductors 10–17 corresponding to the decimal 0 none of the remaining terminals T1–T15 have two positive voltages applied thereto from adjacent of the conductors 45–61. Therefore, a positive output voltage of predetermined value is applied only to terminal T0 corresponding to the decimal 0.

In a similar manner, as successive numbers appear in the binary counter, a predetermined output voltage is switched through the selecting matrix 1 to a particular one of the output terminals T0–T15 corresponding to the number stored in the binary counter. The above is merely an illustration of the operation of the selecting matrix 1 as applied to a binary counter. This electrical selecting matrix or network may be characterized as a multiple stage network having two states, the first including matrices 8 and 9 and the second comprising matrix 36.

It is understood that in application of the selecting matrix 1 the output terminals T0–T15 are electrically connected to an associated grounded electric circuit to be energized from the terminals T0–T15 and that the negative side of the supply source for the binary counter used to energize the selecting matrix 1 is also grounded to provide a complete operable circuit. Each of the terminals T0–T15 for example may be connected to a neon tube or other signal de-

vice the opposite side of which is grounded so that the associated signal device is energized when a positive voltage of the predetermined value appears on some one of the terminals T0–T15. The terminals T0–T15 may also be connected to such digital calculating devices as for example electronic counters, registers or connecters, or to a combination of such devices depending upon the particular use.

Selecting matrices have many other fields of application in addition to digital calculations and conventional selecting matrices may be applied to such applications. However, an important feature of my invention is the fact that the switching above described is accomplished with a matrix having only three single line resistors namely, 28, 29 and 70. In conventional matrices, as for example, the matrices disclosed by Dr. Jan Rajchman in his U. S. Patents 2,428,811 and 2,428,812, a considerably greater number of individual resistors is required. For example, in the four pair input 16 output circuit described above a total of 64 individual resistors is required in a conventional matrix. This number has been reduced to a total of 48 individual resistors which corresponds to the total number of subsegments in the selective matrix 1 described above. Further, by collecting the single resistors into associated groups forming one resistance for each group the total number of single-line resistances in my matrix has been reduced to 3.

The advantage of reducing the number of resistors in a flat-coded matrix lies in the fact that whereas a single-line resistor can be controlled reasonably well for resistivity throughout its length, control of resistance from one unit resistor to another to produce separate unit resistors of equal resistance value is relatively difficult.

Therefore by my invention, I have provided an improved simple, reliable, flat-coded selecting matrix more readily adaptable to low cost manufacturing methods.

It should be noted that my invention is not to be limited to the preferred embodiment illustrated by Fig. 1 as other forms of base may also be used to advantage in certain cases. That is, the base may take any suitable form, as for example, a cylinder or toroid, and the matrices may be flat-coded on one side only of the base, if desired.

Further, the invention is not to be confined to equal size matrices. For example, in Fig. 3, I have shown in diagrammatical form a two family thirty-two output flat-coded selective matrix 73 illustrative of a modification of my invention. In matrix 73 the sixteen input conductors are numbered I_0–I_{15} to correspond with the outputs T0–T15 of the matrix shown in Figs. 1 and 2 as the voltages impressed on I_0–I_{15} may be obtained by connecting the output terminals T0–T15 of the matrix 1 respectively to the inputs I_0–I_{15} of the selecting matrix 73. The thirty-two outputs of matrix 73 are obtained by connecting a plurality of terminals 74–105, the inputs I_0–I_{15} and an additional pair of inputs 106 and 107 to a single-line resistor 108 in spaced relation therealong, as shown in Fig. 3, to provide subsegments 109 of equal resistance value. Thus, a thirty-two output selecting matrix is formed of inputs derived from one and two-family matrices as compared to the sixteen output selecting matrix illustrated by Figs. 1 and 2 and derived from the two two-family matrices 8 and 9.

While I have shown and described a particular embodiment of my invention, it will be obvious to those skilled in the art that various changes and modifications may be made without departing from my invention in its broader aspects and I, therefore, aim in the appended claims to cover all such changes and modifications as fall within the true spirit and scope of my invention.

What I claim as new and desire to secure by Letters Patent of the United States is:

1. A flat-coded electric selecting matrix comprising a base of insulation material, a plurality of two-family matrices, a plurality of single-line resistor means tapped at spaced points to produce segments and subsegments of equal respective resistance values, a plurality of output terminals electrically connected to particular ones of said tap points on one of said resistor means, said two-family matrices being electrically interconnected in a predetermined relation through the remainder of said tap points of said one resistor means and tap points of the others of said resistor means.

2. An electric selecting matrix comprising a base of insulation material, a plurality of two-family electric matrices secured to said base, a plurality of single-line resistor means fixed to said base, said two-family matrices being electrically connected each to a particular one of said resistor means in a predetermined relation at points along said resistor means dividing each into segments of equal resistance value and subsegments of equal resistance value, an additional single-line resistor means fixed to said base and electrically connected to one of said matrices in a predetermined relation to divide said additional resistor means into additional segments of equal resistance value, and a plurality of output terminals supported by said base and electrically connected to said additional resistor at points thereon dividing each of said additional segments into additional subsegments of equal resistance value.

3. An electric selecting matrix comprising two electric conductor matrices each provided with a plurality of input conductors and a plurality of output conductors, a continuous resistor for each of said matrices, electric connections between said output conductors of each of said matrices and equally resistance spaced points of its said resistor, a third matrix provided with a plurality of input conductors and a plurality of output conductors, electric connections between alternate input conductors of said third matrix and said resistors, respectively, at midway resistance points between said connections with the output conductors of said first and second matrices, a third resistor, electric connections between the output conductors of said third matrix and equally resistance spaced points of said third resistor, output terminals connected to said third resistor at midway resistance points between said output conductor connections, and electric connections between the input and output conductors of each of said matrices providing for a voltage of predetermined polarity on any selected one of said terminals in response to selected polarities of said input conductors of said first and second matrices.

4. An electric selecting matrix comprising two electric conductor matrices each provided with pairs of input conductors and an odd number of output conductors, a continuous resistor for each of said matrices, electric connections between said output conductors of each of said matrices and equally resistance spaced points of its said re-

sistor, a third matrix provided with a plurality of input conductors and a plurality of output conductors, electric connections between alternate input conductors of said third matrix and said resistors, respectively, at midway resistance points between said connections with the output conductors of said first and second matrices, a third resistor, electric connections between the output conductors of said third matrix and equally resistance spaced points of said third resistor, output terminals connected to said third resistor at midway resistance points between said output conductor connections, and electric connections between the input and output conductors of each of said matrices providing for a voltage of predetermined value and polarity on any selected one of said terminals in response to selected polarities of each of said pairs of input conductors of said first and second matrices.

5. A flat-coded electric selecting matrix comprising a base of insulation material having opposite ends and flat opposite sides, first and second two-family matrices flat-coded on one side of said base respectively adjacent opposite ends thereof, and a third two-family matrix flat-coded on the opposite side of said base, each of said matrices comprising a plurality of spaced input conductors, a plurality of spaced output conductors electrically connected to said input conductors in a predetermined relation, first, second and third resistors respectively electrically connecting associated ends of said output conductors of said first, second and third matrices, said output conductors being spaced to provide in each of said resistors segments of equal resistance value between adjacent output conductors, connections for connecting each of said first and second resistors to particular ones of said input conductors of said third matrix, said input connectors being connected each to the resistance center of a particular one of said segments of said first and second resistors to provide subsegments of said resistors of equal resistance value, a plurality of input terminals on said base electrically connected to said input conductors of said first and second matrices and a plurality of output terminals on said base each electrically connected to the resistance center of a particular one of said segments of said third resistor of said third matrix to provide subsegments of said third resistor of equal resistance value between adjacent ones of said third matrix output conductors.

6. An electric selecting matrix comprising a base of insulation material, a plurality of two-family matrices flat-coded on said base, each of said matrices comprising a plurality of input and a plurality of output conductors electrically interconnected in a predetermined relation, said input conductors of one of said matrices being divided into groups of associated input conductors, terminal means supported by said base for said input conductors of said matrices other than said one matrix, a plurality of substantially flat single-line resistor means fixed to said base, said output conductors of each of said matrices being connected to a particular one of said resistor means at points dividing said resistor means into segments of equal resistance value, connections for electrically connecting said resistor means each to particular ones of said groups of associated input conductors, said connections being electrically connected to said resistor means at points intermediate of said first mentioned points to divide each of said resistors into subsegments of equal resistance value, an additional substantially flat single-line resistor means fixed to said base, said output conductors of said one matrix being electrically connected to said additional resistor means at points dividing said resistor means into segments of equal resistance value, a plurality of output terminal means on said base for said selecting matrix electrically connected to said additional resistance means at points intermediate of said last mentioned points and further dividing said additional resistor means into subsections of equal resistance value.

7. An electric selecting matrix comprising a base of insulation material having opposite ends and flat opposite sides, first and second two-family matrices flat-coded on one side of said base respectively adjacent opposite ends thereof, each of said matrices comprising a plurality of spaced input conductors, terminal means electrically connected to said input conductors, a plurality of spaced output conductors electrically connected to said input conductors in a predetermined relation, a resistor electrically connecting corresponding ends of said output conductors, said output conductors being spaced to provide segments of said resistor of equal resistance value between adjacent output conductors, and a plurality of connector means on said base each electrically connected to the resistance center of a particular one of said segments to provide sub-segments of said resistor of equal resistance value, each of said connector means extending through said base, a third two-family matrix flat-coded on the opposite side of said base, said third matrix comprising a first and second plurality of spaced input conductors and a plurality of spaced output conductors, said first plurality of input conductors being electrically connected in a predetermined relation to said connector means of said first matrix, said second plurality of input conductors being electrically connected in a predetermined relation to said connector means of said second matrix, said output conductors of said third matrix being electrically connected to particular one of said first and second plurality of input conductors in a predetermined relation, a third resistor electrically interconnecting adjacent ends of said output conductors of said third matrix, said output conductors being spaced to provide segments of said third resistor of equal resistance value between adjacent output conductors, and a plurality of output terminals on said base each electrically connected to the resistance center of a particular one of said last mentioned segments to provide subsegments of said third resistor of equal resistance value.

8. A multiple-stage electrical selecting network, each stage comprising one or more separate electrical matrices having input terminals and output terminals, the output terminals of prior stages being connected to the input terminals of the next subsequent stages, each of said matrices comprising input conductors extending from said input terminals, output conductors suitably respectively directly crossconnected with said input conductors and a single resistor element having a plurality of equally spaced equal resistance taps, alternate ones of said taps being connected to said output conductors and said output terminals whereby simultaneous application of a voltage to two adjacent output conductors causes a similar voltage at the output terminal connected to the resistor tap inter-

mediate the resistor taps to which said two adjacent output conductors are connected.

GEORGE W. HOBBS.

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The following references are of record in the file of this patent:

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Number	Name	Date
2,428,811	Rajchman	Oct. 14, 1947

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