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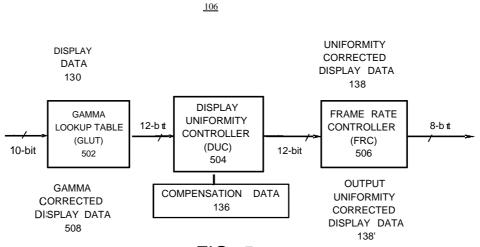


FIG. 5

(57) Abstract: A frame rate controller method and system are provided. Including a data separator separating the display data into an integer part comprising upper bits of the display data, and a fraction part (Din_f) comprising lower bits of the display data; a high/low generator generating a data out high value equal to the integer part plus one and a low value equals the integer part; a multiplier responsive to receiving a frame counter value and the Din_f for outputting a first and a second multiplication result; a pixel sequence LUT containing a pattern of sequence numbers output based on horizontal pixel and vertical line counter values; a comparator for generating a code based on a comparison of the sequence number and the output from the multiplier, wherein the code multiplexes the data out high value and the data out low value from the high/low generator.





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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) WESTfUSPT.PGPB.EPAB.JPAB.USOCR); DialogPR θ (Eng tneering); Google Search terms: frame rate control dither multiply number sequence lower least fraction bit next subsequent adjacent previous temporal image motion sequence LUT look up table pattern address location tile window matrix video pixel greater less than intermediate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/0197776 A1 (MORGAN et al.) 07 September 2006 (07.09.2006), para [0020]-[0024], [003]-[0044], [0052], [0053], [0060]-[0062].	1-3, 5-10, 12-14
Y		4, 11
Υ	US 2005/0024381 A1 (DOTSON et al.) 03 February 2005 (03.02 2005), para [0138H0141].	4, 11
Α	US 2004/0160455 A 1 (WEITBRUCH et al.) 19 August 2004 (19.08.2004), para [0048]-[0050].	1,8
Α	US 2004/0066363 A 1 (YAMANO et al.) 08 April 2004 (08.04.2004), para [0713]-[0715], [0734].	1, 8
Α	US 2005/0219176 A 1 (SONG) 06 October 2005 (06 10.2005), para [0034]-[0036].	1, 8

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