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[Continued on next page]

(54) **Title:** SOLVING UNSTABLE UNIVERSAL ASYNCHRONOUS RECEIVE TRANSMIT (UART) COMMUNICATION BETWEEN A POWER MANAGER AND A UNIVERSAL SERIAL BUS (USB) - BRIDGE DEVICE

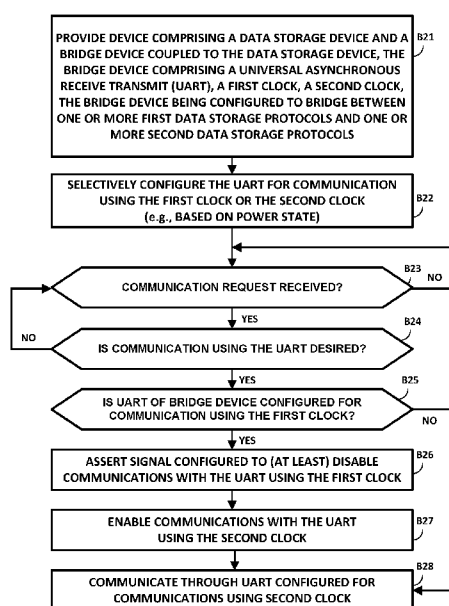


FIG. 2

(57) **Abstract:** A device may comprise data storage, a power manager and a bridge device that is coupled to the data storage and to the power manager, and configured to bridge between at least a first data protocol and at least a second data protocol. The bridge device may comprise a UART, a first clock, a second clock and bridge device firmware configured to cause the bridge device to selectively configure the UART for communication using the first clock or the second clock. The power manager may be configured to, when a command is to be issued to the data storage when the bridge device firmware has configured the UART for communication using the first clock, assert a signal that causes the bridge device firmware to stop configuring the UART for communication using the first clock and to configure the UART for communication using the second clock.

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- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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SOLVING UNSTABLE UNIVERSAL ASYNCHRONOUS RECEIVE TRANSMIT (UART) COMMUNICATION BETWEEN A POWER MANAGER AND A UNIVERSAL SERIAL BUS (USB) – BRIDGE DEVICE

BACKGROUND

[0001] Embodiments are related to devices and methods for solving unstable Universal Asynchronous Receive Transmit (UART) communications between a power manager device a Universal Serial Bus (USB) bridge device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] Fig. 1 is a block diagram of a device according to one embodiment.

[0003] Fig. 2 is a flowchart of a method according to one embodiment.

DETAILED DESCRIPTION

[0004] Fig. 1 is a block diagram of a device 100 according to one embodiment. As shown, device 100 may comprise a power manager device 104 and a bridge device 106. The bridge device 106 may be coupled to the data storage device and to the power manager device 104. The bridge device 106 may be configured to bridge between one or more first data protocols 124 and one or more second data protocols 126. For example, the first data protocol may include USB as shown at 116 or eSATA (external Serial AT Attachment) as shown at 118. The second data protocol 126 may include, for example, SATA as shown at 120 or SPI (Serial peripheral Interface) as shown at 122, to identify but a few possible data protocols. As also shown in Fig. 1, the bridge device 106 may comprise a UART 108, a first clock 110, a second clock 112 and bridge device firmware 114.

[0005] In one embodiment, the first clock 110 may be or may comprise a ring oscillator, which is a device composed of an odd number of logical NOT gates whose output oscillates between two voltage levels, representing true and false. The NOT gates, or inverters, are attached in a chain and the output of the last inverter is fed back into the first. In one embodiment, the second clock 112 may be or comprise a phase-locked loop (PLL) oscillator. A PLL is a control system that generates an output signal whose phase is related to the phase of an input signal. A PLL comprises a variable frequency oscillator and a phase detector. The oscillator generates a periodic signal. The phase detector compares the phase of that signal

with the phase of the input periodic signal and adjusts the oscillator to keep the phases matched. The output signal is brought back toward the input signal for comparison in a feedback loop and the phase difference between the input and the output is used to adjust the frequency of the variable frequency oscillator.

[0006] In one implementation, the bridge device 106 may comprise a JMS562 USB3.0 & eSATA GEN III to Dual SATA GEN III Ports Bridge chip, manufactured by JMicron Technology Corp. The device 100 may, according to one embodiment, facilitate communications between, for example, a computing device coupled to one of the USB ports 116 or eSATA ports 118 and direct access storage devices (DASDs) 122 coupled to SATA or SPI ports 118, 120.

[0007] To save power, bridge device 106 may transition to a low power mode when the device is in suspended or sleep mode or when, for example, no interface cables are plugged in to the communication ports 116, 118, 118 and/or 120. In that case, the UART 108 may be configured to run on the first clock 110, which may include the aforementioned ring oscillator. However, the ring oscillator may have an unacceptably high UART error data rate. When the UART 108 is clocked by the first clock, therefore, it may fail to communicate with the power manager in the low power mode. Therefore, the device 100 may fail to operate (e.g., boot up) reliably. The same device 100, however, may well operate with wholly acceptable error data rates when the UART 108 is clocked by a more precise clock such as second clock 112 configured as a PLL oscillator. Bridge device firmware 114 may be stored in non-volatile or non-transient memory in the form of instructions that, when executed, cause the device 100 to cause the bridge device 106 to selectively configure the UART 108 for communication using either the first clock 110 or the second clock 112.

[0008] According to one embodiment, the power manager device 104 may be configured such that, when a command is to be issued to the data storage device 102 when the bridge device firmware 114 has configured the UART 108 for communication using the first clock 110, a signal is asserted that causes the bridge device firmware 114 of the bridge device 106 to stop configuring the UART 108 for communication using the first clock 110 and to configure the UART 108 for communication using the second clock 112. In this manner, the power manager 104 may cause the bridge device to switch its UART from being clocked by a less precise

first clock (e.g., a ring oscillator) to being clocked by a comparatively more precise second clock (e.g., a PLL oscillator), to ensure a substantially decreased error data rate. This substantially decreased error data rate may be ensured even when the device 100 is in a low power mode in which the UART is configured to use less power-consuming but also less precise UART clocks.

[0009] The bridge device 106 may comprise a plurality of General Purpose Input Output (GPIO) ports. According to one embodiment, the signal asserted by the power manager 104 and received by the bridge device and acted upon by the bridge firmware 114 may be asserted on a selected one of the GPIO ports of the bridge device 106. In the exemplary implementation in which the bridge device comprises a JMS562 Application Specific Integrated circuit (ASIC), the power manager 104 may be configured to use the LINK_STATUS_562 GPIO line to signal the JMS562 to exit suspend or sleep mode when the power manager has a command to send to the JMS562. Upon sensing the assertion of the LINK_STATUS_562 GPIO line, the JMS562 may, according to one embodiment, stop configuring the UART 108 from being clocked by the first clock 110 and will configure the UART 108 for communication using the second clock 112, in effect, switching the UART 108 from being clocked by its internal ring oscillator to being clocked by a PLL oscillator, which is a mode of operation that provides a reliable clock for the UART communication with the power manager 104.

[0010] When the bridge device 106 is in suspend or sleep mode, it may configure the UART 108 to use the first clock 110. To cause the bridge device to, in effect, wake up from its suspend or sleep mode and cause the UART to use the second clock 112 for communication with the power manager 104, the power manager 104 may be configured to set a selected GPIO line of the bridge device (e.g., the LINK_STATUS_562) to a logical high to signal the bridge device 106 to JMS562 to exit the suspend or sleep mode. Firmware of the power manager 104 may be configured to assert the bridge device's GPIO line upon detection of a predetermined event. According to one embodiment, such predetermined event may comprise, for example, a button press, USB cable plug or unplug event, a Thunderbolt cable plug or unplug event, DASDs turned OFF, among other possibilities. In one implementation, once the bridge device 106 has exited suspend or sleep mode and has successfully switched from using the first clock 110 to using

the second clock 112 for UART clocking, the power manager 104 may send, and the bridge device 106 may receive, a first command (the “N” command, for example) and the bridge device 106 may receive all the events one at a time and perform the actions associated therewith. When there are no more events, the power manager 105 may send, and the bridge device 106 may receive, a second command (the “EON” (End of Notification) command, for example), whereupon the power manager 104 may reset the previously set GPIO line (e.g., the LINK_STATUS_562) of the bridge device to a logical low. In this state, the bridge device may continue to clock its UART using the second clock 112 for a period of time or may stop using the second clock 112 and resume clocking its UART 108 with the first clock 110 and resume its suspend or sleep mode, to conserve power or for any other purpose.

[0011] Significantly, causing the bridge device 106 to switch its UART clocking from the first clock 110 to its second clock 112 enables the power manager to reliably communicate with the bridge device 106 when the bridge device is in suspend or sleep mode, without requiring the power manager 104 to initiate iterative and time consuming training sequences in which an acceptable BAUD rate is negotiated at which the bridge device and power manager may communicate without unacceptable data error rates.

[0012] Fig. 2 is a flowchart of a method according to one embodiment. As shown therein, block B21 calls for providing a device comprising a data storage device and a bridge device coupled to the data storage device. As shown in B21, the bridge device may comprise a UART, a first clock, a second clock, and the bridge device may be configured to bridge between at least a first data protocol and at least a second data protocol. The UART may then be selectively configured, as shown at B22, for communication using the first clock or the second clock. For example, in a low power state such as a suspend or sleep mode, the UART may be configured for communication using the first clock. In a higher-power state or normal power mode (i.e., non- suspend or sleep mode), the UART may be configured for communication using the second clock.

[0013] At B23, it may be determined whether a communication request (e.g., from the power manager 104) has been received. This may be determined, according to one embodiment, by monitoring the high/low status of a selected GPIO line on the bridge device 106. For example, as long as no communication request is

detected (NO branch of B23), no further action need be taken. In this state, the bridge controller may continue to clock the UART 108 using the first clock 110 as it would otherwise do when in suspend or sleep mode. Alternatively, the bridge device 108 may continue to clock its UART 108 using the second clock 112 if it was previously in a normal mode (i.e., non-suspend or sleep mode) or may continue to clock its UART 108 using the second clock 112 for a period of time and switch back to clocking the UART 108 using the first clock 110 after some period of time, to conserve power.

[0014] If the power manager 104 requests communications with the bridge device 108 (YES branch of B23), it may be determined whether communication with the UART is desired, as shown at B24. If no (NO branch of B24), the method may revert back to B23. If communication with the UART is indeed desired (YES branch of B24), it may then be determined whether the UART 108 of the bridge device 106 is currently configured for communication using the first clock, as called for by B25. If not (NO branch of B25), communication through the UART may be configured using the second clock 112, as shown at B28. If, however, the UART 108 of the bridge device 106 is, in fact, configured for communication using the first clock 110 (YES branch of B25), then a signal may be asserted to (among other possible uses), disable communication with the UART using the first clock 110, as shown at B26. Communication with the UART 108 of the bridge device 106 may then be enabled using the second clock 112, as shown at B27. After having been so enabled, communications may proceed through the UART 108 that has been configured for communication using the second clock 112 (that includes a PLL oscillator, for example), as shown at B28.

[0015] According to one embodiment, the bridge device 106 referred to in Fig. 2 may further comprise a plurality of GPIO ports and block B26 may be carried out by asserting the signal on a selected one of these GPIO ports. In one embodiment, the first clock of Fig. 2 may be or comprise a ring oscillator and the second clock of Fig. 2 may be or comprise a PLL oscillator. Recall that B22 calls for the UART 108 to be selectively configured for communication using the first clock or the second clock. In one embodiment, this selective configuration may comprise configuring the UART 108 for communication using the first clock 110 when the bridge device 106 is in a first mode such as, for example, a low power mode. This

selective configuring may also configure the UART 108 for communication using the second clock 112 when the bridge device 106 is in a second mode such as, for example, a normal operation power mode.

[0016] In B26, a signal may be asserted, which signal may be configured to disable communications with the UART 108 using the first clock. In one embodiment, asserting this signal may be carried out upon occurrence of a selected event. Although by no means a complete list, exemplary ones of such a selected event may include, for example, an issued command, a data storage device-related event, a cable plug or unplug-related event and/or a button press-related event. Indeed, the firmware of the power manager 104 may be configured to assert the bridge device's GPIO line upon detection of any one of these events or upon detection of another selected event.

[0017] In B27 or B28, after the UART 108 has been configured for communication using the second clock 112, a notification signal, one or more commands, and/or an end of notification signal may be sent. Thereafter, when there are no more events, the power manager 105 may send, and the bridge device 106 may receive, another end of notification command. The power manager 104 may then reset the previously set GPIO line (e.g., the LINK_STATUS_562) of the bridge device to a logical low. In this state, the bridge device may continue to clock its UART using the second clock 112 for a period of time or may stop using the second clock 112 and resume clocking its UART 108 with the first clock 110 and resume its suspend or sleep mode, to conserve power or for any other purpose.

[0018] While certain embodiments of the disclosure have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods, devices and systems described herein may be embodied in a variety of other forms. Furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure. For example, those skilled in the art will appreciate that in various embodiments, the actual physical and logical structures may differ from those shown in the figures. Depending on the embodiment, certain steps described in the

example above may be removed, others may be added. Also, the features and attributes of the specific embodiments disclosed above may be combined in different ways to form additional embodiments, all of which fall within the scope of the present disclosure. Although the present disclosure provides certain preferred embodiments and applications, other embodiments that are apparent to those of ordinary skill in the art, including embodiments which do not provide all of the features and advantages set forth herein, are also within the scope of this disclosure. Accordingly, the scope of the present disclosure is intended to be defined only by reference to the appended claims.

CLAIMS

1. A device, comprising:

a data storage device;

a power manager device; and

a bridge device coupled to the data storage device and to the power manager device, configured to bridge between at least a first data protocol and at least a second data protocol, the bridge device comprising a Universal Asynchronous Receive Transmit (UART), a first clock, a second clock and bridge device firmware configured to cause the bridge device to selectively configure the UART for communication using one of the first clock and the second clock,

wherein the power manager device is configured to, when a command is to be issued to the data storage device when the bridge device firmware has configured the UART for communication using the first clock, assert a signal that causes the bridge device firmware to stop configuring the UART for communication using the first clock and to configure the UART for communication using the second clock.

2. The device of claim 1, wherein the bridge device further comprises a plurality of General Purpose Input Output (GPIO) ports and wherein the power manager is configured to assert the signal on a selected one of the GPIO ports.

3. The device of claim 1, wherein the first clock comprises a ring oscillator.

4. The device of claim 1, wherein the second clock comprises a Phase Locked Loop (PLL) oscillator.

5. The device of claim 1, wherein the bridge device is configured to configure the UART for communication using the first clock when the bridge device is in a first mode.

6. The device of claim 5, wherein the first mode includes a low power mode.

7. The device of claim 1, wherein the bridge device is configured to configure the UART for communication using the second clock when the bridge device is in a second mode.

8. The device of claim 7, wherein the first mode includes a normal operation power mode.

9. The device of claim 1, wherein the power manager is further configured to assert the signal upon occurrence of a selected event.

10. The device of claim 9, wherein the selected event comprises at least one of an issued command, a data storage device-related event, a cable plug or unplug-related event and a button press-related event.

11. The device of claim 1, wherein the power manager is further configured send to the bridge device, after the UART has been configured for communication using the second clock send, a notification signal, one or more commands, and an end of notification signal.

12. A method, comprising:

providing a device comprising a data storage device and a bridge device coupled to the data storage device, the bridge device comprising a Universal Asynchronous Receive Transmit (UART), a first clock, a second clock, the bridge device being configured to bridge between at least a first data protocol and at least a second data protocol;

selectively configuring the UART for communication using one of the first clock and the second clock; and

when a command is to be issued to the data storage device and the UART is configured for communication using the first clock, asserting a signal configured to disable communications with the UART using the first clock and enable communications with the UART using the second clock.

13. The method of claim 12, wherein the bridge device further comprises a plurality of General Purpose Input Output (GPIO) ports and wherein asserting the signal comprises asserting a signal on a selected one of the GPIO ports.

14. The method of claim 12, wherein providing is carried out with the first clock comprising a ring oscillator.

15. The method of claim 12, wherein providing is carried out with the second clock comprising a Phase Locked Loop (PLL) oscillator.

16. The method of claim 12, wherein selectively configuring comprises configuring the UART for communication using the first clock when the bridge device is in a first mode.

17. The method of claim 16, wherein the first mode includes a low power mode.

18. The method of claim 12, wherein selectively configuring comprises configuring the bridge device to configure the UART for communication using the second clock when the bridge device is in a second mode.

19. The method of claim 18, wherein the second mode includes a normal operation power mode.

20. The method of claim 12, wherein asserting is further carried out upon occurrence of a selected event.

21. The method of claim 20, wherein the selected event comprises at least one of an issued command, a data storage device-related event, a cable plug or unplug-related event and a button press-related event.

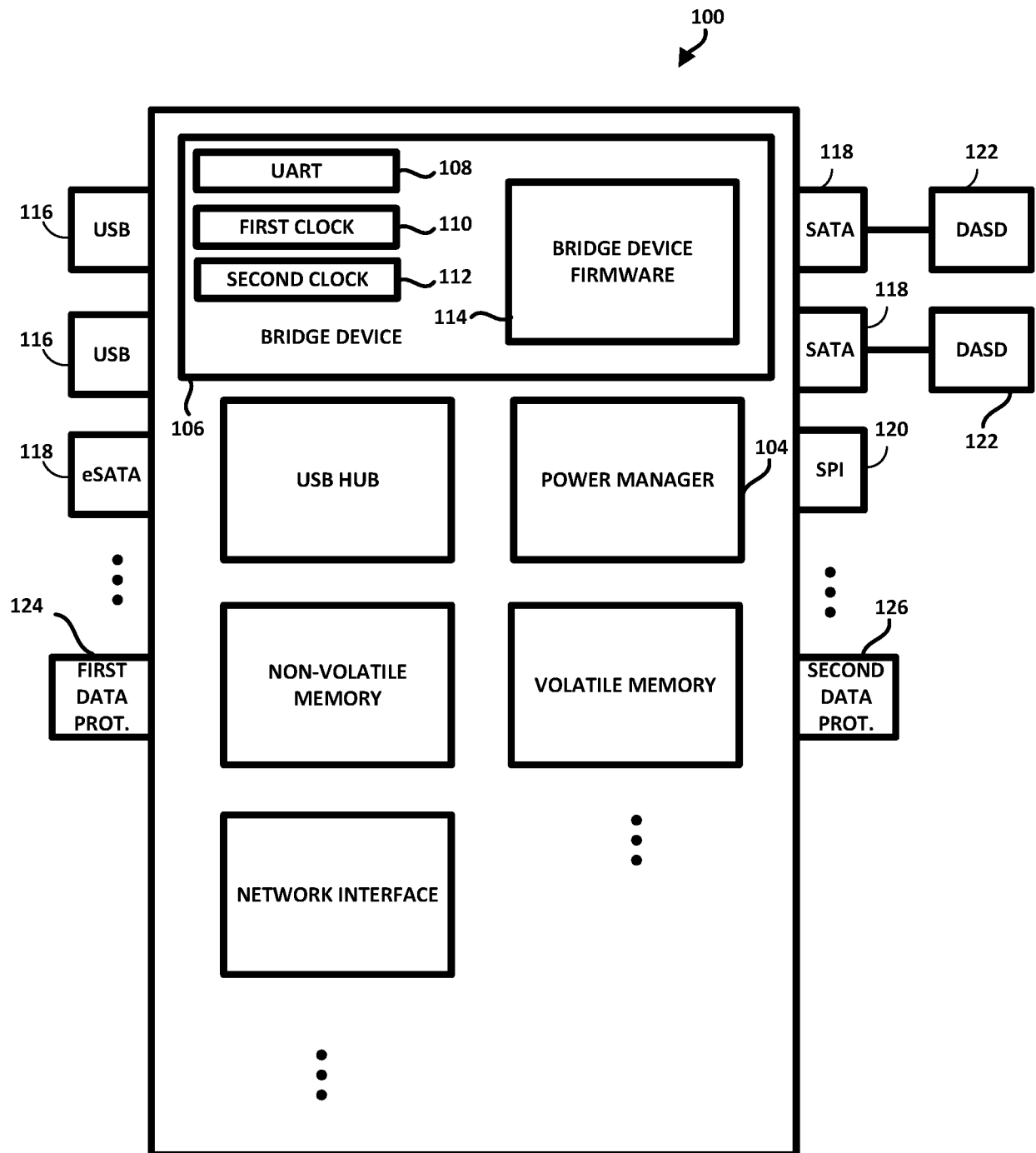
22. The method of claim 12, further comprising sending to the bridge device, after the UART has been configured for communication using the second clock send, a notification signal, one or more commands, and an end of notification signal.

23. A circuit board, comprising:

a power manager device; and

a bridge device configured to couple to the power manager device, the bridge device being configured to couple to a data storage device and to bridge between at least a first data protocol and at least a second data protocol, the bridge device comprising a Universal Asynchronous Receive Transmit (UART), a first clock, a second clock and bridge device firmware configured to cause the bridge device to selectively configure the UART for communication using one of the first clock and the second clock,

wherein the power manager device is configured to, when a command is to be issued to the data storage device when the bridge device firmware has configured the UART for communication using the first clock, assert a signal that causes the bridge device firmware to stop configuring the UART for communication using the first clock and to instead configure the UART for communication using the second clock.

*FIG. 1*

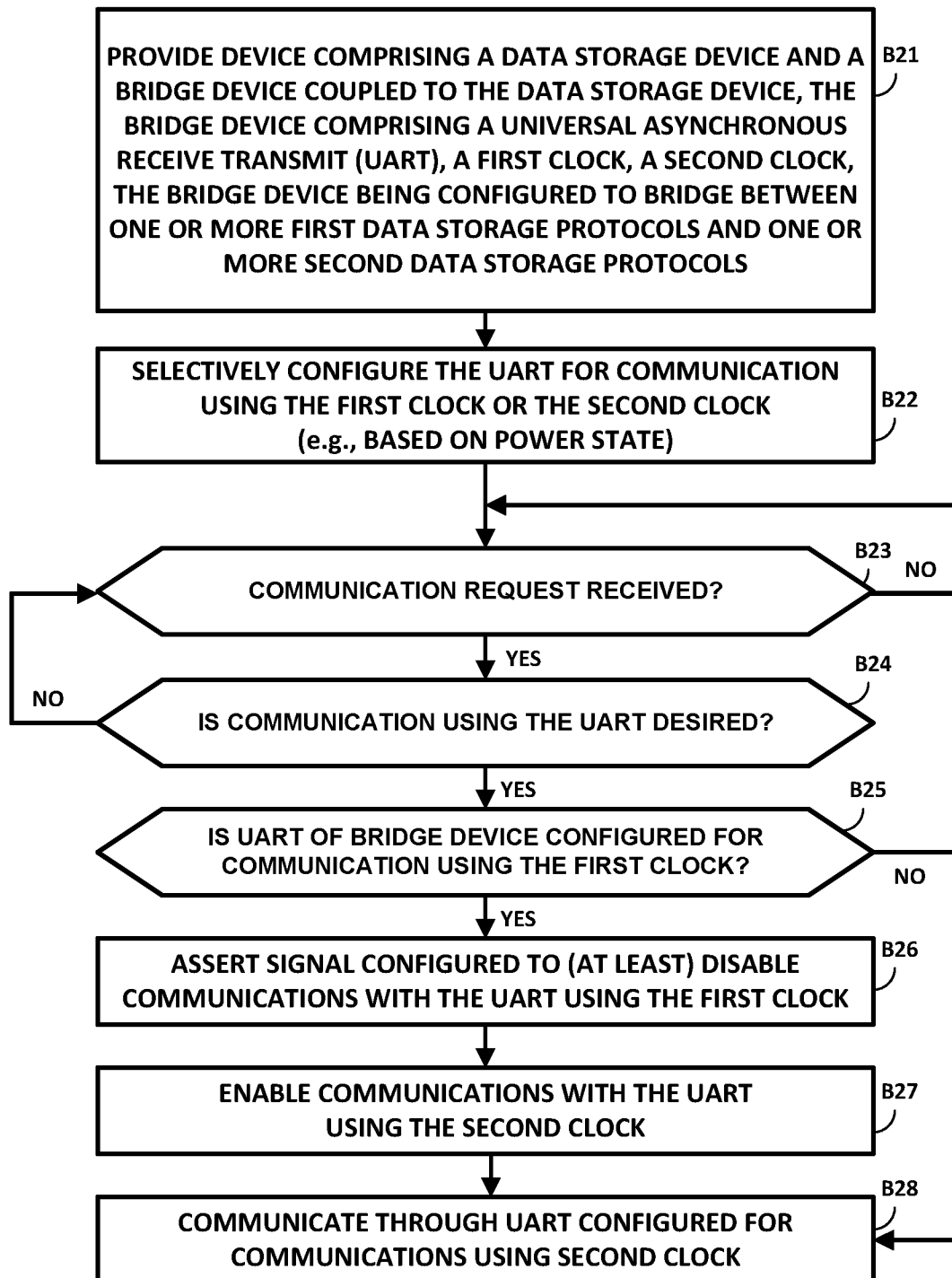


FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/068703**A. CLASSIFICATION OF SUBJECT MATTER****G06F 13/42(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 13/42; H03L 7/00; G06F 13/38; G06F 1/26; G06F 1/12; G06F 1/14; G06F 1/32

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: data storage device, power manager device, UART(Universal Asynchronous Receive Transmit), bridge device, clock change, firmware, and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008-0104434 A1 (MARCUS W. MAY) 01 May 2008 See paragraphs [0018]-[0020] and [0026]; claim 1; and figures 1-2.	1-23
A	US 2008-0077818 A1 (RICHARD RAUSCHMAYER et al.) 27 March 2008 See paragraphs [0006]-[0009] and figure 8.	1-23
A	US 2003-0093702 A1 (ZHENG LUO et al.) 15 May 2003 See paragraphs [0009]-[0012] and figure 1.	1-23
A	US 2007-0063776 A1 (YUICHI OKUDA) 22 March 2007 See paragraphs [0008]-[0034] and figure 9.	1-23
A	EP 1134667 A2 (EXAR CORPORATION) 19 September 2001 See paragraphs [0005]-[0008] and figure 3.	1-23
A	US 7,555,585 B2 (VIKRAM GUPTA et al.) 30 June 2009 See column 7, lines 9-58; and figures 1-4 and 6.	1-23



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/068703

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008-0104434 A1	01/05/2008	US 2011-0145623 A1 US 7917788 B2	16/06/2011 29/03/2011
US 2008-0077818 A1	27/03/2008	US 2010-0218020 A1 US 7739533 B2 US 8245061 B2	26/08/2010 15/06/2010 14/08/2012
US 2003-0093702 A1	15/05/2003	None	
US 2007-0063776 A1	22/03/2007	JP 2005-115715 A JP 4812066 B2 US 2005-0081076 A1 US 7154343 B2 US 7446615 B2	28/04/2005 09/11/2011 14/04/2005 26/12/2006 04/11/2008
EP 1134667 A2	19/09/2001	DE 1134667 T1 EP 1134667 A3 KR 10-2001-0091867 A TW 514790 B US 6754839 B1	18/04/2002 10/03/2004 23/10/2001 21/12/2002 22/06/2004
US 7555585 B2	30/06/2009	US 2008-0005437 A1 US 2009-0240971 A1	03/01/2008 24/09/2009