Aug. 2, 1966 E. GÖTZ 3,264,455

BINARY COUNTER

Filed Jan. 9, 1963 3 Sheets-Sheet 1

Fig. 1

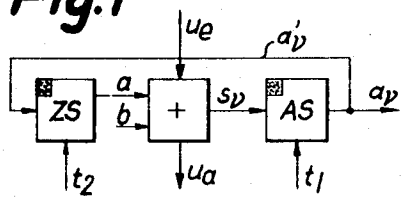


Fig. 2

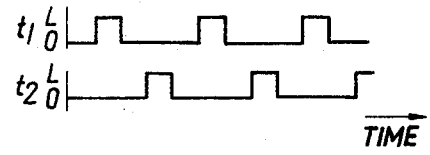


Fig. 3

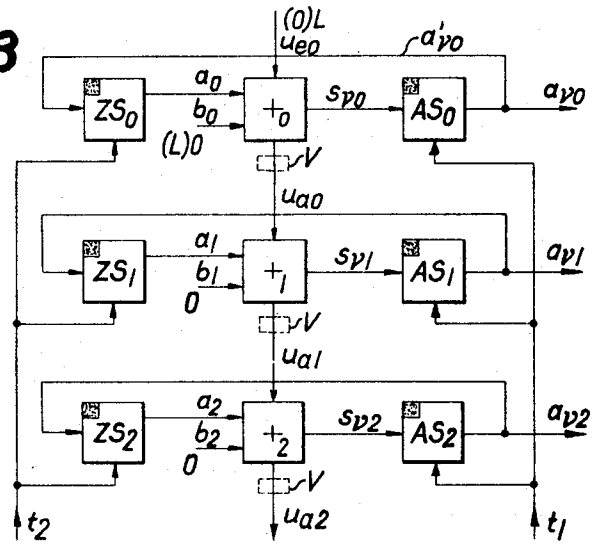


Fig. 4

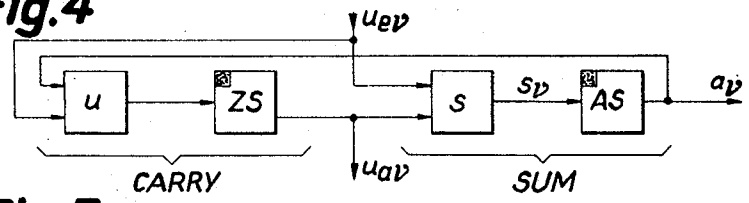
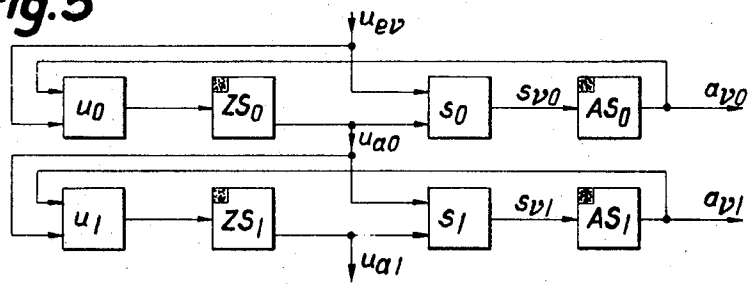


Fig. 5



Inventor:

Elmar Götz

By: Spencer & Kaye

Attorneys

Fig.6

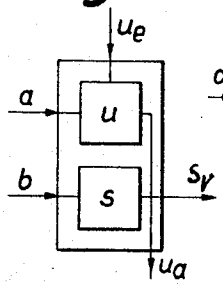


Fig.7

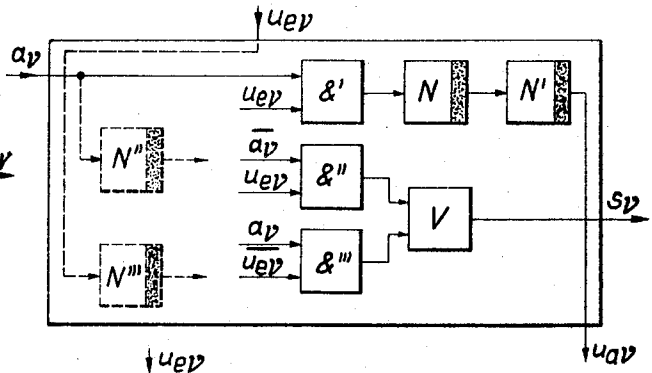


Fig.8

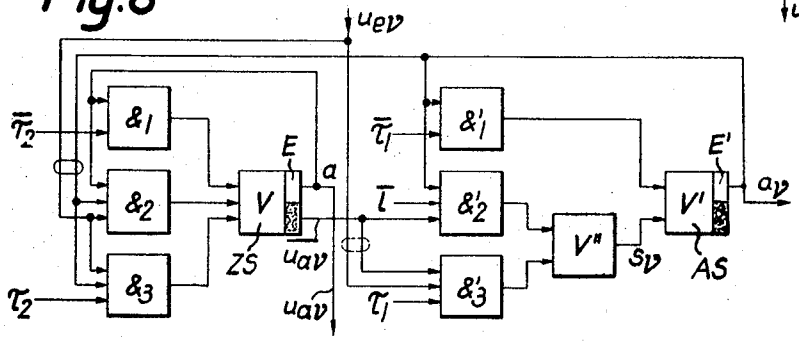


Fig.9

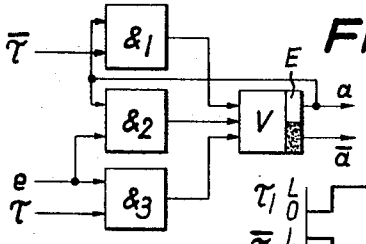
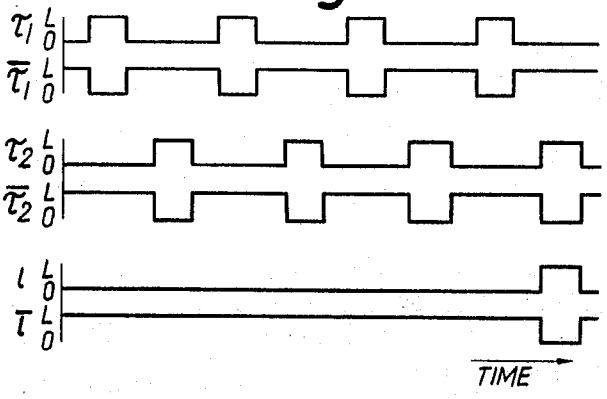


Fig.10



Inventor:

Elmar Götz

By: Spencer & Kaye

Attorneys

Fig. 11

TABLE I

a + b + u_e = s	u_a
a_ν b_ν $u_{e\nu}$ s_ν	u_a
0 0 0 0	0
0 0 L L	0
< 0 L 0 L	0 >
< 0 L L 0	L >
L 0 0 L	0
L 0 L 0	L
< L L 0 0	L >
< L L L L	L >

Fig. 12

TABLE 2

a_ν	$u_{e\nu}$	s_ν	$u_{a\nu}$	$\bar{u}_a$
0	0	0	0	L
0	L	L	0	L
L	0	L	0	L
L	L	0	L	0

Fig. 13

TABLE 3

	+	0	0	0	0	u_{e0}
		0	0	0	L	
1ST CLOCK PULSE t_1	+	0	0	0	L	u_{e0} → DECIMAL 1
		0	0	0	L	
2ND CLOCK PULSE t_1	+	0	0	L	0	u_{e0} → DECIMAL 2
		0	0	0	L	
3RD CLOCK PULSE t_1	+	0	0	L	L	u_{e0} → DECIMAL 3
		0	0	0	L	
4TH CLOCK PULSE t_1	+	0	L	0	0	u_{e0} → DECIMAL 4
		0	0	0	L	
5TH CLOCK PULSE t_1		0	L	0	L	→ DECIMAL 5
		$a_{\nu3}$	$a_{\nu2}$	$a_{\nu1}$	$a_{\nu0}$	

Fig. 14

TABLE 4

t_1	a_0	u_{e0}	$a_{\nu0}$	u_{a0}	a_1	u_{a0}	$a_{\nu1}$	u_{a1}	a_2	u_{a1}	$a_{\nu2}$	u_{a2}
1ST	0	L	L	0	0	0	0	0	0	0	0	0
2ND	L	L	0	L	0	L	L	0	0	0	0	0
3RD	0	L	L	0	L	0	L	0	0	0	0	0
4TH	L	L	0	L	L	L	0	L	0	L	L	0
5TH	0	L	L	0	0	0	0	0	L	0	L	0
6TH	L	L	0	L	0	L	L	0	L	0	L	0
7TH	0	L	L	0	L	0	L	0	L	0	L	0

Fig. 15

TABLE 4a

t_1	$a_{\nu2}$	$a_{\nu1}$	$a_{\nu0}$	
1ST	0	0	L	→ DECIMAL 1
2ND	0	L	0	→ " 2
3RD	0	L	L	→ " 3
4TH	L	0	0	→ " 4
5TH	L	0	L	→ " 5
6TH	L	L	0	→ " 6
7TH	L	L	L	→ " 7

Inventor:
ELmar Götz
By: Spencer & Kaye
Attorneys

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BINARY COUNTER

Elmar Götz, Frankfurt-Gravenbruch, Germany, assignor to Licentia Patents-Verwaltungs-G.m.b.H., Frankfurt am Main, Germany

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3 Claims. (Cl. 235—92)

The present invention relates to a binary counter.

Binary counters are used for carrying out continuous counting operations. As is well known, binary counters consist of flip-flop stages which may be dynamically or galvanically coupled to each other. Such binary counters, made up of flip-flops, represent step-down devices which are controlled by square wave voltages. The flip-flop stages step down the voltage in the ratio 1:2, so that a correspondingly decreased square wave voltage appears at the output of the flip-flop stage. This voltage, in turn, is applied as the control voltage of a further flip-flop stage, at whose output a further stepped down square wave voltage appears. If such binary counters are fashioned as static flip-flop stages, certain difficulties will, under certain circumstances, arise in the transfer characteristics when the individual stages change their state. These stages might then assume the incorrect state. In the case of a binary counter incorporating dynamic-capacitatively coupled flip-flop stages, the respective coupling capacitors between the several stages take over, i.e., store the time delay of the control signal, so that the transfer characteristics of the stages will not cause any difficulties. However, the drawback of capacitatively coupled stages is that the same respond not only to the actual control signals and clock pulses, but also to extraneously generated spurious pulses.

It is, therefore, an object of the present invention to overcome the above disadvantage, and, with this object in view, the present invention resides in an electronic binary counter at whose output natural binary code signals appear in parallel representation, i.e., simultaneously, which counter is characterized, basically, by the following features: (1) there are adders associated with each binary digit (2^0, 2^1, 2^2, . . . 2^n), the carry circuits of which adders are coupled to each other galvanically, (2) the sum signals of the adders (L or 0, where L represents binary 1) are applied to output storage devices which are capable of having clock pulses applied to them, which storage devices feed these sum signals back into the same adders, and (3) one of the binary signals applied to the adder of the lowest order binary digit constantly has the value L.

According to another feature of the present invention, the adders are half-adders.

According to still another feature, an intermediate storage device is provided which is capable of being operated by a clock pulse, which intermediate storage device is connected between the output storage device and the adder pertaining thereto.

According to yet another feature of the present invention, the adders are split up in such a manner that the transfer circuit is cut into the circuit arrangement ahead of the intermediate storage device which then additionally acts as an amplifier, and that the sum circuit is cut ahead of the output storage device which then also additionally acts as an amplifier. The carry and sum signals are formed and amplified by two similar logic circuits comprising AND circuits and OR/OR NOT circuits.

According to still another feature of the present invention, the carry circuit comprises three AND circuits acting as a holding stage, a transient shunt stage, and an input stage, respectively, and the intermediate storage device comprises an OR/OR NOT circuit, which three AND

circuits have their outputs connected to the OR/OR NOT circuit from whose affirmed output the outgoing carry signal is derived. The sum circuit likewise comprises three AND circuits acting as a holding stage, a transient shunt stage, and an input stage, respectively, and the output storage device comprises a further OR/OR NOT circuit, which three last-mentioned AND circuits have their outputs connected to the last-mentioned OR/OR NOT circuit at whose affirmed output there appears the result of the sum formation. The input and shunt stages of the carry circuit are connected to the output of the respective output storage device to receive the sum signal and also to receive the incoming carry signal arriving from the preceding digit, the input stage of the sum circuit is connected to receive the incoming carry signal arriving from the preceding digit and also to receive the negated outgoing carry signal, and the shunt stage of the sum circuit is connected to receive the negated outgoing carry signal and to the output of the respective output storage device to receive the sum signal.

Additional objects and advantages of the present invention will become apparent upon consideration of the following description when taken in conjunction with the accompanying drawings in which:

FIGURE 1 is a schematic diagram showing a basic unit pertaining to one binary digit.

FIGURE 2 shows the timed relationship of clock pulse trains used in the operation of the counter according to the present invention.

FIGURE 3 shows three digits of a counter incorporating three units associated with the respective digits.

FIGURE 4 is a schematic diagram showing a modified embodiment of a basic unit forming part of a counter according to the present invention.

FIGURE 5 shows two interconnected units according to FIGURE 4.

FIGURE 6 shows the details of an adder used in the counter according to the present invention.

FIGURE 7 shows the details of a half-adder used in the counter according to the present invention.

FIGURE 8 shows the details of one embodiment of a unit incorporated in a counter according to the present invention.

FIGURE 9 shows a sub-assembly incorporated in the unit of FIGURE 8.

FIGURE 10 shows the timed relationship of the pulse trains and the erasing pulse used in the operation of the embodiment of FIGURES 8 and 9.

FIGURES 11, 12, 13, 14, and 15 are Tables 1, 2, 3, 4, and 4*a*, respectively, which will be referred to for explanatory purposes.

Referring now to the drawings, FIGURE 1 shows a binary counter according to the present invention which uses an adder + whose output signal s_v is applied into an output storage device AS. The adder comprises a sum circuit whose inputs *a*, *b*, u_e, have binary signals (L or 0) applied to them, while the result of the sum formation appears at the output terminal s_v. The adder further includes a carry circuit having an output terminal u_a.

A binary number *a* and *b* is applied to the adder +. If there is a carry from the preceding digit, such carry is applied to input u_e of the adder. As indicated above, these inputs are voltage signals of given polarity which correspond to the values 0 or L. The result signal is taken from the output a_v of the output storage device AS. According to the present invention, one of the input signals of the adder of the lowest binary digit always has the value L.

The output storage device AS, being a clock pulsable component, is opened, at a given instant, by means of a timing or clock pulse t_1. As soon as this clock pulse t_1

(for example L) appears, the sum of the adder + is taken over by the output storage device AS. The result appearing at the output a_ν is additionally fed back and applied to an intermediate storage device ZS, the latter also being clock pulsable and controlled by a further clock pulse t_2. The clock pulses t_1, t_2, are staggered, as shown in FIGURE 2. Thus, when a certain result appears at the output storage device AS and hence at output terminal a_ν (L or 0), such result is applied, via a line a'_ν, to the intermediate storage device ZS. The same result will, at clock pulse t_2, appear in this intermediate storage device and hence at a. As stated above, the adder + forms the sum $a+b$. Let the value a, in this case, be the value coming from the intermediate storage device ZS, and let the value b in this case (the adder being that of the lowest binary digit) always be the value L. The adder $+_0$ then forms $a+b$, and since b is always equal to L, the value formed will always be $a+L$. This value is then applied, at clock pulse t_1, to the output storage device AS via line s_ν. Furthermore, the adder will form a carry which appears at output u_a. In the instant example, the value of the incoming carry $u_{e0}=0$.

The circuit arrangement depicted in FIGURE 1 and incorporating the adder +, the output storage device AS and the intermediate storage device ZS is a unit intended to handle one binary digit. When a plurality of such units are used, as shown in FIGURE 3, the circuit constitutes a complete binary counter. In the arrangement of FIGURE 3, this circuit includes three basic units each corresponding to the circuitry of FIGURE 1, it being obvious that any suitable number of such units can be provided. In each case, each unit will include the adder +, an output storage device AS connected to the output of the adder, and an intermediate storage device ZS to which the output value is fed back. The storage devices AS and ZS of each of the three units are operated by the same clock pulses t_1, t_2, respectively. The outgoing carry formed in any one adder is applied to the adder of the next digit. In each case, the adders have inputs a, b, and u_e.

More particularly, the unit pertaining to the lowest binary digit comprises the adder $+_0$ with its inputs a_0, b_0, u_{e0}, and the sum output $s_{\nu 0}$; the output storage device AS_0 whose input is connected with the output $s_{\nu 0}$ of the adder $+_0$ and which has a result output $a_{\nu 0}$; and the intermediate storage device ZS_0 whose input is connected with the output $a_{\nu 0}$ via lead $a'_{\nu 0}$. The output of the intermediate storage device ZS_0 is connected with the input a_0 of the adder $+_0$. The adder $+_0$ also has an output u_{a0} for the outgoing carry which is applied to the unit pertaining to the next digit.

The units pertaining to the subsequent digits are characterized by the same basic reference numerals, except that they incorporate, instead of the subscripts 0, the subscripts 1 and 2, respectively. In each case, the result outputs $a_{\nu 0}$, $a_{\nu 1}$, $a_{\nu 2}$, are fed back to the adders via respective intermediate storage devices. In adder $+_0$, the value applied to the carry input u_{e0} is equal to 0, as indicated within the parentheses, while the input b_0 has the value L applied to it and the inputs b_1 and b_2 each have the value 0 applied to them. There will thus be formed in the adder $+_0$

$$a_0+b_0+u_{e0}=s_{\nu 0} \text{ and } u_{a0}$$

In the above equation, $s_{\nu 0}$ represents the sum of a_0+b_0 while u_{a0} represents the outgoing carry. FIGURE 11, containing Table 1, shows the relationship for a full adder.

If the three input values=0, the sum s and the outgoing carry will also be equal to 0. If each of the inputs a and b has the value 0 and the input u_e has the value L, the sum will be L while the outgoing carry will be 0. If only input b has the value L, the sum s again will be L, while the outgoing carry is 0. If both inputs b and u_e have the value L, the sum s will have the value 0

while the outgoing carry $u_a=L$. If all three inputs have the value L, then the sum $s=L$ and the outgoing carry $u_a=L$.

The circuit of FIGURE 3 can be simplified if the input b_0, too, has applied to it not the value L but the value 0 and, instead, the carry u_{e0} for the lowest binary digit is always made equal to L, as indicated at the respective inputs (the values shown not in parentheses). In this case the adders $+_0$ to $+_2$ can be fashioned as half-adders.

The inputs b_0 to b_2 will thus always have the values 0 applied to them. In this case, the first incoming carry $u_{e0}=L$, as shown. This produces the substantial advantage that all of the units pertaining to the individual digits can be simplified and be made completely alike to each other. Insofar as Table 1 (FIGURE 11) is concerned, this means that, thanks to the fact that the value for the carry u_{e0} is fixed and the value 0 is applied to the inputs b_0 to b_2, the value for b will always be 0, i.e., all of those combinations in which b has the value L will never appear. The values for input b which thus drop out are, in Table 1, encircled by dashed lines. Table 2 (FIGURE 12) shows the remaining combinations. It will be seen that the input b is completely eliminated, and all that remains are the four shown combinations. The third, fourth, seventh and eighth combinations of Table 1 are eliminated because here the input b has up to now had the value L, these combinations being the ones which, in Table 1, are within the brackets.

As shown in Table 2, the sum s in the first combination is equal to 0, in the second and third combination the value is equal to L, and in the fourth combination the value is again 0 with an outgoing carry L, the value of the carry, in the first three combinations, having been equal to 0. Table 2 represents the function of a half-adder.

Table 3 (FIGURE 13) again shows the formation of the sum by means of the adders, operating on the basis of the combinations shown in Table 2. In Table 3, the starting position is indicated by 0000. In the lowermost (0^{th}) digit, there will appear, at clock pulse t_1, the incoming carry $u_{e0}=L$. This produces the sum $000L$=decimal 1. Upon occurrence of the clock pulse t_1, the value L of the carry u_{e0} is added. This produces the sum $0L0$=decimal 2. The carry u_{e0} is thereafter again added so as to produce the sum $0LL$=decimal 3, and so on. Depending on the sequence of clock pulses t_1, there thus appears at the outputs $a_{\nu 0}$ . . . $a_{\nu n}$ of the counter of FIGURE 3 either the value 0 or the value L and the complete result of the counting operation can then be read, from the output of the lowest binary digit ($a_{\nu 0}$) to the output of the highest binary digit ($a_{\nu 2}$ or $a_{\nu n}$, as the case may be). The output $a_{\nu 0}$ has the valuation 2^0, the output $a_{\nu 1}$ the valuation 2^1, the output $a_{\nu 2}$ the valuation 2^2, and so on.

Table 4 (FIGURE 14) gives a tabular representation of the operation of the circuit, while FIGURE 4a (FIGURE 15) gives the decimal equivalent outputs derived from the output signals at outputs $a_{\nu 0}$ to $a_{\nu 2}$.

In the counter of FIGURE 3, the starting position of all of the units pertaining to the respective digits are in the state 0. Upon occurrence of the first clock pulse t_1, the incoming carry $u_{e0}=L$ is transferred into the output storage device AS_0. The succeeding units are all in the same state as they were before, namely 0, because the outgoing carry $u_{a0}=0$. Upon occurrence of the first clock pulse t_2, the result appearing at the output $a_{\nu 0}$ is applied to the intermediate storage device ZS_0, whereupon this result also appears at the input a of the adder $+_0$. The contents L of the intermediate storage device ZS_0 and the incoming carry $u_{e0}=L$ produces, in this state of the counter, an output $s_{\nu 0}=0$ with an outgoing carry $u_{a0}=L$. As is apparent from Table 4, this carry is due to the fact that the input a_0 and the input u_{e0} will, after the occurrence of the first clock pulse t_2

each have the value L. The output $s_{\nu 1}$ of the adder $+_1$ will then, due to the outgoing carry $u_{a0}=L$ of the first adder $+_0$ and the value 0 at the inputs a_1, b_1 of the second adder $+_1$, have the value L. There then follows the second clock pulse t_1, upon the occurrence of which the sum $s_{\nu 1}=L$ will appear, as result L, at the output $a_{\nu 1}$ of the adder $+_1$.

The value L which is constantly applied to the input u_{e0} is added, under the influence of the clock pulse train of pulses t_1, with the value appearing at the input a_0 of the first adder $+_0$ and the sum is then put out, while the value 0 or L at the carry output is passed on to the carry input of the next adder $+_1$. Table 4*a* shows the binary signals appearing at the outputs $a_{\nu 0}$, $a_{\nu 1}$, $a_{\nu 2}$, at clock pulses t_1 through t_7.

As explained above, the counter of FIGURE 3 can be expanded. For example, a further pulsable output storage device can be connected to adder $+_0$, which last-mentioned storage device is subjected to a further train of clock pulses and commences to add at a later instant. The counter of FIGURE 3 shows that the value L is added to the starting value as often as there is a clock pulse signal $t_1=L$.

The half adders of FIGURE 3 carry out two operations, namely, the formation of the sum and the formation of the outgoing carry. Accordingly, each half-adder has two outputs s, u_a. The outgoing carry is always applied to the next adder, whose carry, in turn, is applied to the next following adder. As a result, the carry signal becomes progressively weaker. In order to avoid this, the carry paths between the adders $+_0$, $+_1$ and $+_2$ have to be equipped with special amplifiers, indicated at V in FIGURE 3 in dashed lines. In this way, the outgoing carry signal may be brought to the necessary strength. However, the amplifiers increase the expense of the counter, and, while an arrangement incorporating such amplifiers would be operative, it is desirable, if possible, to make do without these amplifiers, and according to another feature of the present invention, these amplifiers can be dispensed with by splitting up the formation of the sum and carry signals. This feature of the present invention is based on the following considerations: the counted result of a particular binary digit is present in an output storage device pertaining to the particular digit. This result is fed back into the respective intermediate storage device. The sum and the outgoing carry are thereafter formed separately, in contradistinction to the operation of FIGURE 3. This separate sum and carry formation is shown in FIGURE 4, in which the carry u is formed ahead of the intermediate storage device ZS. The intermediate storage device ZS is also used for forming the sum. The sum is then applied to the output storage device AS. The result appearing at the output of storage device AS is then fed back to the carry stage u. Also, the carry $u_{e\nu}$ coming from the preceding stage is applied to the carry forming stage u and the sum forming stage s. The carry $u_{a\nu}$ for the following unit is derived from the output of the intermediate storage device ZS.

In the adding process, both the sum as well as the carry have to be formed. Both processes make use of the output a_ν and the input carry $u_{e\nu}$. As shown in FIGURE 4, the value a_ν goes, via the carry stage u and the intermediate storage device ZS, to the sum stage s. The outgoing carry and the sum are thus formed separately. The carry stage u has a_ν and $u_{e\nu}$ applied to it, exactly as in the case of the adder of FIGURE 3. The arrangement of FIGURE 4, however, makes it possible to dispense with the amplifiers V which, in practice, would be needed for the circuit arrangement according to FIGURE 3, the reason for this being that the intermediate storage device ZS of each binary digit can take over this amplifying function. The carry, in FIGURE 4, is formed by the carry stage u which itself does not have any amplifying means, it being the intermediate storage device ZS which amplifies the outgoing carry signal $u_{a\nu}$.

The same effect is achieved by the fact that the sum is formed in the sum stage s which itself likewise has no amplifying means, it being the output storage device AS which acts as an amplifier for amplifying the output signal s_ν of the sum stage s.

FIGURE 5 shows a counter for two binary digits, which counter can, of course, be expanded to as many digits as desired. Each unit of the counter of FIGURE 4 corresponds to the unit shown in FIGURE 3, the first unit including two storage device ZS_0, AS_0. A nonamplifying sum stage s_0 for forming the sum is connected ahead of the output storage device AS_0, there being a nonamplifying carry stage u_0 for forming the outgoing carry connected ahead of the intermediate storage device ZS_0. The outgoing carry u_{a0} is applied to the succeeding carry stage u_1 and sum stage s_1. The carry stage u_1 has its output connected to the input of the intermediate storage device ZS_1, while the output of sum stage s_1 is connected to the input of the output storage device AS_1. For purposes of sum formation, the output value $a_{\nu 1}$ is fed back to the carry stage u_1.

It will be seen from the above that, in the counter of FIGURE 5, the adder of each unit of FIGURE 3 is, in effect, divided into independent sum and carry stages without amplification, the intermediate storage device now being additionally used as a means for amplifying the carry signal while the output storage device is additionally used as a means for amplifying the sum signal. The sum and outgoing carry results are thus available for further processing.

It will be understood that the carry stages u according to the embodiments of FIGURES 4 and 5 do not constitute elements above and beyond the adders of FIGURE 3. The carry stages u of FIGURES 4 and 5 are already part of the adders of FIGURE 3. The same applies to the sum stages s. For purposes of illustration, FIGURE 6 shows the adder of FIGURE 3 with its component sub-parts.

What is involved is a half-adder whose principle of operation was explained in conjunction with Table 2. As can be seen from that table, a carry $u_a=L$ appears when a_ν and $u_{e\nu}=L$. FIGURE 7 shows, in schematic form, one embodiment of such a half-adder. An AND circuit &' is provided which serves for forming the carry, the inputs of this AND circuit having the values a_ν and $u_{e\nu}$ applied thereto. The output of this AND circuit &' produces the outgoing carry $u_{a\nu}$. This AND circuit does not amplify the carry signal; if such amplification is to be obtained, two amplifier stages, for example transistorized NOT circuits, would have to be provided, as indicated by stages N and N'.

According to Table 2, $s=L$ when a_ν and $u_{e\nu}$ have opposite values. Two additional AND circuits &'', &''' are provided in the adder according to FIGURE 7 for purposes of forming the sum. The value L appears at the output of AND circuit &'' when the input values of this circuit are $u_{e\nu}=L$ and $\bar{a}_\nu=L$. The output of AND circuit &''' will be L when the input values are $a_\nu=L$ and $\bar{u}_{e\nu}=L$. Thus, in both cases will the sum be L. The outputs of the AND circuits &'', &''' are connected to an OR circuit v. The lines leading to $\bar{a}_\nu$ and $\bar{u}_{e\nu}$ each incorporate a NOT circuit N'', N''', as shown in dashed lines. The arrangement consisting of the above-described components constitutes, for example, the adder $+_0$ of FIGURE 3. It will be seen that each adder requires four NOT circuits N, N', N'', N'''. In the case of the counters according to FIGURES 4 and 5, these NOT circuits are eliminated, and their functions are taken over by the intermediate and output storage devices which must in any case be provided.

FIGURES 8 and 9 show the details of the counter of FIGURES 4 and 5. More particularly, the circuit arrangement of FIGURE 8 corresponds to that of FIGURE 4 and illustrates a single unit of the counter pertaining to

ne binary digit. The unit uses storage devices whose hange-over characteristics (signal changes from L to 0 r vice versa) are such that they will not assume the wrong ircuit condition (L or 0). FIGURE 9 shows a subssembly of the unit of FIGURE 8, which subassembly omprises three AND circuits &1, &2, &3 whose outputs re applied to an OR circuit v, the output of the latter, in urn, being connected to an OR NOT circuit E. The three ND circuits constitute either the carry circuit u or the um circuit s of FIGURE 4, while the OR/OR NOT ciruit v, E, constitutes the appropriate storage device, i.e., he intermediate storage device ZS if the three AND ciruits are the carry circuit u or the output storage device S if the three AND circuits are the sum circuit s.

The affirmed signal appears at output a and the negated ignal at output $\bar{a}$. The AND circuit &1 has applied to t the fed back signal from output a and the negated clock ulse τ. The AND circuit &3 has applied to it the affirmed lock pulse τ and the input value e to be stored (L or 0). Vhen the clock pulse $\tau=L$ (at which time $\bar{\tau}=0$) and the nput signal $e=L$, the output value of AND circuit &3 will qual L. This value is applied by OR circuit v to the OR OT circuit E and appears, at output a, as the signal L. he signal at output a will then be equal to L, while the gnal at output $\bar{a}$ will be equal to 0. When the storage evice is in this condition, the values applied to the two nputs of AND circuit &2 will be L, so that the output of his AND circuit &2 will likewise be L. It matters not if he clock pulse τ then becomes 0 (whereupon $\bar{\tau}$ becomes), because the value at output a is safely maintained t L by the AND circuit &2 during the time the clock ulses τ, $\bar{\tau}$, change their respective values. The AND ircuit &2 thus serves as a temporary or transient shunt. n general, the signal e lasts longer than the clock pulse τ, nd thanks to the transient shunt afforded by AND circuit &2, the values of the clock pulses τ, $\bar{\tau}$, can change ithout this causing the value appearing at output a to hange. The holding stage &1 maintains the value at utput a, even when the clock pulse τ, after having asumed the value L, thereafter assumes the value 0. With is change, the clock pulse $\bar{\tau}=L$ and if, for example, ie value at output a was L, this output will remain qual to L because $\bar{\tau}=L$ and hence the output of holding tage $\&_1=L$.

The counter unit according to FIGURE 8 shows two ubassemblies as illustrated in FIGURE 9, the AND circuits &1, &2, &3 and the AND circuits &'1, &'2, &'3, being sed for forming the outgoing carry and the sum, respectively.

In FIGURE 8, the AND circuit &1 serves as the holding age, the AND circuit &2 as the transient shunt stage, nd the AND circuit &3 as the input stage. The outputs f these AND circuits are connected to an OR circuit v hose output, in turn, is connected to the OR NOT circuit E. These components serve to form and amplify ie outgoing carry. Similarly, the AND circuit &'1 constitutes the holding stage, the AND circuit &'2 the tranient shunt stage, and AND circuit &'3 the input stage, ie outputs of these circuits being connected to the OR ircuit v', whose output, in turn, is connected to the)R NOT circuit E'. These components serve to form nd amplify the sum. The OR circuit v'' will be described ater'.

The AND circuit &1, constituting the holding stage of he carry circuit, has applied to it the clock pulse $\bar{\tau}_2$, as ell as the fed back signal $u_{a\nu}$ appearing at the output a f the OR NOT circuit E. The AND circuit &2, constituting the transient shunt stage, has applied to it the signal $_{a\nu}$ appearing at output a, as well as the input signal which tself is made up of two components. This input signal, ndicated by the encircled leads, consists of a_ν and $u_{e\nu}$, rom which $u_{a\nu}$ is formed. This corresponds to the arangement depicted in FIGURE 7. In FIGURE 8, a_ν is the output of the output storage device AS, at which the result appears. Thus, there is formed a multiple-component logic circuit constituted by the above-described AND circuits &'1, &'2, &'3, the OR circuit v'', and the OR/OR NOT circuit v', E', it being this multiple-component logic circuit which, technically, constitutes the overall storage unit of which the output storage device AS is a part. The result appearing at a_ν and the applied incoming carry $u_{e\nu}$ thus constitute input signals which are combined with each other via the AND circuits &'3, &'2, thereby forming the outgoing carry $u_{a\nu}$. The AND circuit &3, constituting the input stage, also has the clock pulse τ_2 applied to it. The outgoing carry $u_{a\nu}$ is stored in the intermediate storage device ZS and appears, appropriately amplified, at output a. In this way, there is formed another multiple-component logic circuit constituted by the AND circuits &1, &2, &3, and the OR/OR NOT circuit v, E, which multiple-component logic circuit constitutes, technically, the overall storage unit of which the intermediate storage device ZS is a part.

The AND circuit &'3, constituting the input stage of the sum circuit, has applied to it the composite input signal, indicated by the encircled leads, made up of components $u_{a\nu}$ and $\bar{u}_{a\nu}$, which are the incoming carry and the output signal of the intermediate storage device ZS, respectively. The input stage &'3 also has the clock pulse τ_1 applied to it. The holding stage &'1 is connected in the same manner as holding stage &1 except that the applied clock pulse is $\bar{\tau}_1$. The transient shunt stage &'2 has applied to it the output a_ν of the output storage device AS and the negated outgoing carry $\bar{u}_{a\nu}$ of the intermediate storage device ZS. Finally, the counter can be reset to its starting position ($a_\nu=0$) by applying to the AND circuit &'2 an erasing signal $\bar{1}=0$, as well as by applying $\bar{\tau}_1$, $\bar{\tau}_2$ and $u_{e\nu}=0$.

The outgoing carry $u_{a\nu}$ is formed in the intermediate storage device ZS. The input stage &'3 has applied to it the values of $u_{e\nu}$ *and* $\bar{u}_{a\nu}$ so as to form the sum.

According to the second line of Table 2, the sum $s_\nu=L$ is formed when $u_{e\nu}$ and $\bar{u}_{a\nu}=L$. According to line 3 of Table 2, the sum s_ν will also be equal to L when a_ν and $\bar{u}_{a\nu}=L$.

It will be seen that the input and transient shunt stages &'3, &'2, of the counter according to FIGURE 8 have applied to them the values appearing at $u_{e\nu}$, $\bar{u}_{a\nu}$, and a_ν, $\bar{u}_{a\nu}$, respectively. If the inputs of these stages &'3, &'2 have the value L, and if also the additional inputs τ_1, $\bar{1}$ become L, then the outputs of AND circuits &'2, $\&'_3=L$.

The AND circuit &'2 is thus also used for forming the sum. This circuit also serves to form the transient shunt. The AND circuit &'3 forms a portion of the sum, namely $u_{e\nu}$, and $\bar{u}_{a\nu}$, and AND circuit &'2 forms the other portion of the sum, namely $\bar{u}_{a\nu}$ and a_ν. The sum will appear at the output of either &'2 or &'3. The outputs of these two AND circuits are connected to the inputs of the above-mentioned OR circuit v''. In practice, this OR circuit v'' can be contained in the OR circuit v' pertaining to output storage device AS. The value s_ν is thus formed at the output of OR circuit v''.

FIGURE 10 shows the timed relationship of the clock pulses τ_1, $\bar{\tau}_1$, τ_2, $\bar{\tau}_2$ and the erasing pulses 1, $\bar{1}$. The value 0 can, for example, be equal to a given negative voltage and the value L be equal to a given positive voltage, or vice versa.

The counter can be erased, i.e., reset, when the clock pulses $\bar{\tau}_1$, $\bar{\tau}_2$, the incoming carry signal $u_{e\nu}$, and the erasing signal $\bar{1}$ are made equal to 0. When the clock pulses $\bar{\tau}_1$, $\bar{\tau}_2=0$, the holding action via holding stages &1, &'1 is discontinued.

It will be understood that the above description of the present invention is susceptible to various modifications, changes, and adaptations, and the same are intended to

be comprehended within the meaning and range of equivalents of the appended claims.

What is claimed is:

1. In an electric binary counter at whose outputs there appear signals in natural binary code and in parallel representation, the combination which comprises:

(a) a separate adder associated with each binary digit, each adder having a sum circuit and a carry circuit, the carry circuits of all adders being galvanically coupled with each other;

(b) a separate, clock pulsable output storage device associated with each respective adder, each storage device having an input connected to the sum circuit of its respective adder and an output connected to feed the sum signal back into an input of said respective adder;

(c) means for constantly applying the value L as one of the binary signals applied to the adder associated with the lowest binary digit;

(d) a separate, clock pulsable intermediate storage device associated with each binary digit, each intermediate storage device having an input connected to receive said output from the respective output storage device and an output connected to deliver the sum signal to said input of the respective adder;

(e) said carry circuit of each adder being separate from said sum circuit and being connected ahead of the respective intermediate storage device, the latter being an amplifier for amplifying the carry signal;

(f) said sum circuit of each adder being connected ahead of the respective output storage device, the latter being an amplifier for amplifying the sum signal; and

(g) said carry circuit of said adder and said intermediate storage device being combined into a first multiple-component logic circuit and said sum circuit of said adder and said output storage device being combined into a second multiple-component logic circuit, said first and second multiple-component logic circuits being similar to each other.

2. The combination defined in claim 1 wherein said carry circuit comprises three AND-circuits constituting a holding stage, a transient shunt stage, and an input stage, respectively, and said intermediate storage device comprises an OR/OR NOT-circuit, the outputs of said AND-circuits being connected to said OR/OR NOT-circuit from whose affirmed output the outgoing carry signal is taken off; wherein said sum circuit comprises three further AND-circuits constituting a holding stage, a transient shunt stage, and an input stage, respectively, and said output storage device comprises a further OR/OR NOT-circuit, the outputs of said last-mentioned three AND-circuits being connected to said last-mentioned OR/OR NOT-circuit from whose affirmed output the result of the sum formation appears; wherein said input and shunt stages of said carry circuit are connected (1) to the output of the respective output storage device to receive the sum signal and (2) to receive the incoming carry signal arriving from the preceding digit; wherein said input stage of said sum circuit is connected (1) to receive the incoming carry signal arriving from the preceding digit and (2) to receive the negated outgoing carry signal; and wherein said shunt stage of said sum circuit is connected (1) to receive the negated outgoing carry signal and (2) to the output of said respective output storage device to receive said sum signal.

3. The combination defined in claim 1 wherein said adders are half-adders.

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DARYL W. COOK, *Acting Primary Examiner.*

MALCOLM A. MORRISON, *Examiner.*

J. F. MILLER, *Assistant Examiner.*