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(54) Title: BUBBLE DEFECT REDUCTION

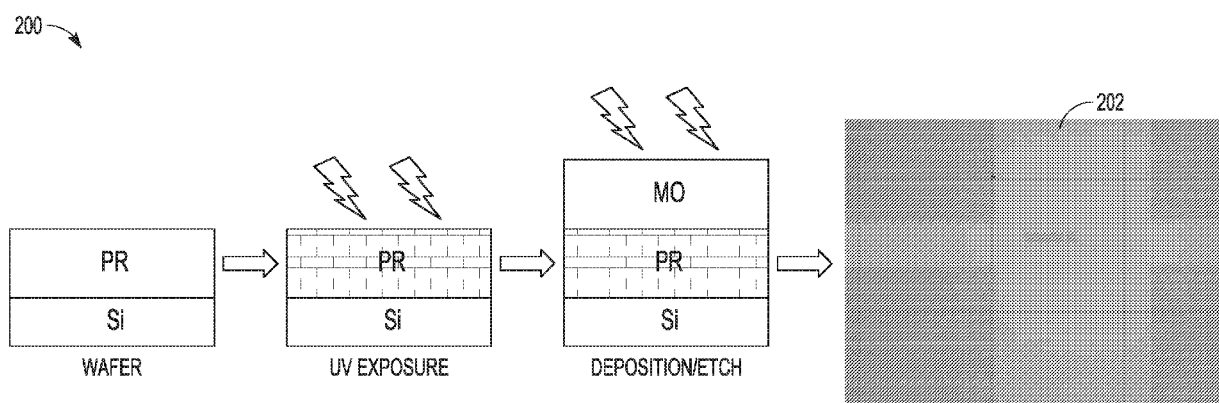


FIG. 2

(57) Abstract: In some examples, a method of processing a substrate comprises applying a photoresist (PR) onto a surface of the substrate, pre-exposing the PR to ultra violet (UV) light before depositing or etching a metal oxide (MO) layer onto the PR, and depositing or etching a MO layer onto the PR subsequent to pre-exposing the PR to UV light.



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BUBBLE DEFECT REDUCTION

CLAIM OF PRIORITY

[0001] This application claims the benefit of priority to United States Patent Application No. 62/768,641, to Singhal et al, entitled "Bubble Defect Reduction" filed on November 16, 2018, which is incorporated by reference herein in its entirety.

FIELD

[0002] The present disclosure relates generally to bubble defect reduction in depositing and/or etching a metal oxide (MO) layer on a photoresist on a substrate.

BACKGROUND

[0003] The background description provided here is for the purpose of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

[0004] Atomic Layer Deposition (ALD) is a deposition method that has the capability of controlling the thickness of thin films formed on semiconductor substrates on the order of one atomic mono-layer. Plasma Enhanced ALD (PEALD) is a further enhancement that enables improved film properties at lower temperatures. PEALD uses chemical precursors, like ALD, in an RF-induced plasma to create the necessary chemical reactions to form the thin films in a highly controlled manner. PEALD offers many advantages, including low temperature processing, excellent conformity and thickness control of deposited layers, and a capability of pre- and post-deposition in-situ treatments.

[0005] Multiple patterning is a technique to enhance feature density for integrated circuits (ICs) beyond the limits of photolithography. Such multi-patterning techniques include, for example, pitch splitting, sidewall image transfer, self-aligned contacts, via patterning, layout splitting, and self-aligned

double or quadruple patterning. It is expected that multi-patterning will be necessary for 10 nm and 7 nm node semiconductor processes and beyond.

[0006] Self-Aligned Quadruple Patterning (SAQP) is essentially two cycles of a double patterning technique, often referred to as Self-Aligned Double Patterning (SADP). Both SAQP and SADP require a substrate with multiple layers formed thereon. For instance, the layers on the substrate may include, from the bottom layer up, a first carbon film referred to as an Ashable Hard Mask (AHM) or a Spin on Carbon layer (SOC), a Silicon Oxide (SiO_2) layer, a second carbon (AHM/SOC) layer, and an Anti-Reflective Layer (ARL).

[0007] SADP uses a photolithography step and additional etch steps to define spacer-like features on a substrate. In the SADP process, the first step is to deposit a resist material (also called a photoresist, or photoresist layer, referred to as PR herein) and then pattern, using photolithography, "mandrels" onto the top ARL layer on the substrate. The mandrels typically have a pitch at or close to the limit of photolithography. The mandrels are next covered with a deposition layer such as Silicon Oxide (SiO_2). A "spacer etch" is subsequently performed, removing (a) the horizontal surfaces of the SiO_2 layer and (b) the PR. As a result, just the vertical surfaces of the SiO_2 remain on the ARL layer. These vertical surfaces define "spacers," which have a pitch finer than can be achieved with conventional photolithography.

[0008] SAQP is a continuation of the double patterning process. With SAQP, the SiO_2 spacers are used as a mask in an etch step removing the underlying ARL and second AHM layers except under the masked regions. Thereafter, the SiO_2 spacers are removed, leaving second mandrels formed in the AHM layer. Another SiO_2 layer is then deposited followed by another "spacer etch," removing (a) the horizontal portions of the SiO_2 layer and (b) the second mandrels. The result is a structure having SiO_2 spacers formed on the underlying SiO_2 layer. With the SAQP process, the pitch of the second SiO_2 spacers are finer than the first spacers and significantly beyond limits of conventional lithography.

[0009] While multi-patterning offers significant benefits and helps extend the usefulness of conventional photolithography to next generation integrated circuitry, the various processes have their limitations. In particular, the multi-patterning requires numerous deposition, photolithography, and

etching steps to form the spacers. The finer the pitch of the spacers, generally the more photolithography-etch cycles are involved. These additional steps significantly add to the cost and complexity of semiconductor fabrication.

[0010] As semiconductor manufacturers increasingly look to adopt SAQP and SADP towards shrinking nodes even further, they are also looking at ways to reduce the cost of adopting this technology. One potential way to do so is to adopt a MO to form spacers and deposit these directly on top of the PR layer. MO is harder and of higher modulus than conventional silicon dioxide and allows thinner spacers to be created and used and can also provide the benefit of being able to be used in a second role as a second mandrel. This approach of using a MO spacer to serve initially as a spacer followed thereafter by its use as mandrel is called spacer-on-spacer technology. Certain methods of spacer-on-spacer technology that achieve a requisite SAQP performance can be very beneficial cost-wise as they can eliminate many deposition, lithography, and etching steps and thus serve to pay for the cost advantage of this technology.

[0011] As part of this spacer-on-spacer technology, certain MOs can be used as spacer material to be deposited directly on top of a PR layer. Some examples have demonstrated that this can be done without causing damage to the PR material. But in some instances, particularly when performing a spacer etch on certain wafers, significant defects can arise. One problem relates to the creation of unwanted bubble defects. The present disclosure seeks to address at least this issue.

DESCRIPTION OF THE DRAWINGS

[0012] Some embodiments are illustrated by way of example and not limitation in the figures of the accompanying drawings:

[0013] **FIG. 1** is a schematic diagram showing bubble defects, according to some examples.

[0014] **FIG. 2** is a block diagram illustrating operations in a method, according to an example embodiment.

DESCRIPTION

[0015] The description that follows includes systems, methods, and techniques that embody illustrative embodiments of the present disclosure. In

the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of example embodiments. It will be evident, however, to one skilled in the art that the present inventive subject matter may be practiced without these specific details.

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[0017] As mentioned above, bubble defect formation can be an issue in certain semiconductor manufacturing operations. Current manufacturing techniques using spacers of silicon oxide (SiO_2) sometimes have limitations when scaling down to accommodate shrinking technology nodes. Other techniques involving MO spacers allow scalability in some examples but nevertheless present issues relating to the formation of bubble defects appearing in the PR layer during the etching of the MO downstream of a deposition phase. The presence of such defects during etching can limit or prevent the use of otherwise helpful MOs such as tin oxide (SnO_2) from being used in smaller scale operations or in a second role serving as a mandrel on the PR layer.

[0018] Without wishing to be bound by theory, it is believed that bubble defect formation may be caused by an interaction of ultraviolet (UV) light or radiation present in a plasma gas with electrons emitted by a MO layer at the interface between the MO layer and a PR during a dry etch chemistry. In certain instances, the PR layer may be a positive tone PR which softens upon the application of UV in a curing process. When a MO is present on a PR layer, secondary electron emission from the MO layer is believed to interact with the positive tone PR and soften it under the action of the applied UV. Bubble defect formation can be particularly significant when using a high-emission MO such as tin oxide as this material has a very high secondary electron emission coefficient. It is believed that the softening of the PR layer leads to outgassing as the material breaks down, which forms bubble defects during curing. Schematic

pictures of bubble defects appearing in three example panes 100 may be seen in **FIG. 1** of the accompanying drawings.

[0019] In some examples, a UV precuring or pre-exposure operation is performed. With reference to **FIG. 2**, an example method 200 includes the performance of precuring or pre-exposure operations on a substrate such as a silicon wafer (Si) that includes a PR. A wafer including the PR is exposed to UV before a MO layer is deposited onto the PR. The precuring or pre-exposure operations may be performed in some examples during, or as a supplement to, an SAQP process, SADP process, or spacer-on-spacer process as described above. In some examples, a PR is exposed to UV light or radiation prior to deposition of a MO layer onto the PR and held immune to UV exposure by a plasma during or after deposition of the MO layer. Some tested examples using this method completely or at least substantially eliminated bubble defects from occurring, as shown in the example pane 202 in **FIG. 2**.

[0020] The preliminary or precuring UV exposure may be performed in an existing tool having a UV source, in an external chamber fitted with a UV source, or in a wafer-processing chamber having a plasma source, for example. Other arrangements are possible. A suitable plasma source may include helium, argon, or nitrogen in an amount sufficient to generate UV for precuring purposes.

[0021] The above examples are merely exemplary and should not be considered limiting. Thus, in other examples, bubble defect reduction may be performed during, or in relation to, other phases in a semiconductor manufacturing operation. In some examples, bubble defect reduction including a precuring or pre-exposure operation is performed during or in relation to a deposition phase, a photolithography phase, an etching phase, or other wafer processing phase involving the use of plasma, for example. In some examples, bubble defect reduction including a precuring or pre-exposure operation is performed during or in relation to a combination of phases.

[0022] Further, while some examples discussed above mention tin oxide as an example MO layer, the present disclosure may be employed on other types of films or layers, some of which may include MOs, metal nitrides, metal carbides, metal, and so forth. Further example layers or films also include dielectric material of metallic or non-metallic material. The example wafer

described in relation to FIG. 2 includes a layer or film of silicon material (Si). Other components or materials making up, or being included in, the illustrated Si, PR and MO layers, are possible.

[0023] Thus, some embodiments may include one or more of the following examples.

[0024] 1. A method of processing a substrate, the method comprising: applying a PR onto a surface of the substrate; pre-exposing the PR to UV light before depositing or etching a MO layer onto the PR; and depositing or etching a MO layer onto the PR subsequent to pre-exposing the PR to UV light.

[0025] 2. The method of example 1, wherein depositing or etching a MO layer onto the PR is performed immediately subsequent to the pre-exposure of UV light.

[0026] 3. The method of example 1 or 2, wherein the substrate includes a silicon wafer.

[0027] 4. The method of any one of examples 1-3, wherein pre-exposing the PR to UV light is performed during, or as a supplement to, a Self-Aligned Quadruple Patterning (SAQP) process.

[0028] 5. The method of any one of examples 1-4, wherein pre-exposing the PR to UV light is performed during, or as a supplement to, a Self-Aligned Double Patterning (SADP) process.

[0029] 6. The method of any one of examples 1-5, wherein pre-exposing the PR to UV light is performed during, or as a supplement to, a spacer-on-spacer process.

[0030] 7. The method of any one of examples 1-6, further comprising holding the PR immune to UV exposure during or after depositing or etching a MO layer onto the PR.

[0031] 8. The method of anyone of examples 1-7, wherein holding the PR immune to UV exposure includes holding the PR immune to UV exposure by a plasma.

[0032] 9. The method of any one of examples 1-8, wherein pre-exposing the PR to UV light before depositing or etching a MO later on-to the PR is performed in an existing substrate processing tool having a UV light source.

- [0033] 10. The method of any one of examples 1-9, wherein pre-exposing the PR to UV light before depositing or etching a MO later on-to the PR is performed in an external chamber fitted with a UV light source.
- [0034] 11. The method of any one of examples 1-10, wherein the substrate is processed in a substrate processing tool, the substrate processing tool including a plasma source for generating plasma, the plasma including a constituent in an amount sufficient to generate UV light for pre-exposing the PR to the UV light.
- [0035] 12. The method of example 11, wherein the plasma constituent includes one or more constituents including helium, argon, and nitrogen.
- [0036] 13. The method of any one of examples 1-12, wherein the MO layer includes tin oxide.
- [0037] 14. A method of processing a substrate, the method comprising: applying a PR onto a surface of the substrate; pre-exposing the PR to ultra violet (UV) light before depositing or etching a layer onto the PR; and depositing or etching a layer onto the PR subsequent to pre-exposing the PR to UV light.
- [0038] 15. The method of example 14, wherein the layer includes one or more of a MO layer, a metal nitride layer, a metal carbide layer, and a metal layer.
- [0039] Although various embodiments and examples have been described with reference to specific example embodiments and examples, it will be evident that various modifications and changes may be made to these embodiments without departing from the broader scope of the disclosure. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense. The accompanying drawings that form a part hereof, show by way of illustration, and not of limitation, specific embodiments in which the subject matter may be practiced. The embodiments illustrated are described in sufficient detail to enable those skilled in the art to practice the teachings disclosed herein. Other embodiments may be utilized and derived therefrom, such that structural and logical substitutions and changes may be made without departing from the scope of this disclosure. This Detailed Description, therefore, is not to be taken in a limiting sense, and the scope of

various embodiments is defined only by the appended claims, along with the full range of equivalents to which such claims are entitled.

[0040] Such embodiments of the inventive subject matter may be referred to herein, individually and/or collectively, by the term “invention” merely for convenience and without intending to voluntarily limit the scope of this application to any single invention or inventive concept if more than one is in fact disclosed. Thus, although specific embodiments have been illustrated and described herein, it should be appreciated that any arrangement calculated to achieve the same purpose may be substituted for the specific embodiments shown. This disclosure is intended to cover any and all adaptations or variations of various embodiments. Combinations of the above embodiments, and other embodiments not specifically described herein, will be apparent to those of skill in the art upon reviewing the above description.

CLAIMS

1. A method of processing a substrate, the method comprising:

applying a photoresist (PR) onto a surface of the substrate;

pre-exposing the PR to ultra violet (UV) light before depositing or etching a metal oxide (MO) layer onto the PR; and

depositing or etching a MO layer onto the PR subsequent to pre-exposing the PR to UV light.
2. The method of claim 1, wherein depositing or etching a MO layer onto the PR is performed immediately subsequent to the preexposure of UV light.
3. The method of claim 1, wherein the substrate includes a silicon wafer.
4. The method of claim 1, wherein pre-exposing the PR to UV light is performed during, or as a supplement to, a Self-Aligned Quadruple Patterning (SAQP) process.
5. The method of claim 1, wherein pre-exposing the PR to UV light is performed during, or as a supplement to, a Self-Aligned Double Patterning (SADP) process.
6. The method of claim 1, wherein pre-exposing the PR to UV light is performed during, or as a supplement to, a spacer-on-spacer process.
7. The method of claim 1, further comprising holding the PR immune to UV exposure during or after depositing or etching a MO layer onto the PR.

8. The method of claim 7, wherein holding the PR immune to UV exposure includes holding the PR immune to UV exposure by a plasma.
9. The method of claim 1, wherein pre-exposing the PR to ultra violet (UV) light before depositing or etching a MO later on-to the PR is performed in an existing substrate processing tool having a UV light source.
10. The method of claim 1, wherein pre-exposing the PR to ultra violet (UV) light before depositing or etching a MO later onto the PR is performed in an external chamber fitted with a UV light source.
11. The method of claim 1, wherein the substrate is processed in a substrate processing tool, the substrate processing tool including a plasma source for generating plasma, the plasma including a constituent in an amount sufficient to generate UV light for pre-exposing the PR to the UV light.
12. The method of claim 11, wherein the plasma constituent includes one or more constituents including helium, argon, and nitrogen.
13. The method of claim 1, wherein the MO layer includes tin oxide.
14. A method of processing a substrate, the method comprising:
 - applying a PR onto a surface of the substrate;
 - pre-exposing the PR to ultra violet (UV) light before depositing or etching a layer onto the PR; and
 - depositing or etching a layer onto the PR subsequent to pre-exposing the PR to UV light.
15. The method of claim 14, wherein the layer includes one or more of a MO layer, a metal nitride layer, a metal carbide layer, and a metal layer.

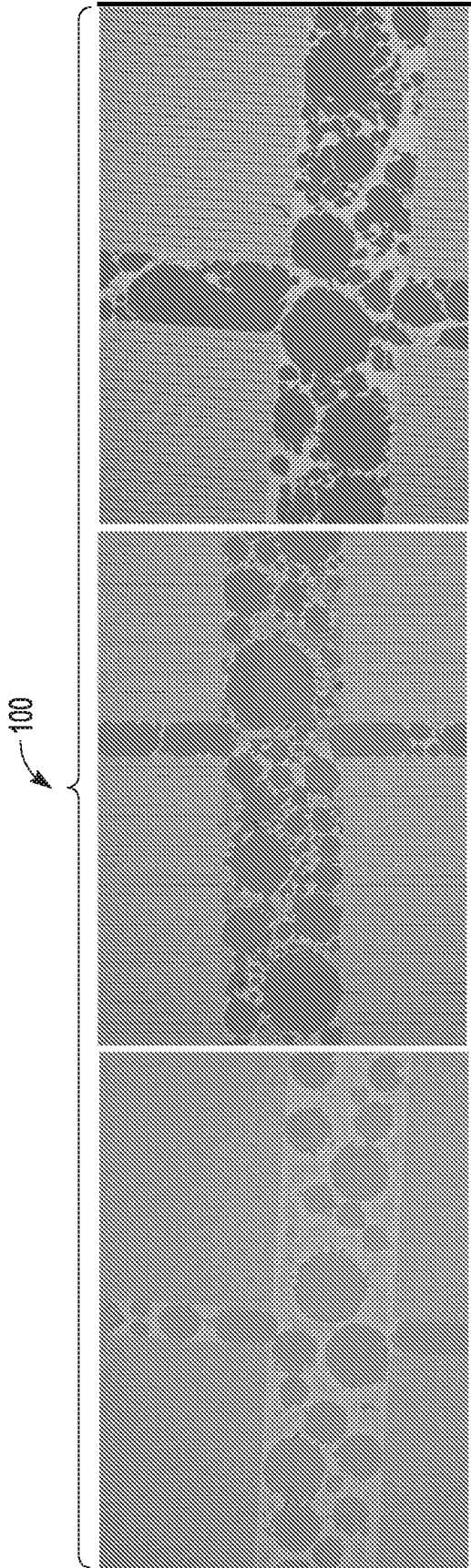


FIG. 1

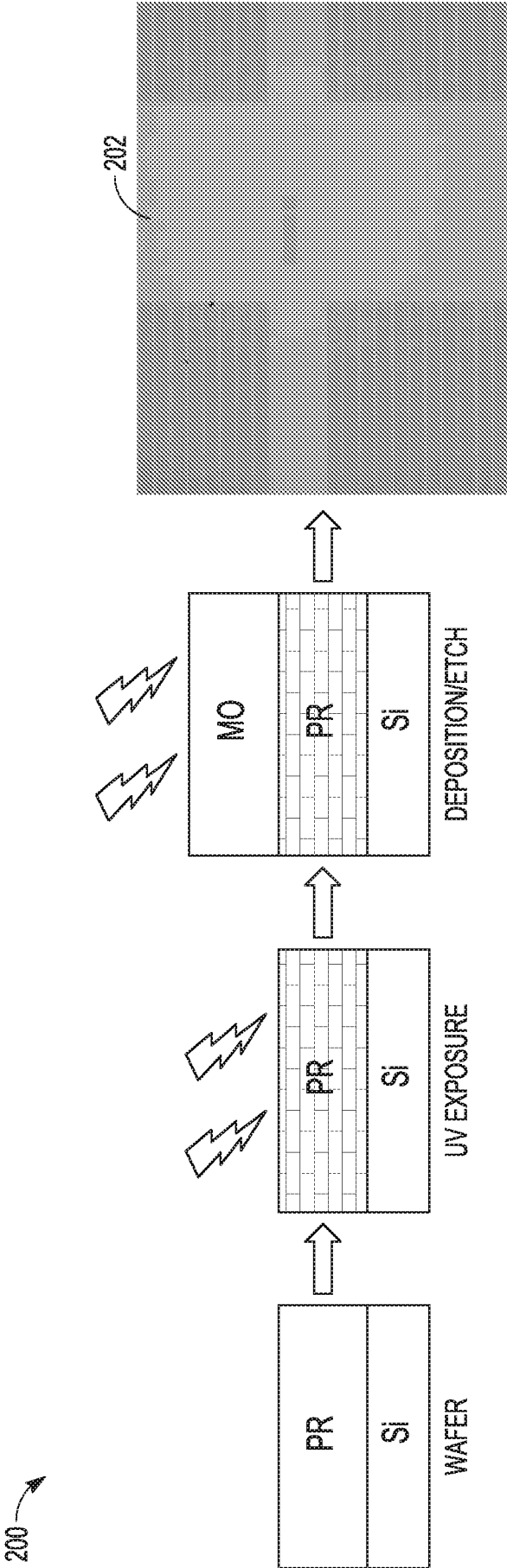


FIG. 2

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/027(2006.01)i, H01L 21/3065(2006.01)i, H01L 21/02(2006.01)i, G03F 7/20(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/027; G03F 7/20; H01L 21/306; H01L 21/3065; H01L 21/316; H01L 21/8242; H01L 27/108

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: self aligned multi patterning, photoresist, metal oxide, ultra violet, bubble defect

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-0669344 B1 (SAMSUNG ELECTRONICS CO., LTD.) 16 January 2007 paragraph [0021], claim 1 and figure 1a	1-15
A	KR 10-0216732 B1 (KEC CORP.) 01 September 1999 page 2, lines 30-40	1-15
A	JP 2018-037656 A (TOKYO ELECTRON LTD.) 08 March 2018 paragraphs [0027]-[0042] and figures 2A-8C	1-15
A	US 2015-0316857 A1 (LAM RESEARCH CORPORATION) 05 November 2015 paragraphs [0029]-[0033]	1-15
A	KR 10-2006-0081454 A (SAMSUNG ELECTRONICS CO., LTD.) 13 July 2006 paragraphs [0018]-[0021]	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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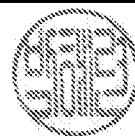


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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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