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(54) **Title**: METHOD AND APPARATUS FOR PROPAGATION DELAY AND EMI CONTROL

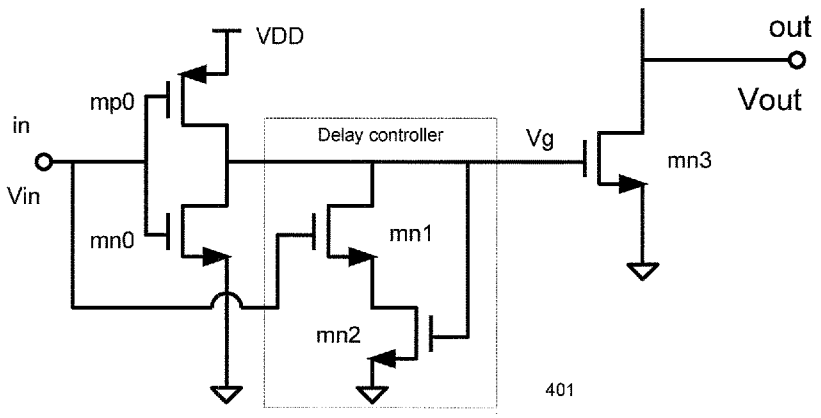

FIG. 4

(57) **Abstract**: An output switch driving capability booster which may effectively reduce a propagation delay in an output switch with an independently controllable output transition change rate. A delay controller coupled to the output switch may be used to control the propagation delay. The delay controlier may have a switch which may be switched on and off approximately simultaneously with the output switch, and a resistance device which may be adjusted to reduce the propagation delay.

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METHOD AND APPARATUS FOR PROPAGATION DELAY AND EMI CONTROL

CROSS REFERENCE TO RELATED APPLICATION

[01] This application claims the benefit of priority to previously filed U.S. provisional patent application Ser. No. 61/051,727, filed May 9, 2008, entitled DYNAMIC SWITCHING EDGE SPEED CONTROL CIRCUIT TO REDUCE EMI AND PROPAGATION DELAY. That provisional application is hereby incorporated by reference in its entirety.

BACKGROUND INFORMATION

[02] The present invention relates generally to driver circuits for output switches, and more specifically to driver circuits with better Electro-Magnetic Interference (EMI) and propagation delay control.

[03] An output switch may be used to provide a switching output voltage in response to a control signal from its driver circuit. Usually, a short propagation delay, the delay from the time of a control signal change to the time of a corresponding output voltage change, is preferred, since it is good for the stability of a circuit using the output voltage. At the same time, a slow transition on the output voltage may generate less EMI and thus is preferable. Prior art driver circuits for output switches have either a short propagation delay or a slow transition on the output voltage, but not both.

[04] Fig. 1 illustrates a prior art driver circuit for a N-type output switch mn3. The driver is inverter based and has a pair of complementary field-effect transistors (FETs): a P-type FET mp0 and a N-type FET mn0. Their gates are coupled to an input switching voltage V_{in}, and their drains are coupled together. A power supply V_{DD} is applied to the source of mp0, and the source of mn0 is grounded. The voltage at the drains of mp0 and mn0 is used to drive an output switch mn3, being applied to the gate of mn3 as V_g. The source of the output switch mn3 is grounded and an output voltage V_{out} is obtained from the drain of mn3. The threshold voltage of mn3 is V_{TH}, and $V_{TH} < V_{DD}$.

[05] Fig. 2 illustrates waveforms of V_{in}, V_g and V_{out} in the driver circuit of Fig. 1 during a process of turning off the output switch mn3. When the input voltage V_{in} is low, mp0 is conductive, mn0 is not conductive and $V_g \approx V_{DD}$. Consequently, mn3 is conductive, and V_{out} is low. When the input voltage V_{in} turns high, mp0 will stop being conductive when V_{in}

reaches its threshold voltage, and mn0 will become conductive when V_{in} reaches its threshold voltage. When mn0 is conductive, it may pull down V_g. When V_g drops below V_{TH}, the threshold voltage of mn3, the conductivity of mn3 reduces and V_{out} starts the transition from low to high.

[06] A propagation delay is measured from the V_{in} change to the point at which the transition of the output voltage V_{out} starts. The propagation delay may be controlled by the strength of the driver, or mn0 more specifically, because the stronger the driving strength of mn0, the faster the V_g may be pulled down, and the shorter the propagation delay. Fig. 2 illustrates waveforms of V_{in}, V_g, and V_{out} when a mn0 with a strong driving strength is used, and Fig. 3 illustrates waveforms of these signals when a mn0 with a weak driving strength is used. As shown, when a mn0 with a strong driving strength is used, the propagation delay is short; but the transition on V_{out} is fast, resulting in more EMI. On the contrary, when a mn0 with a weak driving strength is used, the transition on V_{out} is slower, which is good for EMI performance, but the propagation delay is very long.

[07] Adjusting mn0 current sink capability may change the output transition change rate, but it may affect the propagation delay as well.

[08] Therefore, it would be desirable to provide a driver for an output switch, which has a short propagation delay and a slow transition on the output voltage of the output switch.

BRIEF DESCRIPTION OF THE DRAWINGS

[09] So that features of the present invention can be understood, a number of drawings are described below. It is to be noted, however, that the appended drawings illustrate only particular embodiments of the invention and are therefore not to be considered limiting of its scope, for the invention may encompass other equally effective embodiments.

[10] Fig. 1 illustrates a prior art driver circuit for an output switch.

[11] Fig. 2 illustrates waveforms of signals in the circuit of Fig. 1 during a process of turning off the output switch when a strong driver circuit is used.

[12] Fig. 3 illustrates waveforms of signals in the circuit of Fig. 1 during a process of turning off the output switch when a weak driver circuit is used.

[13] Fig. 4 illustrates a driver circuit for an output switch according to one embodiment of the present invention.

[14] Fig. 5 illustrates waveforms of signals in the driver circuit of Fig. 4 during a process of turning off the output switch according to one embodiment of the present invention.

[15] Fig. 6A illustrates a driver circuit for an output switch according to one embodiment of the present invention.

[16] Fig. 6B illustrates waveforms of signals in the driver circuit of Fig. 6A according to one embodiment of the present invention.

[17] Fig. 7 illustrates a driver circuit for an output switch according to one embodiment of the present invention.

[18] Fig. 8 illustrates a driver circuit for an output switch according to one embodiment of the present invention.

DETAILED DESCRIPTION

[19] Embodiments of the present invention provide an output switch having a driving capability booster which may work just before a switching transition happens. The booster may effectively reduce the propagation delay in the output switch with an independently controllable output transition change rate. Embodiments may include a delay controller coupled to the output switch. The delay controller may have a switch whose conductivity may change approximately simultaneously with the output switch, and a resistance device which may be adjusted to reduce the propagation delay without affecting the output transition change rate. The booster may be used in class-D applications (e.g., switching amplifiers in which switches are either fully on or fully off to improve power efficiency), power management integrated circuits (ICs) having a switching output stage, or any high speed switching design with EMI concerns.

[20] Fig. 4 illustrates a driver circuit of an output switch according to one embodiment of the present invention. A delay controller 401 may be added to the circuit in Fig. 1 to control the propagation delay, which again may be measured from the time of V_{in} change to the time of V_{out} transition. The delay controller 401 may include transistors mn1 and mn2. The transistor mn1 may have its gate coupled to the input voltage V_{in}, its drain coupled to the

gate of the output switch mn3 and its source coupled to the drain of the transistor mn2, respectively. The transistor mn2 may have its gate coupled to the gate of the output switch mn3, its drain coupled to the source of mn1 and its source coupled to the ground, respectively. The transistor mn2 may be the same type of device as the output switch mn3, in this case a N-type FET, or alternatively may have similar transition properties as the output switch mn3, so that their transitions may happen approximately simultaneously. Transistors mn1 and mn0 need not to be similar to each other and may have different threshold voltages.

[21] Fig. 5 illustrates waveforms of signals in the driver circuit of Fig. 4 during a process of turning off the output switch mn3. As shown, before time t1, the input voltage V_{in} may be low, mp0 may be conductive, mn0 and mn1 may not be conductive, and Vg ≈ VDD. Since V_{DD} is higher than the threshold voltage V_{TH} of mn3, and that of mn2 too, mn3 and mn2 may be conductive, and V_{out} may be low.

[22] Around time t1, the input voltage V_{in} may turn high, mp0 may stop being conductive when V_{in} exceeds its threshold voltage, and mn0 and mn1 may become conductive when V_{in} reaches their threshold voltages respectively. When mn0 becomes conductive, it may pull V_g below V_{TH}. Before V_g drops below the threshold voltage V_{TH} of mn3 and mn2, both mn1 and mn2 are conductive, the circuit branch consisting of mn1 and mn2 may accelerate the pull down effect applied to V_g. The resistance of mn1 and/or mn2 may be adjusted to accelerate the drop of V_g: the lower the total resistance of the circuit branch consisting of mn1 and mn2, the faster V_g may be pulled down, the earlier mn3 may stop being conductive, and the earlier the transition of V_{out} may start. Thus, this may help to reduce the propagation delay between the time of V_{in} change and the time of V_{out} transition.

[23] Shortly after time t2, V_g may drop below the threshold voltage V_{TH} of mn3 and mn2. Transistors mn3 and mn2 may stop being conductive, and the V_{out} transition, from low to high, may start.

[24] In the circuit in Fig. 4, when the output switch mn3 is not conductive, mn2 in the delay controller 401 is not conductive either, since they have similar V_{TH} and their gates are coupled together. Accordingly, the delay controller 401 may be operative to pull down V_g only when both mn3 and mn2 are conductive, which is before the output transition, thus avoiding affecting the output transition change rate. As a result, the driving strength of mn0

may be selected solely for the output transition change rate, instead of a balance between the output transition change rate and the propagation delay.

[25] When the propagation delay is adjusted by changing the series resistance of mn1 and mn2, the adjustment may be independent of the driving strength of the driver, the output transition change rate, and so the EMI performance of the output switch mn3. The transistor mn1 may be other types of resistance devices, e.g., a resistor, a variable resistor or a potentiometer. The benefits of using a transistor is that it is conductive only when it is needed to accelerate the change of the voltage V_g, which minimizes power consumption when the delay controller 401 is not operative.

[26] As shown in Figs. 2, 3 and 5, the circuit of Fig. 4 may have the preferable short propagation delay of Fig. 2 achieved by using a mn0 with a strong driving strength in the prior art circuit in Fig. 1, and the preferable slow output transition change rate of Fig. 3 achieved by using a mn0 with a weak driving strength in the circuit of Fig. 1, since its propagation delay may be adjusted independently of its output transition change rate.

[27] Although an N-type FET output switch mn3 is used as an example in the circuit in Fig. 4, the principle of the invention may be used for other kinds of output switches, such as a P-typle FET, a bipolar junction transistor (BJT), and an insulated gate bipolar transistor (IGBT). In such circumstances, the delay controller should be configured to turn on and off approximately simultaneously with the output switch. More embodiments of the delay controller of the present invention will be described below.

[28] Fig. 6A illustrates a driver circuit of an output switch according to another embodiment of the present invention, and Fig. 6B illustrates waveforms of signals in the circuit of Fig. 6A.

[29] In Fig. 6A, the output switch may be a P-typle FET mp3, and a delay controller 601 may comprise transistors mp1 and mp2. The gate of mp1 may be coupled to the input voltage V_{in}, the source of mp1 may be coupled to the drain of mp2, and the drain of mp1 may be coupled to the gate of mp3, respectively. The gate of mp2 may be coupled to the gate of mp3, the source of mp2 may be coupled to the voltage V_{DD}, and the drain of mp2 may be couple to the source of mp1, respectively. Transistors mp2 and mp3 may be the same type of device, in this case P-type FETs, and may have approximately the same

threshold voltage V_{TH}, so that they may become conductive and stop being conductive approximately simultaneously.

[30] Fig. 6B illustrates waveforms of signals in the driver circuit of Fig. 6A during a process of turning off the output switch mp3. As shown, before time t3, the input voltage V_{In} may be high, mn0 may be conductive, mp0 and mp1 may not be conductive, and Vg ≈ 0. Thus, mp3 and mp2 may be conductive, and $V_{out} \approx V_{DD}$.

[31] Around time t3, the input voltage V_{in} may turn low, mn0 may stop being conductive when V_{in} falls below its threshold voltage, and mp0 and mp1 may become conductive when V_{In} reaches their threshold voltages respectively. When mp0 becomes conductive, it may push V_g up. Before V_g reaches the threshold voltage V_{TH} of mp3 and mp2, both mp1 and mp2 are conductive, the circuit branch consisting of mp1 and mp2 may accelerate the push up effect applied to V_g. The resistance of mp1 and/or mp2 may be adjusted to accelerate the rise of V_g: the lower the total resistance of the circuit branch consisting of mp1 and mp2, the faster V_g may be pushed up, the earlier mp3 may stop being conductive, and the earlier the transition of V_{out} may start. Thus, this may help to reduce the propagation delay between the time of V_{in} change and the time of V_{out} transition.

[32] Shortly after time t4, V_g may exceed the threshold voltage V_{TH} of mp3 and mp2. Transistors mp3 and mp2 may stop being conductive, and the V_{out} transition, from high to low, may start.

[33] In the circuit in Fig. 6A, when the output switch mp3 is not conductive, mn2 in the delay controller 601 is not conductive either, since they have similar V_{TH} and their gates are coupled together. Accordingly, the delay controller 601 may be operative to push up V_g only when both mp3 and mp2 are conductive, which is before the output transition, thus avoiding affecting the output transition change rate.

[34] Fig. 7 illustrates a driver circuit of an output switch according to another embodiment of the present invention.

[35] In Fig. 7, the output switch may be a N-type bipolar junction transistor (BJT) mn4, and a similar N-type BJT mn5 may be used to replace the transistor mn2 in the circuit shown in Fig. 4. Particularly, the base of the output switch mn4 may be coupled to the drains of mp0 and mn0, the emitter of mn4 may be grounded, and the output voltage V_{out} may be obtained from the collector of mn4. The base of mn5 may be coupled to the base

of mn4, the collector of mn5 may be coupled to the source of mn1, and the emitter of mn5 may be , grounded.

[36] The operation of the circuit shown in Fig. 7 may be similar to the circuit shown in Fig. 4. When V_{In} is low, mp0 may be conductive, mn0 and mn1 may be not conductive, and $V_g \approx V_{DD}$. Transistors mn4 and mn5 may be conductive and V_{out} may be low.

[37] When V_{in} changes from low to high and exceeds the threshold voltage of mp0, mp0 may stop being conductive. When V_{in} reaches the threshold voltage of mn0, mn0 may become conductive and start to pull down V_g. When V_{In} reaches the threshold voltage of mn1, mn1 may become conductive. Before V_g drops below the threshold voltage of mn4 and mn5, both mn1 and mn5 are conductive, and the circuit branch consisting of mn1 and mn5 may help to accelerate the drop of V_g. Adjusting the resistance of mn1 may help to adjust the change rate of V_g, and accordingly the length of the propagation delay between the time of V_{In} change and the time of V_{out} transition.

[38] When V_g drops below the threshold voltage of mn4, mn4 and mn5 may stop being conductive and the transition of V_{out} may start.

[39] Since mn5 in the delay controller 701 may become conductive and stop being conductive approximately simultaneously with the output switch mn4, the delay controller 701 may be used to adjust the propagation delay independently of the output voltage transition rate.

[40] Fig. 8 illustrates a driver circuit of an output switch according to one embodiment of the present invention.

[41] In Fig. 8, the output switch may be a N-type insulated gate bipolar transistor (IGBT) mn6, and a similar N-type IGBT mn7 may be used to replace the transistor mn2 in the circuit shown in Fig. 4. The operation of the circuit shown in Fig. 8 may be similar to the circuits shown in Figs. 4 and 7. Transistors mn6 and mn7 may be similar devices and become conductive and stop being conductive approximately simultaneously.

[42] Several features and aspects of the present invention have been illustrated and described in detail with reference to particular embodiments by way of example only, and not by way of limitation. Those of skill in the art will appreciate that alternative implementations and various modifications to the disclosed embodiments are within the

scope and contemplation of the present disclosure. Therefore, it is intended that the invention be considered as limited only by the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A circuit, comprising:

an output switch coupled to a source potential at a first terminal and coupled to an output terminal of the circuit at a second terminal thereof,

a driver circuit, having an input terminal and an output terminal, the output terminal coupled to a control input of the output switch, and

a delay controller, having a first terminal coupled to the input terminal of the driver circuit, a second terminal coupled to the control input of the output switch and a third terminal coupled to the source potential, the delay controller responsive to a predetermined input signal at the first terminal by driving the control input of the output switch to the source potential.

2. The circuit of claim 1, wherein the delay controller comprises a switching device which becomes conductive and stops being conductive approximately simultaneously with the output switch.

3. The circuit of claim 2, wherein the switching device and the output switch are the same type of device.

4. The circuit of claim 2, wherein the switching device and the output switch are transistors.

5. The circuit of claim 4, wherein the switching device and the output switch have approximately the same threshold voltage.

6. The circuit of claim 2, wherein the delay controller further comprises a resistance device on a circuit path from the control input of the output switch to the source potential, and reducing the resistance device's resistance shortens a time for driving the control input of the output switch to the source potential.

7. The circuit of claim 6, wherein the output switch is a field-effect transistor (FET); and the switching device is an FET with similar transition properties, with its gate coupled to a gate of the output switch and its source coupled to the source potential.

8. The circuit of claim 7, wherein the resistance device is an FET, with its gate coupled to the first terminal of the delay controller, its drain coupled to the second terminal of the delay controller, and its source coupled to a drain of the switching device.

9. The circuit of claim 7, wherein the output switch and the switching device are N-type FETs.

10. The circuit of claim 7, wherein the output switch and the switching device are P-type FETs.

11. The circuit of claim 6, wherein the output switch is a bipolar junction transistor (BJT); and the switching device is a BJT with similar transition properties, with its base coupled to a base of the output switch and its emitter coupled to the source potential.

12. The circuit of claim 6, wherein the output switch is an insulated gate bipolar transistor (IGBT); and the switching device is an IGBT with similar transition properties, with its base coupled to a base of the output switch and its emitter coupled to the source potential.

13. The circuit of claim 1, wherein the driver circuit comprises a pair of complementary FETs.

14. A circuit, comprising:

a driver, receiving an input voltage and turning on and off an output switch; and

a delay controller, coupled to the driver and the output switch,

wherein the delay controller comprises a switching device coupled to the output switch and being switched approximately simultaneously with the output switch to control a propagation delay between a transition in the input voltage and a transition in an output voltage at the output switch.

15. A method comprising:

receiving an input voltage;

generating a control voltage to control an output switch which provides an output voltage;

controlling a propagation delay between an input voltage transition and an output voltage transition by adjusting the control voltage until the output voltage transition occurs,

wherein the propagation delay control is independent of a change rate of the output voltage.

16. The method of claim 15, further comprising: switching on a current path between the output switch and a fixed voltage to adjust the control voltage.

17. The method of claim 16, wherein the current path and the output switch are switched approximately simultaneously.

18. The method of claim 17, further comprising: adjusting a resistance device on the current path to reduce the propagation delay.

19. The method of claim 16, wherein the current path is switched by a switching device coupled to the output switch.

20. The method of claim 16, wherein the fixed voltage is the ground.

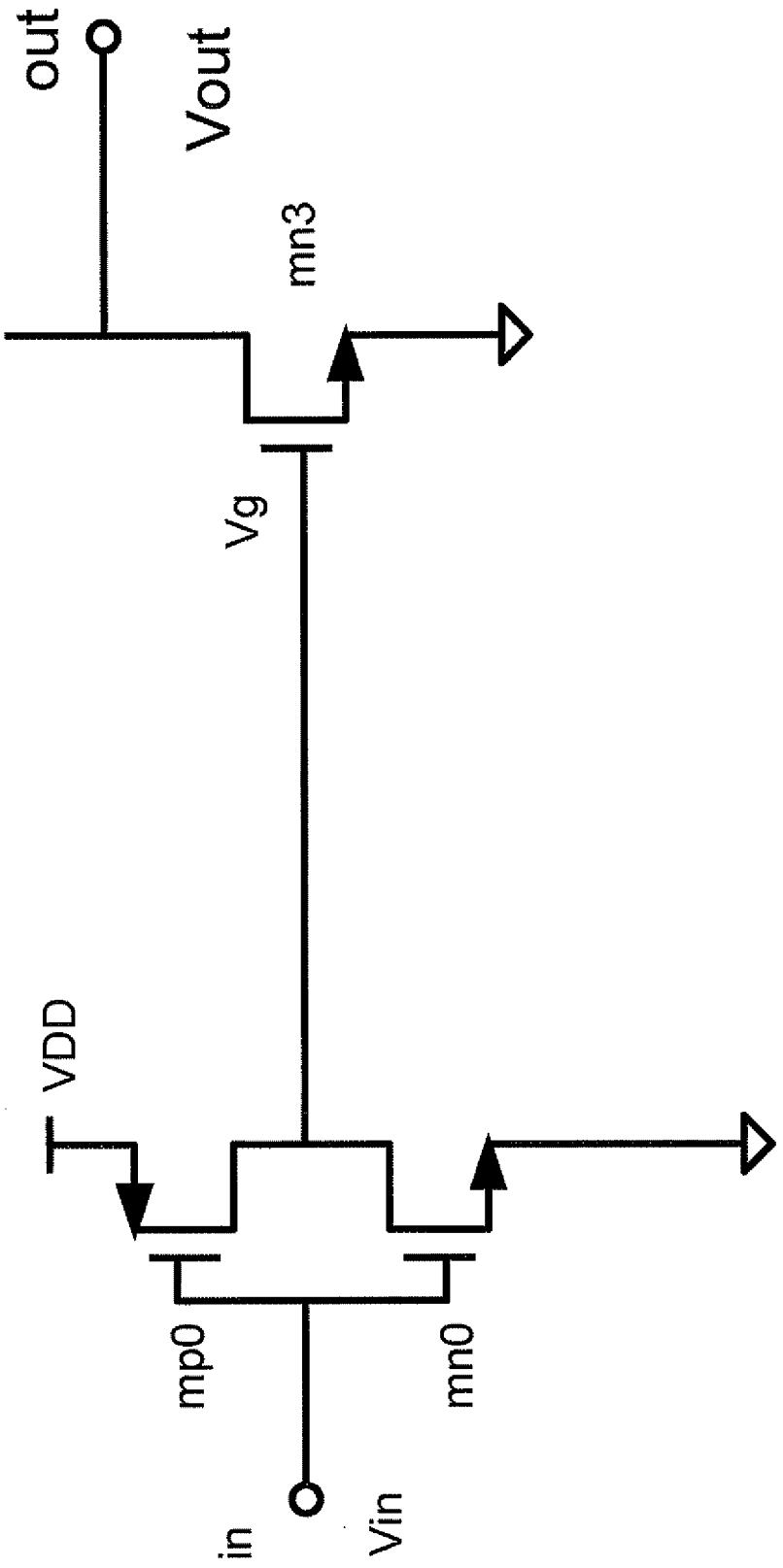


FIG. 1 (PRIOR ART)

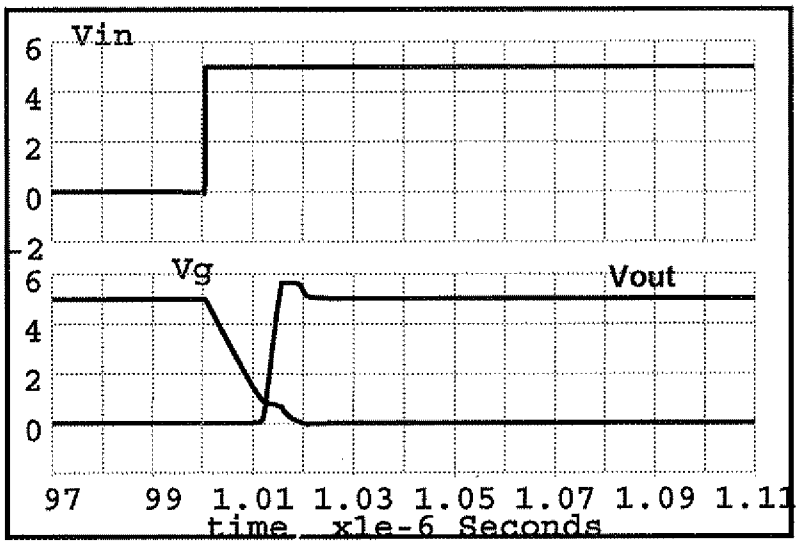


FIG. 2 (PRIOR ART)

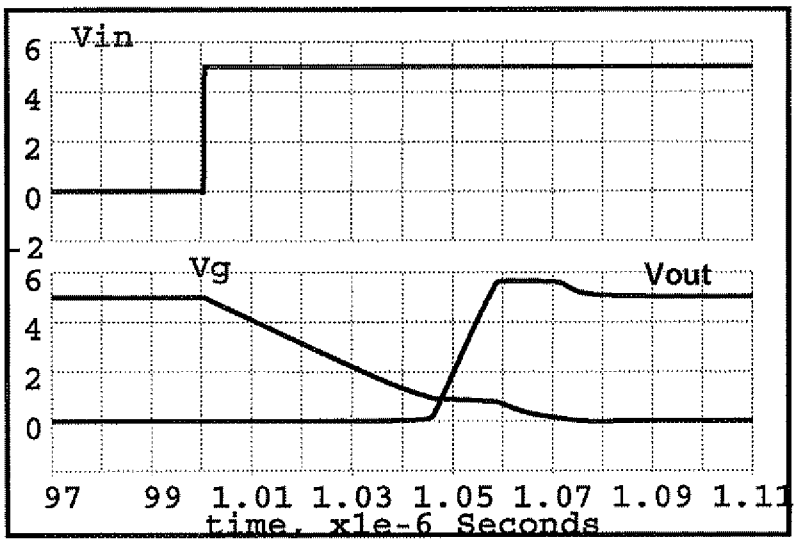
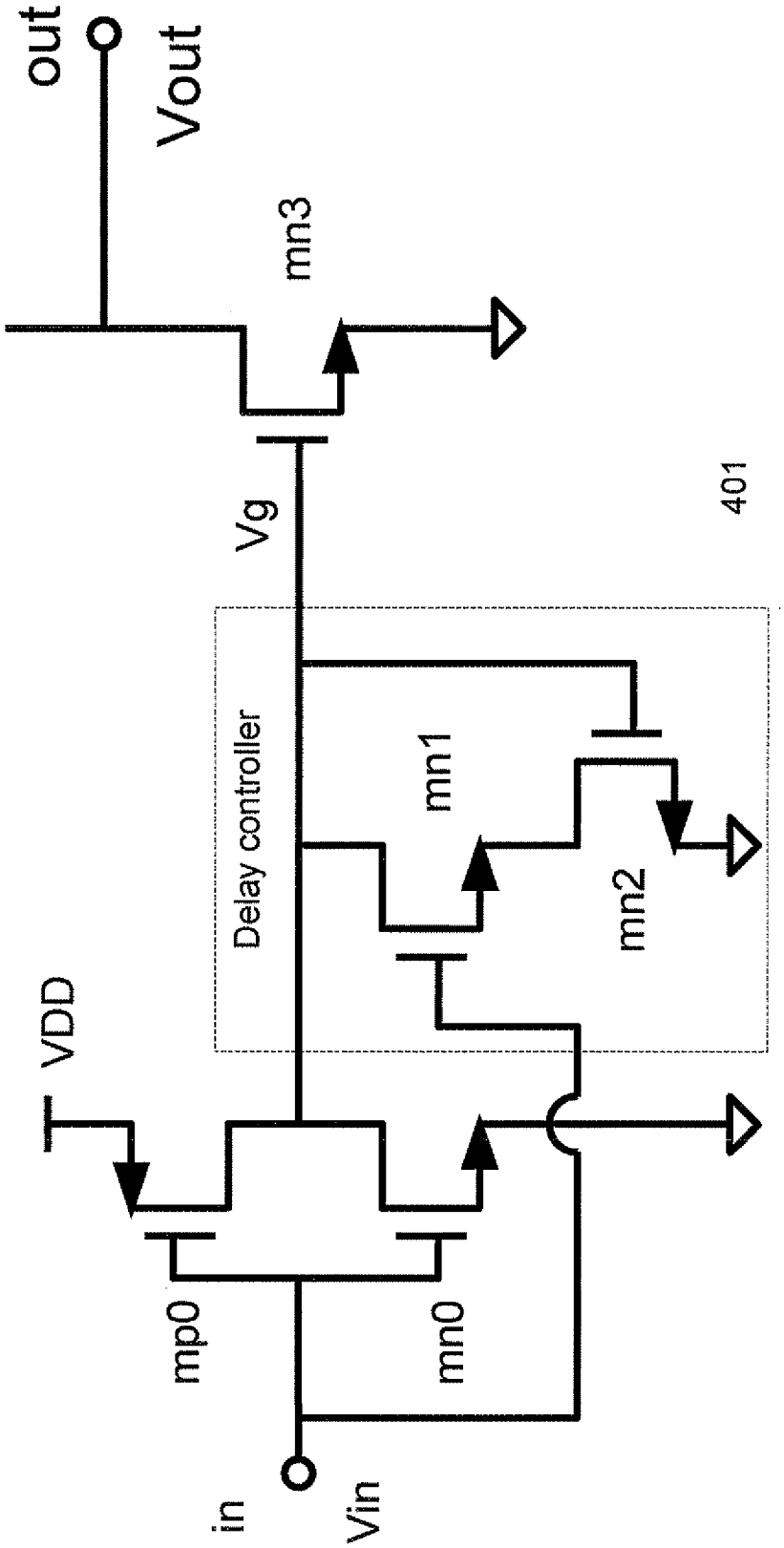


FIG. 3 (PRIOR ART)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mn3
Vg
401
Delay controller
mn1
mn2
VDD
mp0
mn0
in
Vin

FIG. 4

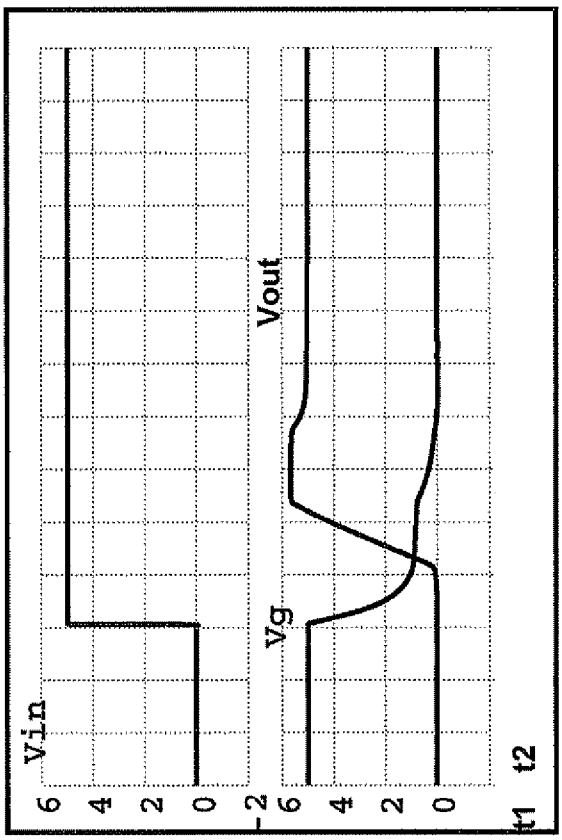
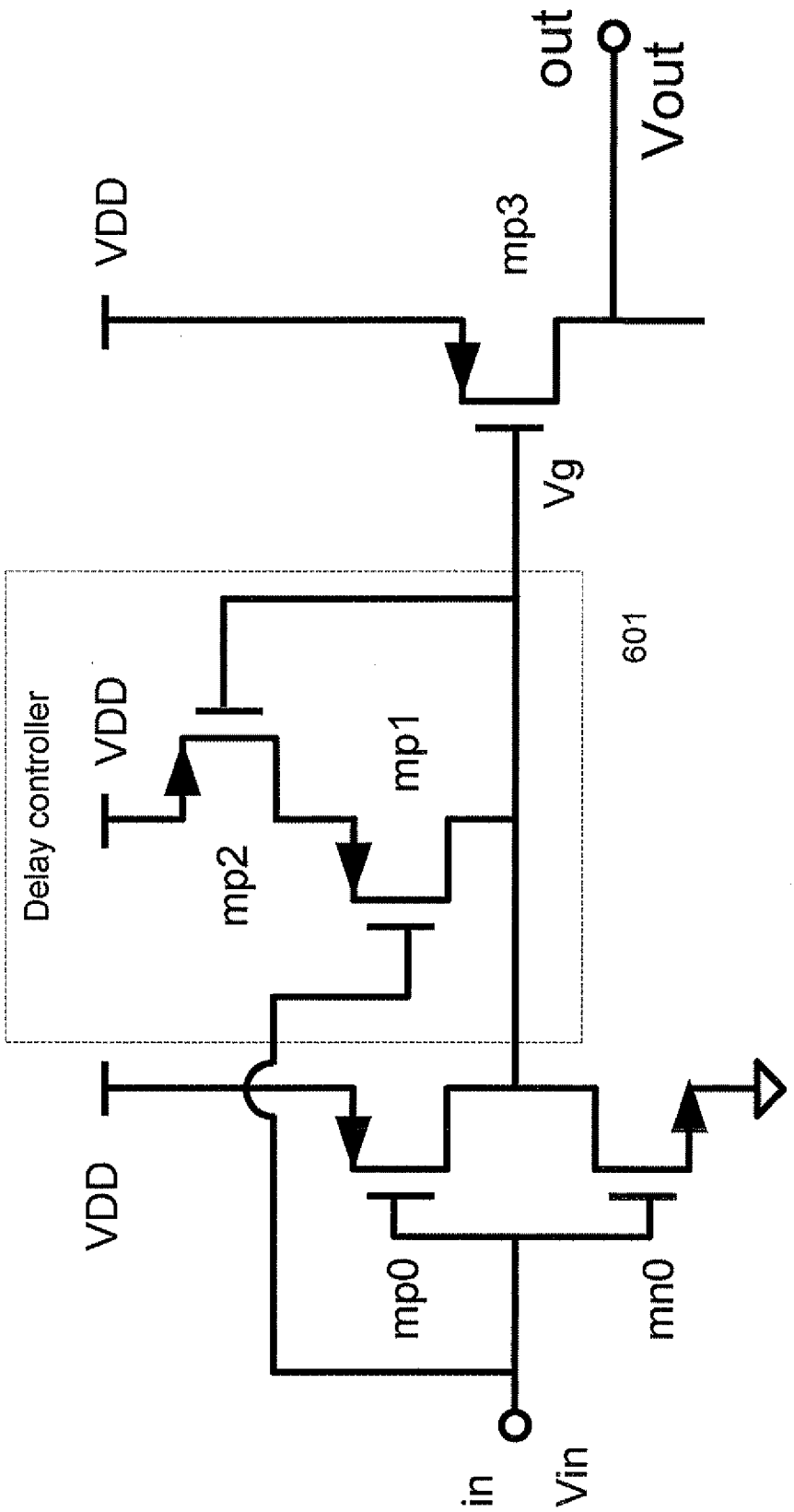


FIG. 5


out
Vout
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mp3
Vg
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VDD
mp1
mp2
601
VDD
mp0
mn0
in
Vin

FIG. 6A

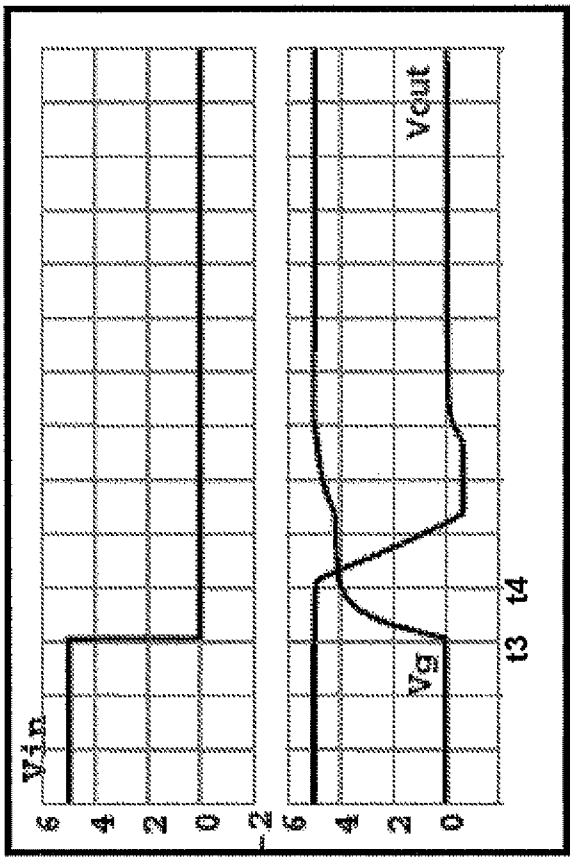
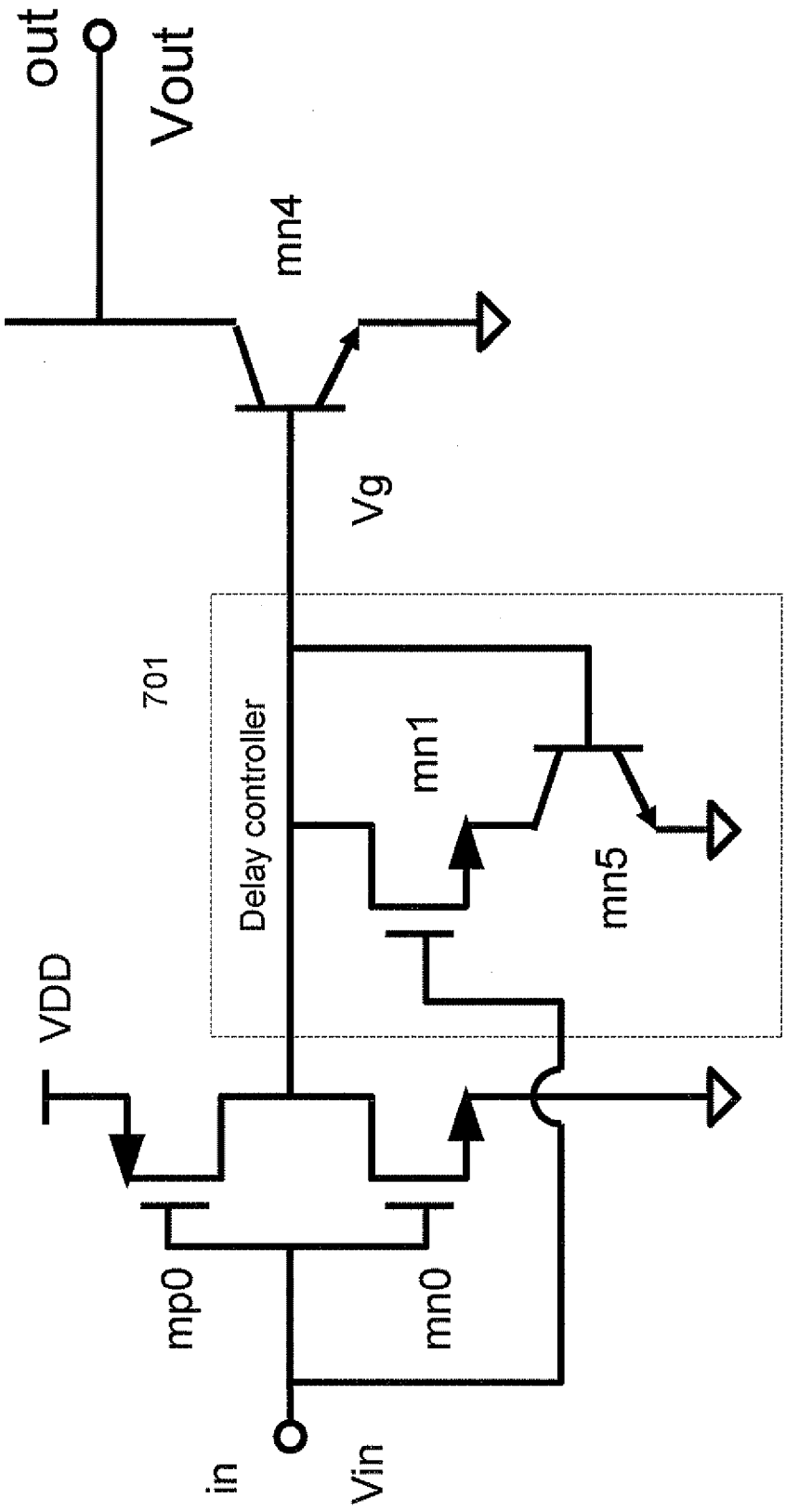


FIG. 6B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Vg
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Delay controller
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VDD
mp0
mn0
in
Vin

FIG. 7

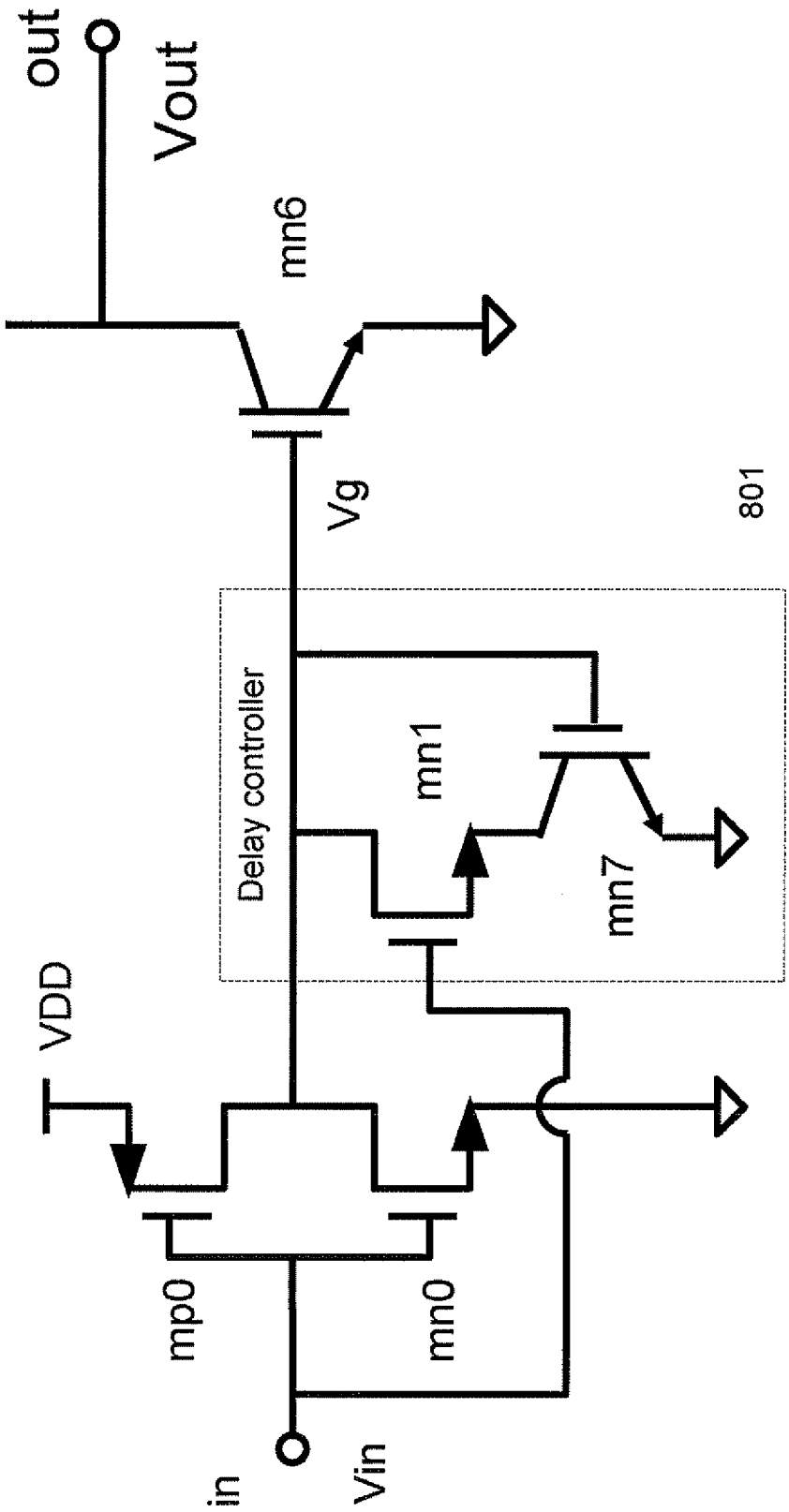
out
Vout
mn6
Vg
801
Delay controller
mn1
mn7
VDD
mp0
mn0
in
Vin

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2009/043014

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H03K 19/094 (2009.01)
USPC - 326/83
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H03K 19/094 (2009.01)
USPC - 326/83

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Minesoft Patbase

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 6,094,086 A (CHOW) 25 July 2000 (25.07.2000) entire document	1, 15 --- 2-14, 16-20
Y	US 4,959,561 A (MCDERMOTT et al) 25 September 1990 (25.09.1990) entire document	2-14
Y	US 6,091,260 A (SHAMARO) 18 July 2000 (18.07.2000) entire document	16-20

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 June 2009	26 JUN 2009
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