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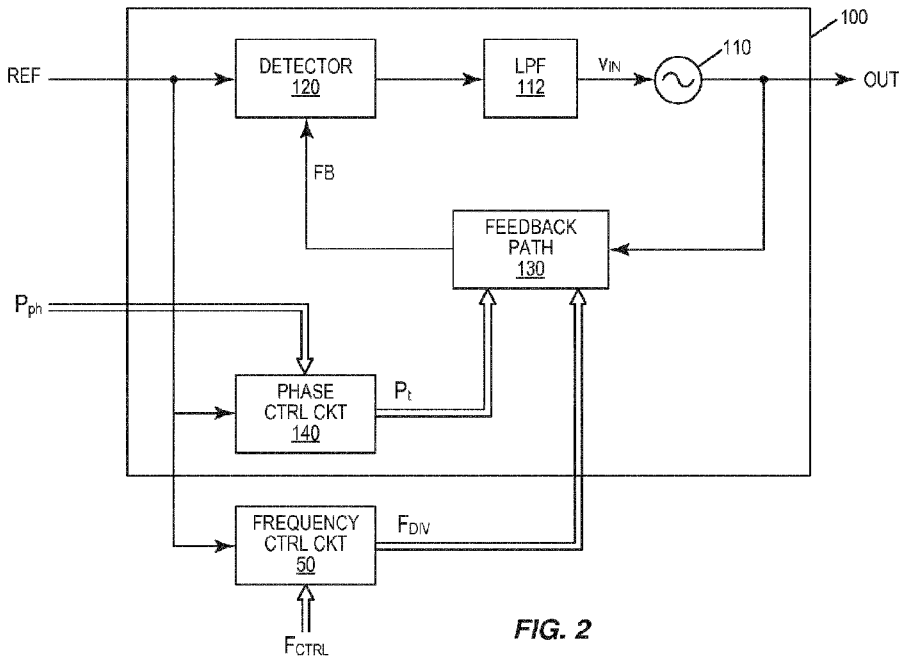

FIG. 2

(57) Abstract: A digital solution for phase control of an output of a phase-locked loop (PLL) (100) is provided to achieve a desired phase shift at the output of the PLL (100). To that end, a fraction of the pulses of a PLL feedback signal are time shifted to achieve a desired average time shift associated with the desired phase shift. As a result, a desired phase shift is generated at the output of the PLL (100), while a desired devisor of the feedback signal is maintained on average. The resulting digital solution provides highly accurate phase control.

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DIGITAL PHASE CONTROLLED PLLS

TECHNICAL FIELD

The solutions presented herein relate to Radio Frequency (RF) integrated circuits, frequency synthesizers, Phase-Locked Loops (PLLs), phase noise, beamforming, 5G wireless systems, etc.

BACKGROUND

Wireless systems typically upconvert a baseband signal to a Radio Frequency (RF) signal for transmission, and downconvert received RF signals to baseband for processing. Such frequency conversion requires producing a reliable mixing frequency signal, typically referred to as a local oscillator (LO) signal, for use in the RF front-end of a wireless device. Phase-Locked Loops (PLLs) are often used to provide such mixing frequency signals.

In some cases, stringent requirements are placed on the mixing frequency signal, such as produced by a PLL. For example, it is foreseen that 5G cellular systems will use millimeter waves, where the frequencies currently in discussion range between 15 GHz and 60 GHz. In order to use such 5G system outdoors, a longer cyclic prefix has to be used compared to newly released 60 GHz indoor systems. Such longer cyclic prefixes necessitate a closer sub-carrier spacing in the OFDM modulation. This closer sub-carrier spacing poses stringent phase noise requirements on the outputs of the PLLs. At the same time, beamforming should be supported to increase the range and capacity of the system, which results in a large number of antenna elements. The signal at each antenna element of a beamforming system will have an individual phase shift that controls the beam direction. In some implementations, the beam controlling phase shifts are imposed on the mixing signal. In any event, accurate beamforming requires accurate phase shifts. It is also desirable to be able to program the frequency of the mixing signal to enable the wireless device to operate on different frequency channels and in different bands.

As a result of all of these considerations, there is a need to improve the generation of the mixing frequency signals so as to provide the desired frequency programmability, to provide the desired phase control, and to provide improved phase noise performance, particularly in light of possible future 5G systems.

SUMMARY

The solution presented herein provides a digital solution for phase control of an output of a phase-locked loop (PLL) to achieve a desired phase shift at the output of the PLL. To that end, the solution presented herein shifts a timing, e.g., delays a fraction, e.g., one or more pulses, of a PLL feedback signal so that an average desired time shift associated with the desired phase shift is obtained. As a result, a desired phase shift is generated at the output of

the PLL, while a desired devisor of the feedback signal is maintained on average. The solution presented herein therefore does not impact the PLL output frequency, and therefore allows independent control of the PLL output phase and frequency. The resulting digital solution provides highly accurate phase control.

In one exemplary embodiment, a PLL comprises an oscillator, a detector, a feedback path, and a phase control circuit. The oscillator is configured to generate a PLL output signal at an output of the PLL responsive to a reference signal input to the PLL. The detector is configured to compare the reference signal to a feedback signal to control a frequency of the PLL output signal, the feedback signal being derived by the feedback path of the PLL from the PLL output signal. The phase control circuit is operatively connected to the feedback path of the PLL, and is configured to generate a timing control signal responsive to a phase control signal. Application of the timing control signal to the feedback path shifts a timing, e.g., delays, one or more pulses of the feedback signal to generate a desired phase shift at the output of the PLL while maintaining a desired average divisor of the feedback signal.

In another exemplary embodiment, a beamforming system comprises an antenna array, a plurality of radio frequency (RF) front-end circuits, and a frequency control circuit. The antenna array comprises a plurality of antenna elements. Each RF front-end circuit is coupled to one of the antenna elements, where each of the RF front-end circuits comprises a PLL comprising an oscillator, a detector, a feedback path, and a phase control circuit. The oscillator of each PLL is configured to generate a PLL output signal at an output of the PLL responsive to a reference signal input to the PLL. The detector of each PLL is configured to compare the reference signal to a feedback signal to control a frequency of the corresponding PLL output signal, the feedback signal being derived by the feedback path of the corresponding PLL from the corresponding PLL output signal. The phase control circuit of each PLL is operatively connected to the feedback path of the corresponding PLL, and is configured to generate a timing control signal responsive to a phase control signal. Application of the timing control signal to the feedback path shifts a timing of one or more pulses of the feedback signal to generate a desired phase shift at the output of the corresponding PLL while maintaining a desired average divisor of the feedback signal. The frequency control circuit is configured to control a frequency of each of the plurality of PLLs relative to the reference signal.

Another exemplary embodiment comprises a method of controlling a phase at an output of a PLL to achieve a desired phase shift at the output of the PLL. The method comprises generating a PLL output signal at the output of the PLL responsive to a reference signal input to the PLL. The method further comprises comparing the reference signal to a feedback signal in a detector to control a frequency of the PLL output signal, the feedback signal being derived by a feedback path of the PLL from the PLL output signal. The method further comprises generating a timing control signal responsive to a phase control signal, and shifting a timing, responsive to the timing control signal, of one or more pulses of the feedback signal to achieve

a desired average time shift to generate a desired phase shift at the output of the PLL while maintaining a desired average divisor of the feedback signal.

Another exemplary embodiment comprises a computer program product stored in a non-transitory computer readable medium for controlling a phase at an output of a PLL to achieve a desired phase shift at the output of the PLL. The computer program product comprises software instructions which, when run on a processing circuit, causes the processing circuit to generate a PLL output signal at the output of the PLL responsive to a reference signal input to the PLL, and compare the reference signal to a feedback signal in a detector to control a frequency of the PLL output signal, the feedback signal being derived by a feedback path of the PLL from the PLL output signal. The software instructions which, when run on the processing circuit, further causes the processing circuit to generate a timing control signal responsive to a phase control signal, and shift a timing, responsive to the timing control signal, of one or more pulses of the feedback signal to achieve a desired average time shift to generate a desired phase shift at the output of the PLL while maintaining a desired average divisor of the feedback signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A shows a simplified block diagram of an exemplary beam forming system.

Figure 1B shows a simplified block diagram of an exemplary RF front-end.

Figure 2 shows a PLL and frequency control circuit according to one exemplary embodiment.

Figure 3 shows a method for controlling a phase at an output of a PLL according to one exemplary embodiment.

Figure 4 shows a block diagram of a PLL feedback path and phase control circuit of the PLL of Figure 2 according to one exemplary embodiment.

Figure 5 shows an exemplary signaling diagram for the embodiment of Figure 4.

Figure 6 shows a block diagram of a PLL feedback path and phase control circuit of the PLL of Figure 2 according to another exemplary embodiment.

Figure 7 shows a block diagram of a filter circuit for the phase control circuit of Figure 6 according to one exemplary embodiment.

Figure 8 shows an exemplary signaling diagram for the embodiment of Figure 6.

Figure 9 shows a frequency control circuit according to one exemplary embodiment.

DETAILED DESCRIPTION

Figure 1A shows a beamforming system 10 comprising an antenna array 20 with M antenna elements 22, where each antenna element 22 is coupled to a corresponding radio frequency (RF) front-end 30. Each RF front-end 30 comprises a phase-locked loop (PLL) 100 coupled to a transmission path and a reception path, as shown in Figure 1B. The PLL 100

generates a PLL output signal OUT having specific frequency and phase characteristics, where a phase control signal P_{ph} controls the phase of OUT, and F_{div} controls the frequency of OUT. In some systems, e.g., those employing Frequency Division Duplexing (FDD), two PLLs may be required, where one PLL 100 is coupled to the transmit path and one PLL 100 is coupled to the receive path. For simplicity, however, Figure 1B only shows one PLL 100. On the transmission side, an upconversion mixer 32 operatively coupled to the output of the PLL 100 upconverts an input signal responsive to the frequency of the output signal supplied by the PLL 100. An amplifier 34, e.g., a power amplifier, amplifies the upconverted signal for transmission by the corresponding antenna element 22. On the receiving side, an amplifier 36, e.g., a low-noise amplifier, amplifies signals received by the corresponding antenna element 22. A downconversion mixer 38 downconverts the amplified signal responsive to the frequency of the PLL output signal. It will be appreciated that Figures 1A and 1B show simplified block diagrams of the exemplary beamforming system 10 and RF front-end 30. Other components not pertinent to the discussion have been excluded from the drawings for simplicity.

The PLLs 100 in the RF front-end circuits 30 of an RF system each receive a common reference signal, either directly from a reference oscillator or from a reference PLL. The PLLs 100 then locally multiply the reference signal to a higher (RF) frequency. By using the common reference signal, the output signals of the PLLs 100 will be fixed in frequency and phase with respect to each other. When part of a beamforming system, each PLL 100 can also execute separate phase control, e.g., based on the a phase control signal P_{ph}, for beamforming purposes. To control the direction of the beam for the antenna array 20, e.g., the phase of the transmission signal applied to at least some of the antenna elements 22 (or of the reception signal received from at least some of the antenna elements 22) must be accurately controlled. In some systems, for example, digitally controlled current sources are used to inject (analog) current into the loop filters of each PLL 100, which will produce an accurate and linear phase shift of the PLL output signal. However, the current injection solution represents an analog phase control solution. The solution presented herein provides an alternative solution that instead relies on digital phase control, which can further improve the accuracy of the phase control.

The general idea for the solution presented herein is to shift a timing of, e.g., delay, a fraction (e.g., one or more) of the pulses of a PLL feedback signal to achieve a desired average delay. When the PLL feedback signal is, e.g., delayed by some number of output clock cycles, the output phase is advanced by the same number of clock cycles to make sure the PLL 100 remains locked. For example, modulating the delay of the feedback signal so that it is zero 40% of the time and one output clock cycle 60% of the time delays the feedback signal by 0.60 output clock cycles on average. For the PLL to remain locked, the output phase is then advanced by 0.60 clock cycles, i.e., 216°. In another example, delaying a quarter of the pulses

of the feedback signal by one cycle results in a 90° phase shift in the PLL output signal. However, this phase shift process does not change the average frequency of the PLL output signal. Thus, delaying a fraction of the pulses of the PLL feedback signal digitally generates a phase shift at the output of the PLL while maintaining a desired average devisor of the feedback signal. Such a digital solution provides highly accurate phase control. Further, such a solution enables independent control of the PLL output frequency and phase.

Figure 2 shows one exemplary block diagram of a PLL 100 that includes phase control according to the solution presented herein. The PLL 100 comprises an oscillator 110, detector 120, feedback path 130, and phase control circuit 140, and optionally includes a low-pass filter 112 disposed between the detector 120 and oscillator 110. Oscillator 110, which may programmable and which, in some embodiments, may comprise a voltage-controlled oscillator (VCO) that is programmable, generates an output signal OUT having an output frequency f_{out} at the output of the PLL 100 responsive to a reference signal REF having a reference frequency f_R input to the detector 120. The feedback path 130 generates a feedback signal FB having a feedback frequency f_{FB} from the output signal OUT, e.g., by dividing the output frequency f_{out} by F_{div}, where F_{div} may comprise an integer or a rational number and where F_{div} is provided by a frequency control circuit 50. The detector 120 compares the reference frequency f_R to the feedback frequency f_{FB} to generate one or more PLL control signals. The PLL control signal(s) output by the detector 120 may be filtered by filter 112 to generate a filtered signal v_{in}. The filtered signal v_{in} is applied to the oscillator 110. When locked, the output signal OUT therefore has a frequency f_{out} that is the average value of F_{div} times the reference frequency f_R.

Phase control circuit 140 generates a timing control signal P_t responsive to a phase control signal P_{ph}. Application of the timing control signal P_t to the feedback path 130 shifts a timing of, e.g., delays, a fraction of the pulses, e.g., one or more pulses, of the feedback signal FB to generate a desired phase shift in the PLL output signal OUT while maintaining a desired average divisor of the feedback signal FB. The time shifting of the pulses of the feedback signal FB, as discussed herein, refers to how the feedback signal pulses are shifted in time relative to the non-shifted timing of the feedback signal FB. In some embodiments, the feedback signal pulses to be, e.g., delayed are randomly selected. While not required, the phase control circuit 140 comprises a modulation circuit, e.g., a delta-sigma modulator, the use of which enables the low-pass characteristic transfer function of the PLL 100 to attenuate any undesirable high frequency components resulting from the phase control solution presented herein.

Figure 3 shows one exemplary phase control method 200 as implemented by the PLL 100. PLL 100 generates the PLL output signal OUT having an output frequency f_{out} at the output of the PLL 100 responsive to a reference frequency f_R of the reference signal REF input to the PLL 100 (block 210). The feedback path 130 of the PLL 100 derives a feedback signal FB having a feedback frequency f_{FB} from OUT, and controls f_{out} based on a comparison between f_R and f_{FB} (block 220). The PLL 100 (phase control circuit 140) generates a timing control signal P_t responsive to a phase control signal P_{ph} (block 230). By applying the timing control signal P_t to the feedback path 130, the PLL 100 shifts a timing of a fraction of the pulses, e.g., one or more pulses, of the feedback signal FB to generate a desired phase shift at the output of the PLL 100 while maintaining a desired average divisor of the feedback signal FB (block 240), and therefore, while maintaining the desired PLL output frequency f_{out}. The following presents two exemplary and non-limiting embodiments for shifting the timing of the pulse(s) of the feedback signal. It will be appreciated that the time shifting implemented herein may comprise delaying and/or advancing the pulse(s) of the feedback signal.

Figure 4 shows a block diagram of the feedback path 130 for the PLL 100 of Figure 2 according to one exemplary embodiment. In this exemplary embodiment, a direct delay as specified by the timing control signal is applied to the feedback signal to delay the pulse(s) of the feedback signal. To that end, feedback path 130 comprises a frequency divider 132, a multiplexer 134, and a delay line 136. The frequency divider 132 divides the frequency of the PLL output signal OUT by a frequency divisor F_{div} output by the frequency control circuit 50. The delay line 136 comprises a plurality of serially connected delay elements 136A, 136B, 136C, etc. The output of the frequency divider 132 and the outputs of at least some of the delay elements of the delay line 136 are input to the multiplexer 134. The multiplexer periodically selects, responsive to the timing control signal P_t, one of the multiplexer inputs as the feedback signal FB. In so doing, the multiplexer 134 controls the delay applied to the feedback signal FB such that only the feedback signal having the desired delay is output by the feedback path 130. For example, multiplexer 134 may select the signal s_{i3} output from delay element 136B as the feedback signal FB.

It will be appreciated that in some embodiments, the delay line 136 of Figure 4 may comprise a plurality of delay elements that each sequentially impart a common delay to the input signal. In other embodiments, the delay elements of the delay line 136 may each impart different amounts of delay to the input signal, depending on the desired phase shift options. Further, while Figure 4 only explicitly shows three delay elements, it will be appreciated that delay line 136 may comprise any number of delay elements.

The phase control circuit 140 for the exemplary embodiment of Figure 4 may generate any type of timing control signal P_t capable of controlling multiplexer 134. For example, in one embodiment the phase control circuit 140 may comprise a modulation circuit 142, clocked by the reference signal REF, that generates the timing control signal P_t responsive to the phase control signal P_{ph}. In general, this timing control signal reduces/increases the feedback divisor during some of the clock cycles to advance/delay the corresponding feedback signal pulse(s).

Figure 5 shows an exemplary signaling diagram that encompasses the operation of the general block diagram of Figure 2, as well as the specific embodiment of Figure 4. As shown in Figure 5, as the timing control signal P_t changes, the feedback signal FB also changes, causing a timing difference between the feedback signal FB and the reference signal REF. This timing difference causes a phase shift in the output signal OUT (not shown in Figure 5 for clarity), while maintaining (on average) the desired output frequency f_{out} in the PLL output signal OUT.

Figure 6 shows a block diagram of the feedback path 130 for the PLL 100 of Figure 2 according to another exemplary embodiment. In this exemplary embodiment, the timing control signal P_t indirectly controls the delay of the feedback signal pulses by modifying the frequency divisor F_{div}. To that end, the feedback path 130 comprises the frequency divider 132 and a combiner 138, e.g., an adder circuit 138, and the phase control circuit 140 comprises the modulation circuit 142 and a filter circuit 144. Modulation circuit 142 generates a modulated output P_{mod} responsive to the phase control signal P_{ph}, and the filter 144 filters the modulated output P_{mod} to generate the timing control signal P_t. In this embodiment, the timing control signal P_t alters the delay of the feedback signal FB by changing the division number of the frequency divider 132 of the feedback path 130. For example, increasing the frequency divisor F_{div} by one by setting the timing control signal P_t to +1 causes the corresponding pulse of the feedback signal FB to be delayed by one output cycle, as shown in Figure 8. By subsequently (in the next division cycle) changing the timing control signal P_t to -1, the next feedback signal pulse will occur in its original (unaltered position). The average value of the timing control signal P_t is therefore zero in the embodiment of Figure 6, unlike in the embodiment of Figure 4, where the timing control signal P_t is proportional to the desired average delay. Combiner 138 sums the timing control signal P_t with the frequency divisor F_{div} to generate a modified frequency divisor $F_{div}^{'}$. Frequency divider 132 divides OUT by the modified frequency divisor $F_{div}^{'}$ to generate the feedback signal FB. The pulses of the resulting feedback signal FB are delayed by some desired average delay, defined by the timing control signal P_t, relative to what the

timing of the feedback signal pulses would have been if the frequency divider 132 had used the non-modified frequency divisor F_{div}.

In one exemplary embodiment, filter 144 comprises a two-tap Finite Impulse Response (FIR) filter with a zero DC gain, which may be implemented using a delay element 146 and combiner 148, e.g., a subtraction circuit 148, as shown in Figure 7. The delay element delays the modulated output P_{mod} by one reference cycle to generate a delayed modulated output. Combiner 148 subtracts the delayed modulated output from the modulated output to generate the timing control signal P_t. In so doing, the filter 144 follows the advancement/delay of a pulse with a delay/advancement of the distance to the subsequent pulse, e.g., the next pulse will not change its position due to the previous pulse being altered.

Figure 8 shows an exemplary signaling diagram that encompasses the operation of the general block diagram of Figure 2, as well as the specific embodiment of Figures 6 and 7. In this example, $F_{div} = 4$ for each pulse. As shown in Figure 8, the filtering operation of Figure 7 creates a timing control signal P_t that indicates how much the distance between each subsequent pulse of the feedback signal FB should be increased or decreased. The modified frequency divisor $F_{div}^{'}$ resulting from adding this timing control signal P_t to the frequency divisor F_{div} therefore momentarily deviates from the desired value of 4 according to the desired phase shift, causing a timing difference between the feedback signal FB and the reference signal REF. This time difference causes a phase shift in the output signal OUT. Because the average frequency divisor is still 4, however, the desired output frequency f_{out} is maintained on average. For example, to delay a pulse of the feedback signal by one cycle, the feedback divisor should be increased by one for one reference clock cycle, and then decreased by one for the next reference clock cycle, as shown in the second and third reference clock cycles of Figure 8. Similarly, to advance a pulse of the feedback signal by one clock cycle, the feedback divisor should be decreased by one for one reference clock cycle, and then increased by one for the next reference clock cycle. As can be understood from Figure 8, the solution presented herein may advance/delay the feedback signal pulses by any number of clock cycles, e.g., some number of clock cycles less than F_{div}.

The digital phase control solution presented herein improves the accuracy of the phase control of a PLL 100, at the cost of introducing a new quantization noise source into the corresponding frequency control system. It will be appreciated that the phase control solution disclosed herein may be used with any frequency control systems that also implement some form of quantization noise reduction. For example, Figure 9 shows an exemplary block diagram for a programmable frequency control system 60 that makes the quantization noise for different PLL output signals independent, and therefore, reduces the effective quantization

noise of the frequency control system 60. For simplicity, Figure 9 shows $N = 2$ PLLs 100. It will be appreciated, however, that any number of PLLs 100 may be included in the frequency control system 60. The frequency control system 60 of Figure 9 comprises a modulation circuit 62 and a delay circuit 64, where modulation circuit 62 differs from that used for phase control. The delay circuit 64 enables the generation of decorrelated data streams, and thus the generation of PLL output signals with independent quantization noise, even when only one modulation circuit 62 is used to generate the modulated data stream. In the embodiment of Figure 9, the modulation circuit 62 is configured to generate a (e.g., first) modulated data stream $F_{div}(t)$ based on, e.g., the fractional part of a frequency control word input to the modulation circuit 62, and provide the modulated data stream $F_{div}(t)$ to the delay circuit 64. Delay circuit 64 is configured to provide delayed versions of the modulated data stream to the corresponding PLLs 100, e.g., by time shifting the modulated data stream to generate the time-shifted data streams applied to at least some of the PLLs 100. For example, delay circuit 64 may generate and apply a first data stream $F_{div1}(t) = F_{div}(t - \Delta t_1)$ to PLL_1 100 by essentially applying a time shift of Δt_1 to the modulated data stream $F_{div}(t)$ output by the modulation circuit 62. In some embodiments, $\Delta t_1 = 0$, while in other embodiments, $\Delta t_1 > 0$. Delay circuit 64 may further shift the first modulated data stream to generate a second data stream $F_{div2}(t) = F_{div}(t - \Delta t_2)$, where $\Delta t_2 > \Delta t_1$, and apply the second data stream to PLL_2 100. As a result, the fractional portions of the frequency control word used to control the PLLs 100 are decorrelated, which reduces the effective quantization noise of the multi-antenna transmitter and/or receiver. In exemplary embodiments, the modulation circuit 62 comprises a delta-sigma modulator, and the delay circuit 64 comprises a shift register.

The solution presented herein discloses delaying a fraction of the pulses, e.g., one or more pulses, of a PLL feedback signal to generate a desired phase shift at the output of the PLL 100. It will be appreciated that in some embodiments, such delay operations are implemented in a random fashion so as to avoid creating spurious tones in the PLL output signal. Further, by using a delta-sigma modulator as part of the phase control circuit 140, as disclosed herein, any high frequency spurious tones may be attenuated by the low-pass characteristic transfer function of the PLL.

The digital phase control solution presented herein improves the accuracy and resolution of PLL phase control over conventional analog techniques. Further, such a digital implementation requires a smaller chip area, and eases porting of the design to different semiconductor processes.

Various elements disclosed herein are described as some kind of circuit, e.g., a phase control circuit, a modulation circuit, a frequency control circuit, delay circuit, etc. Each of these circuits may be embodied in hardware and/or in software (including firmware, resident software,

microcode, etc.) executed on a controller or processor, including an application specific integrated circuit (ASIC). Further, the solution presented herein may be implemented as part of a computer program product comprising software instructions, which when run on a processing circuit, causes the processing circuit to control the PLL as disclosed herein.

The present invention may, of course, be carried out in other ways than those specifically set forth herein without departing from essential characteristics of the invention. The present embodiments are to be considered in all respects as illustrative and not restrictive, and all changes coming within the meaning and equivalency range of the appended claims are intended to be embraced therein.

CLAIMS

What is claimed is:

1. A phase-locked loop (PLL) (100) comprising:

an oscillator (110) configured to generate a PLL output signal at an output of the PLL (100) responsive to a reference signal input to the PLL (100);

a detector (120) configured to compare the reference signal to a feedback signal to control a frequency of the PLL output signal, the feedback signal being derived by a feedback path (130) of the PLL (100) from the PLL output signal; and

a phase control circuit (140) operatively connected to the feedback path (130) of the PLL (100), said phase control circuit (140) configured to generate a timing control signal responsive to a phase control signal, wherein application of the timing control signal to the feedback path (130) shifts a timing of one or more pulses of the feedback signal to achieve a desired average time shift to generate a desired phase shift at the output of the PLL (100) while maintaining a desired average divisor of the feedback signal.

2. The PLL (100) of claim 1 wherein the feedback path (130) of the PLL (100) comprises:

a frequency divider (132) configured to divide the frequency of the PLL output signal by a frequency divisor;

a multiplexer (134) controlled by the timing control signal, the multiplexer (134) comprising a multiplexer output operatively connected to the detector (120) and a plurality of multiplexer input connections; and

a delay line (136) comprising a plurality of serially connected delay elements (136) operatively connected between the frequency divider (132) and the multiplexer (134), said plurality of multiplexer input connections comprising an output of the frequency divider (132) and an output of at least some of the plurality of delay elements (136);

wherein the multiplexer (134) is configured to periodically select, responsive to the timing control signal, the signal at one of the plurality of multiplexer inputs as the feedback signal.

3. The PLL (100) of claim 2 wherein the phase control circuit (140) comprises a modulation circuit (142) configured to generate the timing control signal responsive to the phase control signal.

4. The PLL (100) of claim 1:

wherein the phase control circuit (140) comprises:

a modulation circuit (142) configured to generate a modulated output responsive to the phase control signal; and

a filter (144) operatively connected to an output of the modulator (142) and configured to filter the modulated output to generate the timing control signal; and

wherein the feedback path (130) of the PLL (100) comprises:

a combiner (138) configured to combine the timing control signal with an input frequency divisor to generate a modified frequency divisor; and

a frequency divider (132) configured to divide the frequency of the PLL output signal by the modified frequency divisor such that one or more pulses of the resulting feedback signal are time shifted while the desired average divisor of the feedback signal is maintained.

5. The PLL (100) of claim 4 wherein the filter (144) comprises:

a delay element (146) configured to delay the modulated output to generate a delayed modulated output; and

a second combiner (148) configured to subtract the delayed modulated output from the modulated output to generate the timing control signal.

6. A beamforming system (10) comprising:

an antenna array (20) comprising a plurality of antenna elements (22);

a plurality of radio frequency (RF) front-end circuits (30), each RF front-end circuit (30) coupled to one of the antenna elements (22), wherein each of the RF front-end circuits (30) comprises a PLL (100) according to any of claims 1-5; and

a frequency control circuit (50) configured to control a frequency of each of the plurality of PLLs (100) relative to the reference signal.

7. The beamforming system (10) of claim 6 wherein each of the plurality of PLLs (100) comprises a frequency programmable PLL (100), and wherein the frequency control circuit (50) comprises:

a modulator (62) configured to generate a first modulated data stream based on a first frequency control word input to the modulator (62), the first frequency control word configured to control a first frequency output by at least some of the plurality of frequency programmable PLLs (100); and

a delay circuit (64) operatively coupled to an output of the modulator (62) and configured to:

generate a first data stream based on the first modulated data stream;

shift the first modulated data stream by a first time shift to generate a second data stream;

apply the first data stream to a first PLL (100) of the plurality of PLLs (100) to produce, at an output of the first PLL (100), a first output signal at the first frequency and having a first quantization noise component; and

apply the second data stream to a second PLL (100) of the plurality of PLLs (100) to produce, at an output of the second PLL (100), a second output signal at the first frequency and having a second quantization noise component decorrelated from the first quantization noise component.

8. A method of controlling a phase at an output of a phase-locked loop (PLL) (100) to achieve a desired phase shift at the output of the PLL (100), the method comprising:

generating a PLL output signal at the output of the PLL (100) responsive to a reference signal input to the PLL (100);

comparing the reference signal to a feedback signal in a detector to control a frequency of the PLL output signal, the feedback signal being derived by a feedback path (130) of the PLL (100) from the PLL output signal;

generating a timing control signal responsive to a phase control signal; and

shifting a timing, responsive to the timing control signal, of one or more pulses of the feedback signal to achieve a desired average time shift to generate a desired phase shift at the output of the PLL (100) while maintaining a desired average divisor of the feedback signal.

9. The method of claim 8 further comprising:

dividing, in a frequency divider (132), the frequency of the PLL output signal by a frequency divisor; and

generating a plurality of multiplexer signal inputs by delaying an output of the frequency divider (132) using a plurality of serially connected delay elements (136), said plurality of multiplexer signal inputs comprising the output of the frequency divider and an output of at least some of the plurality of delay elements (136);

wherein shifting the timing of the one or more pulses of the feedback signal comprises periodically selecting, responsive to the timing control signal, one of the plurality of multiplexer signal inputs as the feedback signal.

10. The method of claim 8:

wherein generating the timing control signal comprises:

generating a modulated output responsive to the phase control signal; and

filtering the modulated output to generate the timing control signal;

wherein shifting the timing of the one or more pulses of the feedback signal comprises:

combining the filtered modulated output with an input frequency divisor to generate a modified frequency divisor; and

dividing the frequency of the PLL output signal by the modified frequency divisor such that the one or more pulses of the feedback signal are time shifted while the desired average divisor of the feedback signal is maintained.

11. The method of claim 10 wherein filtering the modulated output comprises:

delaying the modulated output by one reference signal period to generate a delayed modulated output; and

subtracting the delayed modulated output from the modulated output to generate the filtered modulated output.

12. A computer program product stored in a non-transitory computer readable medium for controlling a phase at an output of a phase-locked loop (PLL) (100) to achieve a desired phase shift at the output of the PLL (100), the computer program product comprising software instructions which, when run on a processing circuit, causes the processing circuit to:

generate a PLL output signal at the output of the PLL (100) responsive to a reference signal input to the PLL (100);

compare the reference signal to a feedback signal in a detector to control a frequency of the PLL output signal, the feedback signal being derived by a feedback path of the PLL (100) from the PLL output signal;

generate a timing control signal responsive to a phase control signal; and

shifting a timing, responsive to the timing control signal, of one or more pulses of the feedback signal to achieve a desired average time shift to generate a desired phase shift at the output of the PLL (100) while maintaining a desired average divisor of the feedback signal.

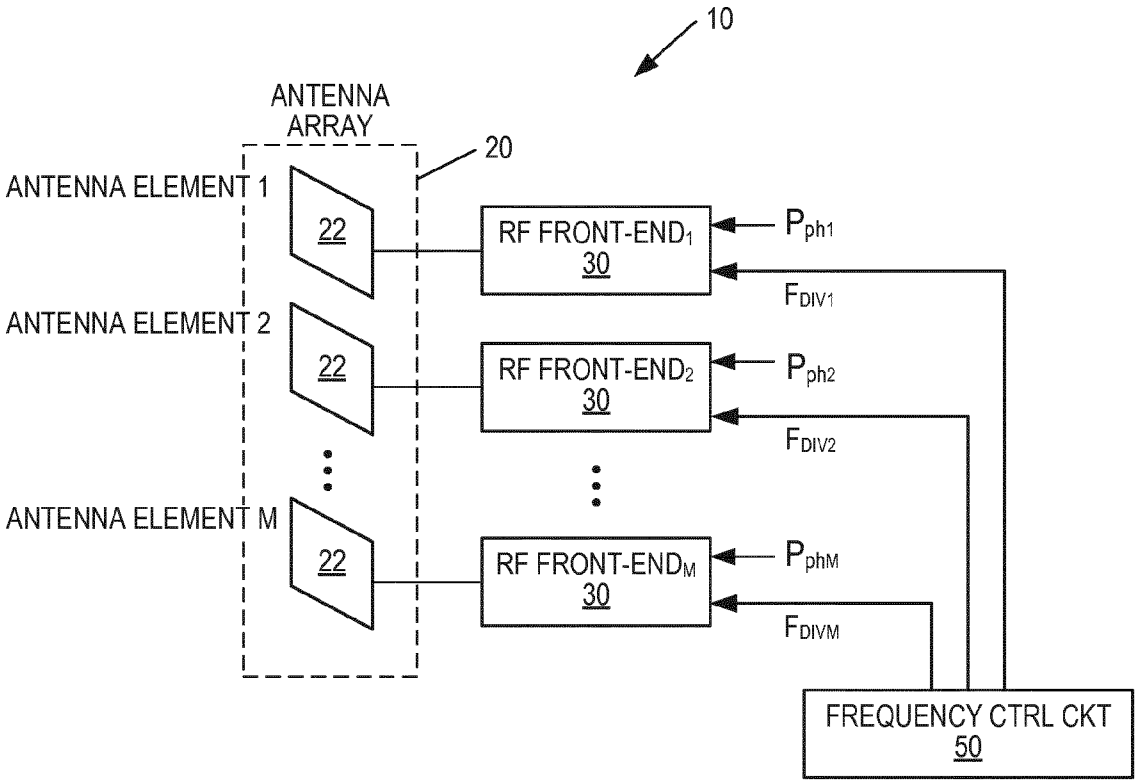
10
ANTENNA ARRAY
20
ANTENNA ELEMENT 1
22
RF FRONT-END1 30
Pph1
FDIV1
ANTENNA ELEMENT 2
22
RF FRONT-END2 30
Pph2
FDIV2
ANTENNA ELEMENT M
22
RF FRONT-ENDM 30
PphM
FDIVM
FREQUENCY CTRL CKT 50

FIG. 1A

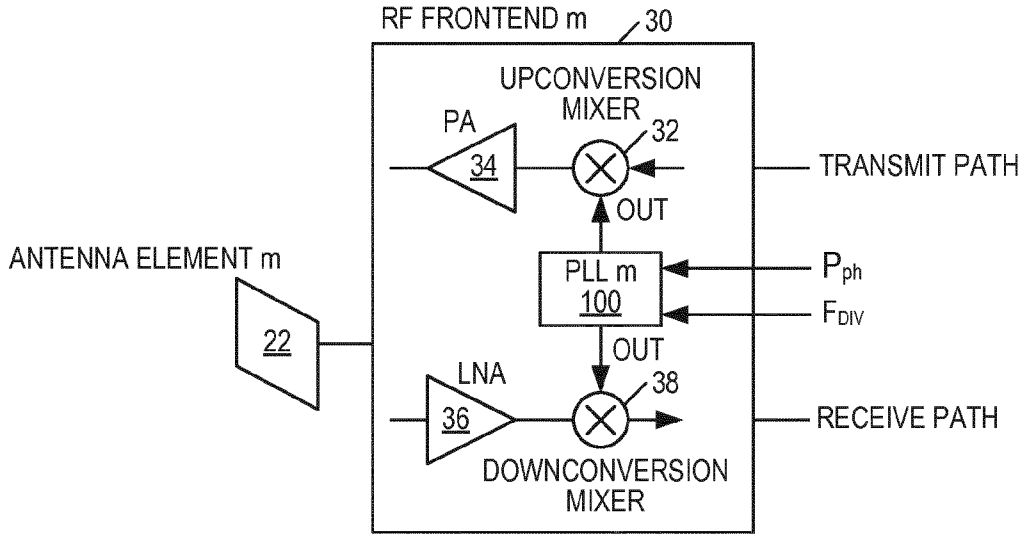
RF FRONTEND m
30
UPCONVERSION MIXER
PA
34
32
TRANSMIT PATH
OUT
ANTENNA ELEMENT m
22
PLL m 100
Pph
FDIV
OUT
LNA
36
38
RECEIVE PATH
DOWNCONVERSION MIXER

FIG. 1B

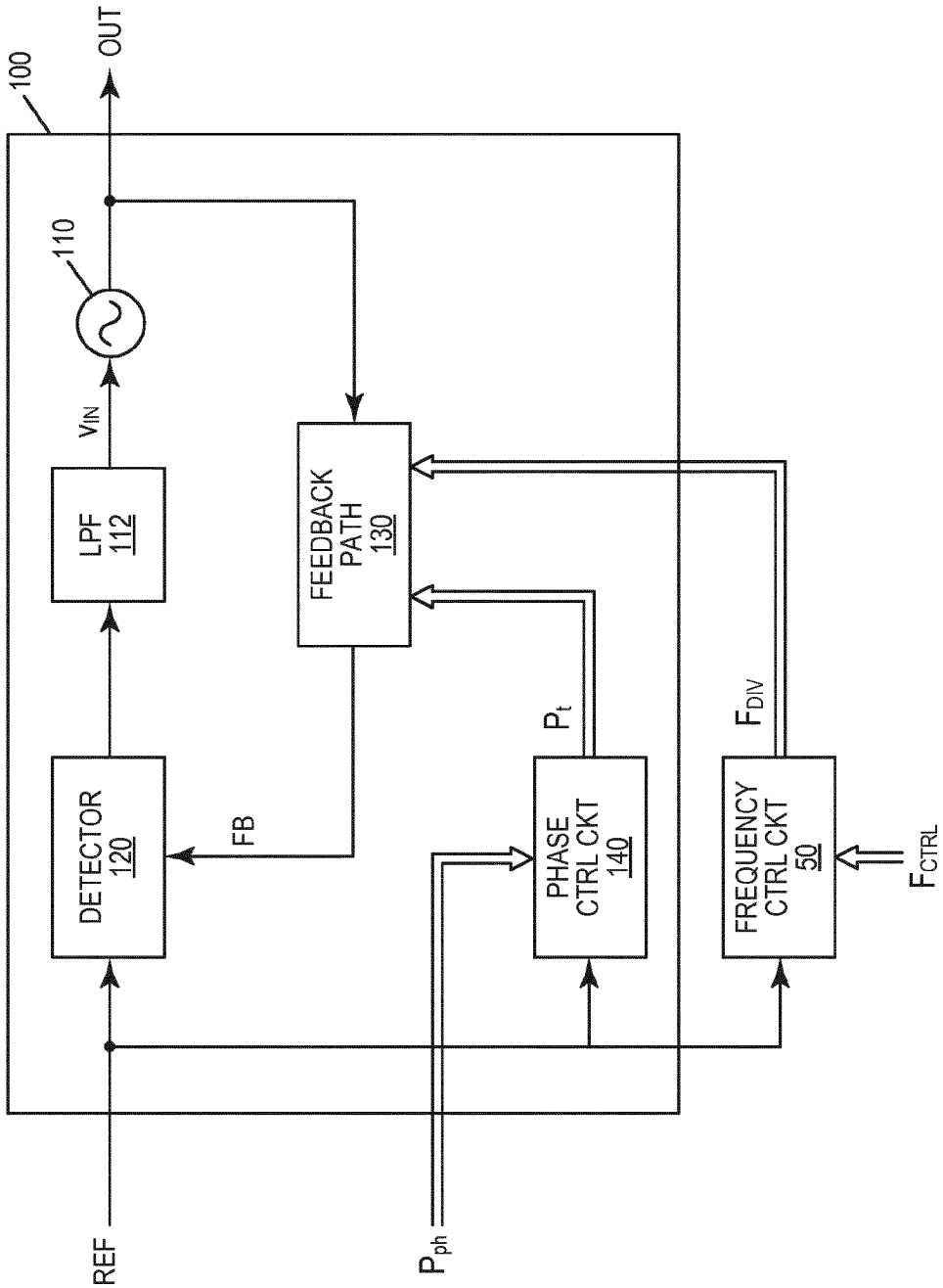
100
OUT
110
VIN
LPF
112
FEEDBACK
PATH
130
DETECTOR
120
FB
Pt
PHASE
CTRL CKT
140
FDIV
FREQUENCY
CTRL CKT
50
FCTRL
REF
Pph

FIG. 2

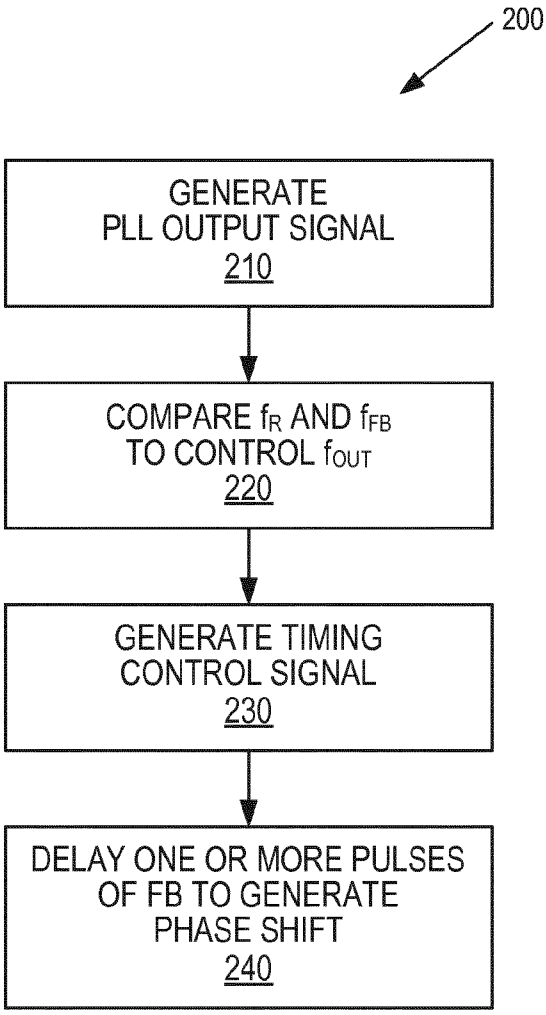
200
GENERATE PLL OUTPUT SIGNAL 210
COMPARE f_R AND f_{FB} TO CONTROL f_{OUT} 220
GENERATE TIMING CONTROL SIGNAL 230
DELAY ONE OR MORE PULSES OF FB TO GENERATE PHASE SHIFT 240

FIG. 3

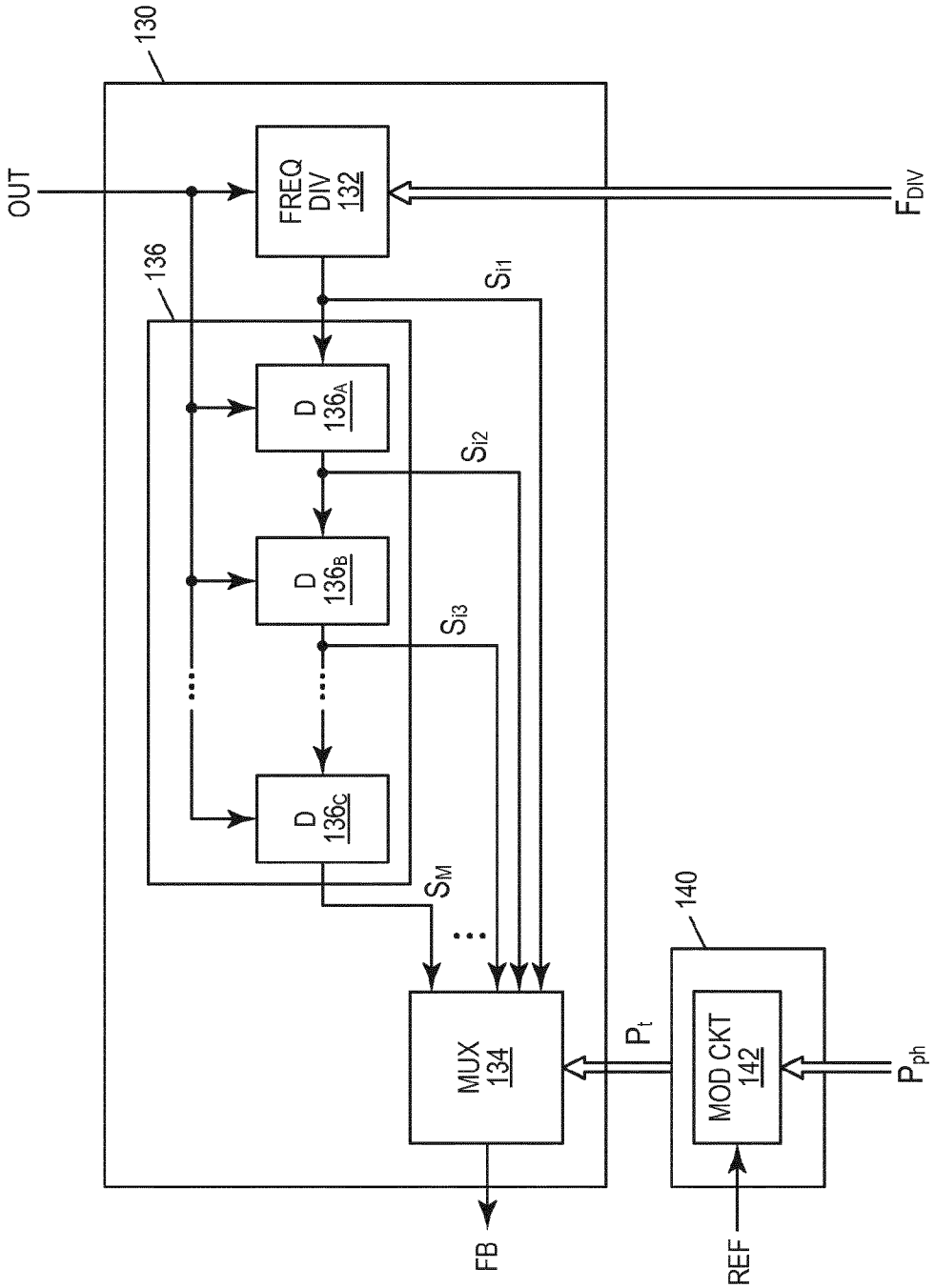
130
OUT
FREQ DIV 132
F_{DIV}
136
S_{i1}
D 136A
S_{i2}
D 136B
S_{i3}
D 136C
S_M
140
MUX 134
P_t
MOD CKT 142
P_{ph}
FB
REF

FIG. 4

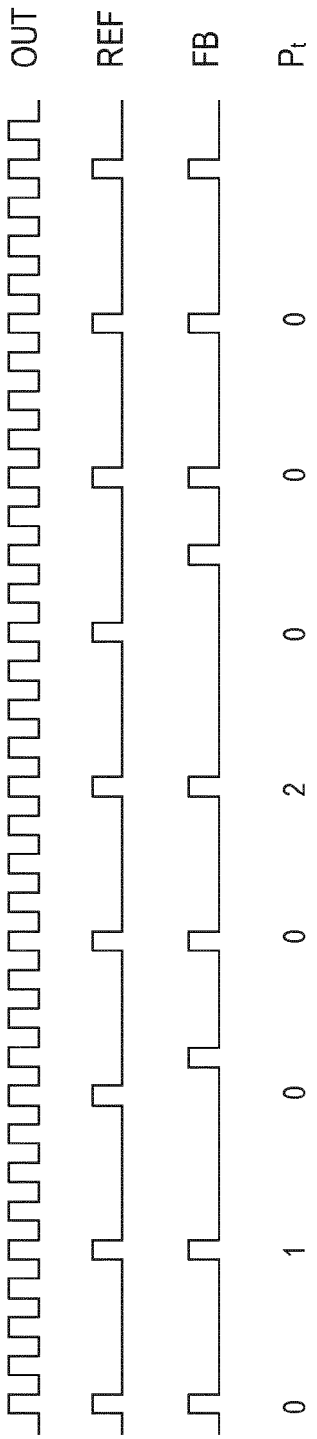

FIG. 5

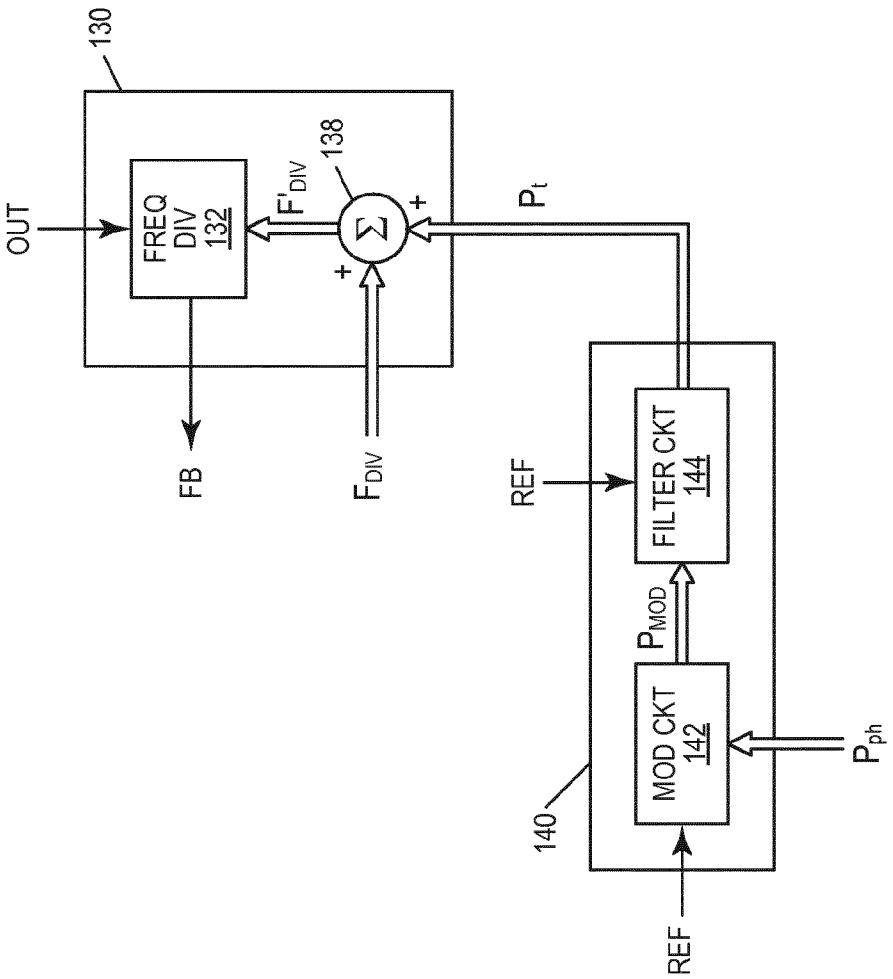
130
OUT
FREQ DIV 132
F'DIV
138
Σ
+
+
+
Pt
FB
FDIV
REF
FILTER CKT 144
PMOD
MOD CKT 142
Pph
140
REF

FIG. 6

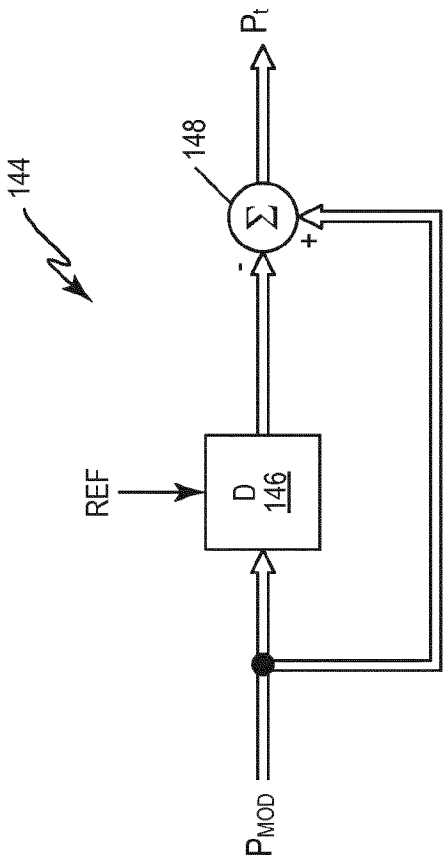

FIG. 7

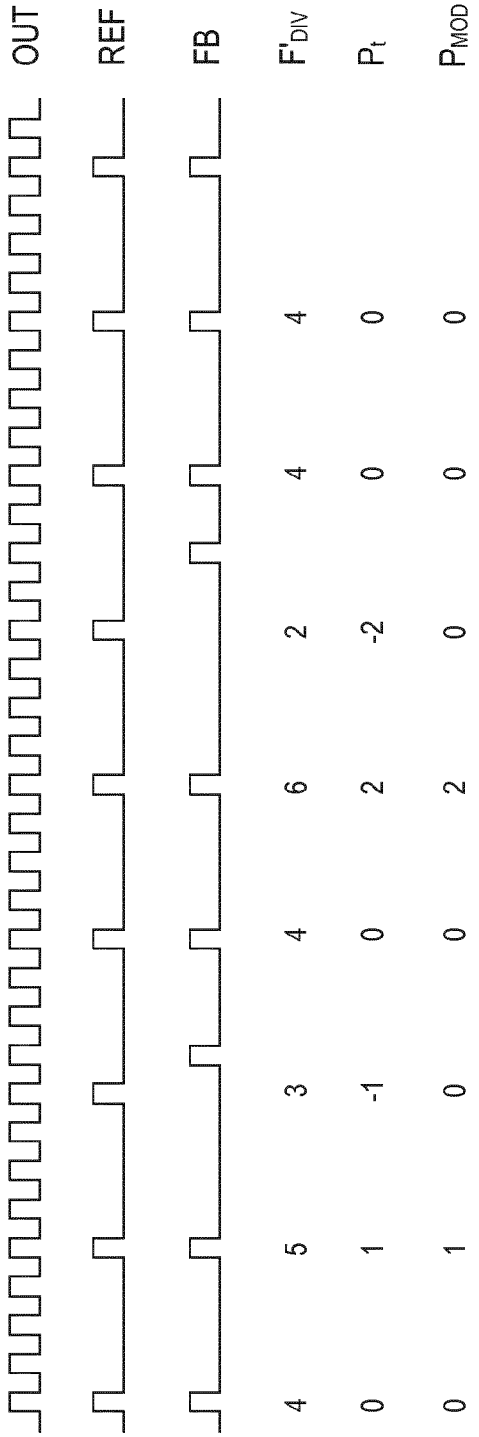

FIG. 8

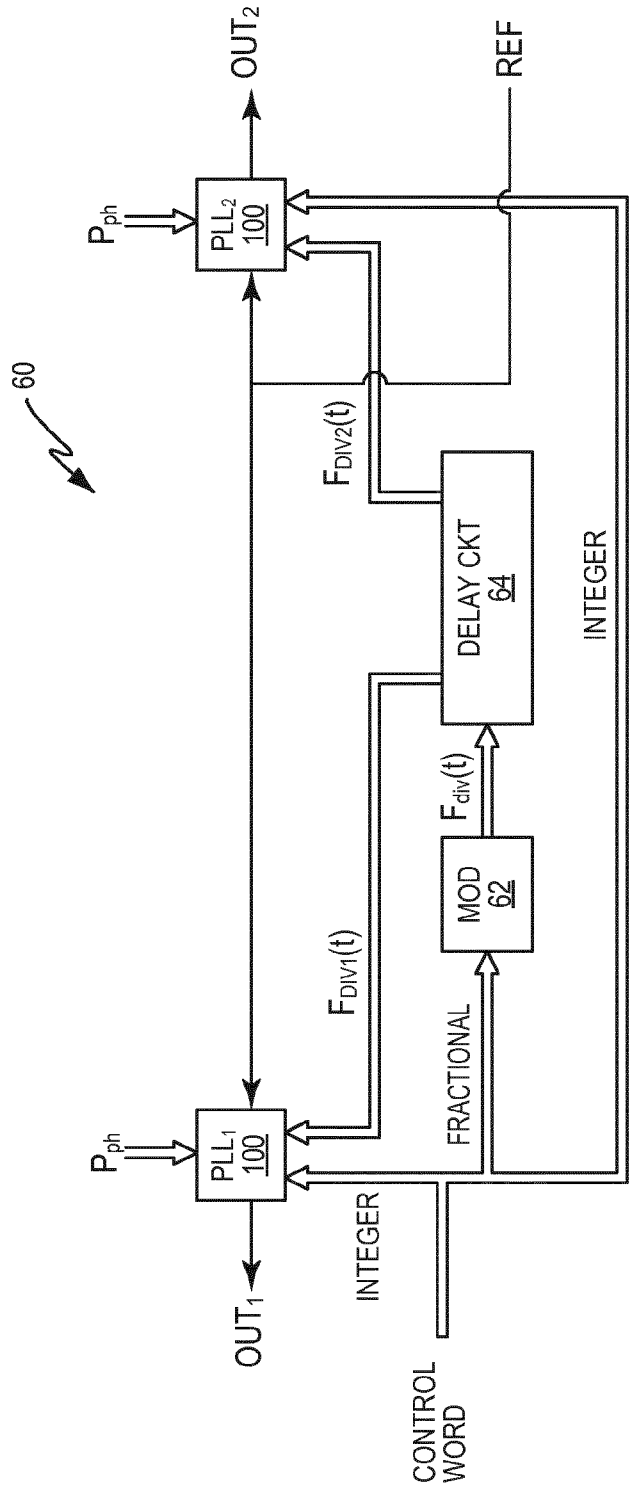
60
P_{ph}
PLL_2 100
OUT_2
REF
$F_{DIV2}(t)$
DELAY CKT 64
INTEGER
$F_{div}(t)$
MOD 62
$F_{DIV1}(t)$
FRACTIONAL
P_{ph}
PLL_1 100
OUT_1
INTEGER
CONTROL WORD

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2015/059071

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2015/059071

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03L7/081 H03L7/183 H04B7/06
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03L H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 7 463 710 B2 (WALSH PATRICK [IE] ET AL) 9 December 2008 (2008-12-09) column 6, line 8 - column 8, line 14; figures 2-5 -----	1,4,8, 10,12 6
X Y	US 6 642 758 B1 (WANG BONNIE I [US] ET AL) 4 November 2003 (2003-11-04) column 12, line 17 - column 13, line 41; figures 16A,16B,17 column 16, line 5 - line 26; figure 24 column 17, line 14 - line 34; figure 26 -----	1,8,12 6
A	US 2011/043289 A1 (WAN KWUN CHIU [HK] ET AL) 24 February 2011 (2011-02-24) paragraph [0037] - paragraph [0061]; figures 2,5,8 -----	1-5,8-12

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 May 2016	11/05/2016

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Aouichi, Mohamed

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	FR 2 647 986 A1 (BROADCAST TELEVISION SYST [DE]) 7 December 1990 (1990-12-07) the whole document	1-5,8-12
Y	EP 1 085 678 A2 (TOSHIBA KK [JP]) 21 March 2001 (2001-03-21)	6
A	paragraph [0034] - paragraph [0062]; figures 3-5	7
Y	EP 1 274 181 A1 (ALPS ELECTRIC CO LTD [JP]) 8 January 2003 (2003-01-08)	6
A	paragraph [0013] - paragraph [0021]; figures 1,2	7

2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2015/059071

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 7463710 B2	09-12-2008	US 2004264622 A1	30-12-2004
		WO 2005002055 A2	06-01-2005
US 6642758 B1	04-11-2003	US 6642758 B1	04-11-2003
		US 7358783 B1	15-04-2008
US 2011043289 A1	24-02-2011	NONE	
FR 2647986 A1	07-12-1990	DE 3918161 A1	06-12-1990
		FR 2647986 A1	07-12-1990
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		US 2006079290 A1	13-04-2006
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		DE 60201474 T2	17-11-2005
		EP 1274181 A1	08-01-2003
		JP 2003018057 A	17-01-2003
		US 2003008630 A1	09-01-2003

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-5, 8-12

   Details of the feedback path circuitry of the PLL

   ---

2. claims: 1, 6, 7

   Details of a beamforming system
