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(54) Title: DIGITAL PHASE DISCRIMINATION BASED ON FREQUENCY SAMPLING
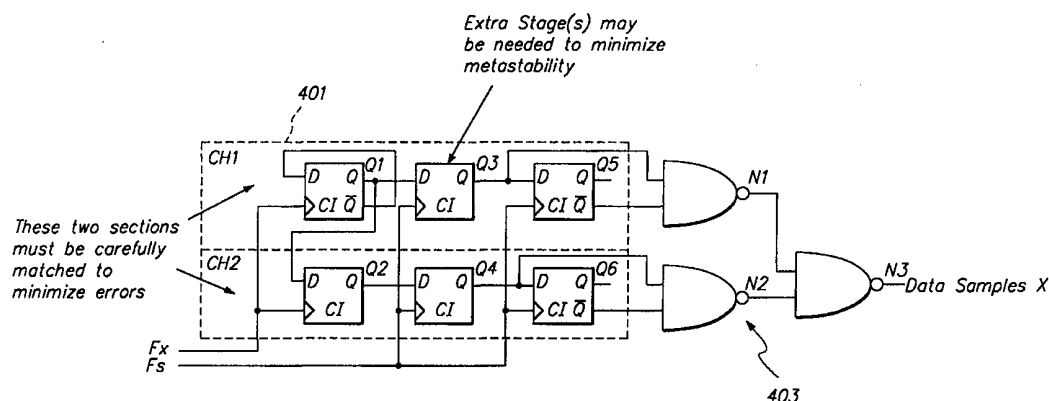
(57) Abstract

    The present invention provides a simple all digital method and apparatus (fig. 4) for determining the phase of a first clock signal (Fs) relative to a second clock signal (Fs). The first clock signal (Fs) may be a digital approximation of a periodic analog signal such as an RF signal. A sampling technique is employed that produces a stream of digital bits (X) containing relative phase information. From the stream of digital data bits is formed a digital word indicative of the relative phase (fig. 11A). The digital word may be formed using a digital filter (fig. 13). Advantageously, an extensive body of digital filtering techniques applicable to Sigma–Delta (sometimes referred to as Delta–Sigma) A/D converters (fig. 1) may be applied directly to he digital stream (X). By using an appropriately chosen weighting function, high accuracy may be obtained.

DIGITAL PHASE DISCRIMINATION BASED
ON FREQUENCY SAMPLING

BACKGROUND OF THE INVENTION

5   **Field of the Invention**

The present invention relates to digital phase discrimination.

State of the Art

Phase discrimination is important in digital radio communications, in particular

10   in any angle modulation digital radio receiver. Phase discrimination and frequency

discrimination are closely related. Frequency discrimination is typically performed

using analog circuitry, e.g. an IQ frequency discriminator. Analog frequency

discriminators have substantial drawbacks. In the case of an IQ frequency

discriminator, the discriminator requires a number of analog components, two A/D

15   conversions and a numerical arctangent operation, rendering the circuit quite complex.

Known methods exist for producing a value representing the instantaneous phase

of a signal using only digital logic elements. Various such methods are described in

U.S. Patent 5,084,669, incorporated herein by reference. In particular, the foregoing

patent describes a digital circuit for determining the instantaneous phase of a signal,

20   from which the instantaneous frequency may be obtained if desired. Although the

implementation of the circuit is all digital, it is quite involved. An improved method

and apparatus for determining in a simple, all-digital manner the instantaneous phase of

a signal would therefore likely be well-received by those skilled in the art.

25   SUMMARY OF THE INVENTION

The present invention, generally speaking, provides a simple, all-digital method

and apparatus for determining the phase of a first clock signal relative to a second clock

signal. The first clock signal may be a digital approximation of a periodic analog signal

such as an RF signal. A sampling technique is employed that produces a stream of

30   digital bits containing relative phase information. From the stream of digital bits is

formed a digital word indicative of the relative phase. The digital word may be formed

using a digital filter. Advantageously, an extensive body of digital filtering techniques applicable to Sigma-Delta (sometimes referred to as Delta-Sigma) A/D converters may be applied directly to the digital stream. By using an appropriately-chosen weighting function, high accuracy may be obtained.

5   In accordance with another aspect of the invention, a method of determining a ratio of frequencies of a first clock signal and a second clock signal is provided. The first clock signal is sampled in accordance with the second clock signal to produce a stream of digital bits or symbols, and from the stream of digital bits or symbols a digital word is formed indicative of the ratio of frequencies. The digital word may be

10   formed by filtering the stream of digital bits or symbols. Apparatus for practicing the foregoing method may include circuitry for sampling the first clock signal in accordance with the second clock signal to produce a stream of digital bits or symbols and circuitry, such as a digital filter, for forming from the stream of digital bits or symbols a digital word indicative of the ratio of frequencies. Preferably, the digital

15   filter employs a weighting function in which different weights are applied to different digital bits or symbols.

        In accordance with a related aspect of the invention, a method is provided of producing a data stream indicative of a ratio of frequencies of two clock signals performed by sampling one of the clock signals in accordance with the other clock

20   signal to form a stream of digital bits or symbols, each digital bit or symbol representing a number of transitions of a predetermined polarity of the one clock signal that occurred during a particular period of the other clock signal, such that the stream of digital bits or symbols may be further processed to determined the ratio of frequencies. A circuit for producing such a data stream indicative of a ratio of

25   frequencies of two clock signals may include a first input terminal to which a first clock signal is applied, a second input terminal to which a second clock signal is applied, the circuit producing as an output signal a stream of digital bits or symbols, each digital bit or symbol representing a number of transitions of a predetermined polarity of the one clock signal that occurred during a particular period of the other clock signal, such that

the stream of digital bits or symbols may be further processed to determined the ratio of frequencies.

In accordance with still a further aspect of the invention, an apparatus is provided for generating a Delta/Sigma modulation of the ratio of two frequencies Fx

5   and Fs, including a counter circuit for counting the number of clock edges of Fs occurring in the time period between clock edges of Fx and a register circuit for storing the value of the counter at each clock edge of Fs. The sequence of values from the register means constitutes the Delta/Sigma modulation quantized data.

10   BRIEF DESCRIPTION OF THE DRAWING

The present invention may be further understood from the following description in conjunction with the appended drawing. In the drawing:

Figure 1 is a block diagram illustrating a sampled-data model of a Sigma-Delta modulator and of a sampling circuit applied to frequency sampling in accordance with

15   one embodiment of the present invention;

Figure 2 is a table helpful in explaining operation of the circuit model of Figure 1 in the instance of an input frequency that is 0.6875 times a reference frequency;

Figure 3 is a timing diagram illustrating the principle of operation of the circuit model of Figure 1 as applied to frequency sampling;

20   Figure 4 is a schematic diagram of one example of a frequency sampling circuit described by the circuit model of Figure 1;

Figure 5 is a first timing diagram illustrating operation of the frequency sampling circuit of Figure 4;

Figure 6 is a second timing diagram illustrating operation of the frequency

25   sampling circuit of Figure 4;

Figure 7 is a graph of two alternative weighting functions that may be used to perform digital filtering of a digital bit stream produced by a circuit such as that of Figure 4;

Figure 8 is a graph illustrating the accuracy obtained from a digital frequency

30   discriminator using a constant weighting function;

Figure 9 is a graph illustrating the accuracy obtained from a digital frequency discriminator using a triangular weighting function; and

Figure 10 is a block diagram of one example of a digital filter that may be used in conjunction with a frequency sampling circuit such as that of Figure 4.

5   Figure 11A is a tabulation illustrating one method of digital phase discrimination;

Figure 11B is a plot showing results of the method of Figure 11A;

Figure 11C is a plot of a weighting function used in connection with Figures 11A and 11B;

10   Figure 12A is a tabulation illustrating another method of digital phase discrimination;

Figure 12B is a plot showing results of the method of Figure 12A;

Figure 12C is a plot of a weighting function used in connection with Figures 12A and 12B;

15   Figure 13 is a block diagram of digital phase discrimination hardware in accordance with the technique of Figure 12;

Figure 14A is a tabulation illustrating yet another method of digital phase discrimination;

Figure 14B is a plot showing results of the method of Figure 14A;

20   Figure 14C is a plot of a weighting function used in connection with Figures 14A and 14B;

Figure 15 is a block diagram of digital phase discrimination hardware in accordance with the technique of Figure 14;

Figure 16A is a tabulation illustrating still another method of digital phase

25   discrimination;

Figure 16B is a plot showing results of the method of Figure 16A;

Figure 16C is a plot of a weighting function used in connection with Figures 16A and 16B;

Figure 17 is a block diagram of digital phase discrimination hardware in

30   accordance with the technique of Figure 16.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The approach followed by the digital frequency discriminator of the present invention may be appreciated by analogy to Sigma-Delta A/D conversion, well-documented in the prior art by such references as "Oversampling Delta-Sigma

5   Data Converters", Candy, et al., *IEEE Press*, pages 1-6, Piscataway, NJ (1992). A Sigma-Delta converter modulates a varying-amplitude analog input signal into a simple digital code at a frequency much higher than the Nyquist rate. The design of the modulator allows resolution in time to be traded for resolution in amplitude. A sampled-data circuit model of a Sigma-Delta modulator, shown in Figure 1, may be

10   directly applied to frequency sampling as described herein.

Referring to Figure 1, an input signal x_i occurring at sample time i has subtracted from it the output signal y_i at sample time i. The result is applied to an accumulator having an output signal w_i. A "new" input signal of the accumulator at sample time i is combined with the "old" output signal of the accumulator to form a

15   new output signal of the accumulator. The output signal of the accumulator is quantized, the quantization being represented as the addition of an error e_i. The output signal of the quantizer is the final output signal y_i.

Assume now that x_i is the ratio of two frequencies and that the quantizer is a two-level quantizer. Further assume that the ratio of the two frequencies for the time

20   period in question is, say, 0.6875. As shown in Figure 2, the latter value is accumulated a first time, giving an accumulated value of 0.6875. This valuing being less than 1, the value 0.6875 is again added to the accumulated value, giving a new accumulated value of 1.375. Since this value is now greater than 1, 1 is subtracted from 0.6875 and the result (0.6875 - 1 = -0.3125) added to the accumulator to give a

25   value of 1.0625. Operation proceeds in this fashion. During the foregoing sequence of operations, a data stream is produced by taking the integer portion, 1 or 0, of each accumulated value.

Referring to Figure 3, the interpretation of the sequence of numbers shown in Figure 2 may be appreciated. Two clock signals are shown. Again, it is assumed that

30   the ratio of the frequency of the upper clock signal to that of the lower clock signal

during the period of interest is 0.6875. At time t = 0, rising edges of both clock

signals coincide. At the first subsequent rising edge of the lower clock signal, 0.6875

periods of the upper clock signal have elapsed. At the next rising edge of the lower

clock signal, 1.375 periods of the upper clock signal have elapsed. At the next rising

5 edge of the lower clock signal, 1.0625 periods of the upper clock signal have elapsed

since the elapse of the first period of the upper clock signal, and so on.

A schematic diagram of a capture circuit, or frequency sampling circuit, that

may be used to data samples corresponding to the data stream described in the

foregoing example is shown in Figure 4. In the illustrated embodiment, it is assumed

10 that the ratio of the clock signals is such that no more than one rising edge of the faster

clock will occur during a single period of the slower clock. In other embodiments, this

assumption need not apply.

The capture circuit includes a input portion 401 and an output portion 403. The

input portion includes two sections Ch1 and Ch2 that must be carefully matched to

15 minimize errors. Each section comprises a chain of two or more D flip-flops coupled

in series. In the following description, the same reference numerals will be used to

reference the respective flip-flops themselves and their respective output signals.

Within each section, the first flip-flop in the chain is clocked by a sampled clock

signal Fx. The succeeding flip-flops in the chain are clocked by a sampling clock

20 signal Fs. The D input of the first flip-flop Q1 in the upper section is coupled to

the $\overline{Q}$ output of the same. The D input of the first flip-flop in the lower section is

coupled to the Q output of the first flip-flop in the upper section. The remaining

flip-flops in both sections are coupled in series--i.e., Q to D, Q to D.

The function of the input portion is to 1) produce two signals, logical inverses

25 of one another, that transition on rising edges of the clock signal Fx; 2) to latch the

values of the two signals on the rising edge of the clock signal Fs; and 3) to detect

transitions from one clock to the next. Additional intermediate stages in series with Q3

and Q4 may be required to minimize metastability resulting from the asynchrony of the

two clock signals, and in fact multiple such stages may be desirable in a particular design.

The output portions include, in an exemplary embodiment, three two-input NAND gates. Respective NAND gates N1 and N2 are coupled to the D and $\overline{Q}$ signal

5   of the final flip-flop stages of the input sections. Output signals of the NAND gates N1 and N2 are combined in the further NAND gate N3 to form the final output of the capture circuit.

The function of the output portion is to detect a change in the input clock signal level from one sample clock to the next in either of two channels formed by the two

10   input sections. The two input sections function in a ping-pong fashion, alternately detecting changes in the input clock signal level.

Operation of the capture circuit of Figure 4 may be more fully appreciated with reference to the timing diagram of Figure 5. The first stages of the two channels form inverse signals Q1 and Q2 approximately coincident with (but slightly delayed from)

15   rising edges of the input clock signal. The signals Q3 and Q4 are formed by sampling the signals Q1 and Q2, respectively, in accordance with the sample clock. The signals Q5 and Q6, respectively, are delayed replicas of the signals Q3 and Q4. The NAND gates together realize the logic function $X = Q3 \cdot \overline{Q5} \ v \ Q4 \cdot \overline{Q6}$.

In the example of Figure 5, the illustrated signals are all idealized square-wave

20   signals. In actuality, the signals will have finite rise and fall times. The possible effect of the finite rise and fall times of the signals Q1 and Q2 and the asynchrony of the circuit is metastability, as illustrated in Figure 6. Here, the signals Q3 and Q5 and the signals Q4 and Q6 are each in an indeterminate state for one cycle. The resulting output of the circuit may or may not be correct. However, because the decision was a

25   "close call" to begin with, the effect of an occasional erroneous decision on the overall operation of the circuit is negligible. The time window of instability is reduced by increasing the overall gain in the path. If the gain in Q3 and Q9 is sufficient to reduce the probability of an error to an acceptable level, then no additional circuitry is required. If not, then additional circuitry will be required to increase the gain.

In order to recover the ratio of the frequencies of the two clock signals from the data stream produced by a capture circuit such as the one of Figure 4, digital filtering is applied. Advantageously, an extensive body of digital filtering techniques applicable to Sigma-Delta (or Delta-Sigma) A/D converters may be applied directly to the digital

5   stream. Furthermore, by using an appropriately-chosen weighting function, high accuracy may be obtained.

The weighted sum of products is an example of an FIR filter. The weighting function described heretofore is therefore that of an FIR filter in digital filtering theory. It should be recognized, however, that IIR filters can also be used. In the process of

10   FIR digital filtering, the weighting function is applied to a "window" of data samples to obtain an estimate of the ratio of frequencies in the center of the window. The window is then "picked up and moved" to the next sequence of samples. Windowing will typically overlap. A window may include 256 samples, for example.

Referring to Figure 7, two alternative weighting functions are shown for a

15   window of 256 samples. The weighting functions are normalized, meaning that the area under the weighting function is unity. One weighting function, indicated in dashed lines, is a straight-line, constant weighting function. Another weighting function, indicated in solid line, is a triangular weighting function. The weighting function is the impulse response function in digital filters.

20   Results of digital filtering using the straight-line weighting function and the triangular weighting function respectively, are shown in Figure 8 and Figure 9. In the case of both Figure 8 and Figure 9, the frequency ratio was increased from just under 0.687 to just over 0.693. As seen in Figure 8, using a straight-line weighting function, the quantized signal oscillates between two levels that are adjacent to the input in such a

25   manner that its local average equals the average input. The average error was calculated to be 1772ppm. As seen in Figure 9, using a triangular weighting function, the quantized signal tracks the input with an average error of 83ppm.

A schematic diagram of an exemplary frequency accumulator that applies a triangular weighting function and that may be used to accomplish the desired digital

30   filtering is shown in Figure 10. In the example shown, the frequency accumulator uses

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a 7-bit counter 101, a 14-bit adder 103 and a 14-bit register 105. The 7-bit counter is
clocked by the sample frequency Fs. The output of the 7-bit counter is provided to one
input of the adder. The function of the 7-bit counter is to count up from 0 to 127 and
then down from 127 to 0. The count of 127 occurs twice in succession. This behavior

5   is achieved using a flip-flop 107. The flip-flop is clocked by the sample frequency Fs.
A Terminal Count signal of the 7-bit adder is input to the flip-flop. The output of the
flip-flop is coupled to a Count Down input of the 7-bit counter.

The "oversampled" data stream is coupled to a control input of the adder.
When the current bit of the data stream is a 1, an addition is performed. When the

10   current bit is a 0, no addition is performed. A Carry In input of the adder is tied high,
effectively causing the range of weights to be 1 to 128.

The 14-bit register is clocked by the sample frequency Fs. Its output is applied
to the other input of the adder. Its input receives the output word produced by the
adder. The function of the 14-bit adder is to perform an accumulation operation for

15   256 clocks. At the conclusion of the 256 clocks, the output of the 14-bit adder is used
as an estimator for the frequency ratio. More particularly, in the example shown, the
output of the accumulator is equal to R x 128 x 129, where R is the frequency ratio
estimator.

The foregoing technique may be readily extended to phase discrimination.

20   Various different methods and apparatus for digital phase discrimination will be
described entailing different design tradeoffs.

The first method is conceptually straightforward but computationally expensive.
Referring to Figure 11A, the same observed frequency data stream and the same set of
weights corresponding to a triangular weighting function (Fig. 11B) are used. The

25   ratio of the reference frequency to the sampled frequency over a relatively long period
of time is first determined using the technique described previously. Having obtained
this frequency ratio estimator, short-term frequency deviations are estimated by
calculating the same frequency estimate as before but at a relatively high rate, as often
as once per sample period. That is, successive samples are all taken using the circuit of

30   Figure 10, as often as each sample period. The difference (ΔF) of each frequency

estimate (F) from the previously-determined frequency ratio (Fr) is calculated,
multiplied by an appropriate scale factor k and accumulated to obtain a corresponding
phase estimate Pf. (The first value of Pf is an arbitrarily chosen initial condition,
chosen for comparison to an ideal estimate. In practice, the phase may be initialized to

5   a value based on a priori knowledge of signal characteristics, or, absent such *a priori*
knowledge, may be set to zero upon detection of a phase inflection point.)

A phase-plot simulation comparing actual phase of a specified waveform (solid-
line) with estimated phase using the foregoing phase estimation method (dashed-line) is
shown in Fig. 11C.

10   The foregoing "frequency difference" phase estimation method is
computationally expensive because of the need to calculate frequency estimates at a
relatively high rate. A "pre-summation difference" phase estimation method obviates
this requirement. Referring to Figure 12A, instead of subtracting the frequency ratio
from a frequency estimate, the frequency ratio Fr is subtracted from the sampled data

15   stream itself. Assuming that the data stream is a bit stream of ones and zeros only, and
assuming a frequency ratio $Fr = 0.6875$, then the pre-summation difference Y will
have one of only two values, $Y = 1 - 0.6875 = .3125$ or $Y = 0 - 0.6875 = -0.6875$.
The Y values are accumulated to obtain corresponding values PX. Phase estimates PP_n
are obtained by filtering the PX values in substantially the same manner as described

20   previously in relation to forming frequency estimates (using the identical weighting
function, Fig. 12B, for example) with the exception that the filtered values are scaled
by the scale-factor k.

The pre-summation difference phase-calculation may be shown to be
mathematically equivalent to the frequency difference phase calculation. Simulation

25   results, shown in Fig. 12C, are therefore the same as in Fig. 11C. The hardware
realization, however, may be considerably simpler using the pre-summation difference
phase calculation, since only one computation is required per phase point. Such a
hardware realization is shown in Figure 13.

The pre-summation difference phase estimator of Figure 13 includes generally a

30   first accumulator ACC1, a weight generator WG similar or identical to the weight

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generator previously described in relation to Figure 10, and a second accumulator ACC2.

The accumulator ACC1 functions to produce phase numbers PX_i in correspondence to bits (or in other embodiments, symbols) of the observed frequency data stream and includes a multiplexer 1301, an adder 1303 and a register (e.g., a 16-bit register) 1305. The multiplexer 1301 selects one of the two possible values of Y_i in accordance with the value of X and applies Y_i to the adder 1303. The register value is added to Y_i to form PX_i, which is then strobed into the register. The adder 1303 and register 1305 therefore accumulate the PX_i values.

The PX_i values are then filtered in the accumulator ACC2, which includes a multiplier 1307, an adder 1309 and a register 1311. The multiplier receives weights from the weight generator WG and PX_i values from the accumulator ACC1. Respective weights and PX_i values are multiplied and the products accumulated, e.g., for 128 clock cycles, to produce a phase estimator PP. The multiplier may be constructed so as to apply the scale factor k to each product during the accumulation process.

An even simpler realization may be achieved using an integer difference phase calculation. The integer difference phase calculation is not mathematically equivalent to the foregoing methods, but is very close. Referring to Fig. 14A, this method uses, in addition to the observed frequency data stream, a reference frequency data stream that would result if the reference frequency were applied to the capture circuit of Figure 4 (with the same clock). A running sum D_i is then formed of the integer difference $X_i - R_i$. In many practical applications, such as the one illustrated in Figures 14 and 15, D_i will have the values 1, 0 and -1 exclusively. The general case in which D_i takes on other values may be appreciated and understood, however, from the present example, and is embraced by the present description.

Phase estimates are formed by filtering the D_i values in the same or similar manner as previously described. The same triangular weighting function may be used Fig. 14B. The integer difference phase calculation method produces identical simulation results, Fig. 14C, as the preceding methods.

Referring to Figure 15, in the instance where D takes on the values 1, 0 and -1 exclusively, the corresponding hardware realization may be substantially simplified (as compared to that of Figure 13, for example).

The integer difference phase estimator of Fig. 15, like that of Fig. 13,

5   includes generally a first accumulator ACC1, a weight generator WG, and a second accumulator ACC2. The accumulator ACC1 is of considerably different construction than the corresponding structure of Figure 13. The accumulator ACC1 of Figure 15 includes a reference pattern generator 1501, a 1-bit subtractor 1503, a 2-bit adder 1505 and a 2-bit register 1507. The 1-bit subtractor subtracts respective R values from

10   respective X values. The 2-bit adder and the register accumulate the resulting D_i values which, as explained previously, may be constrained to 1, 0, -1 only.

The weight generator WG and the accumulator ACC2 are substantially the same as in Figure 13, described previously. However, because D_i takes on the values 1, 0 and -1 exclusively, no multiplier is required. Instead, if $D_i = 1$, the weight value is

15   added to the accumulated value, and if $D_i = -1$, the weight value is subtracted. (If $D_i = 0$, the accumulated value remains unchanged.) The savings of a hardware multiplier is a particular advantage of the implementation of Fig. 15.

A further method of phase estimation is referred to as the clock measure phase calculation method. Referring to Figure 16A, this method is similar to the previous

20   integer difference phase calculation method insofar as R, X and D are concerned. This method, however, uses in addition to the reference frequency data stream R, "clock measure" numbers RG, which are the same as the numbers appearing in Fig. 2. Moreover, the weight function used is distinctly different, as shown in Figure 16B.

Clock measure phase estimate values PC are obtained using the following formula:

$$PC_n = k \cdot (D_n - frac(RG_n) + 0.5 + \sum_i (W_i \cdot X_{i+n-64}))$$

Simulation results using the clock measure phase calculation method are shown

5   in Figure 16C.

Referring to Figure 17, the clock measure phase estimator includes generally a first accumulator ACC1, a weight generator WG, and a second accumulator ACC2. The estimator additionally includes a summation block 1701.

The accumulator block ACC1 is substantially the same as the accumulator block

10   ACC1 of Figure 15. Note, however, that the reference pattern generator generates both the reference frequency data stream R, used within the accumulator ACC1, and the clock measure data stream RG which is input to the summation block 1701.

The weight generator includes a counter 1703 and weight generator logic 1705.

The accumulator ACC2 includes an adder 1707 and a register 1709. When X =

15   1, the weight value from the weight generator is added to the contents of the register 1709. The output of the adder becomes the new input of the register, which performs an accumulator operation for, e.g., 128 clock cycles.

At the conclusion of the accumulation operation of ACC2, the outputs of ACC1 and ACC2, together with the corresponding RG value, are summed in the summation

20   block 1701.

It will be appreciated by those of ordinary skill in the art that the invention can be embodied in other specific forms without departing from the spirit or essential character thereof. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by

25   the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalents thereof are intended to be embraced therein.

Claims:

1.   A method of determining the phase of a first clock signal using a second clock signal, comprising the steps of:

        sampling the first clock signal in accordance with the second clock signal

5   to produce a stream of digital bits; and

        forming from the stream of digital bits a digital word indicative of the phase.

2.   The method of Claim 1, wherein forming the digital word comprises

10   filtering the stream of digital bits.

3.   Apparatus for determining the phase of a first clock signal using a second clock signal, comprising:

        means for sampling the first clock signal in accordance with the second

15   clock signal to produce a stream of digital bits; and

        means for forming from the stream of digital bits a digital word indicative of the phase.

4.   The apparatus of Claim 3, wherein said means for forming comprises a

20   digital filter.

5.   The apparatus of Claim 4, wherein the digital filter employs a weighting function in which different weights are applied to different digital bits.

25   6.   A method of determining the phase of a first clock signal using a second clock signal, comprising the steps of:

        sampling the first clock signal in accordance with the second clock signal to produce a stream of digital symbols; and

        forming from the stream of digital symbols a digital value indicative of

30   the phase.

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7. The method of Claim 6, wherein forming the digital value comprises filtering the stream of digital bits.

8. Apparatus for determining the phase of a first clock signal using a
5 second clock signal, comprising:

means for sampling the first clock signal in accordance with the second clock signal to produce a stream of digital symbols; and

means for forming from the stream of digital bits a digital value indicative of the phase.
10

9. The apparatus of Claim 8, wherein said means for forming comprises a digital filter.

10. The apparatus of Claim 9, wherein the digital filter employs a weighting
15 function in which different weights are applied to different digital bits.

11. A method of producing a data stream indicative of the phase of one clock signal using another clock signal, comprising sampling one of the clock signals in accordance with the other clock signal to form a first stream of digital bits or symbols,
20 each digital bit or symbol representing a number of transitions of a predetermined polarity of the one clock signal that occurred during a particular period of the other clock signal, such that the stream of digital bits or symbols may be further processed to determined the relative phase.

25 12. The method of Claim 11, wherein a frequency difference phase calculation is employed, comprising the further steps of:

filtering the stream to obtain an average ratio of frequencies of the clock signals;

filtering the stream to obtain a series of short-term estimates of the ratio
30 of frequencies of the clock signals;

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for each estimate, calculating a difference between the estimate and the average ratio of frequencies and converting the difference to a phase increment; and

accumulating the phase increments to produce a running phase estimate.

5   13.   The method of Claim 11, wherein a pre-summation difference phase calculation is employed, comprising the further steps of:

producing a first stream of digital values by subtracting from each said digital bit or symbol a ratio of frequencies of the clock signals;

producing a second stream of digital values by accumulating the second

10   stream of digital values; and

filtering the second stream of digital values.

14.   The method of Claim 11, comprising the steps of:

producing a second stream of digital bits or symbols that result when

15   said other of said clock signals is sampled in accordance with said one of said clock signals;

subtracting bits or symbols of the second data stream from bits or symbols of the first stream to produce a third stream of digital bits or symbols; and

accumulating the third stream of digital bits or symbols to form a fourth

20   stream of digital bits or symbols each having one of the values 1, 0 and -1.

15.   The method of Claim 14, wherein an integer difference phase calculation method is employed, comprising the further step of filtering the fourth stream of digital bits or symbols.

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16.   The method of Claim 14, wherein a clock measure phase calculation is employed, comprising the further steps of:

filtering said first stream of digital bits or symbols to produce a filtered value;

producing a fifth stream of digital values that result when said one clock

signal is Sigma-Delta modulated in accordance with said other clock signal;

forming a difference of a value taken from said fourth data stream and a

fractional portion of a value taken from said fifth data stream; and

5   combining said difference and said filtered value.

17.   The method of Claim 16, wherein filtering is performed using a

hyperbolic weighting function.

10   18.   A circuit for producing a data stream indicative of the phase of one clock

signal using another clock signal, comprising a first input terminal to which a first

clock signal is applied, a second input terminal to which a second clock signal is

applied, and producing as an output signal a stream of digital bits or symbols, each

digital bit or symbol representing a number of transitions of a predetermined polarity of

15   the one clock signal that occurred during a particular period of the other clock signal,

such that the stream of digital bits or symbols may be further processed to determined

the relative phase.

19.   The apparatus of Claim 18, further comprising:

20   a weight generator;

a first accumulator; and

a second accumulator;

wherein the first accumulator receives as an input the stream of

digital bits or symbols and produces an output stream of bits or symbols, the weight

25   generator produces a series of weights, and the second accumulator receives the series

of weights and the output stream of bits or symbols and produces a phase estimate.

20.   The apparatus of Claim 19, wherein the second accumulator comprises a

hardware multiplier.

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21.   The apparatus of Claim 19, wherein said first accumulator comprises a reference pattern generator and said output stream consists of the symbols 1, 0 and -1, and wherein said second accumulator comprises an adder/subtractor.

5   22.   The apparatus of Claim 18, further comprising:
            a weight generator;
            a first accumulator;
            a second accumulator; and
            a summation block;
10   wherein the weight generator produces a series of weights, the first accumulator receives as inputs the stream of digital bits or symbols and the series of weights and produces a first output stream of symbols, the second accumulator receives as inputs the stream of digital bits or symbols and produces a second output stream of symbols, and the summation block sums outputs from the first accumulator
15   and the second accumulator to produce a phase estimate.

FIG. 2
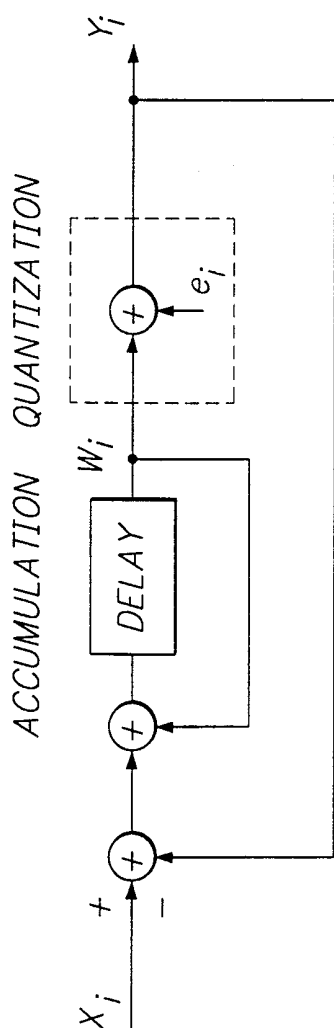
Accumulator $G_n=G_{n-1}+0.6875-INT(G_{n-1})$	Data Stream $R_n=INT(G_n)$
0.6875	0
1.375	1
1.0625	1
0.75	0
1.4375	1
1.125	1
0.8125	0
1.5	1
1.1875	1
0.875	0
1.5625	1
1.25	1
0.9375	0
1.625	1
1.3125	1
1	1
0.6875	0

FIG. 1

ACCUMULATION   QUANTIZATION

FIG. 3
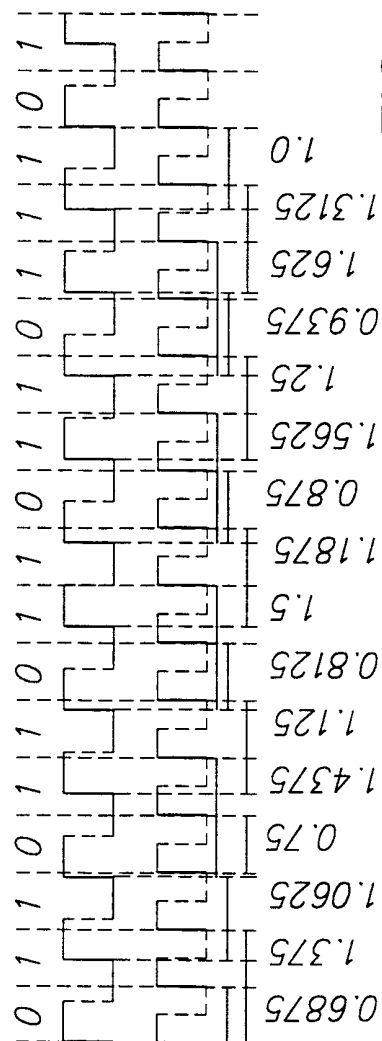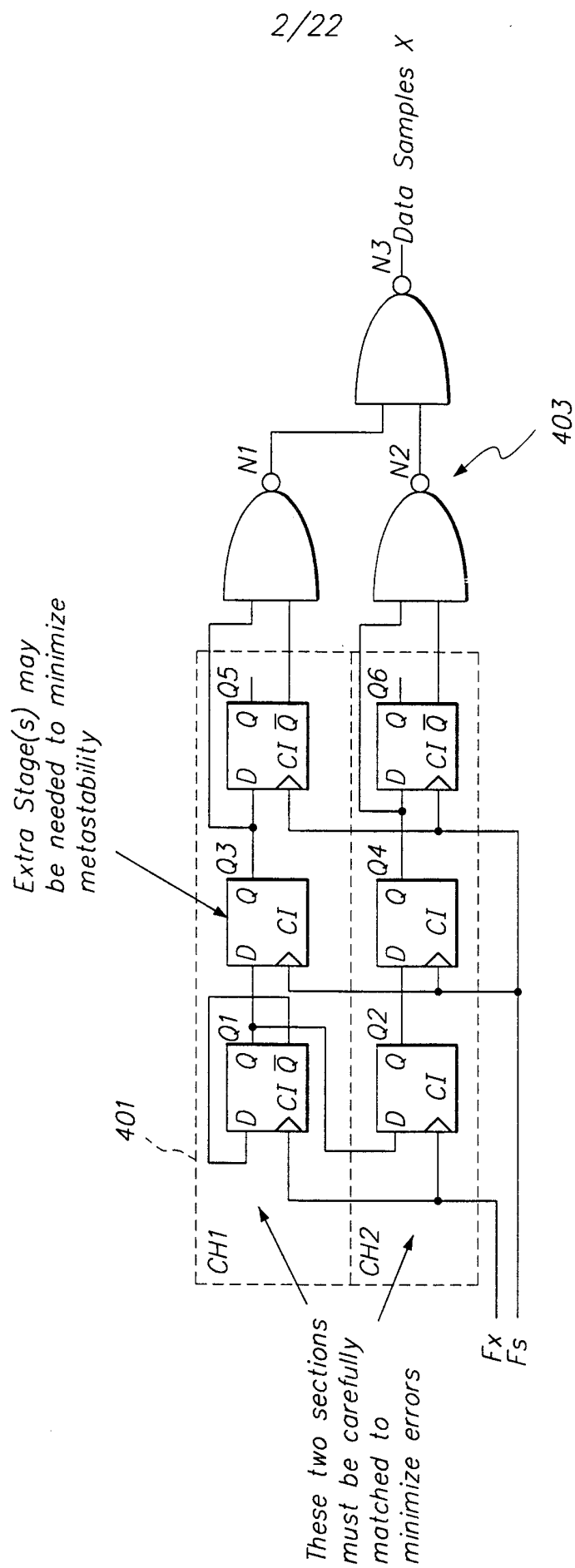
Fig. 4

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FIG. 5

FIG. 6

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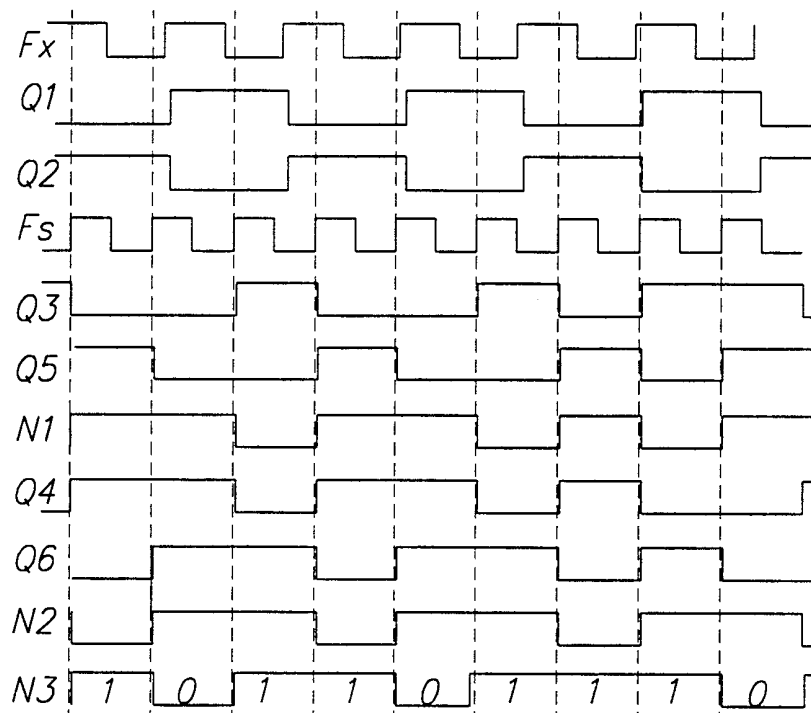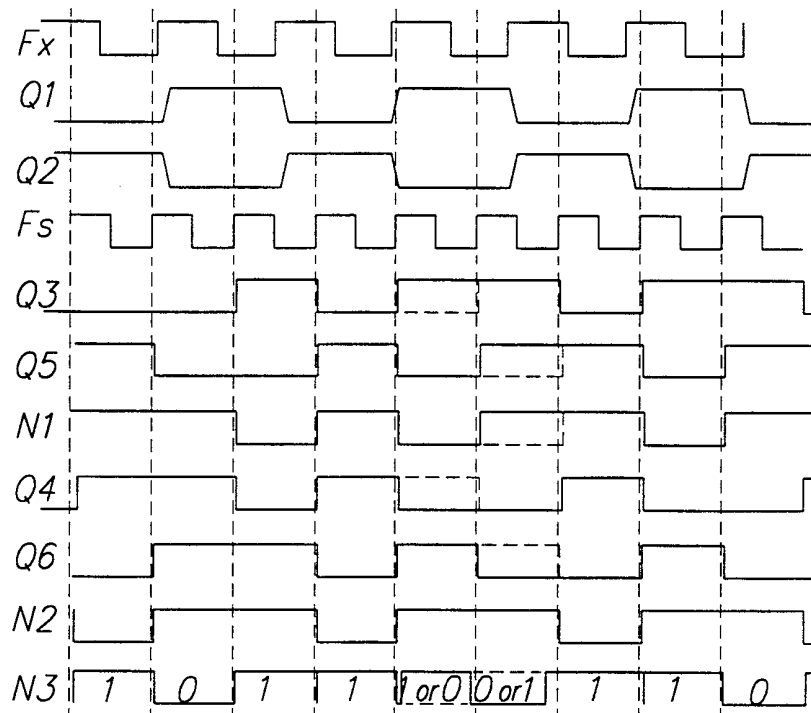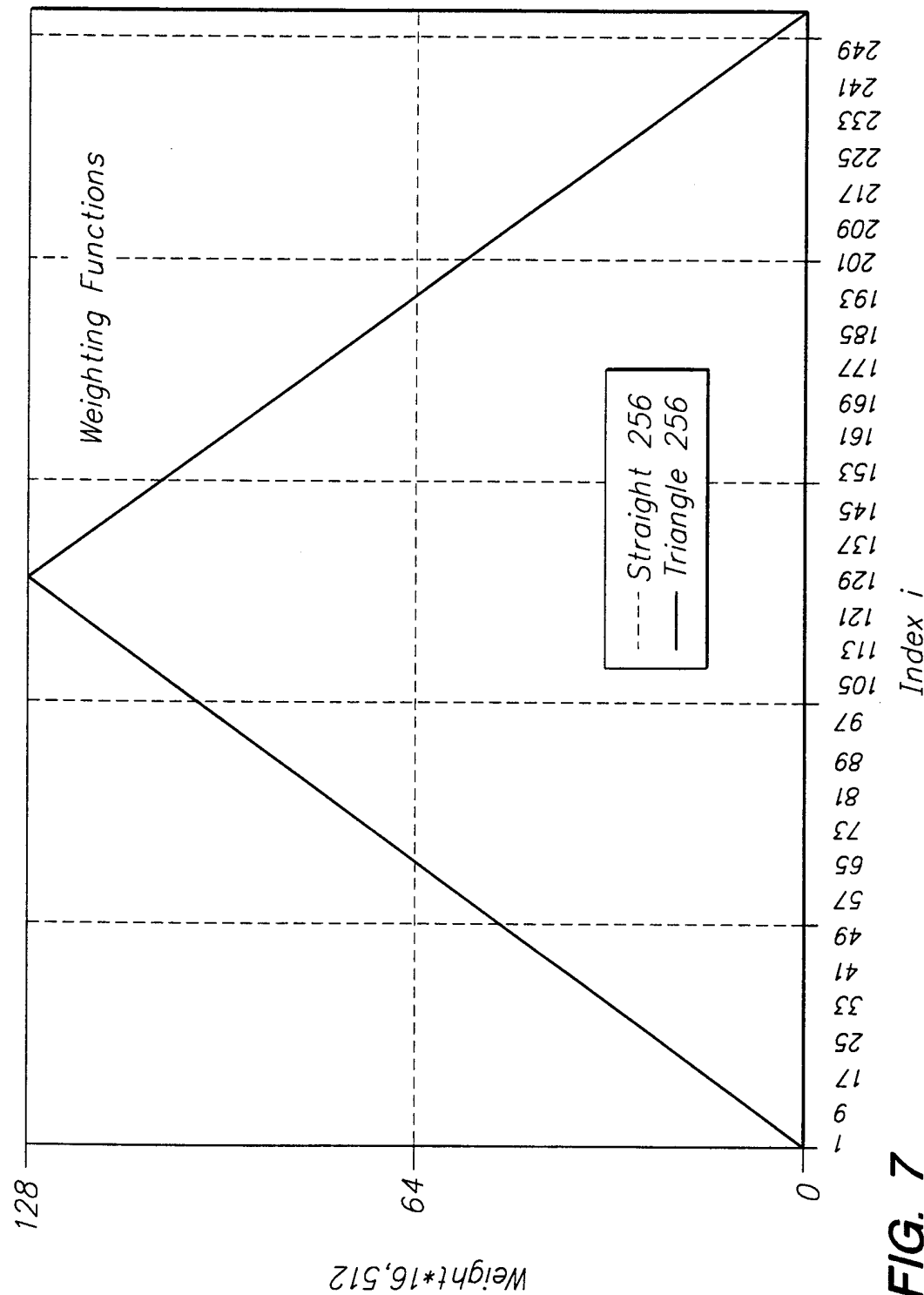
FIG. 7
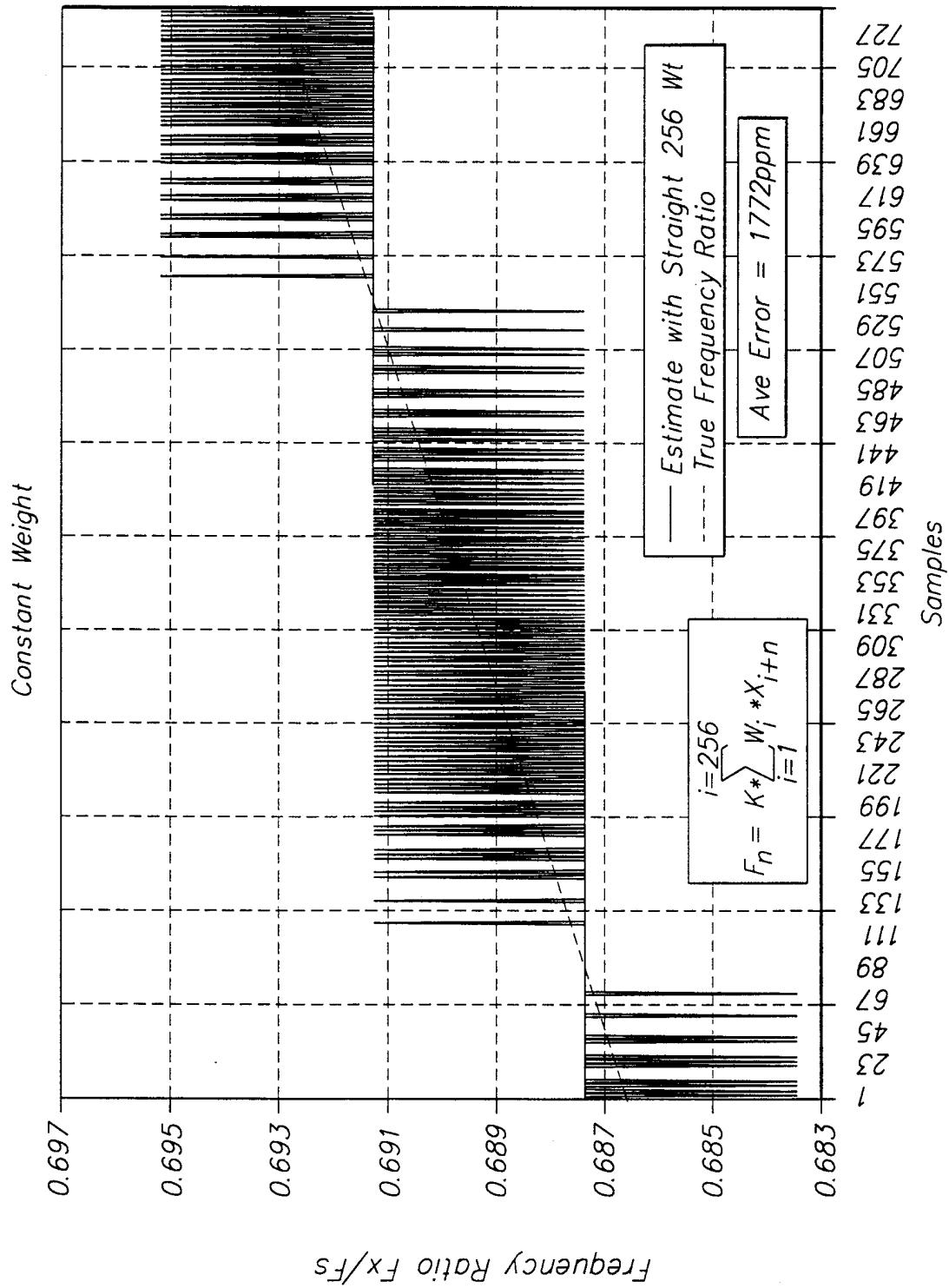
FIG. 8

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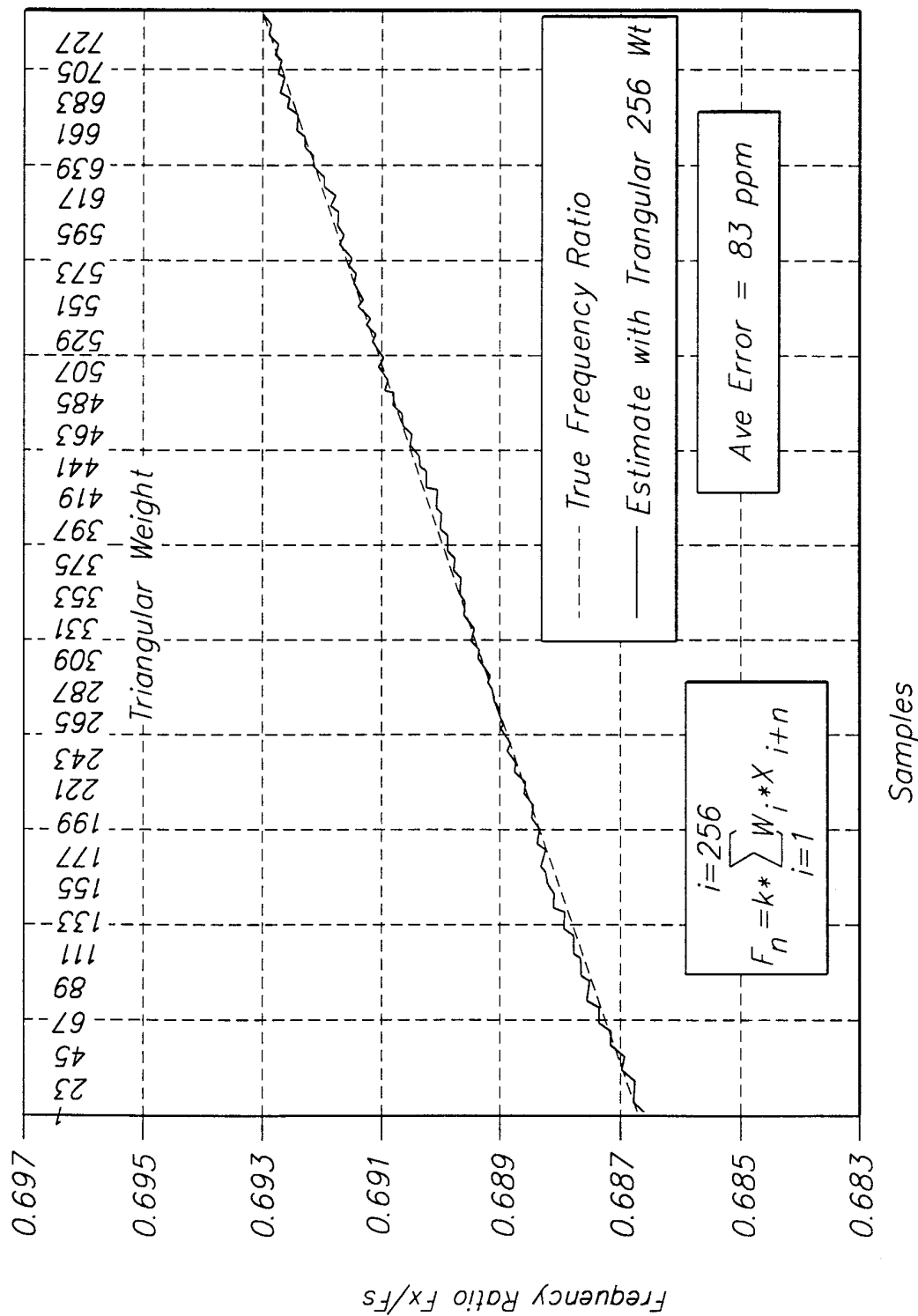
FIG. 9

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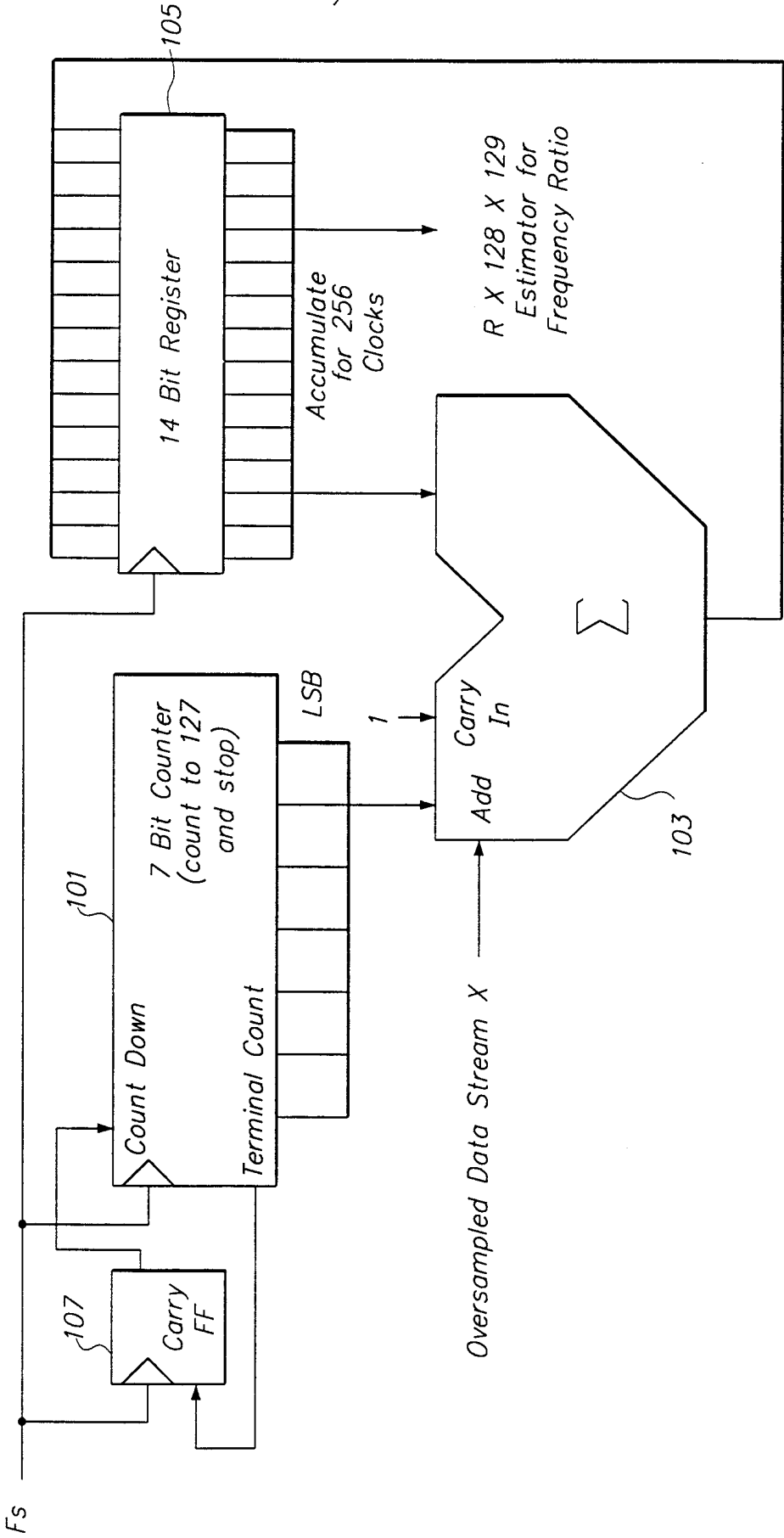
FIG. 10

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Observed Frequency Data Stream X	Weight W	Fr Ratio = Reference Frequency/ Sample Frequency =
1	1	0.6875
1	2	
0	3	
1	4	
1	5	
0	6	
1	7	
1	8	
0	9	
1	10	
1	11	
1	12	
0	13	
1	14	
1	15	
0	16	
1	17	
1	18	
0	19	
1	20	
1	21	
0	22	
1	23	
1	24	
0	25	
1	26	
1	27	
1	28	
0	29	
1	30	
1	31	
0	32	
1	33	
1	34	
0	35	
1	36	
1	37	
0	38	
1	39	
1	40	
0	41	
1	42	
1	43	

FIG. 11A-1

FIG. 11A-1

FIG. 11A-2

FIG. 11A

0	44
1	45
1	46
1	47
0	48
1	49
1	50
0	51
1	52
1	53
0	54
1	55
1	56
0	57
1	58
1	59
0	60
1	61
1	62
1	63
0	64

		Frequency Estimate			Integration
		$F_n =$ $\sum_i(W_i * X_{i+n})$		$\Delta F_i =$ $F_i - Fr$ Ratio	$PF_n =$ $PF_{n-1} * k * \Delta F_i$
	Correct Phase	F		ΔF	Pf
1	64	−53.714763	0.686058	−0.001442	−55.876923
1	63	−54.394811	0.686058	−0.001442	−56.615385
0	62	−55.066978	0.686058	−0.001442	−57.353846
1	61	−55.731139	0.686058	−0.001442	−58.092308
1	60	−56.387171	0.686058	−0.001442	−58.830769
0	59	−57.034949	0.686058	−0.001442	−59.569231
1	58	−57.674350	0.686058	−0.001442	−60.307692

FIG. 11A-2

FIG. 11B

Ave Error=1.501453
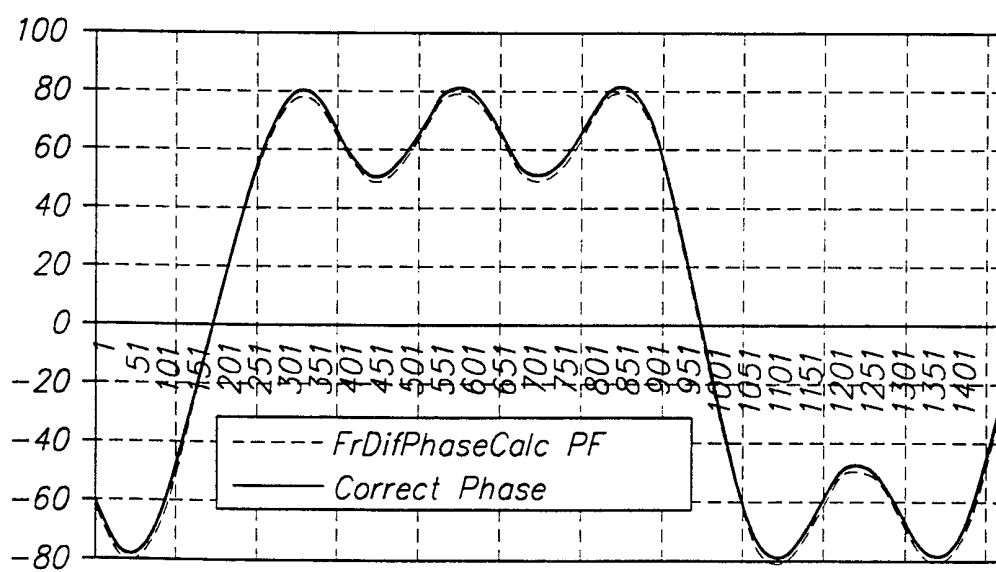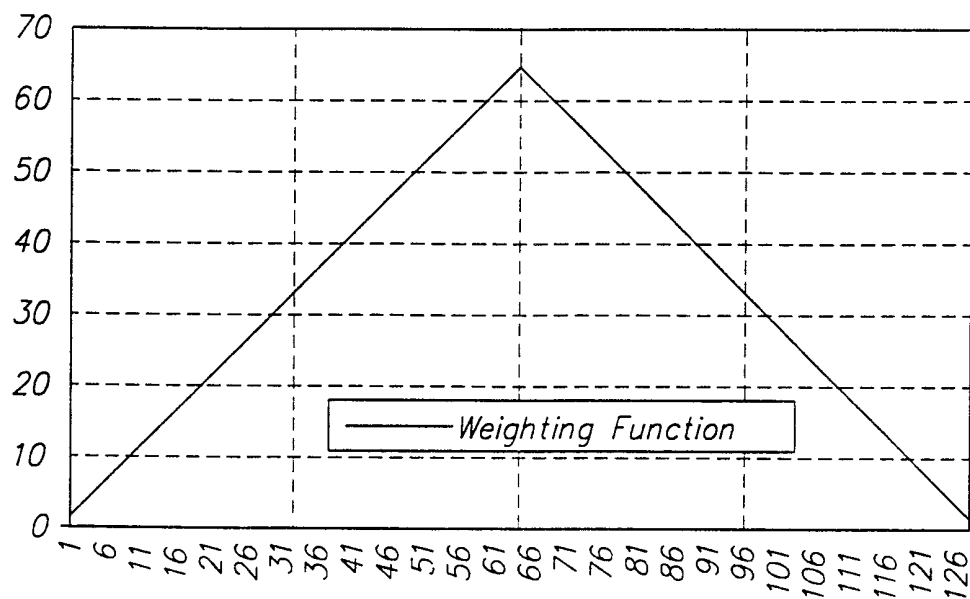
FIG. 11C

Observed Frequency Data Stream X	Weight W	$Y_i = X_i - FrRatio$ Y	$PX_i = PX_{i-1} + Y_i$ Px	Fr Ratio = Reference Frequency/ Sample Frequency = 0.6875
1	1	0.3125	0.0000	
1	2	0.3125	0.3125	
0	3	−0.6875	−0.3750	
1	4	0.3125	−0.0625	
1	5	0.3125	0.2500	
0	6	−0.6875	−0.4375	
1	7	0.3125	−0.1250	
1	8	0.3125	0.1875	
0	9	−0.6875	−0.5000	
1	10	0.3125	−0.1875	
1	11	0.3125	0.1250	
1	12	0.3125	0.4375	
0	13	−0.6875	−0.2500	
1	14	0.3125	0.0625	
1	15	0.3125	0.3750	
0	16	−0.6875	−0.3125	
1	17	0.3125	0.0000	
1	18	0.3125	0.3125	
0	19	−0.6875	−0.3750	
1	20	0.3125	−0.0625	
1	21	0.3125	0.2500	
0	22	−0.6875	−0.4375	
1	23	0.3125	−0.1250	
1	24	0.3125	0.1875	
0	25	−0.6875	−0.5000	
1	26	0.3125	−0.1875	
1	27	0.3125	0.1250	
1	28	0.3125	0.4375	
0	29	−0.6875	−0.2500	
1	30	0.3125	0.0625	
1	31	0.3125	0.3750	
0	32	−0.6875	−0.3125	
1	33	0.3125	0.0000	
1	34	0.3125	0.3125	
0	35	−0.6875	−0.3750	
1	36	0.3125	−0.0625	
1	37	0.3125	0.2500	
0	38	−0.6875	−0.4375	
1	39	0.3125	−0.1250	
1	40	0.3125	0.1875	
0	41	−0.6875	−0.5000	
1	42	0.3125	−0.1875	
1	43	0.3125	0.1250	

FIG. 12A-1

FIG. 12A-1

FIG. 12A-2

FIG. 12A

SUBSTITUTE SHEET (rule 26)

				Correct Phase	$PP_n = k*\sum_i (W_i + PX_{i+n})$ PP
0	44	−0.6875	−0.5625		
.1	45	0.3125	−0.2500		
1	46	0.3125	0.0625		
1	47	0.3125	0.3750		
0	48	−0.6875	−0.3125		
1	49	0.3125	0.0000		
1	50	0.3125	0.3125		
0	51	−0.6875	−0.3750		
1	52	0.3125	−0.0625		
1	53	0.3125	0.2500		
0	54	−0.6875	−0.4375		
1	55	0.3125	−0.1250		
1	56	0.3125	0.1875		
0	57	−0.6875	−0.5000		
1	58	0.3125	−0.1875		
1	59	0.3125	0.1250		
0	60	−0.6875	−0.5625		
1	61	0.3125	−0.2500		
1	62	0.3125	0.0625		
1	63	0.3125	0.3750		
0	64	−0.6875	−0.3125		
1	64	0.3125	0.0000	−53.714763	−55.876923
1	63	0.3125	0.3125	−54.394811	−56.615385
0	62	−0.6875	−0.3750	−55.066976	−57.353846
1	61	0.3125	−0.0625	−55.731139	−58.092308
1	60	0.3125	0.2500	−56.387171	−58.830769
0	59	−0.6875	−0.4376	−57.034949	−59.569231
1	58	0.3125	−0.1250	−57.674350	−60.307692

FIG. 12A-2

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FIG. 12B

Ave Error= 1.501453

FIG. 12C

FIG. 13

Reference Frequency Data Stream R	Observed Frequency Data System X	$D_i = D_{i-1} + X_i - Ri$ D	Weight W	Fr Ratio= Reference Frequency/ Sample Frequency = 0.6875
1	1	0	1	
1	1	0	2	
0	0	0	3	
1	1	0	4	
1	1	0	5	
0	0	0	6	
1	1	0	7	
1	1	0	8	
1	0	-1	9	
0	1	0	10	
1	1	0	11	
1	1	0	12	
0	0	0	13	
1	1	0	14	
1	1	0	15	
0	0	0	16	
1	1	0	17	
1	1	0	18	
0	0	0	19	
1	1	0	20	
1	1	0	21	
0	0	0	22	
1	1	0	23	
1	1	0	24	
1	0	-1	25	
0	1	0	26	
1	1	0	27	
1	1	0	28	
0	0	0	29	
1	1	0	30	
1	1	0	31	
0	0	0	32	
1	1	0	33	
1	1	0	34	
0	0	0	35	
1	1	0	36	
1	1	0	37	
0	0	0	38	
1	1	0	39	
1	1	0	40	
1	0	-1	41	
0	1	0	42	

FIG. 14A-1

FIG. 14A-1
FIG. 14A-2

FIG. 14A

				Correct Phase	$PI_n =$ $k_0 + k_1 * \sum_i (W_i * D_{i+n})$ / F
1	1	0	43		
1	0	−1	44		
0	1	0	45		
1	1	0	46		
1	1	0	47		
0	0	0	48		
1	1	0	49		
1	1	0	50		
0	0	0	51		
1	1	0	52		
1	1	0	53		
0	0	0	54		
1	1	0	55		
1	1	0	56		
1	0	−1	57		
0	1	0	58		
1	1	0	59		
1	0	−1	60		
0	1	0	61		
1	1	0	62		
1	1	0	63		
0	0	0	64		
1	1	0	64	−53.714763	−55.876923
1	1	0	63	−54.394811	−56.615385
0	0	0	62	−55.066978	−57.353846
1	1	0	61	−55.731139	−58.092308
1	1	0	60	−56.387171	−58.830769
0	0	0	59	−57.034949	−59.569231
1	1	0	58	−57.674350	−60.307692

$k_0 = 16$

FIG. 14A-2

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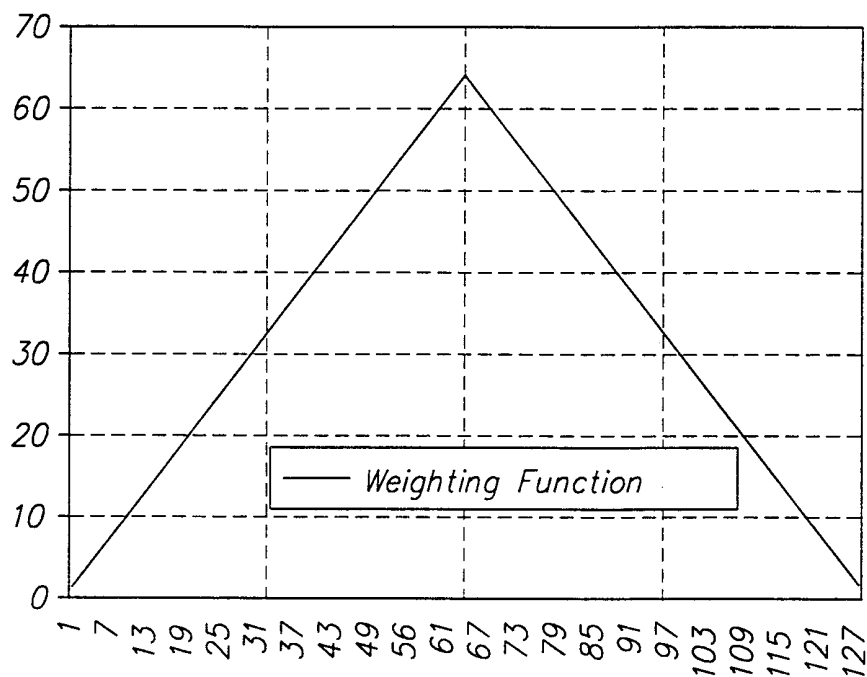
FIG. 14B

Ave Error= 1.501453

FIG. 14C

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FIG. 15

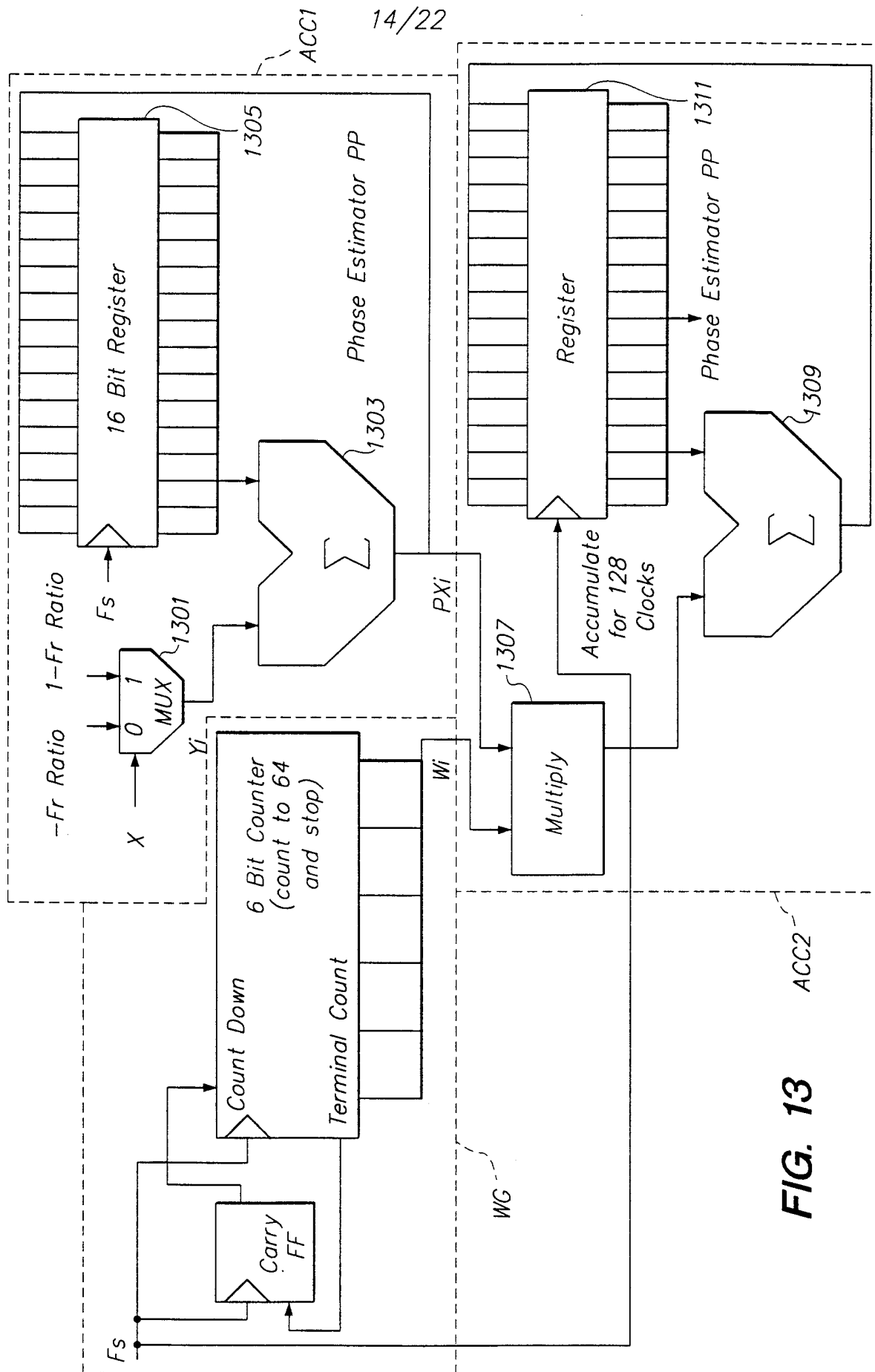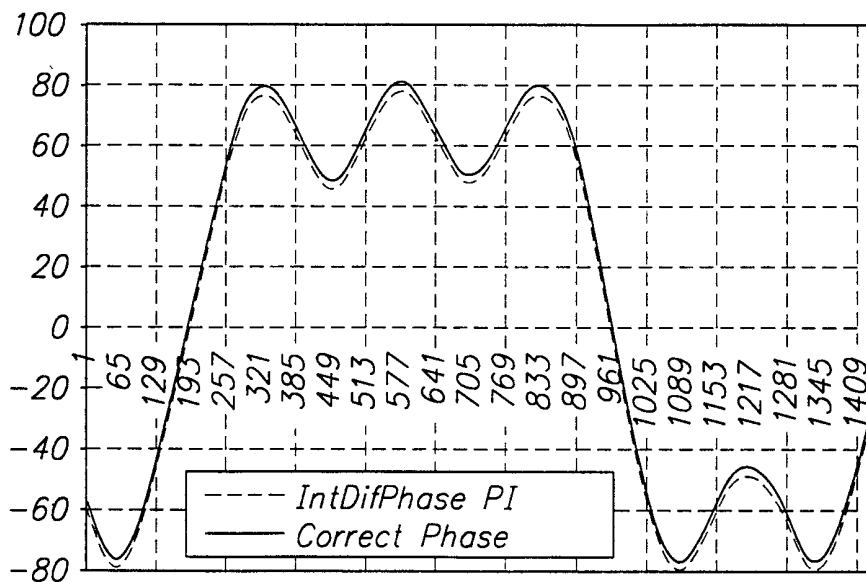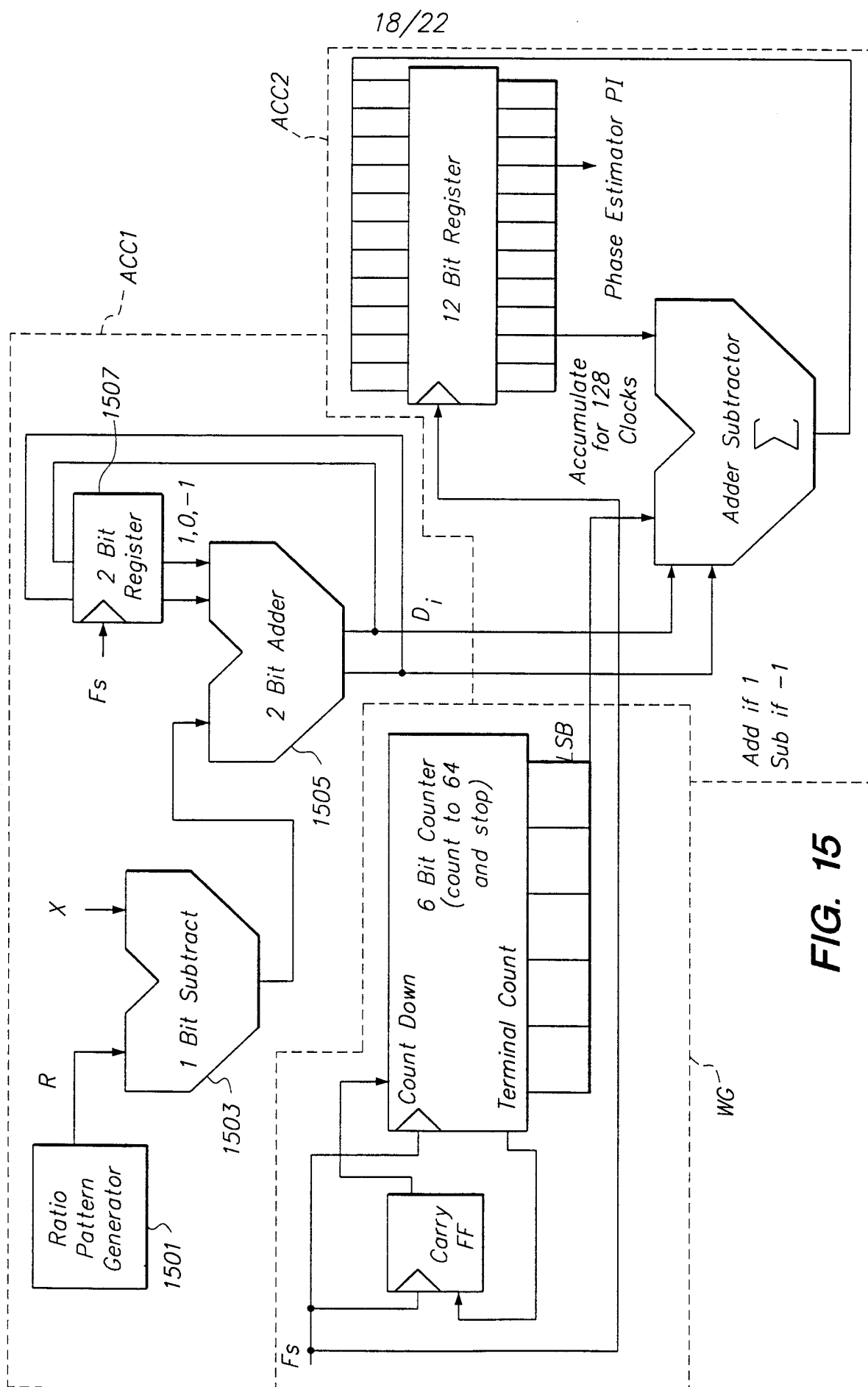| Reference Frequency Generator RG	Reference Frequency Data Stream R	Observed Frequency Data System X	$D_i = D_{i-1} + X_i - R_i$		Fr Ratio= Reference Frequency/ Sample Frequency = 0.6875
			D	Weight W	
1.5	1	1	0	−0.5	
1.1875	1	1	0	−2	
0.875	0	0	0	−4.5	
1.5625	1	1	0	−8	
1.25	1	1	0	−12.5	
0.9375	0	0	0	−18	
1.625	1	1	0	−24.5	
1.3125	1	1	0	−32	
1	1	0	−1	−40.5	
0.6675	0	1	0	−50	
1.375	1	1	0	−60.5	
1.0625	1	1	0	−72	
0.75	0	0	0	−84.5	
1.4375	1	1	0	−98	
1.125	1	1	0	−112.5	
0.8125	0	0	0	−128	
1.5	1	1	0	−144.5	
1.1875	1	1	0	−162	
0.875	0	0	0	−180.5	
1.5625	1	1	0	−200	
1.25	1	1	0	−220.5	
0.9375	0	0	0	−242	
1.625	1	1	0	−264.5	
1.3125	1	1	0	−288	
1	1	0	−1	−312.5	
0.6875	0	1	0	−338	
1.375	1	1	0	−364.5	
1.0625	1	1	0	−392	
0.75	0	0	0	−420.5	
1.4375	1	1	0	−450	
1.125	1	1	0	−480.5	
0.8125	0	0	0	−512	
1.5	1	1	0	−644.5	
1.1875	1	1	0	−578	
0.875	0	0	0	−612.5	
1.5625	1	1	0	−648	
1.25	1	1	0	−684.5	
0.9375	0	0	0	−722	
1.625	1	1	0	−760.6	
1.3125	1	1	0	−800	
1	1	0	−1	−840.5	
0.6875	0	1	0	882	

FIG. 16A-1

FIG. 16A-2

FIG. 16A

FIG. 16A-1

FIG. 16A-2

					Correct Phase	$PC_n = k*(D_n - frac(RC_n) + 0.5 + \sum_i (W_i * x_{i+n-64}))$ PC
1.375	1	1	0	−924.5		
1.0625	1	0	−1	−968		
0.75	0	1	0	−1012.5		
1.4375	1	1	0	−1068		
1.125	1	1	0	−1104.5		
0.8125	0	0	0	−1152		
1.5	1	1	0	−1200.5		
1.1875	1	1	0	−1250		
0.875	0	0	0	−1300.5		
1.5625	1	1	0	−1352		
1.25	1	1	0	−1404.5		
0.9375	0	0	0	−1458		
1.625	1	1	0	−1512.5		
1.3125	1	1	0	−1568		
1	1	0	−1	−1624.5		
0.6875	0	1	0	−1682		
1.375	1	1	0	−1740.5		
1.0625	1	0	−1	−1800		
0.75	0	1	0	−1860.5		
1.4375	1	1	0	−1922		
1.125	1	1	0	−1984.5		
0.8125	0	0	0	−2048		
1.5	1	1	0	2048	−53.374738	−55.507692
1.1875	1	1	0	1984.5	−54.054787	−56.246154
0.875	0	0	0	1922	−54.730895	−56.984615
1.5625	1	1	0	1860.5	−55.399059	−57.723077
1.25	1	1	0	1800	−56.059155	−58.461538
0.9375	0	0	0	1740.5	−56.711060	−59.200000
1.625	1	1	0	1682	−57.354650	−59.938462
1.3125	1	1	0	1624.5	−57.939800	−60.676923
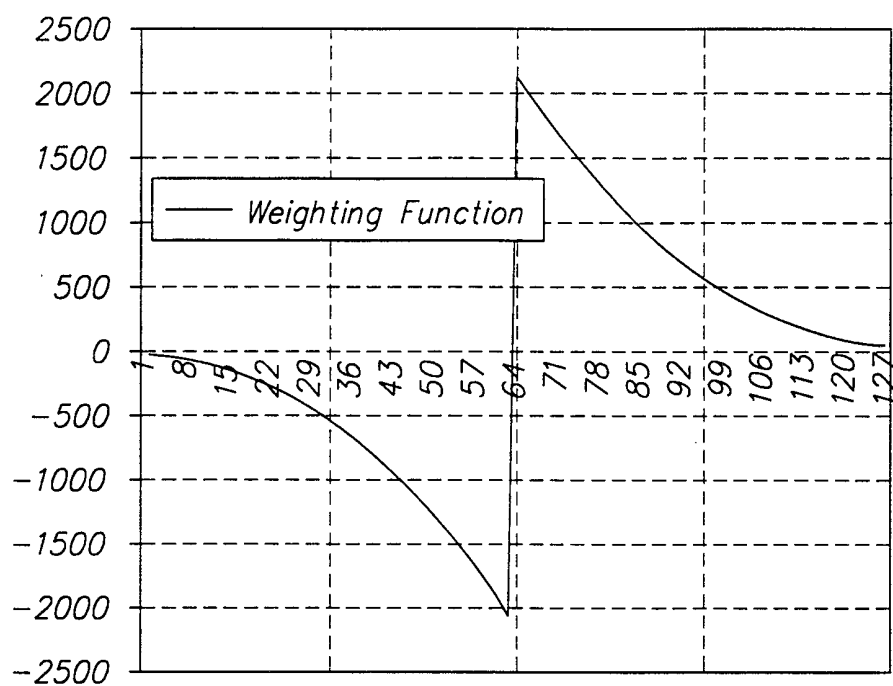
FIG. 16B
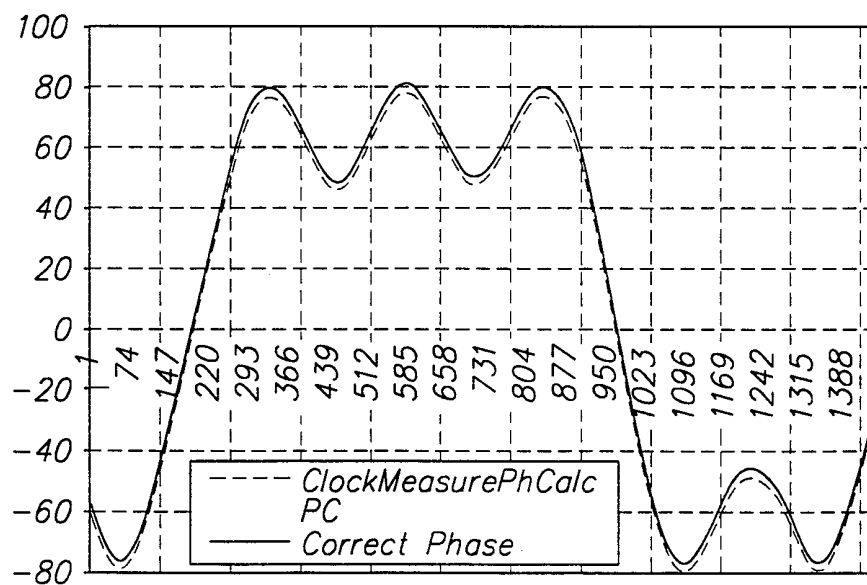
Ave Error= 1.501476

FIG. 16C
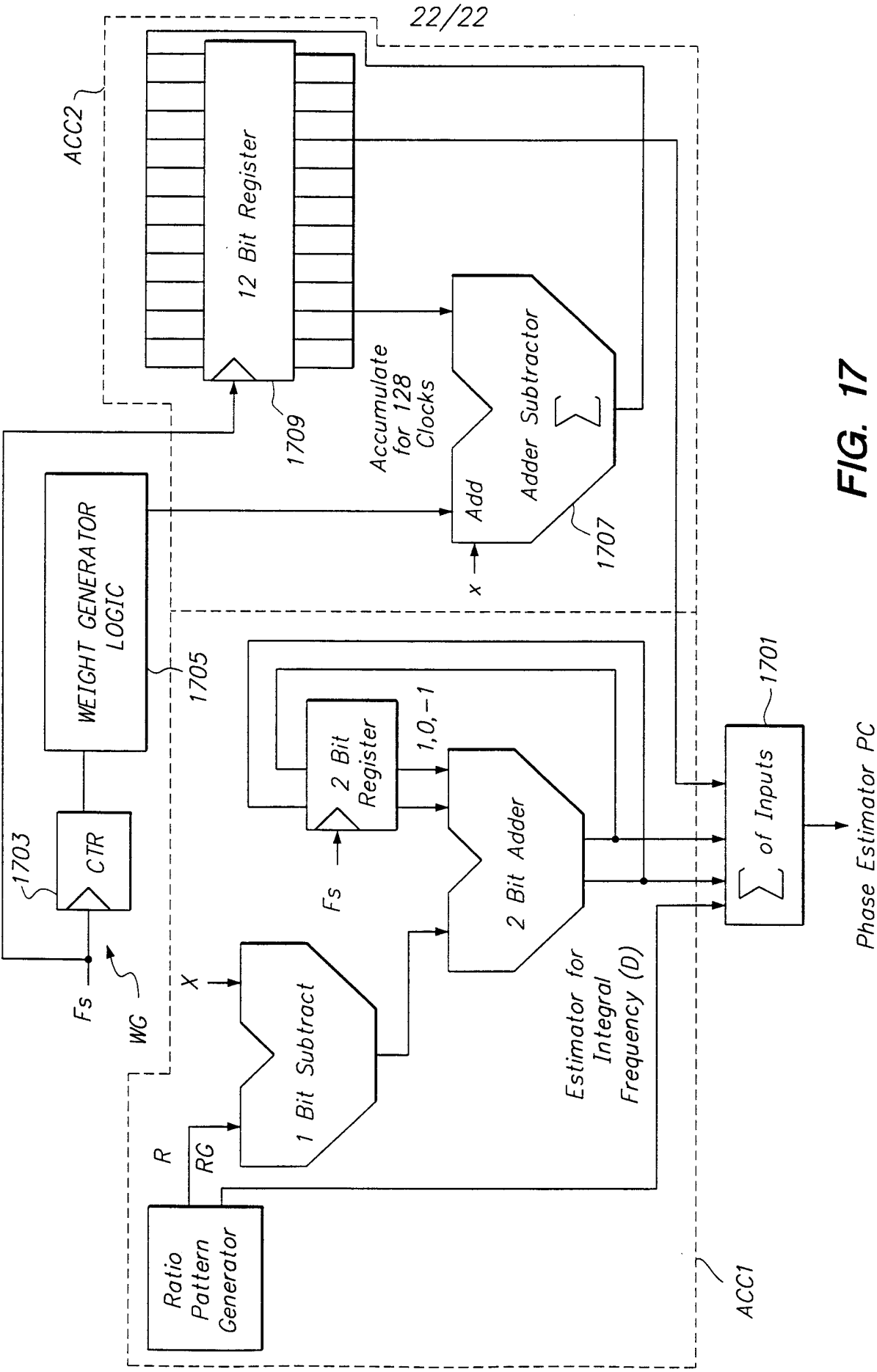
FIG. 17

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H04L 7/04
US CL : 375/362
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
U.S. : 375/362, 354,355, 360, 371,375

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,557,647 A (KUSHIGE et al) 17 September 1996, fig. 6, col. 7, lines 1-4, 13-20.	1, 3, 6, 8, 11, and 18
Y		2, 4, 5, 7, 9, and 10
Y	US 4,764,923 A (FORTH et al) 16 August 1988, fig. 2, col. 4, lines 35-55.	1-11, and 18
Y	US 4,468,794 A (WATERS et al) 28 August 1984, figs. 2 and 3, col. 8, lines 12-22.	1-11, and 18
Y	US 4,527,145 A (HAUSSMANN et al) 02 July 1985,figs. 1, 2, 3, 5, 7 and 10.	1-11 and 18
Y	US 5,513,209 A (HOLM) 30 April 1996, fig. 8, col. 12, lines 18-35.	1-11, and 18

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier document published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
" "	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 DECEMBER 1998	08 FEB 1999
Name and mailing address of the ISA/ US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	Authorized officer JASON CHAN
Facsimile No. (703) 305-3230	Telephone No. (703) 308-0000

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