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(54) IC WAFER CUSHIONED SEPARATORS

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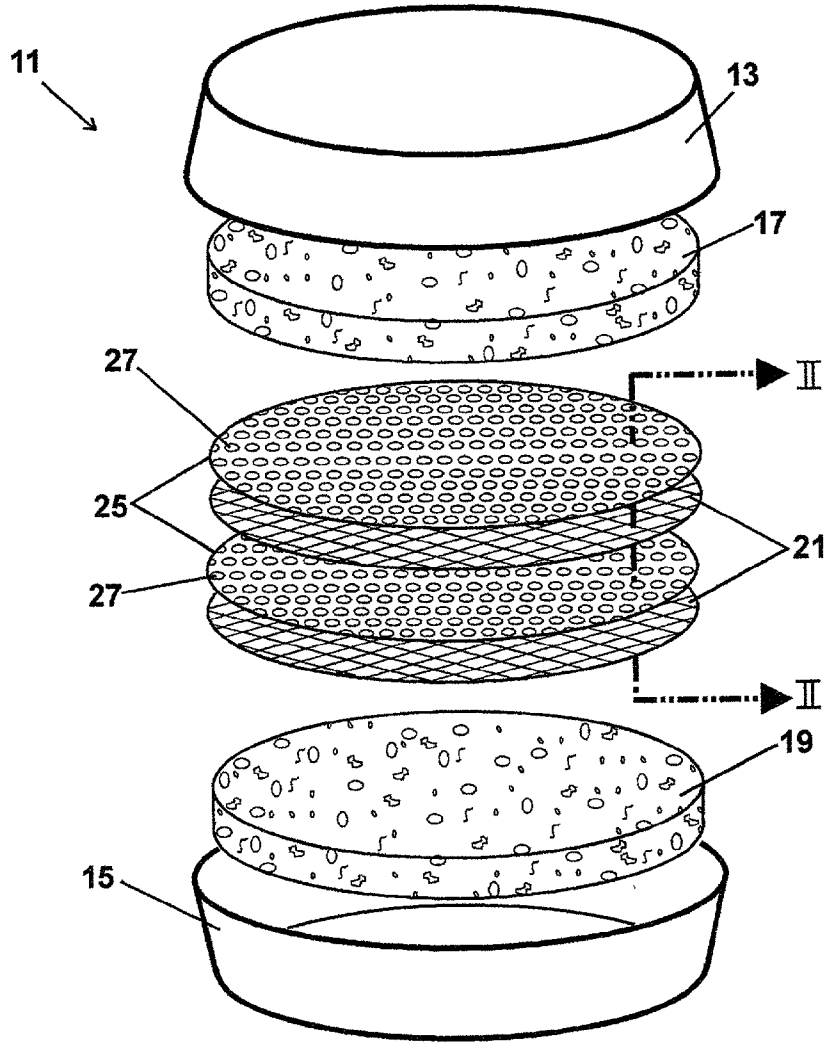
(57) **ABSTRACT**

An IC wafer shipping container has therein a stack of IC wafers. At least one side of each wafer has raised, conductive bump pads. A separator is located between two wafers. The film separators each have a dissipative layer and an insulating layer. The separators are cushioned to protect the wafers from mechanical shock and electrical shock. The separators are cushioned by embossing.



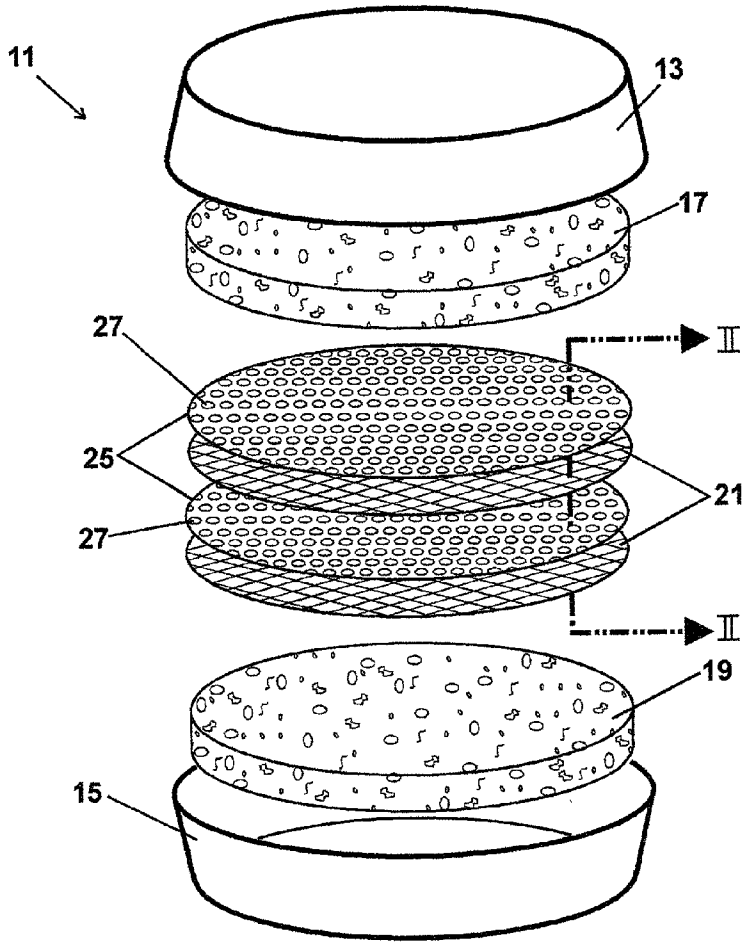

11
13
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FIG. 1

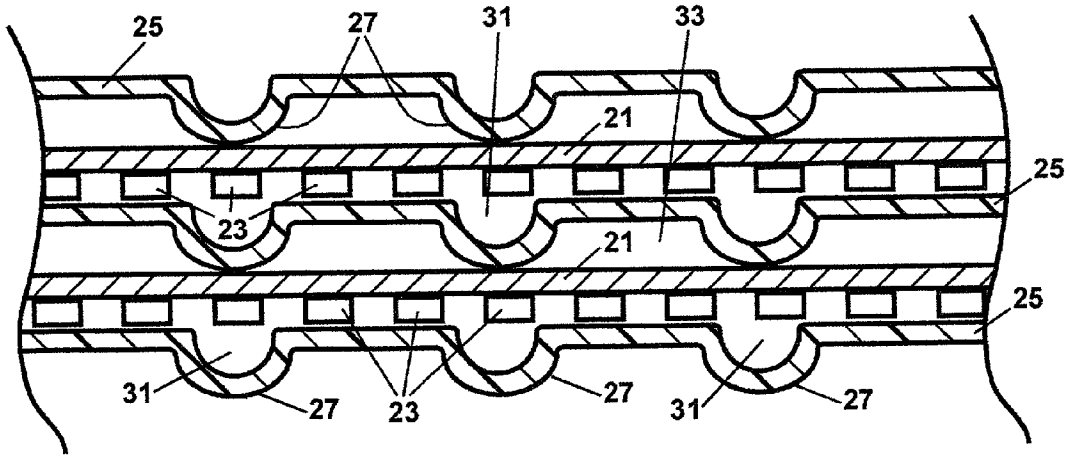
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FIG. 2

IC WAFER CUSHIONED SEPARATORS

[0001] This application is a continuation-in-part of application Ser. No. 60/282,816, filed Apr. 10, 2001.

FIELD OF THE INVENTION

[0002] The present invention relates to a method and apparatus for protecting sensitive articles, such as integrated circuits, from mechanical shock.

BACKGROUND OF THE INVENTION

[0003] There has been a significant advancement in fabrication technology of IC (Integrated Circuit) wafers in that the IC wafers can displace greater amounts of circuitry geometries in a much smaller area as compared to past technologies. These increased geometries are made possible due to advanced photolithography technology that provides much smaller line widths. Additionally, there is new technology to fabricate much smaller bond pads to accommodate and match these smaller line widths. The combination of these technologies enables a new breed of IC wafers to have increased functions at much higher speeds.

[0004] Under this combined technology, bond pads are fabricated in the shape of a ball for the purpose of accommodating "pick & place" operations on Printed Circuit (PC) boards. These balls are normally made of PbSn solder having diameters in the micrometer range. In this invention, bond pads fabricated with solder balls are hereinafter referred to as "bump bond pads" or "bump pads" and the IC wafers having them are referred to as "bumped wafers". This is because the bump pads have elevated heights that are different from wafer surfaces.

[0005] This height difference is critical in that bump pads can become instruments to receive and/or transfer damaging shock energy moving in a direction from one wafer to another when the IC wafers are "coin-stacked" within shipping containers. For the purpose of this invention, shock energy is mechanical in nature and can occur when the shipping container of IC wafers is mishandled, such as when the container is dropped, bumped, or otherwise jarred. The wafers are also subject to damage due to stress energy. Stress damage occurs, for example, when the wafers are tightly packed within the shipping containers or even from the combined weight of the packaged wafers. To prevent wafer damage, shock energy must be absorbed and stress energy must be relieved.

[0006] The problem here is that shock/stress energy becomes accentuated and enhanced with the height of the bump pads. The mechanical impact or stress of one wafer against an adjoining wafer is concentrated at the bump pads instead of being evenly distributed over the entire surface area of the wafer. Consequently, in the absence of a proper cushioning scheme, this enhanced energy can extrapolate to catastrophic energy to damage IC wafers when "coin-stacked" on top of each other within containers.

[0007] It is not always practical for wafers packaged within present day shipping containers using cushions to prevent the transfer of shock/stress energy that damages wafers stored therein. An example would be one prior art wafer shipping container that has a thick wall made of dense hard plastic polymer and that has little ability to absorb shock or stress energy that can easily exceed the ability of enclosed cushions to absorb and this can damage the wafers. A second example would be another prior art wafer shipping container having inner and outer walls where the inner wall is designed for the purpose of eliminating the requirement for cushioning liners to protect wafers from damage during shipment phases. Due to wafer close proximity to the inner wall in this particular container, there is little ability to absorb a resonance of shock energy that can easily exceed of the ability of enclosed cushions to absorb and this can damage the wafers. A third example would be prior art shipping containers made of exceptionally thin walls with little ability to absorb shock or stress energy that can easily become in excess of the ability of enclosed cushions to absorb and this can damage wafers.

[0008] Therefore, any shock or stress energy caused by a sudden impact or mishandling that exceeds the cushions' ability to absorb can transfer damage to: (1) exceptionally thin wafers coin-stacked within any or all of the above described shipping containers, and (2) wafers having bump pads "coin-stacked" within any or all of the above described shipping containers.

[0009] In the prior art, IC wafers stacked within shipping containers are separated from adjacent wafers by sheets of material known as separators or interleafs. Prior art interleafs are made of various materials including sheets of polyethylene fiber (e.g. Tyvek), polymer films, rice paper, etc., and all, by the nature of their structure, have little or no resiliency to absorb any damaging energy. These interleafs are only designed to separate IC wafers from each other without cushioning qualities. Therefore, prior art interleafs, regardless of make or type, will have little or no resiliency, and thus no ability to absorb damaging shock/stress energy to protect wafers stored within containers that exceed the ability of enclosed cushions to absorb.

[0010] Separators that are made of foam do have resiliency through the thickness of the separator and will adequately provide shock protection for wafers with bump pads by absorbing the shock energy. However, foam separators have chemical additives to achieve surface resistivities of 10^4-10^{11} ohms in order to prevent electrostatic discharge (ESD) and electrical overstress (EOS) events. These foam separators are also unnecessarily thick and take up space and leave each and every bump pad subject to corrosive damage caused by chemical depletion or outgassing of airborne molecular contaminants (AMCs). Such AMC's can become a devastating problem for high speed integrated circuit (IC) devices.

SUMMARY OF THE INVENTION

[0011] It is an object of the present invention to provide a separator that reduces damage to integrated circuit wafers due to mechanical shock.

[0012] The present invention provides a packaging configuration for integrated circuit wafers. There are at least two integrated circuit wafers. A film having a pattern of projections extending from the film is interposed between the two wafers which are stacked. The projections are independent from one another and absorb mechanical shock applied to the wafers.

[0013] In accordance with one aspect of the present invention, the film has a dissipative layer and an insulating layer,

with the dissipative layer of the film having a surface resistance of between 1×10^{4}-1×10^{11} ohms.

[0014] In accordance with another aspect of the present invention, the insulating layer of the film is in contact with a circuit side of one of the adjacent wafers.

[0015] In accordance with still another aspect of the present invention, the wafers comprise bump pads, with the film contacting the bump pads of at least one of the wafers.

[0016] In accordance with still another aspect of the present invention, the film projections comprise bosses.

[0017] The present invention also provides a system for providing protection to integrated circuit wafers. A container has an interior space for receiving the wafers. At least two of the wafers are stacked inside of the interior space. The film has a pattern of projections extending from the film, with the film being interposed between the two wafers. The projections are independent from one another and absorb mechanical shock applied to the wafers.

[0018] In accordance with another aspect of the present invention, the film has a dissipative layer and an insulating layer, with the dissipative layer of the film having a surface resistance of between 1×10^{4}-1×10^{11} ohms.

[0019] In accordance with another aspect of the present invention, the insulating layer of the film is in contact with a circuit side of one of the adjacent wafers.

[0020] In accordance with another aspect of the present invention, the wafers comprises bump pads, with the film contacting the bump pads of at least one of the wafers.

[0021] In accordance with still another aspect of the present invention, the film projections comprise bosses.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] **FIG. 1** is an exploded isometric view of a shipping container showing wafers in a coin-stacked configuration, with the separator of the present invention, in accordance with a preferred embodiment.

[0023] **FIG. 2** is a cross-sectional view taken through lines II-II of **FIG. 1**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0024] This invention specifies an interleaf or separator especially designed for the purpose of separating and simultaneously protecting the thin IC wafers and/or wafers having bump bond pads from sudden damage caused by shock energy generally perpetuated by a sudden impact during shipment phases or by stresses caused by mishandling during packaging process prior to shipment phases. Unlike thin wafers and wafers having bump pads, regular IC wafers are more difficult to damage because they are sufficiently thick in structure and have flat bond pads by which to withstand a resonance of shock/stress energy that might occur during handling, packaging and shipment phases. Wafers with thin substrates will easily break if exposed to shock/stress energy, and wafers with bump bond pads will become instruments to transfer shock/stress energy to the next wafer to cause breakage. The fact is, present day packaging methodology using containers with assigned cushions does not always address the adverse concerns of damaging wafers having thin substrates and/or wafers with bump bond pads during packaging and shipment processes. These adverse concerns can only be addressed with new added means to absorb excessive resonance of shock/stress energy coming from the container that cannot be absorbed by the assigned cushions. Excessive energy caused by sudden impact and not absorbed prior to reaching wafers can result in substrate damage. Accordingly, the interleaf invention is designed with a series of bumps. The interleafs are co-extruded from polymer resins having a matrix of either carbon or copper with a surface resistivity ranging from 10^{5} to 10^{11} to avoid ESD events. More specifically, the interleafs are designed to receive and absorb excessive shock/stress energy not absorbed by the cushions assigned to shipping containers. Essentially, these bumps are impressions elevated on one side of the separator and each has a given height with a given distance from each other, thus effecting a cushioning system. Accordingly, each separator having bumps has the unique feature to separate each and every wafer from each other while providing a cushioning system for each and every wafer within shipping container against shock/stress energy during handling, packaging and shipment phases.

[0025] In **FIG. 1**, there is shown an exploded isometric view of an IC wafer shipping container **11**, having top and bottom covers **13**, **15**. Top and bottom cushions **17**, **19** are also provided inside of the top and bottom covers **13**, **15**.

[0026] IC wafers **21** are stacked between the cushions **17**, **19**. The wafers **21** are coin-stacked. As shown in **FIG. 2**, at least one side of each wafer has bump pads **23** thereon.

[0027] Between every two adjacent wafers is a separator **25**. The separators **25** prevent the wafers **21** from contacting each other.

[0028] The separator **23** of the present invention is cushioned to prevent damage, both shock and chemical, to IC wafers having bump pads. The separators are made of relatively AMC free plastic films that provide wafers with protection from stress and/or shock energy in the same resilient manner as those separators that are made of foam. This invention has the means to establish protection from stress and/or shock energy that transfers damage to wafers while simultaneously preventing: (1) corrosive damage to bump pads caused by chemical depletion or outgassing and (2) ESD and EOS electrical damage caused by improper surface resistivity of $<10^{4}$ ohms and $>10^{11}$ ohms. More specifically, the means within this invention that enhances the quality of wafer separation during the shipping phase is a plurality of embossed bumps **27** or bosses. Each boss **27** specifically provides: (1) a cavity **31** that isolates bump pads from stress and/or shock energy that damages wafers and (2) a means to absorb stress and/or shock energy for those bump pads **23** that can transfer damage to wafers, which means is in the form of the void **33** or space between bosses. In other words, this invention provides IC wafers with bump pads (solder balls with height) a means to either absorb or isolate stress and/or shock energy that damages wafers.

[0029] Referring to the drawings, the separator **25** is embossed, not with lines, but with bosses **27** that serve as standoffs. In the preferred embodiment, these bosses are circular. However, the embossed bosses **27** can be any shape. The bosses are spaced together so as to provide support for the separator spanning between the bosses. Thus, the bosses

27 are independent of one another so that mechanical shock by one boss is not transmitted to other bosses.

[**0030**] This invention provides an even greater solution when cushioned copperleaf separators are chosen for packaging wafers within containers for shipment. Unlike no other, copperleafs are sacrificial in that they absorb ionic contaminants and become a cleaning machine that assures packaged wafers arrive at the customer's location in a pristine condition. Such separators **25** are impregnated with copper instead of carbon.

[**0031**] The separators **25** are made from a film. The film has two layers, namely a dissipative layer and an insulating (or insulative) layer. The dissipative layer is polyethylene with carbon (or copper); the carbon serves to dissipate electrical charges. The insulating layer is polyethylene, which is a low density type of polyethylene; however it is also believed that medium and high density polyethylenes will also be satisfactory. The dissipative layer has a sufficient amount of carbon therein so that the surface resistance of the dissipative layer is between 1×10^{4} to 1×10^{11} ohms, as measured by the ESD association test method S11.11. The thickness of the insulating layer is 0.25 mils or less. If a thicker layer is used, then static charges may not be able to discharge effectively through the insulating layer. The thickness of the dissipative layer can vary. We have found that thicknesses of 3, 5 and 9 mils work well. However, other thicknesses, either smaller or greater, will also likely work well depending on the particular application. In the preferred embodiment, simultaneously a polyethylene with carbon and a polyethylene without carbon are extruded into separate layers. The two layers, being extruded together, are coupled together and form the film. The film can likely be made by other processes, such as laminating and coating. Preferably, the embossing is done from the insulating layer to the dissipative layer.

[**0032**] The film is described in our earlier U.S. Pat. No. 6,286,684, the disclosures of which is incorporated by reference. That patent teaches that the film is embossed with a grid to minimize the film separators from sticking to each other. The embossing is a grid and thus does not create independent bosses. Mechanical shock carried by one part of the grid will be transmitted to other parts of the grid.

[**0033**] The separator **25** is the film cut into a circular shape to match the shape of the IC wafer **21**. The separator **25** has a diameter that is slightly larger than the diameter of the particular IC wafers **21**. Each wafer **21** has a circuit side and an opposite or grind side. The bump pads **23** are located on the circuit side of the wafer. As shown in **FIG. 2**, separators **25** are placed between the wafers **21**. The insulating layer of the separator **25** is located in contact with the circuit side (the bump pad side) of the wafer. The dissipative layer is located in contact with the grind (or other) side of the next adjacent wafer. Thus, the insulating layer is interposed between the sensitive circuits and the dissipative layer. A stack of wafers and the separators is formed and placed into the container. The wafers contact only the separators and not other wafers.

[**0034**] The film bosses **27** serve as standoff areas. The embossing provides shock absorption. As stacked wafers are forced against each other, the resilient bosses provide cushioning and prevent wafer damage. The height of the bosses **27** from the film is preferably greater than the height of the wafer bump pads **23**. The greater the height of the bosses **27** relative to the height of the wafer bump pads **23**, the greater the spacing between the bosses.

[**0035**] The film being flexible, the bosses **27** are likewise flexible. Thus, the bosses provide a resiliency that allows the absorption of shock.

[**0036**] The bump pads **23** located adjacent to a void **31** caused by a boss are not in contact with any solid object. Thus, during a mechanical shock, these bump pads are physically isolated from contacting any object. The bump pads that are between bosses are in contact with the separator **25**, but these portions of the separator are backed by voids **33**. Thus, the bosses will flex under mechanical shock and the bump pads and separator will move in and out of the voids.

[**0037**] With the film of the present invention, static sensitive articles, such as integrated circuits, are protected from static discharge. The dissipative layer is made dissipative by the presence of carbon in the polymer. The dissipative layer presents a high resistance path to ground. Any static charge which accumulates on an adjacent article dissipates into the dissipative layer. Because the resistance of the dissipative layer is between 1×10^{4} to 1×10^{11} ohms, the charge dissipates in a controlled manner so as not to damage the article.

[**0038**] The insulating layer protects the article from the carbon. If the article was in direct contact with the dissipative layer, then carbon particles can be sloughed off and remain in contact with the articles. Having such dissipative particles in contact with sensitive articles, such as integrated circuits, is an undesirable contamination. The insulating layer prevents this sloughing of carbon (or other dissipative) particles onto the wafer.

[**0039**] Yet, the insulating layer is configured so as to allow static discharges to pass therethrough. Thus, the insulating layer does not interfere with the electrostatic discharge capabilities of the dissipative layer. The insulating layer, which is a polymer, has myriad microscopic channels therethrough, which channels can serve as paths for static discharges. Polymers typically have some porosity which is a function of the type of polymer, the thickness of the polymer and the particular material which is able to penetrate the polymer. An example of such porosity can be measured as the moisture vapor transmission rate (MVTR). Molecules of water vapor can penetrate some polymer layers. The penetration is possible because the polymer layer has a myriad of microscopic paths for the vapor molecules to follow through the layer.

[**0040**] Furthermore, the possibility of contaminating the wafers **21** by the separators **25** is minimized by the bosses **27**. The bosses **27** minimize physical contact between the separator **25** and the wafer **21**. Much of the wafer surface will not be in contact with the separator, instead being located either in the void **31** inside of the bosses **27** or in the spaces **33** between the bosses. The separators **25** can be oriented as shown in **FIG. 2**, wherein the surface area contact between the separator and the wafer is minimized on the side of the wafer opposite the bump pads, or the separators can be oriented in a reverse manner, wherein the surface area contact between a separator and a wafer is minimized on the bump pad side of the wafer.

[0041] The foregoing disclosure and showings made in the drawings are merely illustrative of the principles of this invention and are not to be interpreted in a limiting sense.

1. A packaging configuration for integrated circuit wafers, comprising:

a) at least two integrated circuit wafers;

b) a film having a pattern of projections extending from the film, the projections being independent from one another, the film being interposed between the two wafers which are stacked, the projections absorbing mechanical shock applied to wafers.

2. The packaging configuration of claim 1 wherein the film has a dissipative layer and an insulating layer, the dissipative layer of the film has a surface resistance of between 1×10^{4}-1×10^{11} ohms.

3. The packaging configuration of claim 2 wherein the insulating layer of the film is in contact with a circuit side of one of the adjacent wafers.

4. The packaging configuration of claim 1 wherein the wafers comprise bump pads, with the film contacting the bump pads of at least one of the wafers.

5. The packaging system of claim 1 wherein the film projections comprise bosses.

6. A system for providing protection to integrated circuit wafers, comprising:

a) a container having an interior space for receiving the wafers;

b) at least two of the wafers stacked inside the interior space;

c) a film having a pattern of projections extending from the film, the projections being independent from one another, the film being interposed between the two wafers, the projections absorbing mechanical shock applied to wafers.

7. The system of claim 6 wherein the film has a dissipative layer and an insulating layer, the dissipative layer of the film has a surface resistance of between 1×10^{4}-1×10^{11} ohms.

8. The system of claim 7 wherein the insulating layer of the film is in contact with a circuit side of one of the adjacent wafers.

9. The system of claim 6 wherein the wafers comprise bump pads, with the film contacting the bump pads of at least one of the wafers.

10. The system of claim 6 wherein the film projections comprise bosses.

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