United States Patent

[11] **3,577,708**

[72] Inventors **John W. Drenning;**
Richard J. Bridges, Baltimore, Md.

[21] Appl. No. **732,615**
[22] Filed **May 28, 1968**
[45] Patented **May 4, 1971**

[73] Assignee **Koppers Company, Inc.**
Pittsburgh, Pa.

[54] **SPARK INTERVAL RESPONSIVE PRECIPITATOR VOLTAGE CONTROL**
28 Claims, 6 Drawing Figs.

[52] **U.S. Cl.** **55/105,** 55/139, 323/23
[51] **Int. Cl.** **B03c 3/66**
[50] **Field of Search** ..... 55/105, 139; 315/111; 323/23 (SCR), 66, 24

[56] **References Cited**

UNITED STATES PATENTS

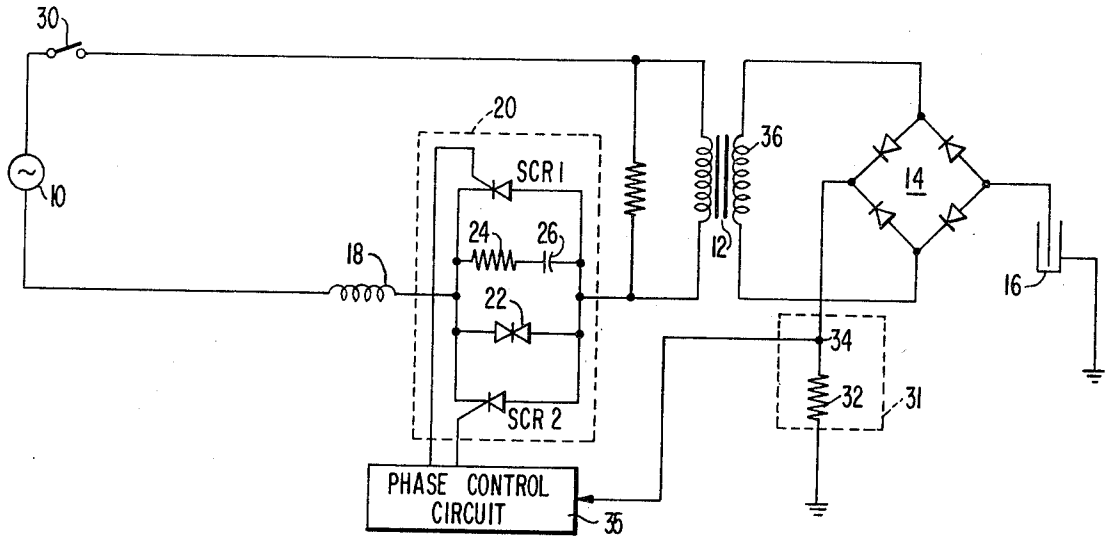
2,297,740	10/1942	Brown	323/46
2,841,239	7/1958	Hall et al.	55/105
2,961,577	11/1960	Thomas et al.	315/111
2,992,699	7/1961	Jarvinen	323/66X
3,089,082	5/1963	Little	55/105
3,166,705	1/1965	Brandt	55/105
3,363,402	1/1968	Taylor	55/105
3,374,609	3/1968	Kide	55/105

FOREIGN PATENTS

248,429	10/1963	Australia	55/105

Primary Examiner—Dennis E. Talbert, Jr.
Attorney—Burns, Doane, Swecker and Mathis

ABSTRACT: A method and digital circuit for modifying the voltage applied to the electrodes of a precipitator in accord with the elapsed time interval between the presently detected spark and the spark immediately preceding. Four predetermined time intervals are established by astable multivibrators each set by each detection of a spark in the precipitator. The outputs of the multivibrators enable gates to control the application of the next successive spark responsive pulse to a reversible digital counter which controls precipitator voltage. The counter is periodically advanced by clock pulses if the time interval between the detection of the next subsequent sparks falls outside the three shorter of the predetermined time intervals. Advancement of the counter is inhibited if the next subsequent spark responsive pulses occur within the second longest of the predetermined time intervals and the counter is respectively reversed one and two steps if the next subsequent spark responsive pulse occurs within the third longest or shortest of the predetermined time intervals.



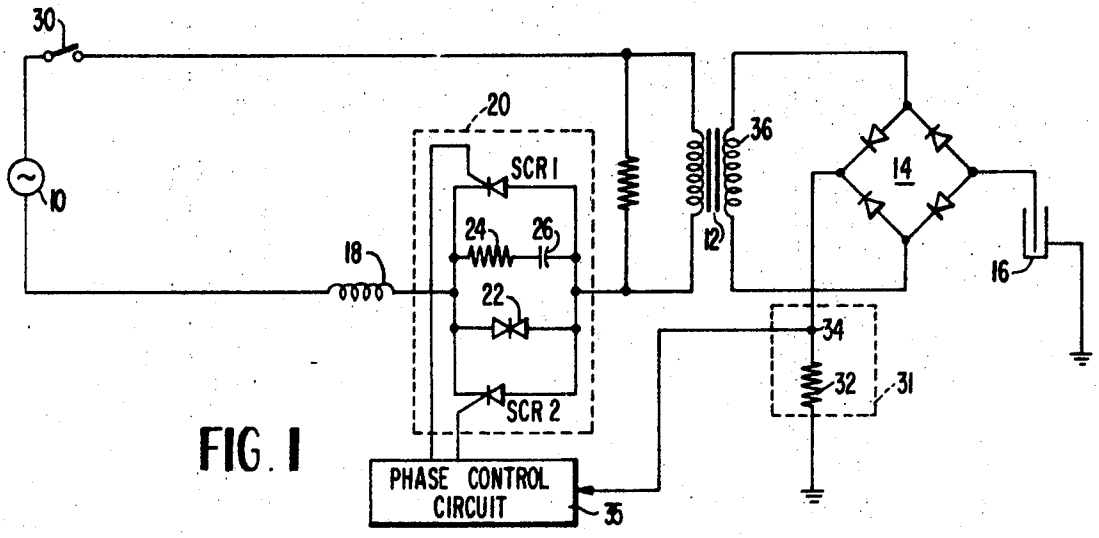


FIG. 1

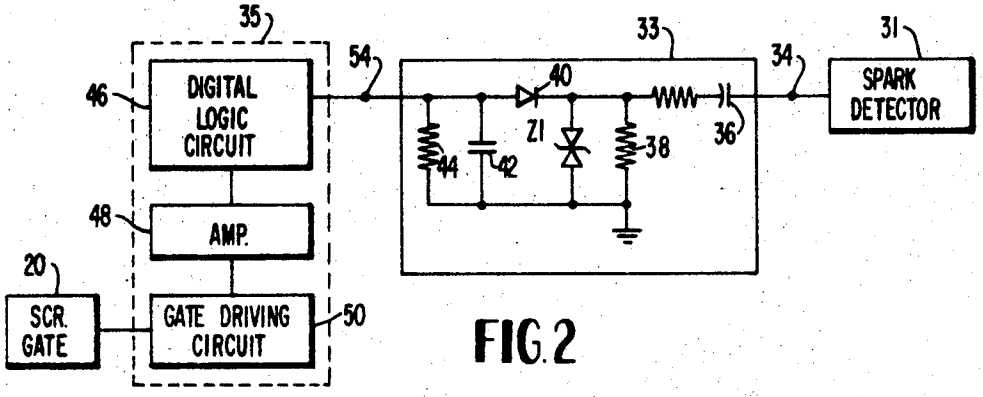


FIG. 2

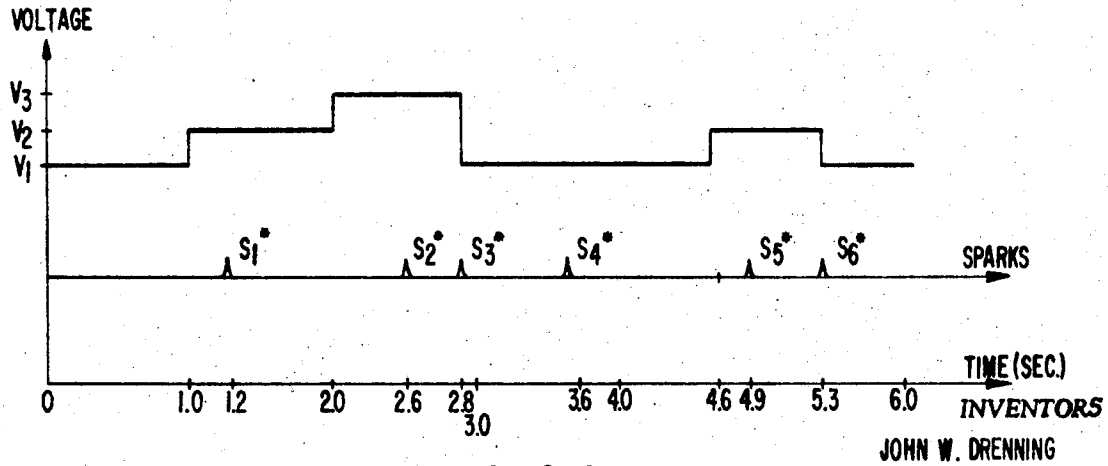


FIG. 6

INVENTORS
JOHN W. DRENNING
RICHARD J. BRIDGES

BY
Burns, Doane, Benedict, Swecker & Mathis
ATTORNEYS

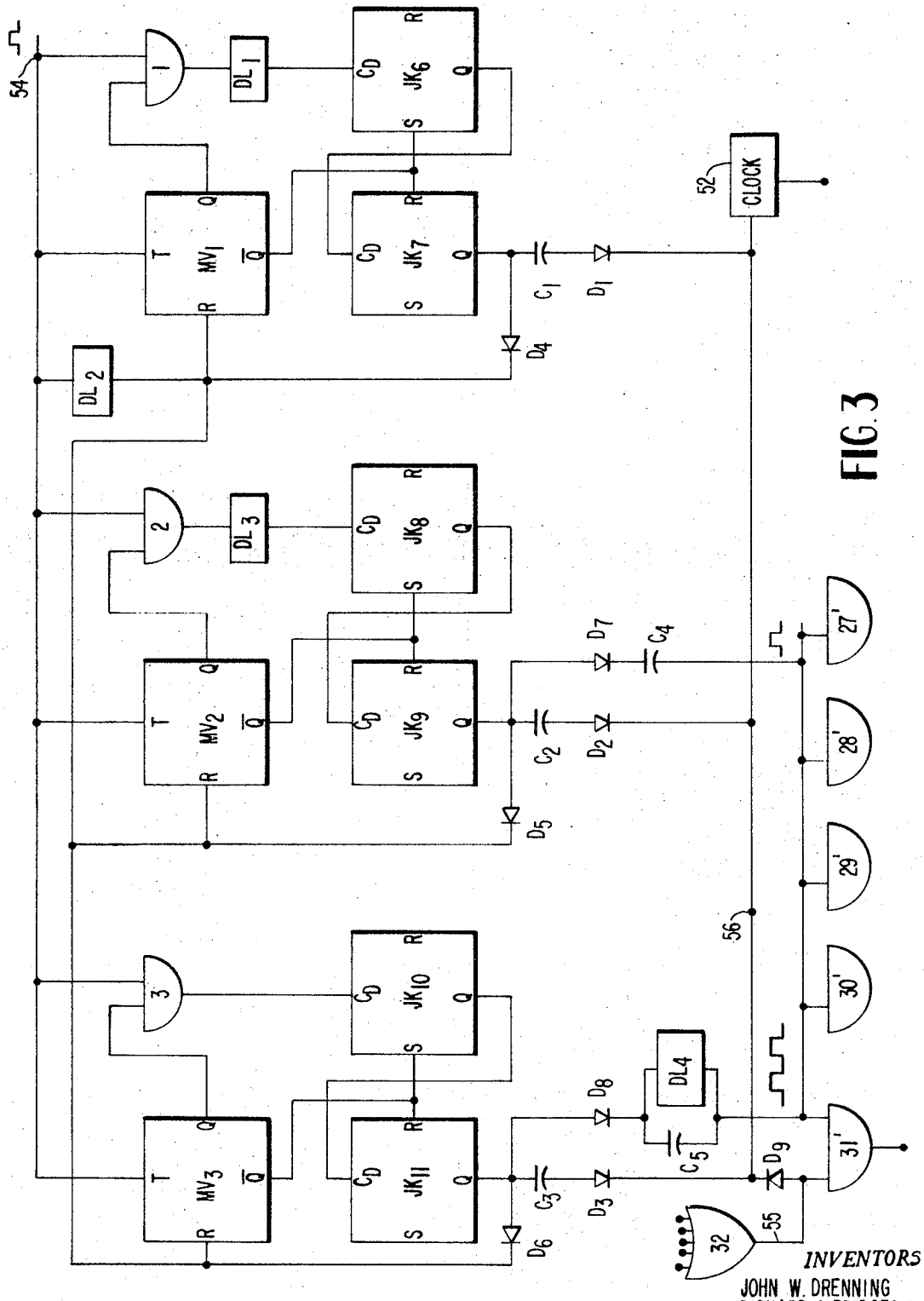


FIG. 3

INVENTORS
JOHN W. DRENNING
RICHARD J. BRIDGES

BY

Burns, Doane, Benedict, Swecker & Mathis
ATTORNEYS

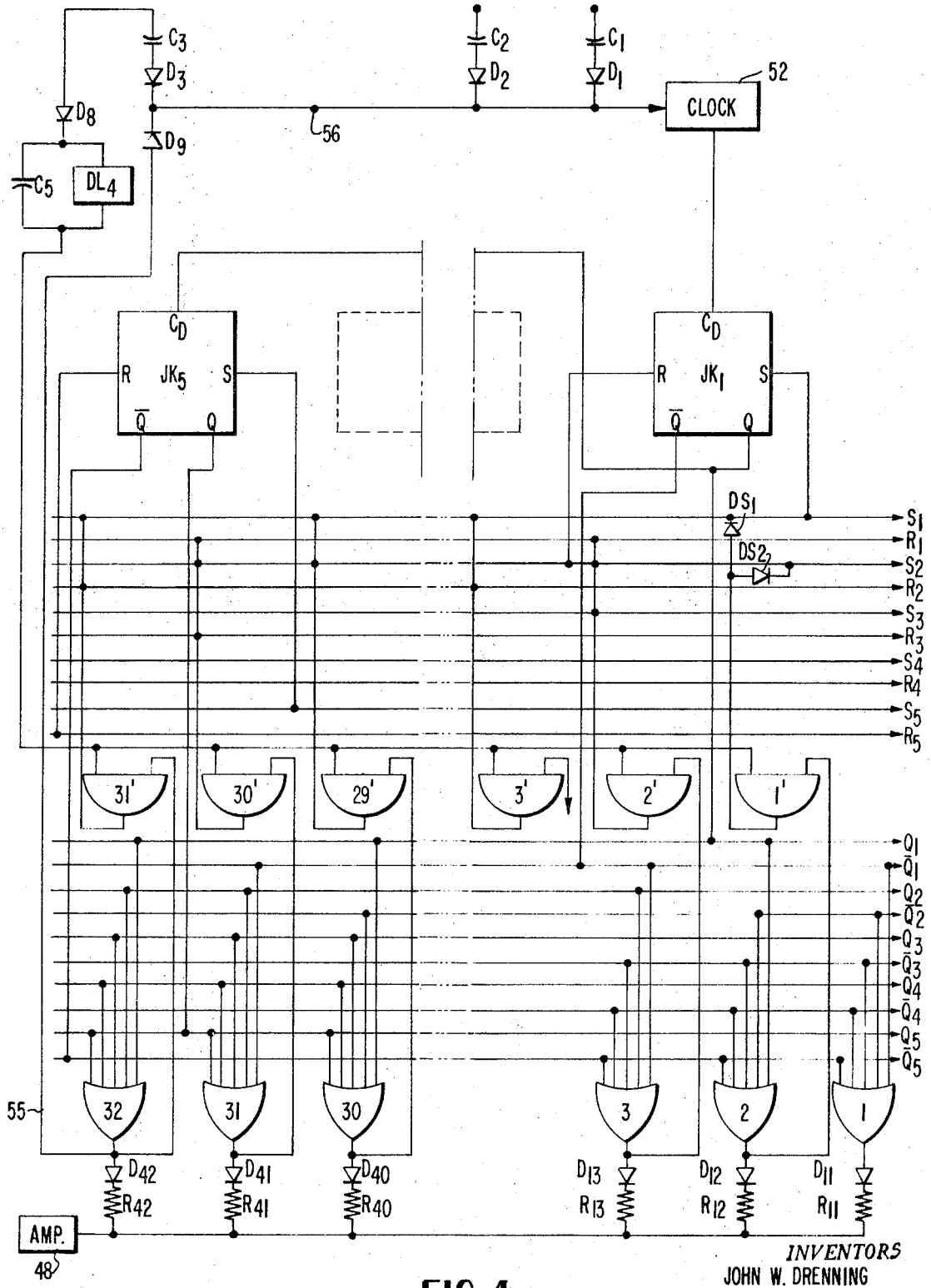


FIG. 4

INVENTORS
JOHN W. DRENNING
RICHARD J. BRIDGES

BY

Burns, Doane, Benedict, Swecker & Mathis
ATTORNEYS

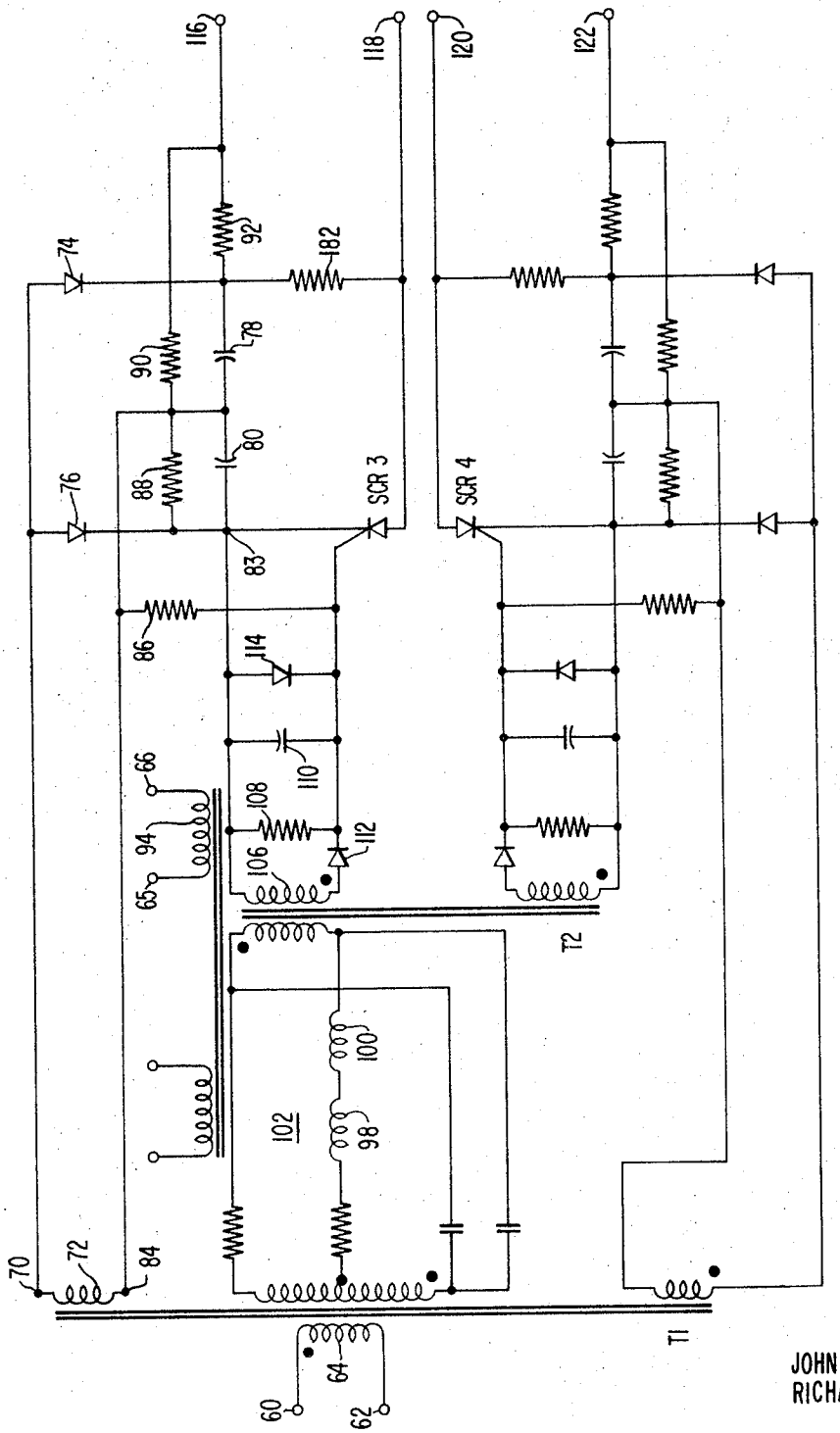


FIG. 5

INVENTORS
JOHN W. DRENNING
RICHARD J. BRIDGES

BY
Burns, Doane, Benedict, Swecker & Mathis
ATTORNEYS

SPARK INTERVAL RESPONSIVE PRECIPITATOR VOLTAGE CONTROL

BACKGROUND OF THE INVENTION

The automatic control of the level of the voltage applied to the electrodes of an electrostatic precipitator has long been a source of concern in the art. In any such system it is desirable to maintain the direct current voltage on the precipitator electrodes at as high a level as is possible consistent with the avoidance of excessive current drain due to arcing or sparking.

Prior art systems have generally utilized gating means such as thyratrons or silicon controlled rectifiers to control the AC current applied to the high voltage transformer and rectifier which apply voltage to the precipitator electrodes. As is well known, such gating means are responsive to the relative phase of a control signal with respect to the AC source. The control of the relative phase of the control signal is conventionally accomplished by the use of a saturable core reactor or the like to which an analog voltage adjustment signal is applied.

One analog adjustment signal, as shown in the prior art systems, is responsive to the rate of sparking in the precipitator over a prolonged period of time. Hence, adjustment of the voltage in fact applied to the precipitator is not immediately responsive to the conditions which actually exist in the precipitator at the time the condition is manifested by a spark. Such adjustments in precipitator voltage are consequently often made after the termination of the condition in the precipitator which required the adjustment and which may thus compound overshooting of the system with an attendant loss in overall collection efficiency.

Other prior art systems reduce precipitator voltage a preset amount for each spark. These may unnecessarily reduce the precipitator voltage, particularly when a spark occurs a relatively long interval after the preceding spark.

In many precipitator applications, a substantial portion of sparks occur in bursts where the initial spark is immediately followed by several others at an interval of one, or a few, half cycles of the source frequency (if full wave energization is used) or cycles thereof (with half wave rectification). This is particularly prevalent with salt cake and basic oxygen furnace applications. Such closely spaced sparks are undesirable because they reduce collection efficiency and cause an undue reduction in precipitator voltage. The present invention is directed to reducing spark bursts through reduction of the precipitator voltage in an amount related to the elapsed time interval between the detection of any spark and the detection of the immediately preceding spark.

It is accordingly a primary object of the present invention to provide a novel automatic control for an electrostatic precipitator in which the deficiencies of the prior art control systems are remedied by making the precipitator voltage more immediately responsive to conditions in the precipitator. This is accomplished by developing a control signal related to the elapsed time interval between the occurrence of immediately successive sparks in the precipitator.

Another object of the present invention is to provide novel means for initiating a predetermined program of precipitator voltage adjustment based solely upon the elapsed time interval between the currently detected spark and the detection of the immediately preceding spark.

Still another object of the present invention is to provide a novel method and digital circuit for precipitator voltage control which is normally operative to raise the operating voltage level in discrete steps in the absence of the detection of successive sparks in the precipitator within a predetermined time interval, and to inhibit the normal increase and to effect a reduction in the level of operating voltage based solely upon the elapsed time interval between successive sparks.

Yet another object is to provide a novel method and circuit for forestalling spark bursts in the precipitator by effecting a reduction in precipitator voltage which varies with the elapsed time interval since the detection of the preceding spark, a second closely spaced spark effectively operating to reduce the operating voltage below the level at which the previous spark occurred.

These and other objects and advantages of the present invention will become more fully apparent from the appended claims and from the following detailed description when read in conjunction with the drawings.

THE DRAWINGS

FIG. **1** is a schematic diagram illustrating the power circuit of the precipitator and the phase control circuit in block form;

FIG. **2** is a functional block diagram of the phase control circuit of FIG. **1**;

FIGS. **3** and **4** together comprise a schematic diagram of the digital logic circuit of FIG. **2**;

FIG. **5** is a schematic diagram of the SCR gate driving circuit of FIG. **2**; and

FIG. **6** is a graph showing the change in precipitator voltage level in response to sparking in the precipitator.

THE OVERALL SYSTEM

Referring now to the drawings, FIG. **1** illustrates the basic power circuit in which an alternating current from a 440 volt, single phase, 60 Hertz source **10** is converted in a high voltage transformer **12** and diode bridge rectifier **14** to a high voltage, direct current which is applied to the electrodes of precipitator **16**. Connected in the line between the AC source **10** and the primary winding **17** of transformer **12** is a surge limiting coil **18** and an SCR gating network **20**.

Gating network **20** includes a pair of silicon controlled rectifiers SCR1 and SCR2 connected in parallel. As is well known, the operation of the SCRs allows proportional control based on the conduction angle thereof as determined by the phase of the signal applied to the trigger electrodes.

Also paralleling SCR1 and SCR2 is a volt trap **22** having a lower rating than the rating of the silicon controlled rectifiers SCR1 and SCR2 to provide protection for the excessive transients which occasionally occur due to the highly transient nature of the load. All transients in excess of the rating of the volt trap **22** are dissipated in the form of heat.

In addition, an RC network which includes a series connected resistor **24** and a capacitor **26** is connected across SCR1 and SCR2. The function of the RC network is to limit the rate of change in the positive going voltage supplied to the anode of a PNPN device, the SCRs, which might otherwise permit the triggering of the SCRs upon initial closure of a circuit breaker **30** or the occurrence of some other excessive transient in the SCR circuitry.

The occurrence of a spark is detected in detector **31** by resistor **32** and the signal appearing at terminal **34** is fed to the phase control circuit **35** for control of the SCR triggering signal. The outputs of phase control circuit **35** are applied to the trigger electrodes of SCR1 and SCR2 to control the conduction angle by shifting the point at which conduction commences relative to the waveforms of the voltage signal applied across the anode and cathode junction. The voltage applied to the precipitator is thus subject to control by the occurrence of sparking in the precipitator.

The occurrence of a spark in the precipitator generates a damped high frequency oscillation of approximately 15 microseconds in duration. The amplitude of the oscillation is initially of the order of 5 to 10 times the normal current appearing in the secondary winding **36** of transformer **12**. The increased voltage drop across resistor **32** is thus responsive to a spark in the precipitator.

Referring now to FIG. **2**, the spark responsive signal appearing at the output of detector **31** as taken from terminal **34** of FIG. **1** is fed to a suitable voltage waveform shaper **33** to provide a signal on terminal **54** having a leading edge that will be used in logic circuit **35**. Shaper circuit **32** conventionally may include a capacitor **36** to block the 120 Hertz ripple in the unfiltered DC output of rectifier **14** in the precipitator **16** supply.

Capacitor **36** also prevents the direct current components of the signal taken from terminal **34** from entering the phase control circuit **35**. A Zener diode Z1 shunts resistor **38** to clip the tops of high amplitude incoming voltage peaks to prevent circuit component damage.

The signal is then passed through diode **40** to a pulse forming network comprising capacitor **42** and resistor **44** connected in parallel across the line. The signal applied to the phase control circuit **35** comprises positive pulses directly related in number and time of occurrence to sparking events in the precipitator **16**.

The shaped output signal on terminal **54** is fed to the digital logic circuit **46** of the present invention where a control signal is developed in a manner to be subsequently described. The control signal is amplified in a conventional DC amplifier **48** and fed to a gate driving circuit **50**. The output of the gate driving circuit **50** is used to control the firing angle of the SCR gate **20** of FIG. **1**.

THE DIGITAL LOGIC CIRCUIT

The preferred embodiment shown in FIGS. **3** and **4** is adapted to control the precipitator voltage in stepwise variations over a range of **32** levels extending between cutoff or zero voltage and the maximum level. In the secondary circuit provided, the steps may be of equal value, such as typically 1500 volts, or the aggregate voltage range may be covered in steps of varying amounts. It may be more desirable, for instance, in a specific installation, to employ smaller voltage step variations at the upper part of the voltage range where precipitator sparking is more highly sensitive to voltage increase. While **32** levels are employed in the embodiment illustrated, more or fewer stages may be used, as desired.

As illustrated in FIG. **1**, the preferred embodiment of the invention contemplates use with controlled rectifiers as a variable impedance element or gate in the primary circuit of the high voltage transformer supply. In such a system, the SCR gate circuit **20** receives separate triggering pulses on each alternating current cycle of the desired phase to establish the desired voltage at the precipitator **16**. While load conditions on the precipitator customarily vary during use and thus produce electrical impedance variations which result in a range of operating voltages at any selected relative gate pulse phase, the following description will refer primarily to the operation of the precipitator under an assumed design load impedance. The variations from such a typical load impedance are fully understood by those familiar with the electrical precipitator voltage control art.

The control networks include an SCR gate driving circuit operable in dependency on a direct current control signal to supply gating pulses to the controlled rectifiers whose phase position varies substantially linearly with input current. In the specific system, the SCR conduction angles advance symmetrically for increasing control current applied to the gate driving circuit to increase the voltage applied to the precipitator. The system of the present invention is designed to supply this output. Other specific types of precipitator voltage control components could clearly be employed, particularly saturable reactors or series transformers, as are well known in the prior art. These components, however, produce a series impedance related to the direct current in the control circuit, and are not as well adapted to effect the full range voltage control which may be accomplished by the use of controlled rectifiers.

In the illustrative circuit of FIGS. **3** and **4** providing the 32-step control, five JK flip-flops, JK_1—JK_5, (see FIG. 4), are arranged in series as a binary counting circuit. The first flip-flop JK_1 is connected to receive the output pulses from clock **52**. The outputs of the flip-flops JK_1—JK_5 are connected to 32 separate five-input NOR gates **1**—**32** arranged so that only one of these gates supplies an output in any specific condition of the flip-flop counting sequence. Thus, as the count proceeds, successive NOR gates from **1** to **32** successively become individually active.

The counting network further includes control circuitry for inhibiting the operation of the clock **52** where it is desired to hold the count presently existing, and also to reduce the existing count in a single step in response to an input pulse. For this purpose, the NOR gates **1**—**32** are individually connected, except for the first below which the count should not be reduced, to 31 AND gates **1′** to **31′**. Thus, the existence of an output at one of the NOR gates **1**—**32** is indicative of the existing count and provides an enabling signal to its corresponding AND gate while simultaneously removing the enabling signal from the other AND gates. The countdown control pulse may therefore be applied simultaneously to all the AND gates but channeled by the sole conductive AND gate only to the appropriate input connections of the five JK flip-flops, JK_1—JK_5, to reduce the count in the manner desired.

In the circuit of FIG. **4**, the flip-flops are shown as JK_1 through JK_5, inclusive. The circuitry of these commercially available modules is well known in the art and supplies output voltage levels at terminals Q and $\overline{Q}$. These output signals are always opposite, e.g., when Q is a mark or logical ONE, the corresponding $\overline{Q}$ is a space or logical ZERO, and vice versa. Input terminal C_D receives a voltage level signal, and will change the state of the flip-flop upon receipt of change in voltage from terminal Q of the preceding flip-flop. Two additional terminals are provided, one an S or set terminal at which an input signal sets and holds the flip-flop so that the Q output is a ONE, and the other, an R or reset terminal at which an input signal resets the flip-flop so that the $\overline{Q}$ output is a ONE.

In the network shown in FIG. **4**, input terminal C_D of the first flip-flop JK_1 is connected to receive the periodic timing pulses from clock **52**. The five flip-flop circuits operate as a conventional five order binary counting circuit and the resultant output voltage levels at Q and $\overline{Q}$ for each of the flip-flops identify the condition of the counter.

These output signals are individually connected in a conventional manner to NOR gates **1**—**32**, as shown in FIG. **4** to produce an output signal on only one NOR gate as determined by the count in the counting circuit of flip-flops JK_1—JK_5. The connections are made as shown in the following table:

NOR gate	Q_1	$\overline{Q_1}$	Q_2	$\overline{Q_2}$	Q_3	$\overline{Q_3}$	Q_4	$\overline{Q_4}$	Q_5	$\overline{Q_5}$
1		X		X		X		X		X
2	X			X		X		X		X
3		X	X			X		X		X
4	X		X			X		X		X
5		X		X	X			X		X
6	X			X	X			X		X
7		X	X		X			X		X
8	X		X		X			X		X
9		X		X		X	X			X
10	X			X		X	X			X
11		X	X			X	X			X
12	X		X			X	X			X
13		X		X	X		X			X
14	X			X	X		X			X
15		X	X		X		X			X
16	X		X		X		X			X
17		X		X		X		X	X	
18	X			X		X		X	X	
19		X	X			X		X	X	
20	X		X			X		X	X	
21		X		X	X			X	X	
22	X			X	X			X	X	
23		X	X		X			X	X	
24	X		X		X			X	X	
25		X		X		X	X			X
26	X			X		X	X			X
27		X	X			X	X			X
28	X		X			X	X			X
29		X		X			X			X
30	X			X			X			X
31		X	X				X			X
32	X		X				X			X

NOR gate **1** is an inactive unit with respect to the AND gates **1′**—**31′**, since the count is never reduced below stage **1**. NOR gate **32**, in addition to its connection to AND gate **31′**, supplies an inhibit signal through diode D_9 to the clock **52** to prevent cycling the counter from maximum voltage corresponding to step **32** to minimum voltage corresponding to step **1**.

The circuits of the flip-flops JK_1—JK_5 are not shown in order to simplify the schematic. The circuits of the flip-flops

are entirely conventional and are well known in the art. The connections of AND gates 1′ through 31′ to leads S_1 through S_5 and R_1 through R_5, inclusive, are actually series diodes $Ds1$ and $Ds2$ poled as shown in connection with AND gate 1′. It will be understood that similar diodes (not shown) are employed at each connection of output of AND gates 2′ through 31′ to the leads connecting with the set S and reset R control inputs of flip-flops JK_1—JK_5. The interconnections between the respective flip-flop inputs S and R and the AND gates 1′—32′ are shown in the following table:

AND gates	S_1	R_1	S_2	R_2	S_3	R_3	S_4	R_4	S_5	R_5
1′	x		x							
2′		x	x		x					
3′	x			x						
4′		x		x	x		x			
5′	x		x							
6′		x	x			x				
7′	x			x						
8′		x		x		x	x		x	
9′	x		x							
10′		x	x							
11′	x			x						
12′		x		x	x			x		
13′	x		x							
14′		x	x			x				
15′	x			x						
16′		x		x		x		x	x	
17′	x		x							
18′		x	x		x					
19′	x			x						
20′		x		x	x		x			
21′	x		x							
22′		x	x			x				
23′	x			x						
24′		x		x		x	x			x
25′	x		x							
26′		x	x		x					
27′	x			x						
28′		x		x	x			x		
29′	x		x							
30′		x	x			x				
31′	x			x						

THE SPARK-RESPONSIVE NETWORK

The spark-responsive network of the present invention operates in dependency on a signal derived from each spark transient occurring in the precipitator **16**. Referring to FIG. **2**, the spark-responsive signal is applied from terminal **34** of the spark detector **31** via the pulse shaper **33** to terminal **54** of the digital logic circuit **46**. As shown in FIG. **3**, the pulse shaper **33** supplies a standardized pulse output having substantial magnitude and a duration on the order of 1 millisecond to terminal **54**. It is used to initiate operation of a plurality of monostable multivibrator timing circuits for determining the response of the voltage control system in dependency on the time intervals between sparks occurring in the precipitator.

As discussed above, the operating principles of the present control apply a normally increasing stepwise voltage to the precipitator at predetermined intervals which may be, for example, 1 second. This stepwise increasing voltage is accomplished by advancing the count of the counter network periodically in dependency on a pulse output supplied by the clock **52**. The clock **52** responsive programmed increase of the voltage on the precipitator **16** is not modified by sparks which occur at intervals longer than a preselected duration such as 1 second. The only exception is the attainment of the upper voltage limit reached at step **32** of the counter. Sparking will be sufficiently frequent under normal operation conditions so that the spark interval will be below the said preselected interval. Sparks at shorter intervals, falling for example within a predetermined range which may be 0.5 to 1 second, cause operation of the control network to maintain a constant voltage on the precipitator **16** by transmitting an inhibiting signal to the clock **52** so that a subsequent clock pulse output will not develop until the full clock timing period elapses. In consequence, the counter networks will not be stepped to the next higher voltage stage.

For sparks occurring with time intervals within a range, e.g. less than 0.5 seconds, the control system is programmed to reduce precipitator voltage by transmitting an inhibit signal preventing development of the clocking pulse on the subsequent pulse cycle as described while simultaneously transmitting a control pulse to the counter network to reduce the count one step.

The circuit shown in FIGS. **3** and **4** further includes an optional feature whereby a spark following the preceding spark event by less than a predetermined interval, 0.25 seconds for instance, effects a two-step reduction in the count existing on the counter network while simultaneously inhibiting development of the output pulse from the clock **52**. The voltage reduction in response to closely spaced sparks in the precipitator is thus double the reduction which normally occurs in response to sparks at slightly a greater spacing. This feature aids in preventing the occurrence of spark bursts in the precipitator **16**.

In describing the operation of the circuit shown in FIGS. **3** and **4**, it is assumed that the precipitator **16** is energized at the lowest level with NOR gate **1** in conduction. Monostable timing multivibrators MV_1, MV_2, MV_3, are inactive. The precipitator voltage is increased stepwise with time as the clock **52** sequences flip-flops JK_1—JK_5 periodically upwardly in the count.

In the circuit as shown, the timing multivibrators JK_1—JK_5 of FIG. **4** supply a ONE or positive logical output at their $\overline{Q}$ terminals. These control potentials are respectively connected to the S control inputs of flip-flops JK_6, JK_8, and JK_{10} of FIG. **3** locking them in their set condition and producing a positive logical ONE output at their Q terminals. The $\overline{Q}$ terminal outputs of the multivibrators MV_1—MV_3 also are connected to the respective R control terminals of flip-flops JK_7, JK_9, JK_{11} consequently locking them in their reset state with a ZERO output at their Q terminals.

As the voltage on the precipitator **16** is programmed to successively higher stages by operation of the clock, a short output pulse from the pulse shaper **33** of FIG. **2** is supplied to terminal **54** of FIG. **3** on the occurrence of a spark in the precipitator **16**. These pulses have a duration on the order of 1 millisecond. All three multivibrators MV_1—MV_3 are thrown instantly by this signal into their active timing states. Considering MV_3, its $\overline{Q}$ output terminal shifts from ONE to ZERO unlocking flip-flops JK_{10} and JK_{11}. Simultaneously, multivibrator MV_2 unlocks flip-flops JK_8 and JK_9 and multivibrator MV_1 unlocks flip-flops JK_6 and JK_7.

At the same time the Q outputs of the multivibrators MV_1—MV_3 shift from ZERO to ONE to supply an enabling input signal to AND gates 1″, 2″, and 3″. In this manner flip-flops JK_6, JK_8, and JK_{10} receive triggering inputs through AND gates 2″—3″ from the same signal which originated in the pulse shaper **33** and which triggered the monostable multivibrators MV_1—MV_3. Each of these flip-flops JK_6, JK_8, and JK_{10} shifts in response to this signal from the set to the reset state. The outputs at their Q terminals accordingly shift from ONE to ZERO. No change is effected in the outputs of flip-flops JK_7, JK_9, and JK_{11} which remain quiescent.

If no further spark occurs during the timing periods for any of the multivibrators MV_1—MV_3, they successively time out and resume their inactive state. Multivibrator MV_3 times out first to remove the ONE output at the Q terminal thereby disabling AND gate 3″. The shift from ZERO to ONE resets flip-flop JK_{10} and again locks flip-flops JK_{11} in the reset condition. JK_{11} is thus disabled and cannot respond to the resulting shift from ZERO to ONE at the Q terminal of flip-flop JK_{10} which occurs upon the application of the next spark responsive pulse to the C_D terminal.

As the monostable multivibrators MV_2 and then MV_1 successively time out, identical operations are performed with regard to respective flip-flops JK_8 and JK_9 and JK_6 and JK_7.

Thus, an isolated spark does not produce any interruption of the programmed stepwise increase in the voltage applied to the precipitator **16** under operation of the output from the clock **52**. As described above, the clock **52** will program the precipitator voltage to the highest level and will supply an out-

put signal at NOR gate 32 of FIG. 4. The output of NOR gate 32 is directly applied through diode D_9 to the clock 52 by lines 55 and 56 as an inhibiting signal to prevent further clock output.

If, however, a subsequent spark occurs during the timing period of any of the monostable multivibrators MV_1—MV_3, the voltage raise function of the clock 52 will be inhibited on the succeeding cycle, and, as will be hereinafter described, the voltage applied to the precipitator 16 may be reduced by the application of down-count pulses to the counter network.

The operation of the monostable multivibrators MV_1—MV_3 and flip-flops JK_6—JK_{11} on the occurrence of a spark-responsive signal delivered at terminal 54 by the pulse shaper 33 during the active multivibrator timing periods has been described. If a subsequent spark occurs during the timing period of any of the individual multivibrators, the periodic voltage raise operation effected by the clock 52 is interrupted, and, if the spark interval is sufficiently short, the voltage on the precipitator 16 will be immediately reduced. A double step reduction in precipitator voltage is produced if the succeeding spark occurs within the shortest of the predetermined timing periods of multivibrator MV_3. During this period, AND gate 3'' is conductive and the signal from the pulse shaper is applied to the C_D terminal of flip-flop JK_{10}. The spark signal is also passed by AND gates 1 and 2 as will be subsequently described.

With AND gate 3'' enabled, the second spark signal is applied to the C_D terminal of flip-flop JK_{10} and switches its output signal at the Q terminal from ZERO to ONE to cause a transition of flip-flop JK_{11} to the active state. The triggering of flip-flop JK_{11} instantaneously shifts the latter's output signal at the Q terminal from ZERO to ONE to supply an inhibit signal through condenser C_3 and diode D_3 to the clock 52. An inhibit signal on line 56 resets the timing period of the clock 52 to zero to insure that no subsequent up-count pulse will be applied to the flip-flop JK_1 for the full timing period of the clock, typically 1 second. A countdown pulse is simultaneously applied through diode D_8 and condenser C_5 to one input of each of the AND gates 1'—31'. The AND gate at that time enabled by the positive logic output signal of one of the NOR gates 2—32 will pass the countdown pulse through busses S_1— S_5 and R_1—R_5 to the flip-flops JK_1—JK_5 to reduce the count one stage and result in a corresponding reduction of one step on the voltage of the precipitator 16. This countdown pulse is immediately followed by a second pulse through delay line DL_4. This second pulse is programmed through the next adjacent lower AND gate 1'—31' in a like manner to effect a second voltage reduction step at the precipitator 16.

Returning to the flip-flops JK_{10} and JK_{11} associated with monostable multivibrator MV_3, of FIG. 3, the positive logical shift in the output signal at the Q terminal of flip-flop JK_{11} is applied through diode D_6 to the R terminals of the multivibrators MV_1—MV_3. This control potential switches MV_3 into its stable reset condition, removes the enabling signal from AND gate 3'', sets flip-flop JK_{10}, and holds flip-flop JK_{11} in its stable reset condition disabling its response to the output shift at the Q terminal of the flip-flop JK_{10} from ZERO to ONE.

Inasmuch as this control signal from the Q terminal of flip-flop JK_{11} is also applied to the reset control terminals R of multivibrator MV_2 and multivibrator MV_1, both multivibrators MV_1 and MV_2 are simultaneously reset with multivibrator MV_3. Flip-flops JK_8 and JK_6 will not yet have received the input signal from the pulse shaper 32 due to the delay effected by delay lines DL_3 and DL_1 respectively. Consequently, the positive shift from ZERO to ONE at the terminals $\overline{Q_1}$ and $\overline{Q_2}$ of monostable multivibrators MV_1 and MV_2 merely resume their function of locking the controlled flip-flops respectively in their reset and set conditions.

The shift from ZERO to ONE at output terminal Q of flip-flop JK_{11} is then applied through delay line DL_2 to the input bus from the pulse shaper 32. The delay of delay line DL_2 may be typically a few milliseconds. This delayed pulse is applied to the monostable multivibrators MV_1—MV_3 at their T terminals to set all three simultaneously into the active timing condition commencing anew their timing cycles.

Thus, the operation of the illustrated circuit in response to the occurrence of the spark within the timing period of monostable multivibrator MV_3 produces a two-step reduction of precipitator voltage by programming the counter and effects a reset of all of the multivibrators MV_1—MV_3 to reinitiate their timing periods in dependency on the same spark occurrence for which the voltage reduction was made.

For the purposes of explanation, we may then assume that the next spark fails to occur during the timing period of multivibrator MV_3 and that MV_3 thus times out. As explained above in connection with an isolated spark, the timing out of multivibrator MV_3 locks flip-flop JK_{10} in the set condition and simultaneously resumes holding flip-flop JK_{11} in the reset condition by the unit output signal supplied at its $\overline{Q}$ terminal. No further response in the network is thus produced.

The subsequent spark is assumed to supply an input signal at AND gate 2 after multivibrator MV_3 times out before multivibrator MV_2 times out at the end of its typical operating period of 0.5 seconds. After a slight delay effected by delay line DL_3, this input signal is applied to the C_D terminal of flip-flop JK_8 to shift the latter to its set condition. Setting flip-flop JK_8 causes the transition of the output signal at its Q terminal from ZERO to ONE. This signal shift is applied at the C_D terminal to shift flip-flop JK_9 to its active condition. As this occurs, the output signal at the terminal of flip-flop JK_9 shifts from ZERO to ONE and an inhibit signal is applied through condenser C_2 and diode D_2 to the clock 52 to reinitiate its timing period. The step-up pulse otherwise applied to the precipitator voltage control network is thus inhibited. Simultaneously, a single down-count signal is applied through diode D_7 and condenser C_4 and through the then active AND gate 1'—31< to effect a single step countdown and the accompanying reduction in precipitator voltage.

As previously described in connection with the operation of a shift in the condition of flip-flop JK_{11}, flip-flop JK_9 applies an immediate reset signal to the R terminal of monostable multivibrator MV_2 as well as the other monostable multivibrators MV_1 and MV_3. Multivibrator MV_1 has not responded to the present spark occurrence because delay line DL_1 effects a longer delay than delay line DL_3. Consequently, resetting multivibrator MV_1 applies a signal to the S terminal of flip-flop JK_6 and to the reset terminal R of flip-flop JK_{11}. Then, as previously described, delay line DL_2 applies a triggering signal to the inputs of all three multivibrators MV_1—MV_3 to reinitiate a timing period subsequent to the spark event under discussion.

Again, for the purposes of explanation, it will be assumed that the next occuring spark does not take place until multivibrators MV_3 and MV_2 have both timed out only leaving multivibrator MV_1 active. Under these circumstances, only AND gate 1'' is conductive and the spark signal from the pulse shaper 33 is slightly delayed by delay line DL_1 and applied to the control terminal C_D of flip-flop JK_6 to shift the latter from its reset to its set condition. This shift effects transition of the output signal at the Q terminal of flip-flop JK_6 from ZERO to ONE. As previously described in connection with the other portions of this network, this switches flip-flop JK_7 from its reset to its set condition and effects a transition from ZERO to ONE at its Q terminal. The Q terminal pulse of flip-flop JK is applied through condenser C_1 and diode D_1 to the clock 52 to reset the latter's timing period. Because the spark occurred with a predetermined time interval following the preceding spark, typically between 0.5 and 1 second, no voltage reduction is applied to the precipitator and the system operates simply to maintain the precipitator voltage temporarily until it is subsequently raised another step by operation of the clock 52 at the end of its typically 1 second timing period.

Thus, successive sparks occuring in the precipitator outside the largest predetermined interval duration allow precipitator voltage to increase and sparks occurring within a lesser predetermined interval duration are effective to reduce precipitator voltage. Sparks occurring at an interval duration falling within a range of interval durations less than the first interval duration but greater than the second interval duration are effective to maintain existing precipitator voltage.

Referring again to FIGS. 2 and 4, the output of the digital logic circuit 46 is amplified in a conventional DC amplifier 48 and applied to the gate driving circuit 50 for effecting control of the firing angle of the SCR gate 20 of FIG. 1. It will be understood that suitable ground returns are included for the components of FIGS. 3 and 4 of the system to develop the desired input signals to amplifier 48.

Depending on the state of the connector, only one of the NOR gates 1—32 is conductive at any specific setting. The output signal is determined by the individual value of the respective resistors R11—R42 feeding the amplifier 48 from its connected diode D11—D42.

SCR GATE DRIVING CIRCUIT

The operation of the SCR gate driving circuit 50 of FIG. 2 may more easily be explained with reference to FIG. 5. The unit is available commercially from the Sprague Electric Company, Special Components Division, North Adams, Massachusetts under the name VecTrol VS6732.

The DC input to the SCR gate driving circuit 50 determines the phase shift of the triggering pulses SCR1 and SCR2 with respect to the AC source 10. The output signal of the amplifier 48 of FIG. 2 is applied to the terminals 65 and 66 in the circuit of FIG. 5. Line voltage from source 10 is applied to the primary winding 64 of the transformer T1. When the instantaneous polarity of terminal 60 is positive, the potential at terminal 70 of the secondary winding 72 is also positive. This signal is passed through the diodes 74 and 76 to charge the capacitors 78 and 80 respectively to the same potential. This same positive signal is applied through resistor 182 to the anode and directly from terminal 83 to the cathode of SCR3. Since the cathode of SCR3 is maintained at the same potential as the anode, SCR3 is prevented from firing and the conduction angle of SCR1 remains at zero degrees.

Concurrently with the above, the corresponding negative potential at terminal 81 of the secondary winding 72 is fed through resistor 86 to the trigger electrode of SCR3. The application of a negative potential to the trigger electrode of SCR3 prevents the firing thereof in response to any transients which may be induced in the circuit. Diodes 74 and 76 prevent the capacitors 78 and 80 from discharging when the polarity of the voltage of winding 72 is reversed.

During the negative cycle, however, capacitor 80 begins to discharge through resistor 88 and capacitor 78 through resistors 90 and 92. The RC time constant of capacitor 80 is much smaller than that of capacitor 78. The discharging of capacitor 80 prior to the discharging of capacitor 78 allows the voltage on the anode of SCR3 to become positive with respect to the voltage applied to the cathode thereof. SCR3 is thus enabled and will conduct upon the occurrence of a pulse on the trigger electrode.

The negative bias on the trigger electrode of SCR3 is removed upon the reversal on polarity. The voltage appearing at terminals 65 and 66 of transformer T2 is taken from the amplifier 48 of FIG. 2. The inductance of the windings 98 and 100 of a saturable reactor 102 is reduced with an increase in the current in the input winding 94. The phase of the signal generated across winding 106 of transformer T2 is thus shifted when the saturable reactor 102 fires advancing the firing angle of SCR3. Resistor 108 and a capacitor 110 give the SCR3 triggering pulse a fast rise time and diode 112 blocks a reversal of current in the winding 106 of transformer T2. Diode 114 is used to prevent the cathode of SCR3 from becoming positive with respect to the trigger electrode.

The operation of the lower half of the circuit of FIG. 5 and the firing of SCR4 is identical to the upper half as explained supra and will not be further discussed, the firing of SCR4 occurring 180° later in all cases.

The triggering of SCR3 and SCR4 controls the voltage across terminals 116 and 118 and terminals 120 and 122, respectively. These terminals are connected to the trigger electrodes of SCR1 and SCR2 in the gating circuitry 20 of FIG. 1 to control the voltage of precipitator 16.

PRECIPITATOR VOLTAGE RESPONSE

The response of the level of the voltage applied to the precipitator 16 to the occurrence of sparks therein may be more easily summarized in conjunction with FIG. 6 and the three timing periods previously discussed, MV_3 at 0.25 seconds, MV_2 at 0.50 seconds and MV_1 at 1.0 seconds.

The illustration of FIG. 6 assumes a voltage of V_1 at time zero. Since the first spark S_1= occurs more than 1 second after time zero, the voltage of the precipitator is raised one step to level V_2 at time 1.0. Inasmuch as the spark S_1* does not fall within the 1.0 time interval previously begun, the generation of a timing pulse from clock 52 is not inhibited and the precipitator voltage is further increased a second step to level V_2 at time 2.0.

The occurrence of a spark S_2* 1.4 seconds after the occurrence of spark S_1* again does not interrupt the timing period of the clock 52. The 1.0 second timing period thus continues to run from time 2.0. The occurrence of the spark S_3* 0.2 seconds after the occurrence of the spark S_2* is still prior to the normal occurrence of the normal clock 52 responsive increase at time 3.0. The occurrence of the second spark S_3* within 0.2 seconds of the first spark S_2* is prior to the timing out of multivibrator MV_3 and not only resets the timing cycle of clock 52, but results in a two-step reduction of the precipitator voltage to level V_1.

A spark S_4* occurring at time 3.6 falls within the 0.5 to 1 second multivibrator timing interval begun by spark S_3* and thus finds only multivibrator MV_1 in its enabled state, multivibrators MV_3 and MV_2 having respectively timed out at 0.25 and 0.5 seconds. The result is the inhibiting of the counter advancing output of the clock 52 and thus restarting of the 1.0 record clock timing cycle but no change in the voltage of the precipitator.

The occurrence of a spark S_5* more than 1.0 after the resetting of the clock 52 timing period by the spark S_4* finds all of the multivibrators MV_1—MV_3 disabled and thus does not inhibit the clock 52. Clock 52 thus causes the precipitator voltage to be raised to level V_2 at time 4.6, 1.0 second after the occurrence of the spark S_4*.

Spark S_6* is illustrated as occurring at time 5.5 and thus within the 1.0 second clocking interval begun by spark S_4* at time 4.6. Since the spark S_6* also occurs within the period 0.25 to 0.5 seconds after the occurrence of spark S_5*, both multivibrators MV_1 and MV_2 are found enabled by the spark-responsive signal and a one step reduction in precipitator voltage to level V_1 and a resetting of the timing period of clock 52 results.

SCOPE OF THE INVENTION

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The disclosed spark control program in which precipitator voltage is controlled as a function of the elapsed time interval between the detection of immediately successive sparks in the precipitator may be varied as to the number of control levels, the time intervals, and the magnitude of the change in the operating voltage of the precipitator. The present embodiment is therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing detailed description, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

What is claimed and desired to be secured by Letters Patent is:

We claim:

1. A digital control for an electrostatic precipitator comprising:

a detector for supplying a signal in response to the occurrence of a spark in the precipitator;

a source of clock pulses;

a precipitator voltage controlling digital counter connected to said source for stepwise periodic advancement by the clock pulses from said source; and

circuit means connected to said detector for inhibiting the advancement of said counter by disabling the generation of one of the clock pulses by said source upon the detection of successive sparks within a predetermined time interval.

2. The control of claims 1 wherein said counter is reversible and wherein said circuit means includes means for reducing the count in said counter upon the detection of successive sparks within a second predetermined time interval less than said first mentioned predetermined time interval.

3. The control of claim 2 wherein said circuit means includes means for additionally reducing the count in said counter upon the detection of successive sparks within a third predetermined time interval less than said second predetermined interval.

4. An automatic energization control for an electrical precipitator supplied with current by a high voltage transformer and rectifier from a source of alternating current comprising:

gating means connected in the line between said source and said transformer for selectively supplying power from said source to said transformer;

means for generating a signal for controlling the operation of said gating means; and

circuit means substantially independent of the phase of said alternating current source and responsive to the time interval between immediately successive sparks in said precipitator for modifying the phase of said generated signal with respect to the phase of said source.

5. The control of claim 4 wherein said circuit means includes means for advancing the phase of said generated signal with respect to the phase of said source in the absence of a spark within a predetermined time interval.

6. The control of claim 5 wherein said circuit means includes means for inhibiting the advancement of the phase of said generated signal with respect to the phase of said source in response to the occurrence of a spark within a second predetermined time interval.

7. The control of claim 6 wherein said circuit means includes means for retarding the phase of said generated signal with respect to the phase of said source in response to the occurrence of a spark within a third predetermined time interval.

8. The control of claim 7 wherein said circuit means includes means for additionally retarding the phase of said generated signal with respect to the phase of said source in response to the occurrence of a spark within a fourth predetermined time interval.

9. The control of claim 8 wherein each of said predetermined time intervals are concurrently initiated and includes each of the subsequently mentioned ones of said predetermined time intervals.

10. An automatic energization control for an electrical precipitator supplied with high voltage direct current by a high voltage transformer and rectifier from a source of alternating current comprising:

gating means connected in the line between said source and said transformer for selectively supplying power from said source to said transformer;

means for generating a signal for controlling the operation of said gating means; and

circuit means responsive to the time interval between immediately successive sparks in said precipitator for modifying the phase of said generated signal with respect to the phase of said source,

said circuit means including:

means for stepwise advancing the phase of said generated signal with respect to the phase of said source in the absence of a spark within a predetermined time interval,

a counter connected to said signal generating means for controlling the relative phase of said generated signal,

an AND gate connected to receive spark-responsive signals on one input terminal thereof,

timing means for enabling said AND gate for a predetermined time interval commencing with the detection of each spark in the precipitator,

means for generating periodic pulses for advancing said counter, and

a bistable circuit connected to the output terminal of said AND gate for inhibiting the generation of said periodic pulses when in a set condition, said bistable circuit being placed in said set condition by the passage of a spark responsive signal through said enabled AND gate.

11. An electrostatic precipitator comprising:

a source of alternating current;

a transformer;

gating means connecting said source to said transformer;

a plurality of precipitator electrodes;

a detector of sparks between said electrodes;

rectifier means connecting said transformer to one of said electrodes;

a digital counter connected to said gating means for controlling the current through said gating means; and

circuit means connected to said detector and said counter for modifying the output of said counter in accord with the elapsed time interval between immediately successive sparks between said electrodes, said circuit means including:

an AND gate connected to said detector,

timing means connected to said detector for enabling said AND gate for a predetermined time interval following the detection of a spark,

a source of pulses connected to said counter for periodically advancing the output thereof, and

a bistable circuit for inhibiting said source, said circuit being connected to the output of said AND gate.

12. The precipitator of claim 11 wherein said counter is reversible and includes:

a second AND gate having one input connected to said bistable circuit;

second circuit means connected to receive the output of said second AND gate and said source;

a NOR gate connected to receive the output of said second circuit means and to supply an input to said gating means, said NOR gate being connected to the other input of said second AND gate.

13. The control of claim 10 wherein said counter is reversible and wherein said circuit means further includes:

a second AND gate connected to receive a spark-responsive signal to one input terminal thereof;

second timing means for enabling said second AND gate for a predetermined time interval less than said first predetermined time interval and commencing concurrently therewith; and

a second bistable circuit connected to the output of said second AND gate for applying a count down pulse to said counter when in a set condition, said second bistable circuit being placed in said set condition by the passage of a spark-responsive signal through said enabled second AND gate.

14. The control of claim 13 wherein said circuit means includes:

a third AND gate connected to receive spark-responsive signals on one input terminal thereof;

third timing means for enabling said third AND gate for a predetermined time interval less than said second predetermined time interval and commencing concurrently therewith; and

a third bistable circuit connected to the output terminal of said third AND gate for applying a plurality of count down pulses to said counter when in a set condition, said bistable circuit being placed in said set condition by the passage of a spark-responsive signal through said enabled third AND gate.

15. An electrostatic precipitator voltage control comprising:

timing means for determining whether the time interval between successive precipitator sparks is less than a first predetermined value, greater than said first predetermined value but less than a second higher predetermined value, or greater than said second predetermined value; and

precipitator voltage modifying means responsive to said timing means for increasing precipitator voltage responsive to a determination that the time interval between said sparks is greater than a said second predetermined value, decreasing precipitator voltage responsive to a determination that the time interval between said sparks is less than said first predetermined lower value, and maintaining precipitator voltage responsively to a determination that the time interval between said sparks is greater than said second predetermined lower value and less than said first predetermined value.

16. An electrostatic precipitator voltage control comprising:

means for providing electrical signals related in occurrence to two successive precipitator sparks;

timing means substantially independent of the phase of the precipitator voltage source for detecting whether the time interval between said spark-related electrical signals is less than a first predetermined value, and for generating a first output signal responsive thereto; and

voltage means responsive to said first output signal for reducing precipitator voltage.

17. The control of claim 16 wherein said timing means includes:

clock means, and means for detecting whether the time interval between said spark related electrical signals is less than a second predetermined value and for generating a second output signal responsively thereto; and

wherein said voltage means is responsive to said clock means to raise precipitator voltage at clocked time intervals, the raising of precipitator voltage by said voltage means responsively to said clock means being inhibited for a fixed period of time responsively to said second output signal.

18. The control of claim 17 wherein said fixed period of time is substantially equal in duration to the duration of a clocked time interval.

19. The control of claim 17 wherein said clock means is reset responsively to said second output signal so that said clocked time intervals commence with the occurrence of said second output signal.

20. An electrostatic precipitator voltage control comprising:

means for providing electrical signals related in occurrence to two successive precipitator sparks;

timing means for detecting whether the time interval between said spark-related electrical signals is less than a first predetermined value and for generating a first output signal responsive thereto, and for detecting whether the time interval between said spark-related electrical signals is less than a second predetermined value and for generating a second output signal responsively thereto, said timing means including clock means; and

voltage means responsive to said first output signal for reducing precipitator voltage, and responsive to said clock means for raising precipitator voltage at clocked time intervals, the raising of precipitator voltage by said voltage means responsively to said clock means being inhibited for a fixed period of time substantially equal in duration to the duration of a clocked time interval responsively to said second output signal.

21. An electrostatic precipitator voltage control comprising:

means for providing electrical signals related in occurrence to two successive precipitator sparks;

timing means for detecting whether the time interval between said spark-related electrical signals is less than a first predetermined value and for generating a first output signal responsive thereto, and for detecting whether the time interval between said spark-related electrical signals is less than a second predetermined value and for generating a second output signal responsively thereto, said timing means including clock means; and

voltage means responsive to said first output signal for reducing precipitator voltage, and responsive to said clock means for raising precipitator voltage at clocked time intervals, the raising of precipitator voltage by said voltage means responsively to said clock means being inhibited for a fixed period of time responsively to said second output signal, said clock means being reset responsively to said second output signal so that said clocked time intervals commence with the occurrence of said second output signal.

22. The method of controlling the voltage supplied to an electrostatic precipitator from an alternating current source comprising the steps of:

a. detecting the occurrence of two successive sparks in the precipitator independently of the phase of the source; and

b. reducing precipitator voltage a predetermined amount when the time interval between the two detected sparks is less than a first predetermined value.

23. The method of claim 22 including the further step of increasing precipitator voltage when the time interval between detected sparks is greater than a second predetermined value.

24. The method of claim 23 wherein the second and third values are substantially the same.

25. The method of claim 23 wherein the second value is greater than the first value and wherein precipitator voltage in unchanged when the time interval between detected sparks is greater than the first value and less than the second value.

26. The method of claim 25 including the step of reducing precipitator voltage by an amount greater than the first predetermined amount when the time interval between detected sparks is less than a third predetermined value less than the first predetermined value.

27. The method of claim 22 including the further step of controlling the amount of precipitator voltage reduction in dependency on the time interval between the detected sparks.

28. An electrostatic precipitator voltage control comprising:

means substantially independent of the phase of the precipitator voltage source for providing electrical signals related in occurrence to two successive precipitator sparks;

timing means for detecting whether the time interval between said spark-related electrical signals is less than a first predetermined value, and for generating a first output signal responsive thereto; and

voltage means responsive to said first output signal for reducing precipitator voltage.