ABSTRACT

A receiver integrated circuit is disclosed that includes a filter and a linear equalization circuit. The filter has an input to receive a signal symbols a main tap and a pre-cursor tap to reduces a pre-cursor ISI acting on the data symbols. The linear equalization circuit couples to the output and cooperates with the filter to further reduce ISI.
FIG. 2

Amplitude (volts)

X(t)

Y(t)

Z(t+ΔT)

Time
Receive Signal 702

Filter Pre-Cursor ISI With Transversal Filter and Equalize with Linear Equalizer 704

Adjust Receiver Sampling Phase 706

Filter Post-Cursor ISI With A Decision Feedback Equalizer 708

FIG. 7
FIG. 11

\[ Y(t) = \sum_{n=-\infty}^{\infty} w_n x(t - n(\Delta T)) \]

Pre cursor taps
Main tap
Post cursor taps
RECEIVER WITH ENHANCED ISI MITIGATION

TECHNICAL FIELD

[0001] The disclosure herein relates generally to communications, and more specifically to high-speed electronic signaling within and between integrated circuit devices.

BACKGROUND

[0002] Chip-to-chip signaling systems often employ equalization to reduce the effects of inter-symbol-interference (ISI) acting on transferred data symbols. The ISI is generally data dependent, and includes pre-cursor and post-cursor signal components having contributions based on prior and post received signals. Various techniques exist to address pre-cursor and post-cursor ISI, both at the transmit end of a channel, and at the receive end of a channel. While these techniques help reduce ISI, they are generally not 100% effective. Moreover, conventional techniques are often neither power nor space efficient.

[0003] Thus, the need exists for improved equalization techniques that provide improved effectiveness in reducing ISI while maintaining power and space efficiencies.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Embodiments of the disclosure are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0005] FIG. 1 illustrates a high-level signaling system having a receiver integrated circuit of an embodiment;

[0006] FIG. 2 graphically shows a plurality of overlayed single-bit-response waveforms illustrating ISI mitigation due to the system of FIG. 1;

[0007] FIG. 3 illustrates further detail of one embodiment of the transversal filter of FIG. 1;

[0008] FIG. 4 illustrates one embodiment of a portion of the transversal filter of FIG. 3 with a digital-to-analog converter (DAC) for use in programming the filter taps of FIG. 3;

[0009] FIG. 5 illustrates further detail of one embodiment of the additional ISI cancellation circuitry shown in FIG. 1, in the form of a linear peaking equalizer;

[0010] FIG. 6 illustrates further detail of another embodiment of the additional ISI cancellation circuitry of FIG. 1, in the form of a sampling phase offset circuit;

[0011] FIG. 7 illustrates a flowchart of high-level steps and corresponding single-bit-response waveforms corresponding to each step;

[0012] FIG. 8 illustrates a high-level signaling system similar to that of FIG. 1;

[0013] FIG. 9 illustrates further detail of one embodiment of the sampling/DFE circuitry of FIG. 8;

[0014] FIG. 10 illustrates a further embodiment of a high-level signaling system similar to FIGS. 1 and 8 that employs a transversal filter with distributed ESD circuitry; and

[0015] FIG. 11 illustrates one embodiment of a transversal filter having main, pre-cursor and post-cursor taps that cooperate with distributed ESD elements for use in the signaling system of FIG. 10.

DETAILED DESCRIPTION

[0016] Embodiments of receiver integrated circuits are disclosed herein that provide improved effectiveness in mitigating intersymbol interference (ISI).

[0017] One embodiment of such a device includes a transversal filter to receive a signal from outside the device, and a circuit to sample the transversal filter output. The output of the transversal filter represents time-delayed combinations of the input signal and may be optionally used to reduce pre-cursor ISI. The sampler samples the output of the transversal filter to produce a stream of symbols representing digital values. Further equalization techniques can then be applied as desired.

[0018] Optionally, the transversal filter can be at least partially implemented in electrostatic discharge (ESD) protection circuitry for an integrated circuit signaling pad. The ESD protection circuitry optionally has plural nodes, with inductive-capacitive (LC) delay elements in between these nodes and discharge diodes connecting the nodes to reference rails to provide ESD protection. Implemented in this manner, the transversal filter consumes little to no additional die penalty and provides powerful equalization capabilities.

[0019] Optionally also, a linear equalization circuit (sometimes called a continuous-time equalizer) can be used in between the transversal filter and the sampler to further equalize the transversal filter output. In one specific embodiment, this linear equalizer can be used to compensate for post-cursor ISI, providing a ready complement to a transversal filter implemented to mitigate pre-cursor ISI.

[0020] In further embodiments, a transversal filter can be combined with a data clock recovery (CDR) circuit and/or a decision feedback equalizer, each operating in at least partial dependent on samples taken in dependence on the transversal filter output.

[0021] These various embodiments will be additionally detailed below.

[0022] FIG. 1 illustrates one embodiment of a signaling system, generally designated 100, that effectively mitigates the effects of pre-cursor ISI at a high level of efficiency. In some specific embodiments, compensation for post-cursor ISI is also provided. The system includes a first integrated circuit 102 having at least one transmitter 104a to drive data symbols Data along a channel 106c to a second integrated circuit 108. The channel typically exhibits a low-pass filter effect resulting in attenuation of high-frequency signal components. Equalization provides compensation to offset the effects of the line attenuation in the received signal.

[0023] With continued reference to FIG. 1, the second integrated circuit 108 includes receiver circuitry 110 in the form of a plurality of receiver interface slices 112a-112r. Each receiver interface slice 112 employs a transversal filter, coupled to the receiver circuit to process corresponding, received signal by applying a level of filtering directed to a first component of pre-cursor ISI acting on inbound data symbols. The transversal filter generates a filtered output in the form of a filtered signal that is fed to additional ISI cancellation circuitry 116. The additional ISI cancellation circuitry applies further compensation of ISI acting on the data symbols. The additional compensation may be directed to enhance pre-cursor compensation or post-cursor compensation, depending on the application. In this manner, pre-cursor ISI, and in some cases post-cursor ISI, may be flexibly and effectively mitigated before the data symbols are transferred via a databus 118 to core circuitry 120. Note that a digital sampler or other form of
logic level discrimination ("sampler" or "sampler circuit") can be located between transversal filter 114 and additional ISI cancellation circuitry 116, can be part of the latter, or can follow the latter, depending on embodiment.

[0024] Further referring to FIG. 1, the first and second integrated circuits 102 and 108 may employ additional sets of transmitters 104b-104r and receiver interface slices 112b-112r to establish multiple signaling channels or lanes. Multiple channels operating in parallel may provide significant data bandwidth improvements for selected applications. Note that, although not separately illustrated in FIG. 1, each interface slice 112b-112r can be identical in design to the interface slice 112a, with an independent transversal filter 114 and additional ISI cancellation circuitry not separately depicted to simplify the Figure; if desired, such circuitry can be independently controlled (e.g., have independent coefficient setting for each lane), or can be controlled in common (e.g., to have like-coefficients based on a common set of register entries or control signals), depending on the particular embodiment.

[0025] FIG. 2 illustrates a set of overlaid single bit response (SBR) curves that show the mitigation of pre-cursor ISI as a result of the filtering carried out by the transversal filter. A first one of the curves shows a single bit response corresponding to an ISI-impacted dispersed waveform X(t) corresponding to a received data symbol presented to the input of the filter. Applying filtering via the transversal filter results in the generation of a compensating waveform Z(t+Δt). The compensating waveform is summed with the original waveform X(t). The resulting waveform Y(t) exhibits significantly reduced pre-cursor ISI and has an improved rising edge rise time that further resolves the pulse response. Depending on the application, the mitigation results to the pre-cursors may be adjusted through appropriate weighting of one or more pre-cursor taps employed by the transversal filter 114 as more fully described below.

[0026] FIG. 3 illustrates further detail relating to one embodiment of the transversal filter 114 of FIG. 1. The filter includes an input that sequentially feeds input data symbols to a delay line of delay elements D1-Dn. The delay elements are separated by respective nodes N0-Nn. Each delay element comprises circuitry that introduces a delay of Δτ. In one implementation, the delay elements D1-Dn apply a maximum aggregate delay of at least one-half unit interval. For the implementation seen in FIG. 3, it should be assumed that each delay element (i.e., each delay between adjacent filter taps) provides delay of approximately one unit interval time, though this is not required for all embodiments. Each node may be "tapped" by an amplifier or "tap" that is programmed by, for example, a digital-to-analog converter (DAC), such that shown in FIG. 4, to multiply an input sensed from the given node by a weighted gain, which in many instances may be a negative gain. One or more tapped versions of the inputs signal, with relatively slight delay to represent subsequent symbols, and/or one or more tapped versions of the input signal delayed so as to represent previously-transmitted symbols, may be combined at a summing node 302. The composite waveform resulting from the summation effectively reduces ISI-induced signal dispersion by boosting portions of the composite signal and attenuating other portions. By selecting one of the taps to correspond to the "current value" or current symbol of the signal (i.e., a "main" or "primary" tap), and appropriately selecting relative delay associated with different delayed versions of the signal, outputs of the various taps may be weighted and combined depending on the extent of the ISI compensation desired. Note that the transversal filter can operate on an analog input and be followed by a sampler to convert this input to digital form; the sampler in this case (not seen in FIG. 3) would receive output 304.

[0027] Further referring to FIG. 3, the transversal filter taps are identified consistent with the symbols that are amplified, with a main tap Wm, applying a programmed gain to a current symbol while taps Wi-1 to Wi+n apply gain to subsequent symbols and taps Wi-n to W-1 apply previous symbols. The main tap gain is typically highest, with pre and post tap gains set significantly lower based on the expected contribution of ISI from the respective pre and post data symbols. The summation of all the symbol components with the main tap produces a narrowed output pulse at the output 304 and thus plays a significant role in reducing the effects of pre-cursor and post-cursor ISI. In one specific embodiment, described more fully below, the transversal filter takes advantage of distributed passive circuit elements coupled to the integrated circuit chip to improve power and space efficiencies associated with ISI mitigation.

[0028] Further detail relating to a transversal filter and a digital-to-analog converter (DAC) circuit for programming various filter tap weights is shown in FIG. 4. As explained above, each of the taps W can be used to contribute gain corresponding to a different input symbol, with taps relating to past or future symbols generally having lower magnitude gains as compared to the main tap. Each tap includes an amplifier having complementary transistors Q1 and Q2 disposed as a differential pair. The output of the differential pair receives an integrated circuit input signal S(t). The output of the differential pair ties to the summing node 302.

[0029] Further referring to FIG. 4, the tap gain, or weighting for each tap may be programmatically set through a digital-to-analog converter (DAC) that utilizes a programmable current source 402 to draw a selectable amount of current. The current level may be specified by a multi-bit input D1-Dn that activates one or more current fingers 404a-404d disposed in parallel. The fingers generate currents at levels that have binary-weighted analog current values w, 2w, 4w, and 2nw, for example. The level of current drawn through the current source 402 corresponds to the gain applied by the differential pair, and thus represents the weighting applied by the tap.

[0030] FIG. 5 illustrates further detail associated with one embodiment of the additional ISI cancellation circuitry (see, e.g., element 116 of FIG. 1) in the form of a linear peaking equalizer 500. In general, the linear peaking equalizer provides a way to further boost or selectively provide gain to certain high frequency signal components associated with the data symbols from the transversal filter output (e.g., such as a specific band of frequencies). A modified differential receiver M1 having RC load impedances 502 and 504 can be coupled to a power supply 506. Each load impedance includes a load resistance Rl coupled to a load capacitance Cl. The receiver further includes transistors Q1 and Q2 that are source-coupled to respective current sources I1 and I2. Interposed between the current sources is a source RC impedance 508 defined by a parallel configuration of a source resistance Rs and capacitance Cs. The values of the passive resistor and capacitor elements Rs, Rl, Cs, and Cl are chosen to achieve a desired boost to frequency content of interest above a certain frequency threshold. The RC impedance values are related to the amount of boost desired at high frequencies. Note that the linear peaking equalizer shown in FIG. 5 compensates for post-cursor ISI and complements the functionality of the
transversal filter. As explained below, the level of post-cursor compensation provided by the linear peaking equalizer may depend on whether any further forms of post-cursor compensation are provided in the system. In one specific embodiment, a first post cursor component of ISI is mitigated by an optionally-provided decision-feedback-equalization circuit (DFE) and the remaining post-cursors are reduced by a combination of the optional DFE circuit and the linear peaking equalizer of FIG. 5.

[0031] FIG. 6 illustrates a specific embodiment of a sampler circuit, generally designated 600. The sampler circuit includes sampling offset circuit includes input circuitry 602, itself consisting of a data sampler 604, a reference data sampler 606, and a reference edge sampler 608. A clock recovery circuit 610 receives data and edge samples from the reference samplers 606 and 608 and generates a reference clock signal RDCcycl. The reference clock is fed to an adaptive phase offset control circuit 612 which adjusts the phase of a timing signal to a sampling phase that triggers sampling of an equalized signal by the data sampler 604. Data output from the data sampler 604 is then further processed by core logic 614.

[0032] Further referring to FIG. 6, in one embodiment, the adaptive phase offset control circuit 612 responds to a further input generated by a signal quality measurement circuit 616. The signal quality measurement circuit evaluates the sampled data, develops measure of extent of pre-cursor ISI affecting the symbols, such as through a determination and analysis of bit error rate during a calibration phase, and generates a correction signal for application to the adaptive phase offset control circuit 612. In response to receiving the correction signal, the sampling phase of the data sampler is adjusted, thereby completing the adaptive control loop. The adjustments may be carried out continuously during operation. Note that conventionally, the sampling instant for a sampler is set at the expected midpoint of a data eye. Contrary to this conventional wisdom, the techniques just described can be used to shift the sampling instant to a non-intuitive point, earlier within the data eye; that is, the adaptive phase offset control circuit 612 can be used to sacrifice voltage margin in exchange for reduced pre-cursor ISI—although the resulting voltage margin is less, the additional post-cursor interference from sampling later in the data eye (closer to ensuing samples) can straightforwardly be corrected for via DFE techniques, ultimately resulting in a cleaner signal (that is, one with less margin but with less difficult-to-correct-for pre-cursor ISI). Note that the use of the specifically-depicted sampler circuit 600 and control over sampling phase is not required for all embodiments.

[0033] In one specific embodiment, the sampler circuit 600 can be used in a staged manner with the linear peaking equalizer 500 (from FIG. 5) to form the additional ISI cancellation circuit 116 from FIG. 1. Viewed in the context of the embodiment of FIG. 1, the data symbols can be first filtered via the transversal filter 114 to compensate for a first component of pre-cursor ISI. The filtered output from the transversal filter can then be equalized by the linear peaking equalizer 500 to compensate for post-cursor ISI. The equalized output is then fed to the sampler circuit 600 to generate sampled data.

[0034] A further specific embodiment for the additional ISI cancellation circuitry 116 from FIG. 1 may take the form of a decision feedback equalizer (DFE). The DFE can receive the transversal filter output directly (with the DFE employing a sampler circuit front-end), or can follow the linear peaking equalizer from FIG. 5 and/or follow or be combined with the sampler circuit from FIG. 6. In one embodiment, the DFE compensates for post-cursor ISI. Note that in a detailed embodiment that combines many of the techniques presented above, the DFE circuit can be used with the transversal filter, the linear equalizer, and the sampler circuit just discussed, to provide a multi-faceted scheme for effectively mitigating pre and post-cursor ISI. Note that when the transversal filter is implemented by using ESD protection circuitry, these structures can be implemented to provide superior ISI correction with little to no die area penalty or power penalty relative to many conventional designs.

[0035] FIG. 7 illustrates a high-level method of operation of an embodiment that includes a transversal filter and additional ISI cancellation circuitry, including the linear peaking equalizer from FIG. 5 and the sampling offset circuit from FIG. 6, to reduce both pre-cursor and post-cursor ISI. Each high-level step described below is paired in FIG. 7 with a corresponding single bit response waveform showing the contributions with various tap weights and/or sampling instants.

[0036] Further referring to FIG. 7, the receiver receives data symbols transmitted from the transmit integrated circuit via a lossy channel, at step 702. An exemplary single bit response for a transmitted symbol is shown adjacent the step block 702, with points in the single bit response identified in a manner showing correspondence to filter taps (such as h_0, h_1, h_2) and sampling points more fully described below. The single bit response generally represents the variation of the bit waveform as a function of time assuming a logic value of “1”, and having adjacent pre and post bits with logic “0” values.

[0037] With continued reference to FIG. 7, a signal representing received data symbols is fed to a receiver transversal filter, which filters the symbols (e.g., to reduce pre-cursor ISI), and is then equalized by the linear peaking equalizer, at step 704. Note that both of these elements operate effectively in series in the analog domain. In one embodiment, the linear peaking equalizer compensates for post-cursor ISI. The level of post-cursor compensation may depend on the intended application, and whether other post-cursor compensation schemes are also utilized, such as DFE. Note that in other embodiments, the linear equalizer can be configured to compensate for pre-cursor ISI, to supplement if desired the operation of the transversal filter. It should be assumed, relative to FIG. 7, that the linear peaking equalizer mitigates ISI associated with a specific range of latencies (e.g., first post-cursor).

[0038] A corresponding post-filtered/equalized single bit response is shown adjacent the filtering/equalizing step block 704. A comparison of the filtered/equalized waveform to the initially received waveform reveals significant improvement in pre-cursor ISI reduction (the signal components with points labeled h_1 and h_2). For instance, the amplitude of the point corresponding to the filter main tap, h_0, shows an increased amplitude, with pre-cursor points h_1 and h_2 significantly attenuated.

[0039] Further referring to FIG. 7, when optionally employing a sampling circuit which provides for sampling offset from the peak of the single bit response, further improvements to pre-cursor ISI reduction may be realized by adjusting, such as by selectively advancing or delaying, the sampling phase of the sampler that receives the signal from the linear equalizer, at step 706. The effect to the single bit response waveform is shown with a delay of the sampling phase by an amount Δτ, which slightly reduces the magnitude of the main tap sample h_0, while effectively reducing the
pre-cursor sample values \( h_{-1} \) and \( h_{-2} \) to values close to zero. Note once again that conventional wisdom would typically call for selecting a sampling phase to correspond to peak voltage margins (equated with the peak of the single bit waveform); by deliberately offsetting phase based on a measure of ISI (e.g., based on the output of signal quality measurement circuit 616 from Fig. 6), a cleaner signal can ultimately be obtained.

[0040] As noted above, in some embodiments, it may be beneficial to supplement the linear equalizer with a DFE circuit to provide enhanced post-cursor ISI compensation. This optional step is shown at 708, with a corresponding single-bit response curve illustrating the effect of DFE on the post-cursor ISI. Note that the DFE 708 would typically use feedback of previously-resolved digital symbols, i.e., the feedback at this point is typically post-sampler digital feedback.

[0041] Fig. 8 illustrates an alternative embodiment of a signaling system, generally designated 800, that employs a combination of filtering, sampling phase adjusting and equalizing to address pre and post-cursor ISI. Like the previously described signaling system embodiments, the system of Fig. 8 employs a transmit integrated circuit chip 802 with a plurality of transmitters Tx that deliver data symbols DATAn along corresponding channels or lanes 804. A receiver integrated circuit chip 805 receives the resultant signals with a plurality of receiver interface slices 806a-806x acting to process the signals from corresponding lanes. Each receiver slice includes a transversal filter 808, linear equalization circuitry 810, and sampling/DFE circuitry 812, although these elements are only depicted for receiver interface slice 806a to simplify the Figure. The combination of elements 808-812 provides ability to finely tune the equalized waveforms discussed above to mitigate the pre and post-cursor ISI attributable to energy associated with pre and post-symbols (symbols transmitted after and before a “current” symbol, respectively). Processed data symbols are then passed to a receiver integrated circuit chip core 814.

[0042] In one specific embodiment, the sampling/DFE circuitry 812 supplements the transversal filter 808 and linear equalization circuitry 810, to provide enhanced pre-cursor and post-cursor ISI compensation.

[0043] Fig. 9 illustrates one specific embodiment of the sampling/DFE circuitry from element 812 of Fig. 8, including respective sampling phase adjustment circuitry 902, and DFE circuitry 903. One embodiment of the sampling circuitry 902 employs a similar circuit arrangement as that shown in Fig. 6. The DFE circuit 903 generally includes a finite impulse response (FIR) filter 905 that receives data samples from a data sampler 904 and timing information from an adaptive phase offset control circuit 912. The filter also receives control signals from an equalizer control circuit 907. The FIR filter output is fed to a summing node 909 where it is summed with input symbols prior to being sampled by the data sampler 904. The FIR filter 905 employs programmable taps that are similar to the taps described earlier with respect to the transversal filter.

[0044] Note that further details of the structure and operation of one embodiment of adaptive phase offset circuitry, an associated DFE circuit, and the selection of sampling phase through bit error rate measurement, are disclosed in U.S. Patent Application Publication number US 2010/0135378, titled “Receiver with Clock Recovery Circuit and Adaptive Sample and Equalizer Timing,” assigned to the assignee of the disclosure herein, and expressly incorporated by reference in its entirety.

[0045] Fig. 10 illustrates a further embodiment of a signaling system, generally designated 1000, similar to Figs. 1 and 7, that includes respective transmitter and receiver integrated circuit chips 1002 and 1004. The receiver chip includes multiple receiver slices 1005a-1005n that each employ a transversal filter 1006 that incorporates distributed electro-static-discharge (ESD) circuitry associated with the receiver integrated circuit chip. The ESD-based transversal filter significantly reduces pre-cursor ISI while minimizing power and area efficiency by taking advantage of ESD structures disposed at the receiver inputs. In this context, each channel or lane DATA1n-DATAm may be a conductive signaling link connecting the respective integrated circuit chips, for example, disposed on a printed circuit board which mounts those chips.

[0046] In one specific embodiment of a transversal filter, illustrated in Fig. 11 and generally designated 1100, the ESD-based transversal filter includes distributed LC segments 1102 that are each defined by a distributed series inductance represented by L_Series and a distributed capacitance, consisting of pad capacitance (C_Pad) and a capacitance associated with each LC segment. The LC segments are each coupled to distributed sets of forward and reverse biased diodes D_F, and D_R, to provide discharge protection, which also are the source of capacitance. The LC element values may be chosen to generate the Δt delays typically exhibited along the transversal filter delay line, and that exhibits an acceptable frequency response characteristic.

[0047] Further referring to Fig. 11, the transversal filter 1100 further includes respective tap circuits Wp-Wn and a summing node 1104 to aggregate selected signal components from a main tap Wp pre-cursor Wn and/or post-cursor Wn tap circuitry. The ESD circuitry may be formed on-chip or as part of a network of passive components disposed off-chip but coupled to the input of the second integrated circuit chip.

[0048] Those skilled in the art will appreciate the many benefits and advantages afforded by the embodiments described herein. For example, by combining a transversal filter with additional ISI cancellation circuitry, aspects of pre-cursor ISI may be more efficiently cancelled. Optionally including post-cursor ISI circuitry further enhances the ISI mitigation capabilities in a flexible manner. Further, by incorporating ESD structures into an optional transversal filter design, significant power and space efficiency advantages may be realized.

[0049] In the foregoing description and in the accompanying drawings, specific terminology and drawing symbols have been set forth to provide a thorough understanding of the present invention. In some instances, the terminology and symbols may imply specific details that are not required to practice the invention. For example, any of the specific numbers of bits, signal path widths, signaling or operating frequencies, component circuits or devices and the like may be different from those described above in alternative embodiments. Also, the interconnection between circuit elements or circuit blocks shown or described as multi-conductor signal links may alternatively be single-conductor signal links, and single conductor signal links may alternatively be multi-conductor signal links. Signals and signaling paths shown or described as having active-high or active-low logic levels may have opposite logic
levels in alternative embodiments. Component circuitry within integrated circuit devices may be implemented using metal oxide semiconductor (MOS) technology, bipolar technology or any other technology in which logical and analog circuits may be implemented. With respect to terminology, a signal is said to be "asserted" when the signal is driven to a low or high logic state (or charged to a high logic state or discharged to a low logic state) to indicate a particular condition. Conversely, a signal is said to be "deasserted" to indicate that the signal is driven (or charged or discharged) to a state other than the asserted state (including a high or low logic state, or the floating state that may occur when the signal driving circuit is transitioned to a high impedance condition, such as an open drain or open collector condition). A signal driving circuit is said to “output” a signal to a signal receiving circuit when the signal driving circuit asserts (or deasserts, if explicitly stated or indicated by context) the signal on a signal line coupled between the signal driving and signal receiving circuits. A signal line is said to be “activated” when a signal is asserted on the signal line, and “deactivated” when the signal is deasserted. Additionally, the prefix symbol “!” attached to signal names indicates that the signal is an active low signal (i.e., the asserted state is a logic low state). A line over a signal name (e.g., "$\overline{signalname}\$”) is also used to indicate an active low signal. The term “coupled” is used herein to express a direct connection as well as a connection through one or more intervening circuits or structures. Integrated circuit device “programming” may include, for example and without limitation, loading a control value into a register or other storage circuit within the device in response to a host instruction and thus controlling an operational aspect of the device, establishing a device configuration or controlling an operational aspect of the device through a one-time programming operation (e.g., blowing fuses within a configuration circuit during device production), and/or connecting one or more selected pins or other contact structures of the device to reference voltage lines (also referred to as strapping) to establish a particular device configuration or operation aspect of the device. The term “exemplary” is used to express an example, not a preference or requirement.

While the invention has been described with reference to specific embodiments thereof, it will be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. For example, features or aspects of any of the embodiments may be applied, at least where practicable, in combination with any other of the embodiments or in place of counterpart features or aspects thereof. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

1. A device having a signaling pad to receive an input signal, the device comprising:
   - a transversal filter to receive the input signal from the signaling pad and generate an intermediate signal;
   - a circuit to equalize and sample the intermediate signal, and to thereby generate a digital output.

2. The device of claim 1 where the transversal filter includes at least one pre-cursor tap.

3. The device of claim 2 where the transversal filter is formed by at least one electrostatic discharge (ESD) structure.

4. The device of claim 2 where the transversal filter includes at least one post-cursor tap.

5. The device of claim 1 where the circuit includes a sampler circuit and a linear equalizer, the linear equalizer coupled to the transversal filter to receive the intermediate signal, the sampler circuit coupled to the linear equalizer to receive an output of the linear equalizer and generate the digital output therefrom.

6. The device of claim 5 where the circuit includes a sampling phase offset circuit, to shift a sampling phase used by the sampler circuit to sample at a data eye point less subject to precursor intersymbol interference (ISI).

7. The device of claim 5 where the circuit includes a sampling phase offset circuit, to shift a sampling phase used by the sampler circuit away from a point of maximum voltage margin to sample at a data eye point less subject to precursor intersymbol interference (ISI).

8. The device of claim 7 further comprising a decision feedback equalizer (DFE) circuit to adjust at least one of sampling or the intermediate signal to compensate for a previously-resolved digital symbol.

9. The device of claim 1 where the circuit includes a decision feedback equalizer (DFE) circuit to adjust sampling to compensate for a previously-resolved digital symbol.

10. The device of claim 1 where the transversal filter is formed by at least one electrostatic discharge (ESD) structure.

11-17. (canceled)

18. A receiver integrated circuit comprising:
   - a filter to receive an external signal and responsively produce an intermediate signal, the filter including a main tap and at least one secondary tap to reduce intersymbol interference (ISI);
   - a sampler circuit to generate a sampled output in dependence on the intermediate signal; and
   - a decision-feedback equalization circuit coupled to the sampler circuit, the decision-feedback equalization circuit including at least one post-cursor equalization tap, such that the sampled output is equalized to reduce post-cursor ISI based on prior symbols from the sampled output.

19. The receiver integrated circuit of claim 18 and further including a linear equalizer to receive the intermediate signal and to generate an input for the sampler circuit.

20. The receiver integrated circuit of claim 19 where the linear equalizer is to equalize the intermediate signal to compensate for post-cursor ISI.

21. The receiver integrated circuit of claim 18 where the receiver integrated circuit further comprises phase adjustment circuitry to receive and adjust a timing signal for phase based on a measure representing pre-cursor ISI, to generate a sampler circuit timing signal.

22. A method of operation in a receiver integrated circuit, the receiver integrated circuit to receive an input signal, the method comprising:
   - filtering the input signal using a filter at least two taps, including a main tap and a secondary tap, to generate an intermediate signal; and
   - using a circuit to equalize and sample the intermediate signal to generate a stream of digital symbols.

23. The method of claim 22 where the circuit includes a linear equalizer to equalize the intermediate signal to produce an output, and a sampler circuit to sample the output of the linear equalizer to produce the stream of digital symbols.
24. The method of claim 23 where:
sampling is performed in response to a timing signal repre-
senting a sampling phase; and
the method further comprises adjusting the sampling phase
based on a measure of pre-cursor ISI, to force a sampling
instant displaced from maximum voltage margin rela-
tive to a data threshold.

25. The method of claim 23 where the receiver integrated
circuit includes a decision feedback equalization (DFE) cir-
cuit and where:
sampling includes equalizing an output of the linear equal-
izer in dependence upon a binary state of a prior symbol
in the stream of digital symbols.

26. The method of claim 22 where filtering comprises:
filtering a current data symbol based on electrical charac-
teristics exhibited by a plurality of distributed LC circuit
elements.

27. The method of claim 26 where the input signal is
received via a signal pad and where the plurality of distributed
LC circuit elements provide electrostatic discharge (ESD)
protection to the signal pad.

28-59. (canceled)