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(54) Title: FILLING OPENINGS THROUGH FLUID PRECURSOR INFILTRATION OF A HOST MATRIX IN MANUFACTURING INTEGRATED CIRCUIT COMPONENTS

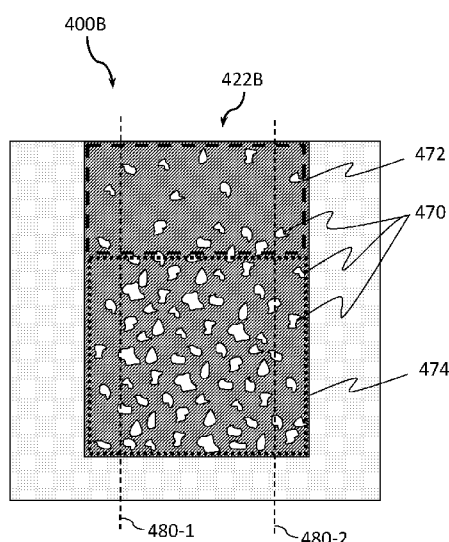
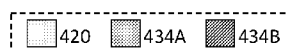


FIG. 4B



(57) Abstract: Disclosed herein are methods for manufacturing IC components using bottom-up fill of openings by infiltrating one or more fluid precursors for forming dielectric materials into a solid host matrix provided within the openings. One exemplary method includes providing a host matrix within a plurality of openings in a structure, infiltrating the host matrix within the openings with one or more fluid precursors for forming a dielectric material, and, following the infiltration, removing at least a portion of the host matrix. Assemblies and devices manufactured using such methods are disclosed as well.

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**FILLING OPENINGS THROUGH FLUID PRECURSOR INFILTRATION OF A HOST MATRIX
IN MANUFACTURING INTEGRATED CIRCUIT COMPONENTS**

Background

[0001] For the past several decades, the scaling of features in integrated circuits (ICs) has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited area of semiconductor IC chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to fabrication of products with increased capacity. Since products that implement IC chips are used in a variety of devices including automobiles, computers, appliances, mobile phones and consumer electronics, increasing capacity of the chips is always desirable.

[0002] The drive for the ever-increasing capacity, however, is not without issue. The desire to make smaller IC chips continuously places demands on the methods and materials used to manufacture these devices. For example, integration of advanced backend interconnects of IC chips requires materials with unique compositions that can be deposited completely into openings/gaps without forming voids. In particular, there is a need for fabricating structures that include openings filled with dielectric materials which have specified properties desired for a given implementation, such as e.g. a certain dielectric constant, low electrical leakage, thermal stability, and specific etch properties. Unfortunately, fabricating such structures remains a challenge, especially when the openings have high aspect ratios often needed in manufacturing of various IC components.

Brief Description of the Drawings

[0003] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements (e.g. the same, similar, or analogous elements) and, therefore, discussions of these elements provided with respect to one of the drawings are applicable to other drawings and, in the interests of brevity, are not repeated for each of the drawings separately. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0004] FIGS. 1A and 1B are cross-sections illustrating various example stages in the manufacture of a structure with openings filled with a dielectric material using conventional methods.

[0005] FIG. 2 is a flow diagram of an example method of manufacturing a structure with one or more openings filled with a dielectric material by infiltrating fluid dielectric precursor(s) into a solid host matrix provided within the openings, in accordance with various embodiments of the present disclosure.

[0006] FIGS. 3A-3K are cross-sections illustrating various example stages in the manufacture of a structure with openings filled with a dielectric material using the host matrix infiltration method of FIG. 2, in accordance with various embodiments of the present disclosure.

[0007] FIG. 3L illustrates schematic cross-sections of various assemblies in which an opening filled with a dielectric material using the host matrix infiltration method of FIG. 2 may be provided, in accordance with various embodiments of the present disclosure.

[0008] FIGS. 4A and 4B are illustrations of exemplary real world structures with openings having a straight profile filled with a dielectric material using, respectively, a conventional method and a host matrix infiltration method described herein.

[0009] FIGS. 5A and 5B are illustrations of exemplary real world structures with openings having a re-entrant profile filled with a dielectric material using, respectively, a conventional method and a host matrix infiltration method described herein.

[0010] FIGS. 6A and 6B are illustrations of exemplary real world structures with openings having a non-re-entrant profile filled with a dielectric material using, respectively, a conventional method and a host matrix infiltration method described herein.

[0011] FIGS. 7A and 7B are top views of a wafer and dies that include one or more structures which have openings with infiltrated dielectric materials in accordance with any of the embodiments disclosed herein.

[0012] FIG. 8 is a cross-sectional side view of an IC device that may include one or more structures which have openings with infiltrated dielectric materials in accordance with any of the embodiments disclosed herein.

[0013] FIG. 9 is a cross-sectional side view of an IC device assembly that may include one or more structures which have openings with infiltrated dielectric materials in accordance with any of the embodiments disclosed herein.

[0014] FIG. 10 is a block diagram of an example computing device that may include one or more structures which have openings with infiltrated dielectric materials in accordance with any of the embodiments disclosed herein.

Detailed Description

[0015] Disclosed herein are methods for manufacturing IC components using bottom-up fill of openings by infiltrating one or more fluid (i.e. liquid and/or gaseous) precursors for forming dielectric materials (referred to herein as “dielectric precursors”) into a solid host matrix (i.e. a substantially continuous solid phase in which guest particles such as atoms, molecules, ions, compounds, etc. may be embedded) provided within the openings, part or all of which host matrix is subsequently removed. Such methods are referred to herein as “host matrix infiltration” methods.

Assemblies/structures and devices manufactured using such methods are disclosed as well, which assemblies and devices are referred to herein as having “openings with infiltrated dielectric materials” due to the host matrix infiltration process used to form them.

[0016] In one aspect, an exemplary host matrix infiltration method includes providing a host matrix within a plurality of openings in a structure, infiltrating the host matrix within the openings with one or more fluid dielectric precursors, and, following the infiltration, removing at least a portion of the host matrix. The plurality of openings may include openings, holes, or gaps (all together referred to herein simply as “openings”) of various aspect ratios, where, as used herein, “aspect ratio” (AR) refers to a ratio between a depth/height of an opening to a width of an opening. In various embodiments, openings described herein may have ARs between about 1 and 20, including all values and ranges therein, e.g. between about 1 and 15 or between about 5 and 10. In some implementations, dimensions of the openings may be on the nanometer scale, e.g. with a width of an opening being about 20 nm and a depth of an opening being about 100 nm, i.e. AR of 5. Therefore, such structures with openings may sometimes be described as “nanostructures” or “nanopatterned structures.”

[0017] The devices and assemblies having openings with infiltrated dielectric materials as described herein could be a part of a semiconductor device or an IC package, e.g. a part of an interconnect, e.g. a backend interconnect, used for providing electrical conductivity in a semiconductor device or an IC package. As used herein, the term “backend interconnect” is used to describe a region of an IC chip containing wiring between components associated with an IC, e.g. transistors, and other elements, while the term “frontend interconnect” is used to describe a region of an IC chip containing the rest of the wiring. Structures having openings with infiltrated dielectric materials as described herein may be used in any devices or assemblies where one electrically conductive element of the wiring needs to be separated from another electrically conductive element, which could be done both in backend and frontend interconnects. Such devices or assemblies would typically provide an electronic component, such as e.g. a transistor, a die, a sensor, a processing device, or a memory device, and one or more interconnects for providing electrical connectivity to the component. The interconnect(s) may include a plurality of conductive regions, e.g. trenches and/or vias filled with electrically conductive materials as known in the art. Another term commonly used in the art for a plurality of trenches and vias filled with electrically conductive materials is a “metallization stack.” The devices and assemblies having openings with infiltrated dielectric materials as described herein could be used to electrically isolate at least some of the conductive regions from one another.

[0018] The devices and assemblies having openings with infiltrated dielectric materials as described herein may be implemented in one or more components associated with an IC or/and between

various such components. In various embodiments, components associated with an IC include, for example, transistors, diodes, power sources, resistors, capacitors, inductors, sensors, transceivers, receivers, antennas, etc. Components associated with an IC may include those that are mounted on IC or those connected to an IC. The IC may be either analog or digital and may be used in a number of applications, such as microprocessors, optoelectronics, logic blocks, audio amplifiers, etc., depending on the components associated with the IC. The IC may be employed as part of a chipset for executing one or more related functions in a computer.

[0019] For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details or/and that the present disclosure may be practiced with only some of the described aspects. In other instances, well known features are omitted or simplified in order not to obscure the illustrative implementations.

[0020] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which are shown, by way of illustration, embodiments that may be practiced.

[0021] In order to not clutter the drawings, some of the elements referred to in the description of various drawings with reference numerals may be indicated in the corresponding drawings with different patterns, with a legend showing the correspondence between the reference numerals and patterns being provided below the corresponding drawings, and are not labeled in these drawings with arrows pointing to them.

[0022] The accompanying drawings are not necessarily drawn to scale. For example, to clarify various layers, structures, and regions, the thickness of some layers may be enlarged.

[0023] Furthermore, while drawings illustrating various structures/assemblies of exemplary devices may be drawn with precise right angles and straight lines, real world process limitations may prevent implementations of devices exactly as shown. Therefore, it is understood that such drawings revised to reflect example real world process limitations, in that the features may not have precise right angles and straight lines, are within the scope of the present disclosure. Drawings revised in this manner may be more representative of real world structure/assemblies as may be seen on images using various characterization tools, such as e.g. scanning electron microscopy (SEM) or transmission electron microscopy (TEM). In addition, the various structures/assemblies of the present drawings may further include possible processing defects, such as e.g. the rounding of corners, the drooping of the layers/lines, unintentional gaps and/or discontinuities, unintentionally uneven surfaces and

volumes, etc., although these possible processing defects may not be specifically shown in the drawings.

[0024] It is to be understood that other embodiments may be utilized and structural or logical changes to the drawings and descriptions may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0025] Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0026] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0027] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. Furthermore, stating in the present disclosure that any part (e.g. a layer, film, area, or plate) is in any way positioned on or over (e.g. positioned on/over, provided on/over, located on/over, disposed on/over, formed on/over, etc.) another part means that the referenced part is either in contact with the other part, or that the referenced part is above the other part with one or more intermediate part(s) located therebetween. On the other hand, stating that any part is in contact with another part means that there is no intermediate part between the two parts.

[0028] The terms "substantially," "close," "approximately," "near," and "about," generally refer to being within +/- 20% of a target value. Unless otherwise specified, the use of the ordinal adjectives "first," "second," and "third," etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so

described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0029] In the following detailed description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. In some examples, a "high-k dielectric" may refer to a material having a dielectric constant higher than that of silicon oxide, a "low-k dielectric" may refer to a material having a dielectric constant lower than that of silicon oxide, while the terms "oxide," "carbide," "nitride," etc. may refer to compounds containing, respectively, oxygen, carbon, nitrogen, etc. In another example, the term "connected" means a direct electrical or magnetic connection between the things that are connected, without any intermediary devices, while the term "coupled" means either a direct electrical or magnetic connection between the things that are connected or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function.

[0030] For purposes of illustrating structures having openings with infiltrated dielectric materials as proposed herein, it is important to understand the phenomena that may come into play in a typical IC manufacturing process. The following foundational information may be viewed as a basis from which the present disclosure may be properly explained. Such information is offered for purposes of explanation only and, accordingly, should not be construed in any way to limit the broad scope of the present disclosure and its potential applications. For example, in the following, some descriptions are provided with reference to infiltration of a poly(methyl methacrylate) (PMMA) polymer host matrix with trimethyl aluminum (TMA) and water to form a metal oxide, in particular to form aluminum oxide. However, descriptions of various embodiments provided herein are equally applicable to infiltration of host matrices formed of polymers other than PMMA, or formed of non-polymeric materials altogether, are applicable to using fluid precursors other than TMA, are applicable to using co-reactants other than water, and/or are applicable to forming dielectric materials other than metal oxides.

[0031] FIGS. 1A-1B are cross-sections illustrating various example stages in the manufacture of a structure with openings filled with a dielectric material using conventional methods.

[0032] FIG. 1A illustrates a structure 102 comprising a substrate 120 with two openings 122, indicated as a first opening 122-1 and a second opening 122-2. In IC component manufacturing, it may be necessary to fill the openings 122 with a dielectric material such as e.g. a metal oxide. Such a dielectric material may later serve as an etch stop material with suitable etch selectivity and dielectric properties.

[0033] Conventionally, atomic layer deposition (ALD) or chemical vapor deposition (CVD) processes are used to fill such openings with a dielectric material. In general, CVD or ALD is a chemical process in which one or more reactive precursor gases are introduced into a reaction chamber and directed towards a substrate in order to induce controlled chemical reactions that result in growth of a desired material on the substrate. For example, an ALD process may be carried out by placing the structure 102 into a reaction chamber and introducing into the chamber a gaseous dielectric precursor such as e.g. TMA, as well as a co-reactant such as e.g. water. TMA and water will nucleate on the sidewalls of each of the openings 122 to form a dielectric material in the form of aluminum oxide, which oxide will then grow towards the center of the opening. Because of the nature of this growth (i.e. from the sidewalls towards the center), oftentimes characteristic center voids are formed, i.e. areas substantially in the center of the openings where the dielectric material is absent. Such a situation is illustrated in FIG. 1B showing a structure 104. The structure 104 is the same as the structure 102 but after a dielectric material 124, e.g. aluminum oxide, was grown by ALD within the openings 122. As illustrated in FIG. 1B, as a result of this ALD growth, a void 126 is formed within each of the openings 122 (shown in FIG. 1B as a void 126-1 within the opening 122-1 and a void 126-2 within the opening 122-2). The voids 126 are located approximately along a centerline 128 of the openings (shown in FIG. 1B as a centerline 128-1 within the opening 122-1 and a centerline 128-2 within the opening 122-2).

[0034] FIGS. 1A and 1B illustrate openings having a perfect straight profile, i.e. a profile where the openings have sidewalls extending perpendicularly from the surface. While such profiles are often desirable for various openings, they are not always achievable in real world manufacturing processes. Namely, a real world opening, although designed to have a straight profile, may end up having a so-called “re-entrant” profile, where the width at the top of the opening is smaller than the width at the bottom of the opening, or a so-called “non-re-entrant” profile, where the width at the top of the opening is larger than the width at the bottom of the opening. The nature of ALD dielectric growth within the openings would typically depend on the actual profile of the openings and may be different than that illustrated in FIG. 1B. For example, a void in the center may be substantially triangular in form, where the dielectric material pinches off at the top of a re-entrant profile opening, or the dielectric material may form a seam substantially in the center of the opening, instead of a void. All of these imperfections in the dielectric material within the openings (i.e. voids, seams, etc.) result in major yield issues during pattern transfer in subsequent IC manufacturing steps, with the problems only getting worse as, in order to accommodate IC manufacturing scaling trends, dimensions of the openings shrink and ARs of the openings get higher. In addition, conventional techniques do not allow sufficient control of various properties of the

resulting dielectric material within the openings, such as dielectric constant, low electrical leakage, thermal stability, and specific etch properties. For example, the dielectric material which may be provided in the openings by the process described above is aluminum oxide, but certain applications may require that a dielectric material has a dielectric constant that is lower than that of aluminum oxide.

[0035] Embodiments of the present disclosure aim to improve on one or more shortcomings of conventional dielectric fill techniques described above. To that end, several different embodiments of a host matrix infiltration method are proposed, where a structure with one or more openings filled with a dielectric material are manufactured by infiltrating fluid dielectric precursor(s) into a solid host matrix provided within the openings. The host matrix is subsequently removed, leaving a porous dielectric material, e.g. a metal oxide such as e.g. aluminum oxide, within the openings. Some advantages of the disclosed techniques may include that relatively high AR structures, e.g. structures having an AR of at least 3, e.g. an AR of 10 or even greater, may be filled with dielectric materials in a manner that does not result in formation of voids or seams while, at the same time, achieving adequate high etch selectivity and improved control of the dielectric properties of the resulting fill material. The porous dielectric material left within the openings after removal of the original host matrix may then itself serve as a solid host matrix which may subsequently be filled with same or different dielectric precursors in the next round of ALD growth. Using the same dielectric precursors in the next round of ALD growth would allow creating a more uniform or/and more dense dielectric fill within the openings, while using different dielectric precursors would allow creating hybrid materials (e.g. aluminum oxide infiltrated with hafnium oxide) with improved etch performance and/or carefully controlled dielectric properties. Overall, the techniques disclosed herein may enable manufacturing devices having improved performance and using a wider array of materials, than realizable using conventional approaches.

[0036] In some embodiments, the porosity of the dielectric material left within the openings after removal of the original host matrix may be substantially lower than the porosity of the original host matrix. In some embodiments, there may be a gradient in the porosity of the dielectric material left within the openings after removal of the original host matrix in that the upper regions within the openings post infiltration will have lower porosity than the lower regions because infiltrating the lower regions with the fluid dielectric precursor may be more challenging than infiltrating the upper regions.

[0037] FIG. 2 is a flow diagram of an example host matrix infiltration method 200, in accordance with various embodiments of the present disclosure. FIGS. 3A-3K are cross-sections illustrating various example stages in the manufacture of a structure with openings filled with a dielectric

material using the host matrix infiltration method of FIG. 2, in accordance with various embodiments of the present disclosure. Although the operations of the method 200 are illustrated in FIG. 2 once each and in a particular order, the operations may be performed in any suitable order and repeated as desired. For example, one or more operations may be performed in parallel to manufacture multiple structures having openings with infiltrated dielectric materials substantially simultaneously. In another example, the operations may be performed in a different order to reflect the architecture of a particular IC component in which one or more structures having openings with infiltrated dielectric materials are to be included. In addition, the manufacturing method 200 may include other operations, not specifically shown in FIG. 2, such as e.g. various cleaning operations as known in the art.

[0038] Implementations of the present disclosure may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

[0039] As described above, in various embodiments, the structures having openings with infiltrated dielectric materials as described herein may be used to connect various components associated with an integrated circuit. In the embodiments where at least some of the components associated with an integrated circuit are transistors, a plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations of the disclosure, the MOS transistors may be planar transistors, non-planar transistors, or a combination of both. Non-planar transistors may include FinFET transistors such as e.g. double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as e.g. nanoribbon and nanowire transistors.

[0040] Each MOS transistor includes a gate stack formed of at least two layers, a gate interconnect support layer and a gate electrode layer. The gate interconnect support layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO₂) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium,

lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate interconnect support layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate interconnect support layer to improve its quality when a high-k material is used.

[0041] The gate electrode layer is formed on the gate interconnect support layer and may include at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may include a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer.

[0042] For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

[0043] In some implementations, when viewed as a cross section of the transistor along the source-channel-drain direction, the gate electrode may include a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may include a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may include one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0044] In some implementations of the disclosure, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed

from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0045] As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[0046] One or more interlayer dielectrics (ILDs) may be deposited over the MOS transistors. In general, an ILD or inter metal dielectric (IMD) refers to an insulating material used between metal conductors and devices (such as transistors) in integrated circuit devices. ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide, carbon-doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

[0047] Referring to FIG. 2, the first method 200 may begin with 202 where a structure with one or more openings is provided. An example of such a structure is a structure 302 shown in FIG. 3A.

[0048] As shown in FIG. 3A, the structure 302 includes what is referred to herein as a “gapfill base layer” 320 because this is a layer in which one or more openings (gaps) to be filled with one or more dielectric materials using host matrix infiltration described herein will be provided. An example of

FIG. 3A illustrates two openings 322, indicated as a first opening 322-1 and a second opening 322-2, formed within the gapfill base layer 320. The openings 322 within the gapfill base layer 320 are to be filled with one or more dielectric materials using host matrix infiltration described herein.

[0049] In general, the structure provided at 202 may be provided over any of the substrates described herein.

[0050] In some embodiments, the gapfill base layer 320 may be a layer of one or more electrically conductive materials which may e.g. be a part of a metallization stack in an IC die. Such a layer of one or more electrically conductive materials may be a patterned layer, e.g. a layer in which one or more trenches are formed, e.g. if the structure is a part of a metallization stack.

[0051] In some embodiments, the gapfill base layer 320 may be a layer of one or more dielectric material(s). Providing the openings 322 filled with a dielectric material different from those of the surrounding layer may be useful in scenarios where providing regions of dielectric materials with sufficient etch selectivity is desired, i.e. the dielectric material of the opening 322 would not be substantially etched when etchants which can etch the dielectric material of the surrounding dielectric gapfill base layer 320 are used, or/and vice versa.

[0052] Some examples of devices/assemblies where the opening 322 filled with one or more dielectric materials as described herein may be provided are shown in FIG. 3L, described below.

[0053] It should be noted that, in various embodiments, the structures as shown in FIGS. 3A-3L may include additional layers below the views shown in FIGS. 3A-3L, such as e.g. layers below the gapfill layer 320 which have other features (e.g. additional metallization layers) or a carrier substrate commonly used to provide mechanical support during manufacture (e.g., a metal sheet, a dielectric material, or a reinforced dielectric material).

[0054] In some embodiments, each of the openings 322 may have an AR between about 1 and 20, including all values and ranges therein, such as e.g. between about 1 and 15 or between about 5 and 10. In some embodiments, each of the openings 322 may have a depth between about 5 and 100 nm, including all values and ranges therein, such as e.g. between about 10 and 80 nm or between about 20 and 50 nm. In some embodiments, each of the openings 322 may have a width between about 1 nm and several micrometers (microns), including all values and ranges therein, such as e.g. between about 5 and 500 nm or between about 5 and 50 nm.

[0055] In some embodiments, more than two openings 322 may be provided within the gapfill base layer 320 provided at 202, the openings 322 having a pitch (i.e. a center-to-center distance between a pair of two adjacent openings) between e.g. about 10 and 200 nm, including all values and ranges therein. In other embodiments, any other patterns of openings 322 may be used as well. In still other embodiments, the structure 302 may include any other number of one or more openings,

different instances of which openings may but do not have to have the same shape and/or dimensions.

[0056] The method 200 may then proceed with 204, where the openings 322 are filled with a material of a host matrix. A result of this is shown in FIG. 3B with a structure 304 which illustrates that the openings 322 in the gapfill base layer 320 of the structure 302 are now filled with a solid host matrix material 324.

[0057] The material for a host matrix should be such that, in its fluid form, it can fill openings, including high AR openings as described herein, substantially uniformly (i.e. have good gapfill capabilities where it can fill the openings substantially without forming voids), and that, when solidified, the material would form pores which can subsequently be infiltrated by fluid dielectric precursors and would form nucleation sites for growing solid dielectric material from the infiltrated dielectric precursors.

[0058] Polymeric materials containing nucleation sites in the backbone such as e.g. poly(methyl methacrylate) (PMMA), polyethylene oxide (PEO), or poly(2-vinylpyridine) (P2VP) are examples of such materials for a host matrix because they have excellent gapfill capabilities and can be infiltrated with a variety of dielectric precursors using ALD, CVD, or liquid-phase chemistry. In various embodiments, such polymeric materials may have a molecular weight between about 1k and 100k g/mol, including all values and ranges therein. The molecular weight may be tuned to be suitable for the width and/or the AR of the openings 322. In general, any polymeric materials that have polar, electron-rich, or hydrophilic functional groups, such as e.g. one or more of hydroxyl groups, alkene groups, alkyne groups, alkoxy groups, ester groups, ether groups, amine groups, and carbonyl groups, may be used as a host matrix material. Such materials are particularly suitable for use with the metal oxide ALD/CVD dielectric precursors to be infiltrated at a later process.

[0059] Other examples of materials which may be used as a host matrix material provided at 204 include non-polymeric materials having hydroxyl functional groups and interconnected to form pores, such as e.g. silicon oxide, carbon-doped silicon oxide, aluminum-doped silicon oxide, metal oxides such as aluminum oxide, hafnium oxide, zirconium oxide, etc.

[0060] In various embodiments, providing the host matrix within the plurality of openings at 204 may include performing spin-coating of one or more materials of the future host matrix onto the structure 302 or dip-coating the structure 302 in such materials as known in the art. For example, for spin-coating, spin speed of about 100 - 5000 revolutions per minute may be used, with the spin time of about 10-300 seconds.

[0061] The checkered pattern shown in FIG. 3B is intended to schematically illustrate that, once filled into the openings 322, the solidified host material 324 (shown in black) includes pores (shown

in white) distributed substantially uniformly throughout the openings 322. In various embodiments, such pores may have dimensions between about 0.2 and 5 nm, including all values and ranges therein.

[0062] FIG. 3B illustrates an embodiment of process 204 where the host material 324 fills up the opening 322 completely, i.e. the upper surface 326 of the host material 324 is aligned with the upper surface 328 of the gapfill base layer 320. In some embodiments, initially the host material 324 may first be deposited over the upper surfaces 328 of the gapfill base layer 320, which excess of the host material may then be removed, e.g. using chemical mechanical polishing, dry etching, wet etching or ashing, to arrive with the scenario as shown in FIG. 3B. In other embodiments, the process 204 may be performed so that the host material 324 fills only a certain lower portion of the openings 322, as e.g. shown in FIG. 3C.

[0063] In case it is desirable to ensure that the host matrix material 324 does not fill the openings 322 completely but only fills a certain lower portion of the openings 322, the method 200 may then proceed with 206 where the host matrix material provided at 204 is recessed to a desired depth (thus, as indicated in FIG. 2, process 206 is optional). A result of this is shown in FIG. 3C with a structure 306' which illustrates that the host matrix material 324 is recessed within the openings 322 by a recess depth 330. In various embodiments, the recess depth 330 may be between 10 and 90 % of the depth of the openings 322, including all ranges and values therein. Forming such recesses may be desirable in case of e.g. generating a bilayer of two dielectric materials on top of each other or a bilayer of a metal and a dielectric, or multilayers of alternating dielectric or metal layers, etc. Often dielectric materials either display high etch resistance or low dielectric constant, but rarely both properties. In case of a dielectric bilayer it may be attractive to have a material with high etch resistance on top and a material with the desired low dielectric constant at the bottom.

[0064] In some embodiments, recesses of the host material 324 to the depth 330 may be formed by irradiating a structure resulting from the process 204 (e.g. the structure 304) with optical radiation, e.g. by applying ultraviolet (UV) radiation, to cross-link on or more materials of the host matrix 324 to the specified depth (e.g. to cross-link the polymers of the host matrix 324), followed by selectively etching the one or more materials of the host matrix 324 which were not cross-linked.

[0065] In some embodiments when the host matrix material 324 is recessed within the openings, as a subsequent part of the process 206, the sidewalls of the openings 322 which become exposed due to the recess may be passivated in order to reduce or eliminate nucleation of the dielectric materials on the sidewalls once the fluid dielectric precursors are provided. A result of this is shown in FIG. 3D with a structure 306'' which illustrates a layer of a passivation material 332 provided on such sidewalls of the openings 322.

[0066] Such passivation may e.g. include processing the surface of the inner sidewalls to make them hydrophobic, e.g. using self-assembled monolayers (SAMs), hydrophobic polymers, implanting of carbon and fluorine. SAM's that attach to dielectric surfaces may be assembled in the solution, spin-coating or vapor phase using molecules with small or long (C1-C22) alkyl chains or fluorinated chains and head groups that may include alkoxysilanes, aminosilanes and chlorosilanes. SAMs that attach to metals or metal oxides may be assembled in the solution, spin-coating or vapor phase using molecules with head groups such as alkenes, alkynes, amines, phosphines, thiols, phosphonic acids or carboxylic acids that selectively combine to metals. Octadecylphosphonic acid or octadecylthiol are common examples of chemical compounds that can be used as passivants.

[0067] In some embodiments, a thickness of the passivation layer 332 (i.e. a dimension measured in the horizontal direction shown in FIG. 3D) may be between about 0.5 and 5 nm, including all values and ranges therein.

[0068] Once the solid host matrix is provided within the openings 322, the method 200 may proceed with 208, where the porous host matrix material 324 is infiltrated with one or more dielectric precursors which form a solid dielectric material 334 within the pores of the host matrix 324. A result of this is shown in FIG. 3E with a structure 308 which illustrates that the pores within the host matrix material 324 are filled with the dielectric material 334.

[0069] In some embodiment, ALD or CVD processes may be used to provide the dielectric precursors into the pores of the host matrix 324. To that end, one or more reactive dielectric precursor gases are introduced into a reaction chamber and directed towards a substrate (e.g. any one of the structures 304, 306', or 306'') in order to induce controlled chemical reactions that result in growth of the dielectric material 334 on the host material 324. In some embodiments, co-reactants such as e.g. water or isopropanol may also be provided during the ALD/CVD process in order to promote nucleation of the dielectric material on the material of the host matrix 324. In some embodiments, the ALD/CVD may need to be adjusted according to the melting point and thermal stability of the host material.

[0070] The choice of the dielectric precursors and, possibly co-reactants, used in the ALD/CVD process carried out at 208 would depend on the dielectric material 334 which is to be grown. For example, in case the dielectric material 334 is a metal oxide, the choice of the dielectric precursors and, possibly co-reactants would depend on which metal oxide is to be grown. If the dielectric material 334 is aluminum oxide, the one or more dielectric precursors infiltrated into the host matrix 324 at 208 may include TMA and a co-reactant such as e.g. water or isopropanol. If the dielectric material 334 is hafnium oxide, the one or more dielectric precursors infiltrated into the host matrix

324 at 208 may include (ethylmethylamino) hafnium (Hf-EMA), e.g. tetrakis (ethylmethylamino) hafnium (Hf(EMA)₄) or/and hafnium chloride, e.g. hafnium tetrachloride (HfCl₄), and a co-reactant such as e.g. water or isopropanol. If the dielectric material 334 is titanium oxide, the one or more dielectric precursors infiltrated into the host matrix 324 at 208 may include titanium chloride, e.g. titanium tetrachloride (TiCl₄), and a co-reactant such as e.g. water or alcohols such as ethanol or isopropanol or gases such as silane, ammonia, hydrogen. In general, a suitable co-reactant which may be used with any of the above-mentioned dielectric precursors may be a compound that converts the metal containing precursor into the corresponding metal oxide or nitride. If the dielectric material 334 is a mixture of silicon oxide and aluminum oxide, the one or more dielectric precursors infiltrated into the host matrix 324 at 208 may include TMA and silanol.

[0071] As an alternative to ALD/CVD processes described above where dielectric precursors are provided as gases, the infiltration can also happen in a solution phase (i.e. the dielectric precursors may be liquid) though sol-gel reactions involving the reaction of metal alkoxides, such as e.g. hafnium isopropoxide, metal nitrates, such as e.g. aluminum nitrates, and a suitable co-reactant such as e.g. water or ethanol, and, possibly, an appropriate thermal treatment. The liquid dielectric precursors may be provided by spin-coating or dip-coating on the structure with the host matrix 324 in the openings, such as e.g. any one of the structures 304, 306', or 306". Examples of the dielectric materials 334 which may be formed by sol-gel process include, but are not limited to, cerium oxide, iron oxide, hafnium oxide, titanium oxide, copper oxide, and aluminum oxide. In such processes, a dielectric precursor may be the sol (monomer) that has low viscosity and can permeate between the polymer chains of the host material 324, and the gel forms when the co-reactant cross links the sol to form a metal oxide polymer. In some embodiments, a suitable thermal treatment or thermal treatment successively or concurrently combined with UV-light treatment may be used to convert the gel into a more ceramic or a more metal oxide like material (where "more metal oxide like" generally means three-dimensional network formation, some crystalline order, less/no organic/carbon bonds and more inorganic bonds metal to oxygen).

[0072] In various embodiments, the amount of the dielectric material 334 within the host matrix material 324 may be between about 1% and 70% of the total volume of the openings 322 occupied by the host matrix material 324, including all ranges and values therein, e.g. between about 10% and 70%.

[0073] It should be noted that while FIG. 3E and, subsequently, FIGS. 3F-3K illustrate embodiments of dielectric precursor infiltration and subsequent processes carried out on the structure 304, descriptions of the method 200 provided herein are equally applicable, possibly with minor

modifications which would be apparent to a person of ordinary skill in the art based on the present disclosure, to performing these processes on the structures 306' or 306".

[0074] Turning back to FIG. 2, once the host matrix 324 has been infiltrated with the dielectric material 334, some or all of the host matrix material 324 may be removed, at 210. A result of this is shown in FIG. 3F with a structure 310 which illustrates an embodiment where all of the host matrix material 324 is removed. In other embodiments, some of the host matrix may be left behind, either deliberately (e.g. in order to improve the mechanical strength/elastic modulus of the structure) or unintentionally due to manufacturing limitations. Presence of such the host matrix material 324 may be detected in a cross-sectional TEM or SEM images of the final structures, or/and by performing a compositional analysis of the final structures.

[0075] In some embodiments, removing the host matrix 324 may include etching or ashing the host matrix material using an appropriate etchant or ashing process. For example, ashing as conventionally used in photolithography in order to remove photomasks of polymer materials (e.g. PMMA) may be used for this purpose. In other examples, removal of the host matrix 324 may include UV cross linking of the polymer followed by dissolution in an organic solvent such as isopropanol or acetic acid, or by strongly oxidizing peroxide-based wet etch that does not attack the infiltrated dielectric material.

[0076] As is shown in the schematic illustration of FIG. 3F, removal of the host matrix material 324 results in formation of pores in the dielectric material 334. However, in contrast to the conventional techniques described above, the pores are much smaller in their dimension than voids which could be formed when using conventional techniques, and are distributed more uniformly throughout the opening (although there may be some differences in the porosity throughout the volume of the opening, as described below with reference to FIGS. 4A-4B, 5A-5B, and 6A-6B). In some embodiments, the largest dimension of each of the pores formed as a result of removing the host matrix material 324 from the openings 322 may be less than about 5 nm, including all values and ranges therein, e.g. less than about 3 nm or less than about 1 nm. Thus, because use of a host matrix material avoids formation of keyhole-type seam voids (i.e. voids substantially in the center of an opening) which would often be much larger in dimensions, the resulting dielectric material filling the openings 322 does not have voids (or seams) either.

[0077] In some embodiments, a volume of the pores formed within the dielectric material 334 as a result of the removal of at least a part of the host matrix material 324 at 210 may be between *about* 1% and 70% of a volume of the each opening.

[0078] According to various embodiments of the present disclosure, the density of the dielectric material 334 in a central portion of each opening 322 (which central portion may be about 50%, or

about 33% or about 25%, of a total volume of each opening) may be substantially equal to the density of the dielectric material in the remaining portion of each opening (the remaining portion being a portion of the total volume that does not include the central portion). Such central portions are illustrated in FIG. 3F with central portions 336 (thick dashed lines, shown in FIG. 3F as a central portion 336-1 within the opening 322-1 and a central portion 336-2 within the opening 322-2) within each opening 322, centered along centers of the openings 338 (shown in FIG. 3F as a centerline 338-1 within the opening 322-1 and a centerline 338-2 within the opening 322-2).

[0079] In some embodiments, the method 200 may stop at this point. In other embodiments, the method 200 may proceed with an optional process 212 where the porous structure of the dielectric material 334 created as a result of removing at least a portion of the host matrix material 324 may be infiltrated with same or different dielectric precursors as those used previously to form the dielectric material 334 within the host matrix 324. To that end, any one of the infiltration processes similar to those described above with reference to the process 208 may be used for the process 212, except that now the porous network of the dielectric material 334 acts as a host matrix, instead of the host matrix material 324 (or in addition to the host matrix 324, in case any of this material remains in the openings after the process 210).

[0080] A result of performing the process 212 using different dielectric precursors than those used at the process 208 is shown in FIG. 3G with a structure 312', showing that the infiltration of the process 212 results in formation of a second dielectric material, the dielectric material 340, within the pores of the first dielectric material 334. In this manner, hybrid materials may be provided within the openings 322, which is a way to fine-tune various dielectric properties of the materials filling the openings 322. For example, the first dielectric material 334 may be aluminum oxide and the second dielectric material 340 may be hafnium oxide, or vice versa, so that, overall, the materials filling the openings 322 have the improved etch performance but not the high dielectric constant compared to openings filled completely with hafnium oxide.

[0081] A result of performing the process 212 using the same dielectric precursor(s) as those used at the process 208 is shown in FIG. 3F with a structure 312'', showing that the infiltration of the process 212 allows densifying the dielectric material 334 within the openings 322. By repeating the infiltration with the same precursors again, the dielectric precursors of the process 212 can get into the pores in the dielectric material 334 and nucleate on the surfaces of the dielectric material 334 or on the remaining portions of the original host matrix 324. In some such embodiments, substantially the entire volume of the openings 322 may be filled with the dielectric material 334, without the voids or seams undesirably characteristic of conventional gapfill techniques.

[0082] The method 200 may also include an optional process 214, where the one or more openings 322 may be sealed with a capping layer once the desired dielectric material has been provided therein. The process 214 may follow the process 212, or, in the embodiments where the process 212 is not used, follow the process 210.

[0083] A result of performing the process 214 following the process 212 where different dielectric precursors were used than those used at the process 208 is shown in FIG. 3I with a structure 314'. A result of performing the process 214 using the same dielectric precursor(s) as those used at the process 208 is shown in FIG. 3J with a structure 314". Finally, a result of performing the process 214 when the process 212 was not used (i.e. the process 214 follows the process 210 in absence of the process 212) is shown in FIG. 3K with a structure 314"". All of these structures which may result from the process 214 illustrate a capping layer 342 provided over the dielectric material(s) within the openings 322.

[0084] In some embodiments, the capping layer material 342 may be the same dielectric material as any of the dielectric materials infiltrated within the openings 322 as described above, which may be attractive for applications where e.g. the etch properties of a particular dielectric material are desired but not the high dielectric constant which would result from the complete fill of the openings 322 with such dielectric. For example, the structure 314"" may be such that the capping layer 342 and the dielectric material 334 is hafnium oxide, resulting in a structure that has etch characteristics of hafnium oxide capping the openings 322 (which etch characteristics are often desirable for manufacturing of IC components), but advantageously having a reduced dielectric constant in the openings 322 as compared to if the dielectric material 334 in the openings 322 was not porous but fully filled with hafnium oxide.

[0085] In other embodiments, the capping layer material 342 may be a different dielectric material than that of any of the dielectric materials infiltrated within the openings 322 as described above, which may be attractive for applications where e.g. different dielectric properties are desirable for the capping layer 342 and the dielectric material filling the openings 322. For example, the capping material 342 may have improved (enhanced) etch resistance compared to the dielectric material within the openings 322, and may act as an etch stop to certain etchants. Such a capping material may e.g. include hafnium oxide, while the dielectric material within the openings (i.e. the dielectric material 334 and/or the dielectric material 340) may e.g. be aluminum oxide. While porous aluminum oxide advantageously has relatively low dielectric constant, it has poor etch resistance to certain commonly used etchants. By providing a hafnium oxide capping layer 342, enhanced etch resistance may be achieved over the dielectric material in the openings 322, while advantageously preserving the relatively low dielectric constant of the dielectric material in these openings. In other

words, providing such a capping layer allows benefiting from the improved etch resistance without the associated high dielectric constant of the openings being filled with the material of the capping layer.

[0086] In various embodiments described above, excess dielectric material which may incidentally be deposited on the upper surfaces of the gapfill base layer 320 may be removed at any suitable point in time, e.g. by performing polishing to expose the uppermost surfaces of the gapfill base layer 320. For example, the excess dielectric material may be removed before or/and after one or more of the processes 210, 212, and 214.

[0087] As previously described herein, the devices and assemblies utilizing structures having openings with infiltrated dielectric materials as described herein could be a part of a semiconductor device or an IC package, e.g. a part of an interconnect, e.g. a backend interconnect, in a semiconductor device or an IC package, and/or could be used to electrically isolate different electrically conductive regions from one another.

[0088] In one example, one or more of the openings 322 may be used as so-called “plugs” commonly employed in metallization stacks, where a plug refers to a region in a metallization stack (e.g. a region cut out in a trench or between two trenches) where the electrically conductive material (e.g. any one of suitable metals commonly used in metallization stacks) of a given trench is removed and a dielectric material is filled in instead. Such a scenario is illustrated with a structure 362 of FIG. 3L, showing the opening 322 (which opening is filled with one or more dielectric materials in accordance with any of the embodiments described herein) being provided as a cut/plug in a first trench 344 (i.e. in this situation the gapfill base layer 320 described herein refers to the material of the trench 344 formed on a substrate).

[0089] In another example, one or more of the openings 322 may be created in a layer of an electrically conductive material as a part of patterning the layer to form trenches, where the dielectric material filled in such openings may serve to provide electrical isolation between different trenches. Such a scenario is illustrated with a structure 364 of FIG. 3L, showing the opening 322 (which opening is filled with one or more dielectric materials in accordance with any of the embodiments described herein) being provided to separate a first trench 346 from a second trench 348 (i.e. in this situation the gapfill base layer 320 described herein refers to the material(s) of the first trench 346 and the second trench 348, where, for ease of fabrication, the materials of the first and second trenches are typically, but not necessarily, the same conductive materials formed on a substrate).

[0090] In yet another example, the one or more openings 322 may be created in a layer of a dielectric material provided over a layer that contains one or more trenches, where the dielectric

material filled in such openings may serve to cap the trenches. Such a scenario is illustrated with a structure 366 of FIG. 3L, showing a trench layer 350 comprising a trench 352, and a dielectric layer 354 provided over the trench layer 350, where the opening 322 (which opening is filled with one or more dielectric materials in accordance with any of the embodiments described herein) is provided in the dielectric layer 354 to effectively cap the trench 352 (i.e. in this situation the gapfill base layer 320 described herein refers to the material of the dielectric layer 354 provided above the trench layer 352). Providing the opening 322 filled with a dielectric material that has sufficient etch selectivity compared to the material of the surrounding dielectric layer 354 may be used to make an electrical connection to the trench 352 by etching the dielectric material of the opening 322 without substantially etching the material of the dielectric layer 354. This is advantageous because, otherwise, etching a dielectric material covering the trench layer to expose and make a contact to the trench 352 may result in accidentally exposing and contacting other trenches which may be present within the trench layer 350, other trenches not specifically shown in the structure 366, a problem commonly described in the art as a “contact edge placement error” (i.e. misalignment resulting in electrical short between a via or contact and wrong metal trench/via).

[0091] In various embodiments, the use of the host matrix infiltration methods as described herein may be detected by examining cross-sections of the final structures using e.g. TEM or SEM.

Examples of what could be detected in cross-sectional SEM or TEM images are shown in FIGS. 4A-4B, 5A-5B, and 6A-6B, where each pair of these drawings (e.g. a pair of FIGS. 4A-4B, a pair of FIGS. 5A-5B, or a pair of FIGS. 6A-6B) provides illustrations of exemplary real world structures with openings of different profiles being filled with a dielectric material using, respectively, a conventional method and a host matrix infiltration method described herein. As can be seen, each of FIGS. 4A-4B, 5A-5B, and 6A-6B is drawn to reflect example real world process limitations, in that the features are not drawn with precise right angles and straight lines.

[0092] FIGS. 4A and 4B are illustrations of exemplary real world structures 400A and 400B with openings 422A and 422B having a straight profile filled with dielectric materials 434A and 434B using, respectively, a conventional method and a host matrix infiltration method described herein. The opening 422A is one real world example of the opening 122 described herein, the opening 422B may be viewed as one real world example of one of the openings 322 described herein, while 420 illustrates a gapfill base layer in which the openings are provided. Thus, the dielectric material 434A filling the opening 422A is the dielectric material 124 described above, the dielectric material 434B filling the opening 422B is any of the dielectric materials described above with reference to FIG. 2 and FIGS. 3A-3L, and the gapfill base layer 420 is the gapfill base layer 320 described above

[0093] As can be seen in the structure 400A, use of the conventional techniques to fill a straight opening 422A often results in formation of a void 426 (similar to the void 126 described above) substantially in the center of the opening 42A. In contrast, the structure 400B does not have such a void, but may have pores 470 (white objects shown within the dielectric material 434B, where, in order to not clutter the drawing, only some of these objects, not all, are labeled with the reference numeral 470).

[0094] The structure 400B further illustrates that, in some implementations, there may be a density gradient in the dielectric material 434B from top to bottom, in that the density of the dielectric material 434B in an upper portion 472 of the opening 422B (a portion outlined with a dashed line) may be higher (i.e. in the upper portion 474, the pores 470 occupy a smaller proportion of the volume of the dielectric material 434B) than that in a lower portion 474 (a portion outlined with a dotted line), which portions are schematically illustrated in FIG. 4B (in other embodiments, the upper and lower portions 472, 474 may have different sizes relative to one another).

[0095] The structure 400B also illustrates that, in some implementations, there may be a density gradient in the dielectric material 434B from sidewalls to the center of the opening 422B, in that the density of the dielectric material 434B in sidewall portions 476 of the opening 422B (a portion to the left of a dash-dotted line 480-1 and a portion to the right of a dash-dotted line 480-2, shown in FIG. 4B) may be higher (i.e. in the sidewall portions 476, the pores 470 occupy a smaller proportion of the volume of the dielectric material 434B) than that in a center portion 478 (a portion between the lines 480-1 and 480-2), which portions are also schematically illustrated in FIG. 4B (in other embodiments, the sidewall and center portions 476, 478 may have different sizes relative to one another).

[0096] FIGS. 5A and 5B are illustrations of exemplary real world structures 500A and 500B with openings 522A and 522B having a re-entrant profile filled with dielectric materials 434A and 434B using, respectively, a conventional method and a host matrix infiltration method described herein. The opening 522A is another real world example of the opening 122 described herein, while the opening 522B may be viewed as another real world example of one of the openings 322 described herein. Elements of FIGS. 5A and 5B having the same reference numerals as those used in FIGS. 4A and 4B refer to analogous elements, descriptions of which provided with respect to one of the set of drawings (e.g. FIGS. 4A and 4B) are not repeated for the other set (e.g. FIGS. 5A and 5B.)

[0097] As can be seen in the structure 500A, use of the conventional techniques to fill a re-entrant opening 522A often results in formation of a keyhole-shaped void 526 (similar to the void 126 described above) substantially along a centerline of the opening 522A (i.e. the dielectric material

434A pinches off at the top). In contrast, the structure 500B does not have such a void, but may have pores and density gradients as described above with reference to FIGS. 4A and 4B.

[0098] FIGS. 6A and 6B are illustrations of exemplary real world structures 600A and 600B with openings 622A and 622B having a non-re-entrant profile filled with dielectric materials 434A and 434B using, respectively, a conventional method and a host matrix infiltration method described herein. The opening 622A is yet another real world example of the opening 122 described herein, while the opening 622B may be viewed as yet another real world example of one of the openings 322 described herein. Elements of FIGS. 6A and 6B having the same reference numerals as those used in FIGS. 4A and 4B refer to analogous elements, descriptions of which provided with respect to one of the set of drawings (e.g. FIGS. 4A and 4B) are not repeated for the other set (e.g. FIGS. 6A and 6B.)

[0099] As can be seen in the structure 600A, use of the conventional techniques to fill a non-re-entrant opening 622A often results in formation of a seam 626 substantially along a centerline of the opening 622A. In contrast, the structure 600B does not have such a seam, but may have pores and density gradients as described above with reference to FIGS. 4A and 4B.

[0100] In some implementations of the structures 400B, 500B, and 600B there may be only one of the density gradients present – e.g. only a density gradient from top to bottom or only a density gradient from sidewalls to center. In other implementations, both of these density gradients may be present.

[0101] Structures having openings with infiltrated dielectric materials as disclosed herein may be included in any suitable electronic device. FIGS. 7-10 illustrate various examples of apparatuses that may include such structures.

[0102] FIGS. 7A-B are top views of a wafer 2000 and dies 2002 that may include one or more structures which have openings with infiltrated dielectric materials in accordance with any of the embodiments disclosed herein. The wafer 2000 may be composed of semiconductor material and may include one or more dies 2002 having IC structures formed on a surface of the wafer 2000. Each of the dies 2002 may be a repeating unit of a semiconductor product that includes any suitable IC (e.g., ICs including one or more components having structures with openings with infiltrated dielectric materials as described herein). After the fabrication of the semiconductor product is complete (e.g., after manufacture of one or more components having structures with openings with infiltrated dielectric materials as described herein), the wafer 2000 may undergo a singulation process in which each of the dies 2002 is separated from one another to provide discrete "chips" of the semiconductor product. In particular, devices that include one or more components having structures with openings with infiltrated dielectric materials as disclosed herein may take the form

of the wafer 2000 (e.g., not singulated) or the form of the die 2002 (e.g., singulated). The die 2002 may include one or more transistors (e.g., one or more of the transistors 2140 of FIG. 8, discussed below, and/or supporting circuitry to route electrical signals to the transistors, as well as any other IC components, each of which may include structures with openings with infiltrated dielectric materials as described herein. In some embodiments, the wafer 2000 or the die 2002 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., an AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 2002. For example, a memory array formed by multiple memory devices may be formed on a same die 2002 as a processing device (e.g., the processing device 2302 of FIG. 10) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0103] FIG. 8 is a cross-sectional side view of an IC device 2100 that may include one or more structures which have openings with infiltrated dielectric materials in accordance with any of the embodiments disclosed herein. The IC device 2100 may be formed on a substrate 2102 (e.g., the wafer 2000 of FIG. 7A) and may be included in a die (e.g., the die 2002 of FIG. 7B). The substrate 2102 may be a semiconductor substrate composed of semiconductor material systems including, for example, N-type or P-type materials systems. The substrate 2102 may include, for example, a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In some embodiments, the semiconductor substrate 2102 may be formed using alternative materials, which may or may not be combined with silicon, that include, but are not limited to, germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. Further materials classified as group II-VI, III-V, or IV may also be used to form the substrate 2102. Although a few examples of materials from which the substrate 2102 may be formed are described here, any material that may serve as a foundation for an IC device 2100 may be used. The substrate 2102 may be part of a singulated die (e.g., the dies 2002 of FIG. 7B) or a wafer (e.g., the wafer 2000 of FIG. 7A).

[0104] The IC device 2100 may include one or more device layers 2104 disposed on the substrate 2102. The device layer 2104 may include features of one or more transistors 2140 (e.g., MOSFETs) formed on the substrate 2102. The device layer 2104 may include, for example, one or more source and/or drain (S/D) regions 2120, a gate 2122 to control current flow in the transistors 2140 between the S/D regions 2120, and one or more S/D contacts 2124 to route electrical signals to/from the S/D regions 2120. The S/D regions 2120 may be formed within the substrate 2102 adjacent to the gate 2122 of each transistor 2140, using any suitable processes known in the art, some of which are described above. The transistors 2140 may include additional features not depicted for the sake of

clarity, such as device isolation regions, gate contacts, and the like. The transistors 2140 are not limited to the type and configuration depicted in FIG. 8 and may include a wide variety of other types and configurations such as, for example, planar transistors, non-planar transistors, or a combination of both. Non-planar transistors may include FinFET transistors, such as double-gate transistors or FinFETs, and wrap-around or all-around gate transistors, such as nanoribbon and nanowire transistors. In particular, at least some of the one or more of the transistors 2140 may include structures which have openings with infiltrated dielectric materials disclosed herein.

[0105] Each transistor 2140 may include a gate 2122 formed of at least two layers, a gate dielectric layer and a gate electrode layer. Generally, the gate dielectric layer of a transistor 2140 may include one layer or a stack of layers, and the one or more layers may include silicon oxide, silicon dioxide, and/or a high-k dielectric material.

[0106] In some embodiments, when viewed as a cross section of the transistor 2140 along the source-channel-drain direction, the gate electrode may include a U-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate (e.g., in a FinFET). In other embodiments, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In other embodiments, the gate electrode may include a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may include one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers. In some embodiments, the gate electrode may include a V-shaped structure (e.g., when the fin of a FinFET does not have a "flat" upper surface, but instead has a rounded peak).

[0107] In some embodiments, a pair of sidewall spacers may be formed on opposing sides of the gate stack to bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In some embodiments, a plurality of spacer pairs may be used; for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0108] Electrical signals, such as power and/or input/output (I/O) signals, may be routed to and/or from the transistors 2140 of the device layer 2104 through one or more interconnect layers disposed on the device layer 2104 (illustrated in FIG. 8 as interconnect layers 2106-2110). For example, electrically conductive features of the device layer 2104 (e.g., the gate 2122 and the S/D contacts

2124) may be electrically coupled with the interconnect structures 2128 of the interconnect layers 2106-2110. The one or more interconnect layers 2106-2110 may form an ILD stack 2119 of the IC device 2100. Although not specifically shown in FIG. 8, each of the one or more interconnect layers 2106-2110 may advantageously include one or more structures which have openings with infiltrated dielectric materials in accordance with any of the embodiments disclosed herein.

[0109] The interconnect structures 2128 may be arranged within the interconnect layers 2106-2110 to route electrical signals according to a wide variety of designs (in particular, the arrangement is not limited to the particular configuration of interconnect structures 2128 depicted in FIG. 8). Although a particular number of interconnect layers 2106-2110 is depicted in FIG. 8, embodiments of the present disclosure include IC devices having more or fewer interconnect layers than depicted.

[0110] In some embodiments, the interconnect structures 2128 may include trench structures 2128a (sometimes referred to as "lines") and/or via structures 2128b (sometimes referred to as "holes") filled with an electrically conductive material such as a metal. The trench structures 2128a may be arranged to route electrical signals in a direction of a plane that is substantially parallel with a surface of the substrate 2102 upon which the device layer 2104 is formed. For example, the trench structures 2128a may route electrical signals in a direction in and out of the page from the perspective of FIG. 8. The via structures 2128b may be arranged to route electrical signals in a direction of a plane that is substantially perpendicular to the surface of the substrate 2102 upon which the device layer 2104 is formed. In some embodiments, the via structures 2128b may electrically couple trench structures 2128a of different interconnect layers 2106-2110 together.

[0111] The interconnect layers 2106-2110 may include a dielectric material 2126 disposed between the interconnect structures 2128, as shown in FIG. 8. In some embodiments, the dielectric material 2126 disposed between the interconnect structures 2128 in different ones of the interconnect layers 2106-2110 may have different compositions; in other embodiments, the composition of the dielectric material 2126 between different interconnect layers 2106-2110 may be the same.

[0112] A first interconnect layer 2106 (referred to as Metal 1 or "M1") may be formed directly on the device layer 2104. In some embodiments, the first interconnect layer 2106 may include trench structures 2128a and/or via structures 2128b, as shown. The trench structures 2128a of the first interconnect layer 2106 may be coupled with contacts (e.g., the S/D contacts 2124) of the device layer 2104.

[0113] A second interconnect layer 2108 (referred to as Metal 2 or "M2") may be formed directly on the first interconnect layer 2106. In some embodiments, the second interconnect layer 2108 may include via structures 2128b to couple the trench structures 2128a of the second interconnect layer 2108 with the trench structures 2128a of the first interconnect layer 2106. Although the trench

structures 2128a and the via structures 2128b are structurally delineated with a line within each interconnect layer (e.g., within the second interconnect layer 2108) for the sake of clarity, the trench structures 2128a and the via structures 2128b may be structurally and/or materially contiguous (e.g., simultaneously filled during a dual-damascene process) in some embodiments.

[0114] A third interconnect layer 2110 (referred to as Metal 3 or "M3") (and additional interconnect layers, as desired) may be formed in succession on the second interconnect layer 2108 according to similar techniques and configurations described in connection with the second interconnect layer 2108 or the first interconnect layer 2106.

[0115] The IC device 2100 may include a solder resist material 2134 (e.g., polyimide or similar material) and one or more bond pads 2136 formed on the interconnect layers 2106-2110. The bond pads 2136 may be electrically coupled with the interconnect structures 2128 and configured to route the electrical signals of the transistor(s) 2140 to other external devices. For example, solder bonds may be formed on the one or more bond pads 2136 to mechanically and/or electrically couple a chip including the IC device 2100 with another component (e.g., a circuit board). The IC device 2100 may have other alternative configurations to route the electrical signals from the interconnect layers 2106-2110 than depicted in other embodiments. For example, the bond pads 2136 may be replaced by or may further include other analogous features (e.g., posts) that route the electrical signals to external components.

[0116] FIG. 9 is a cross-sectional side view of an IC device assembly 2200 that may include one or more structures which have openings with infiltrated dielectric materials in accordance with any of the embodiments disclosed herein. The IC device assembly 2200 includes a number of components disposed on a circuit board 2202 (which may be, e.g., a motherboard). The IC device assembly 2200 includes components disposed on a first face 2240 of the circuit board 2202 and an opposing second face 2242 of the circuit board 2202; generally, components may be disposed on one or both faces 2240 and 2242. In particular, any suitable ones of the components of the IC device assembly 2200 may include any of the structures having openings with infiltrated dielectric materials in accordance with any of the embodiments disclosed herein.

[0117] In some embodiments, the circuit board 2202 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 2202. In other embodiments, the circuit board 2202 may be a non-PCB substrate.

[0118] The IC device assembly 2200 illustrated in FIG. 9 includes a package-on-interposer structure 2236 coupled to the first face 2240 of the circuit board 2202 by coupling components 2216. The coupling components 2216 may electrically and mechanically couple the package-on-interposer structure 2236 to the circuit board 2202, and may include solder balls (as shown in FIG. 9), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0119] The package-on-interposer structure 2236 may include an IC package 2220 coupled to an interposer 2204 by coupling components 2218. The coupling components 2218 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 2216. Although a single IC package 2220 is shown in FIG. 9, multiple IC packages may be coupled to the interposer 2204; indeed, additional interposers may be coupled to the interposer 2204. The interposer 2204 may provide an intervening substrate used to bridge the circuit board 2202 and the IC package 2220. The IC package 2220 may be or include, for example, a die (the die 2002 of FIG. 7B), an IC device (e.g., the IC device 2100 of FIG. 8), or any other suitable component. Generally, the interposer 2204 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 2204 may couple the IC package 2220 (e.g., a die) to a ball grid array (BGA) of the coupling components 2216 for coupling to the circuit board 2202. In the embodiment illustrated in FIG. 9, the IC package 2220 and the circuit board 2202 are attached to opposing sides of the interposer 2204; in other embodiments, the IC package 2220 and the circuit board 2202 may be attached to a same side of the interposer 2204. In some embodiments, three or more components may be interconnected by way of the interposer 2204.

[0120] The interposer 2204 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some implementations, the interposer 2204 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 2204 may include metal interconnects 2208 and vias 2210, including but not limited to through-silicon vias (TSVs) 2206. The interposer 2204 may further include embedded devices 2214, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 2204. The package-on-interposer structure 2236 may take the form of any of the package-on-interposer structures known in the art.

[0121] The IC device assembly 2200 may include an IC package 2224 coupled to the first face 2240 of the circuit board 2202 by coupling components 2222. The coupling components 2222 may take the form of any of the embodiments discussed above with reference to the coupling components 2216, and the IC package 2224 may take the form of any of the embodiments discussed above with reference to the IC package 2220.

[0122] The IC device assembly 2200 illustrated in FIG. 9 includes a package-on-package structure 2234 coupled to the second face 2242 of the circuit board 2202 by coupling components 2228. The package-on-package structure 2234 may include an IC package 2226 and an IC package 2232 coupled together by coupling components 2230 such that the IC package 2226 is disposed between the circuit board 2202 and the IC package 2232. The coupling components 2228 and 2230 may take the form of any of the embodiments of the coupling components 2216 discussed above, and the IC packages 2226 and 2232 may take the form of any of the embodiments of the IC package 2220 discussed above. The package-on-package structure 2234 may be configured in accordance with any of the package-on-package structures known in the art.

[0123] FIG. 10 is a block diagram of an example computing device 2300 that may include one or more components including one or more structures having openings with infiltrated dielectric materials in accordance with any of the embodiments disclosed herein. For example, any suitable ones of the components of the computing device 2300 may include a die (e.g., the die 2002 (FIG. 7B)) having one or more interconnects or other IC chip components incorporating structures having openings with infiltrated dielectric materials in accordance with any of the embodiments disclosed herein. Any one or more of the components of the computing device 2300 may include, or be included in, an IC device 2100 (FIG. 8). Any one or more of the components of the computing device 2300 may include, or be included in, an IC device assembly 2200 (FIG. 9).

[0124] A number of components are illustrated in FIG. 10 as included in the computing device 2300, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the computing device 2300 may be attached to one or more motherboards. In some embodiments, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die.

[0125] Additionally, in various embodiments, the computing device 2300 may not include one or more of the components illustrated in FIG. 10, but the computing device 2300 may include interface circuitry for coupling to the one or more components. For example, the computing device 2300 may not include a display device 2306, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 2306 may be coupled. In another set of examples, the computing device 2300 may not include an audio input device 2318 or an audio

output device 2308, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 2318 or audio output device 2308 may be coupled.

[0126] The computing device 2300 may include a processing device 2302 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 2302 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices. The computing device 2300 may include a memory 2304, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the memory 2304 may include memory that shares a die with the processing device 2302. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random access memory (STT-MRAM).

[0127] In some embodiments, the computing device 2300 may include a communication chip 2312 (e.g., one or more communication chips). For example, the communication chip 2312 may be configured for managing wireless communications for the transfer of data to and from the computing device 2300. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0128] The communication chip 2312 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 2312 may operate in

accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 2312 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 2312 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 2312 may operate in accordance with other wireless protocols in other embodiments. The computing device 2300 may include an antenna 2322 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0129] In some embodiments, the communication chip 2312 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 2312 may include multiple communication chips. For instance, a first communication chip 2312 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 2312 may be dedicated to longer-range wireless communications such as global positioning system (GPS), EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 2312 may be dedicated to wireless communications, and a second communication chip 2312 may be dedicated to wired communications.

[0130] The computing device 2300 may include battery/power circuitry 2314. The battery/power circuitry 2314 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the computing device 2300 to an energy source separate from the computing device 2300 (e.g., AC line power).

[0131] The computing device 2300 may include a GPS device 2316 (or corresponding interface circuitry, as discussed above). The GPS device 2316 may be in communication with a satellite-based system and may receive a location of the computing device 2300, as known in the art.

[0132] The computing device 2300 may include a display device 2306 (or corresponding interface circuitry, as discussed above). The display device 2306 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0133] The computing device 2300 may include an audio output device 2308 (or corresponding interface circuitry, as discussed above). The audio output device 2308 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0134] The computing device 2300 may include an audio input device 2318 (or corresponding interface circuitry, as discussed above). The audio input device 2318 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0135] The computing device 2300 may include an other output device 2310 (or corresponding interface circuitry, as discussed above). Examples of the other output device 2310 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0136] The computing device 2300 may include an other input device 2320 (or corresponding interface circuitry, as discussed above). Examples of the other input device 2320 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0137] The computing device 2300 may have any desired form factor, such as a handheld or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device. In some embodiments, the computing device 2300 may be any other electronic device that processes data.

[0138] The following paragraphs provide various examples of the embodiments disclosed herein.

[0139] Example 1 provides a method for manufacturing a structure with a plurality of openings filled with a dielectric material. The method includes providing a host matrix within the plurality of openings; infiltrating the host matrix within the plurality of openings with one or more fluid precursors for forming the dielectric material; and, following the infiltration, removing at least a portion of the host matrix.

[0140] Example 2 provides the method according to Example 1, where the plurality of openings have aspect ratios between 1 and 20, where an aspect ratio is a ratio of a depth of an opening to a width of the opening.

[0141] Example 3 provides the method according to Examples 1 or 2, where the host matrix includes poly(methyl methacrylate) (PMMA).

[0142] Example 4 provides the method according to Examples 1 or 2, where the host matrix includes polyethylene oxide (PEO).

[0143] Example 5 provides the method according to Examples 1 or 2, where the host matrix includes poly(2-vinylpyridine) (P2VP).

[0144] Example 6 provides the method according to any one of the preceding Examples, where the host matrix includes a polymer with functional groups including one or more of hydroxyl groups, alkene groups, alkyne groups, alkoxy groups, ester groups, ether groups, amine groups, and carbonyl groups.

[0145] Example 7 provides the method according to Examples 1 or 2, where the host matrix includes a solid non-polymeric material having hydroxyl functional groups and interconnected to form pores.

[0146] Example 8 provides the method according to any one of Examples 1-7, where the one or more precursors include TMA and a co-reactant such as e.g. water or isopropanol.

[0147] Example 9 provides the method according to any one of Examples 1-7, where the one or more precursors include (ethylmethylamino) hafnium (Hf-EMA), e.g. tetrakis (ethylmethylamino) hafnium (Hf(EMA)₄), and a co-reactant such as e.g. water or isopropanol.

[0148] Example 10 provides the method according to any one of Examples 1-7, where the one or more precursors include hafnium chloride, e.g. hafnium tetrachloride (HfCl₄), and a co-reactant such as e.g. water or isopropanol.

[0149] Example 11 provides the method according to any one of Examples 1-7, where the one or more precursors include titanium chloride, e.g. titanium tetrachloride (TiCl₄), and a co-reactant such as e.g. water or isopropanol.

[0150] Example 12 provides the method according to any one of Examples 1-7, where the one or more precursors include TMA and silanol.

[0151] Example 13 provides the method according to any one of the preceding Examples, where providing the host matrix within the plurality of openings includes spin-coating or dip-coating one or more materials of the host matrix onto the structure with the plurality of openings.

[0152] Example 14 provides the method according to any one of the preceding Examples, where infiltrating the host matrix within the plurality of openings with one or more precursors includes providing the one or more precursors into the plurality of openings by spin-coating, dip-coating, CVD, or ALD.

[0153] Example 15 provides the method according to any one of the preceding Examples, where removing at least a portion of the host matrix includes etching or ashing the host matrix.

[0154] Example 16 provides the method according to any one of the preceding Examples, further including, prior to infiltrating the host matrix within the plurality of openings with one or more precursors, recessing the host matrix to be of a specified depth within the plurality of openings.

[0155] Example 17 provides the method according to Example 16, where recessing the host matrix includes irradiating the structure with the host matrix within the plurality of openings with optical radiation, e.g. applying UV radiation, to cross-link one or more materials of the host matrix to the specified depth, followed by selectively etching the one or more materials of the host matrix which were not cross-linked.

[0156] Example 18 provides the method according to Examples 16 or 17, further including passivating inner walls of the plurality of openings above the specified depth of the host matrix. Such passivation may e.g. include processing the surface of the inner walls to make them hydrophobic.

[0157] Example 19 provides the method according to any one of the preceding Examples, further including, after removing at least a portion of the host matrix, infiltrating the plurality of openings with the one or more precursors. As a result of removing at least a portion of the host matrix after the first round of infiltration, pores will form within the dielectric material formed/nucleated within the openings. By repeating the infiltration with the same precursors again, precursors can get into these pores and nucleate on the surfaces of the already present dielectric material or on the remaining portions of the original host matrix. In this manner, the dielectric material within the openings can be made denser.

[0158] Example 20 provides the method according to any one of the preceding Examples, where the one or more precursors are one or more first precursors, the method further including, after removing at least a portion of the host matrix, infiltrating the plurality of openings with one or more second precursors, different from the first precursors. In this case, by repeating the infiltration with different precursors, hybrid dielectric material can form within the openings, which allows carefully tuning the properties of the dielectric material within the openings. For example, if the first precursors formed aluminum oxide, second precursors could be used to form some hafnium oxide, improving the etch characteristics of the final dielectric material.

[0159] Example 21 provides the method according to any one of the preceding Examples, further including removing the dielectric material from uppermost surfaces of the structure.

[0160] Example 22 provides the method according to Example 21, where removing the dielectric material from uppermost surfaces of the structure includes performing polishing of the structure to expose the uppermost surfaces of the structure.

[0161] Example 23 provides the method according to any one of the preceding Examples, further including depositing a capping material over the dielectric material within at least one of the plurality of openings.

[0162] Example 24 provides the method according to Example 23, where the capping material and the dielectric material have different etch properties. For example, the capping material may have improved (enhanced) etch resistance compared to the dielectric material within the openings, and may act as an etch stop to certain etchants.

[0163] Example 25 provides the method according to any one of the preceding Examples, where the structure is made of one or more electrically conductive materials.

[0164] Example 26 provides an assembly that includes a structure including a plurality of openings; and a dielectric material disposed within the plurality of openings, where, for each opening of the plurality of openings, the dielectric material includes a plurality of pores distributed substantially uniformly within the each opening.

[0165] Example 27 provides the assembly according to Example 26, where a largest dimension of each of the plurality of pores is less than 5 nanometer, e.g. less than 3 nm or less than 1 nm.

[0166] Example 28 provides the assembly according to Examples 26 or 27, where, for the each opening, a density of the dielectric material in a central portion of the each opening (which central portion includes about 50%, or about 33% or about 25%, of a total volume of the each opening) is substantially equal to a density of the dielectric material in a remaining portion of the each opening, the remaining portion being a portion of the total volume that does not include the central portion.

[0167] Example 29 provides the assembly according to any one of Examples 26-28, where, within the each opening, the dielectric material lacks a seam or/and a seam void substantially in the middle of the opening and having the largest dimension substantially perpendicular to the substrate on which the structure is provided (i.e. substantially along the axis of symmetry (e.g. centerline) of the opening). A seam void is a void in the middle of the opening.

[0168] Example 30 provides the assembly according to any one of Examples 26-29, where the dielectric material is a first dielectric material, and, within the each opening, at least some of the plurality of pores include a second dielectric material, e.g. the first dielectric material may be aluminum oxide and the second dielectric material may be hafnium oxide.

[0169] Example 31 provides the assembly according to any one of Examples 28-30, where, within the each opening, a volume of the plurality of pores is between about 1 and 70 percent of a volume of the each opening.

[0170] Example 32 provides the assembly according to any one of Examples 28-31, where the dielectric material includes one or more metal oxides.

[0171] Example 33 provides the assembly according to any one of Examples 28-32, where the dielectric material includes aluminum oxide.

[0172] Example 34 provides the assembly according to any one of Examples 28-33, where the dielectric material includes hafnium oxide.

[0173] Example 35 provides the assembly according to any one of Examples 28-34, where the dielectric material includes titanium oxide.

[0174] Example 36 provides the assembly according to any one of Examples 28-35, where the plurality of openings have aspect ratios between 1 and 20, where an aspect ratio is a ratio of a depth of an opening to a width of the opening.

[0175] Example 37 provides the assembly according to any one of Examples 28-36, where the plurality of openings have depths of 5 to 100 nanometers.

[0176] Example 38 provides the assembly according to any one of Examples 28-37, further including a capping material over the dielectric material.

[0177] Example 39 provides the assembly according to Example 38, where the capping material and the dielectric material have different etch properties.

[0178] Example 40 provides the assembly according to Examples 38 or 39, where the dielectric material is aluminum oxide and the capping material is hafnium oxide.

[0179] Example 41 provides an integrated circuit package that includes a substrate and a component on the substrate. The component includes a structure including a plurality of openings, and a dielectric material disposed within the plurality of openings, where, for each opening of the plurality of openings, a density of the dielectric material in a central portion of the each opening is substantially equal to a density of the dielectric material in a remaining portion of the each opening, where the central portion includes about 50%, or about 33% or about 25%, of a total volume of the each opening, and the remaining portion is a portion of the total volume that does not include the central portion.

[0180] Example 42 provides the integrated circuit package according to Example 41, where the component includes/is an interconnect, a transistor, a die, a sensor, a processing device, or a memory device.

[0181] In various further Examples, said structure and said dielectric material of the component may be included within an assembly according to any one of the preceding Examples.

[0182] Example 43 provides a computing device, including a substrate and an IC die coupled to the substrate. The IC die includes a semiconductor device including a structure including a plurality of openings, and a dielectric material disposed within the plurality of openings, where, for each opening of the plurality of openings, the dielectric material lacks a seam or/and a seam void substantially in the middle of the each opening.

[0183] In various further Examples, said structure and said dielectric material of the semiconductor device may be included within an assembly according to any one of the preceding Examples.

[0184] Example 44 provides the computing device according to Example 43, where the computing device is a wearable or handheld computing device.

[0185] Example 45 provides the computing device according to Examples 43 or 44, where the computing device further includes one or more communication chips and an antenna.

[0186] Example 46 provides the computing device according to any of Examples 43-45, where the substrate is a motherboard.

[0187] The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

[0188] These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Claims:

1. A method for manufacturing a structure with a plurality of openings filled with a dielectric material, the method comprising:
 - providing a host matrix within the plurality of openings;
 - infiltrating the host matrix within the plurality of openings with one or more precursors for forming the dielectric material; and
 - following the infiltration, removing at least a portion of the host matrix.
2. The method according to claim 1, wherein the plurality of openings have aspect ratios between 1 and 100, where an aspect ratio is a ratio of a depth of an opening to a width of the opening.
3. The method according to claim 2, wherein the host matrix comprises a polymer with functional groups comprising one or more of hydroxyl groups, alkene groups, alkyne groups, alkoxy groups, ester groups, ether groups, amine groups, and carbonyl groups.
4. The method according to claim 2, wherein the host matrix comprises a solid non-polymeric material having hydroxyl functional groups and interconnected to form pores.
5. The method according to claim 2, wherein the one or more precursors comprise trimethyl aluminum (TMA), (ethylmethyldamino) hafnium (Hf-EMA), hafnium chloride, or titanium chloride.
6. The method according to any one of claims 1-5, wherein providing the host matrix within the plurality of openings comprises spin-coating or dip-coating one or more materials of the host matrix onto the structure with the plurality of openings.
7. The method according to any one of claims 1-5, wherein infiltrating the host matrix within the plurality of openings with one or more precursors comprises providing the one or more precursors into the plurality of openings by spin-coating, dip-coating, chemical vapor deposition (CVD), or atomic layer deposition (ALD).
8. The method according to any one of claims 1-5, wherein removing at least a portion of the host matrix comprises etching or ashing the host matrix.

9. The method according to any one of claims 1-5, further comprising, prior to infiltrating the host matrix within the plurality of openings with one or more precursors, recessing the host matrix to be of a specified depth within the plurality of openings.
10. The method according to any one of claims 1-5, further comprising, after removing at least a portion of the host matrix, infiltrating the plurality of openings with the one or more precursors.
11. The method according to any one of claims 1-5, wherein the one or more precursors are one or more first precursors, the method further comprising, after removing at least a portion of the host matrix, infiltrating the plurality of openings with one or more second precursors.
12. The method according to any one of claims 1-5, further comprising depositing a capping material over the dielectric material within at least one of the plurality of openings.
13. The method according to any one of claims 1-5, wherein the structure is made of one or more electrically conductive materials.
14. An assembly comprising:
a structure comprising a plurality of openings; and
a dielectric material within the plurality of openings,
wherein, for each opening of the plurality of openings, the dielectric material includes a plurality of pores within the each opening.
15. The assembly according to claim 14, wherein a largest dimension of each of the plurality of pores is less than 5 nanometer.
16. The assembly according to claim 14, wherein, for the each opening, a density of the dielectric material in a central portion of the each opening is substantially equal to a density of the dielectric material in a remaining portion of the each opening, the remaining portion being a portion of the total volume that does not include the central portion.
17. The assembly according to any one of claims 14-16, wherein, within the each opening, the dielectric material lacks a seam and a void substantially in the middle of the opening.

18. The assembly according to any one of claims 14-16, wherein the dielectric material is a first dielectric material, and, within the each opening, at least some of the plurality of pores include a second dielectric material.
19. The assembly according to any one of claims 14-16, wherein the dielectric material comprises one or more metal oxides.
20. The assembly according to any one of claims 14-16, wherein the plurality of openings have aspect ratios between 1 and 20, where an aspect ratio is a ratio of a depth of an opening to a width of the opening.
21. The assembly according to any one of claims 14-16, wherein the plurality of openings have depths of 5 to 100 nanometers.
22. The assembly according to any one of claims 14-16, further comprising a capping material over the dielectric material, wherein the capping material and the dielectric material have different etch properties.
23. The assembly according to claim 22, wherein the dielectric material is aluminum oxide and the capping material is hafnium oxide.
24. An integrated circuit package, comprising:
a substrate;
a component on the substrate, the component comprising:
a structure comprising a plurality of openings, and
a dielectric material within the plurality of openings, wherein, for each opening of the plurality of openings, a density of the dielectric material in a central portion of the each opening is substantially equal to a density of the dielectric material in a remaining portion of the each opening, wherein the central portion includes 50% of a total volume of the each opening, and the remaining portion is a portion of the total volume that does not include the central portion.
25. The integrated circuit package according to claim 24, wherein the component comprises an interconnect, a transistor, a die, a sensor, a processing device, or a memory device.

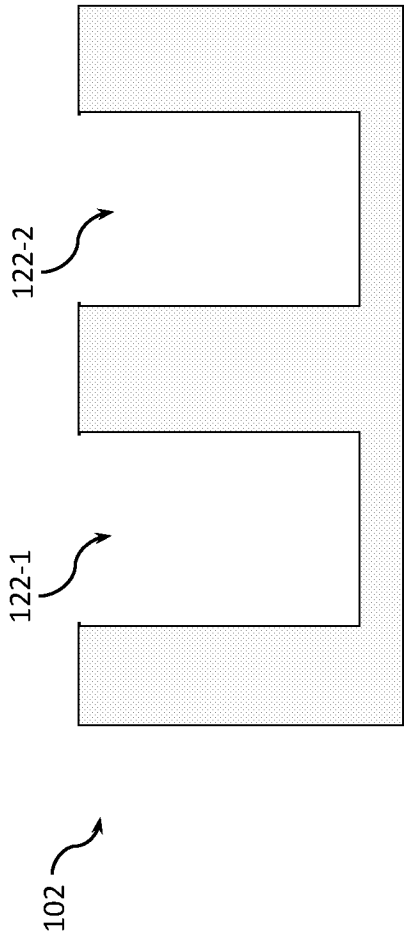


FIG. 1A

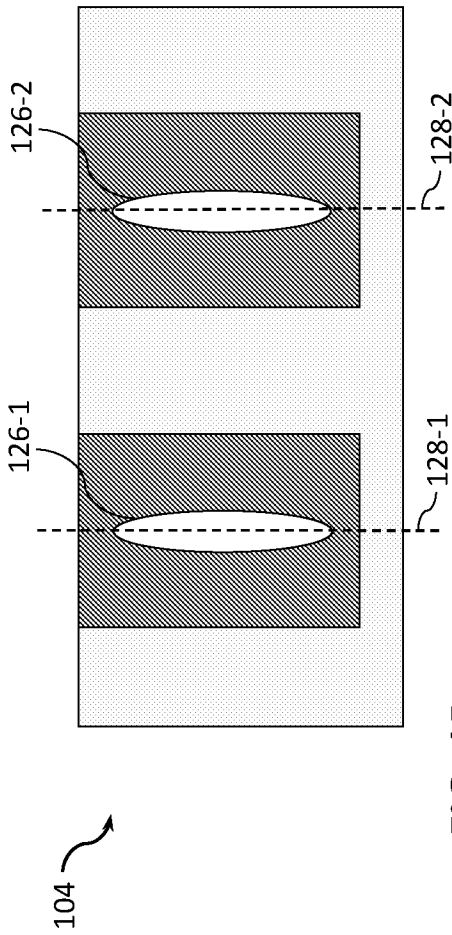
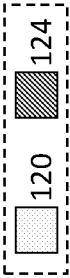


FIG. 1B



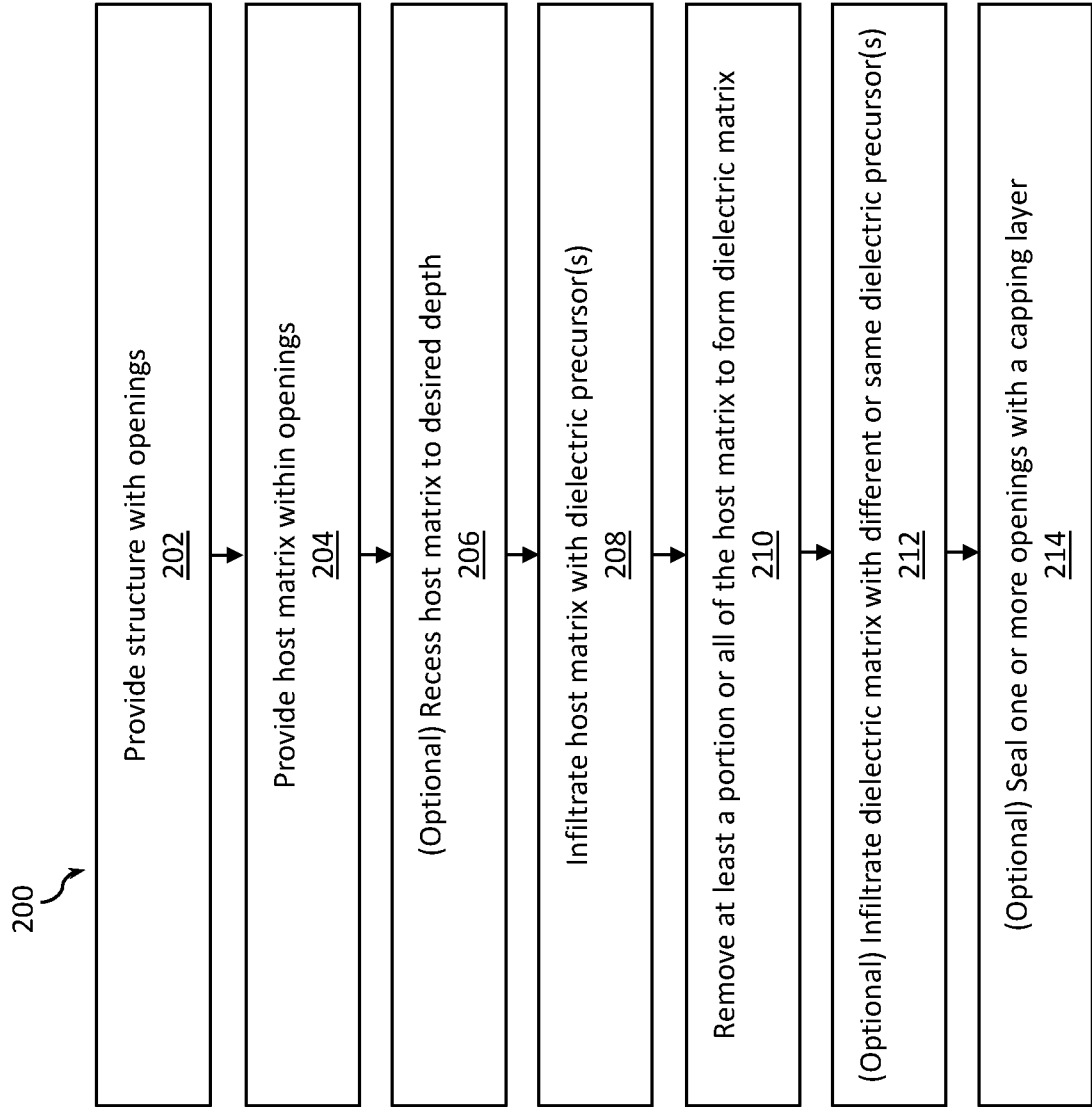


FIG. 2

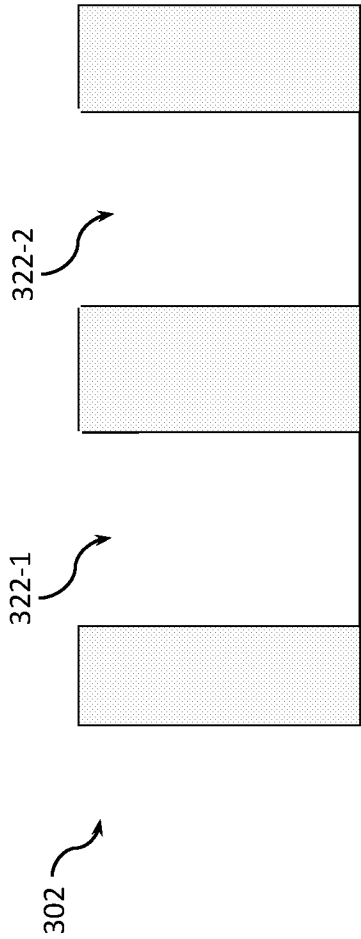


FIG. 3A

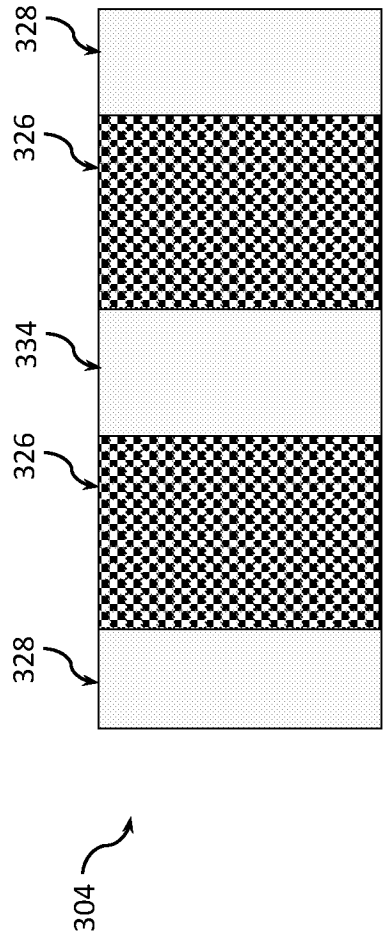


FIG. 3B



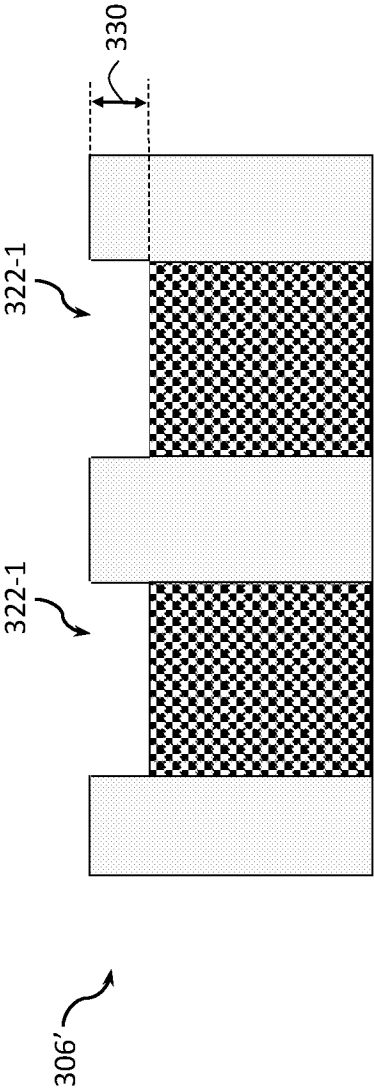


FIG. 3C

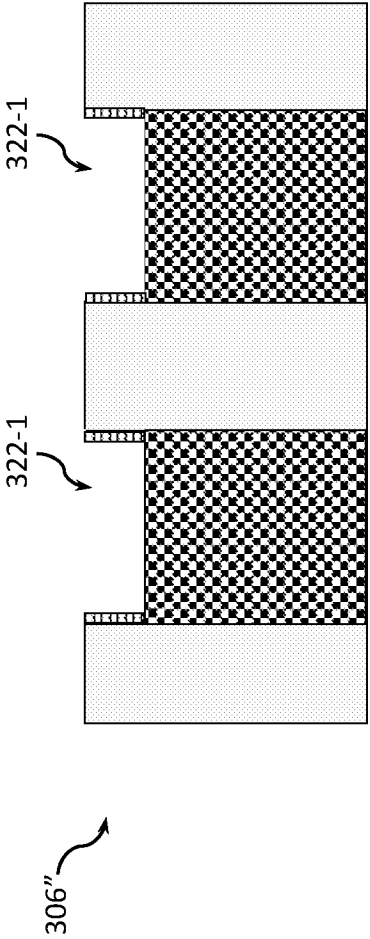


FIG. 3D



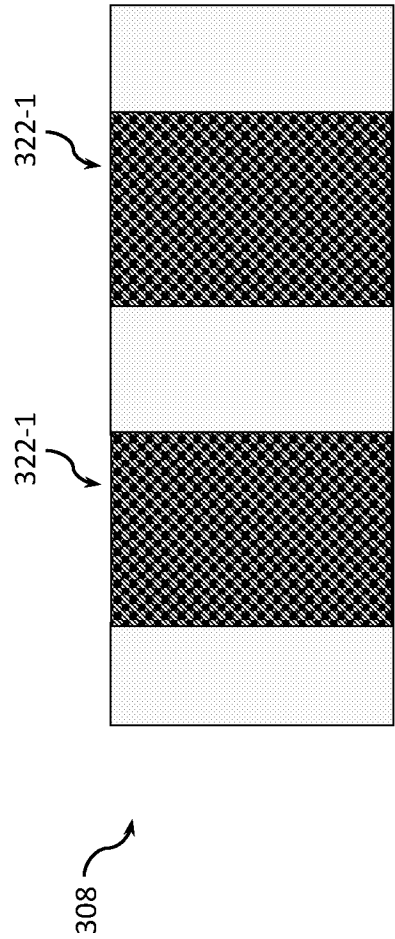


FIG. 3E

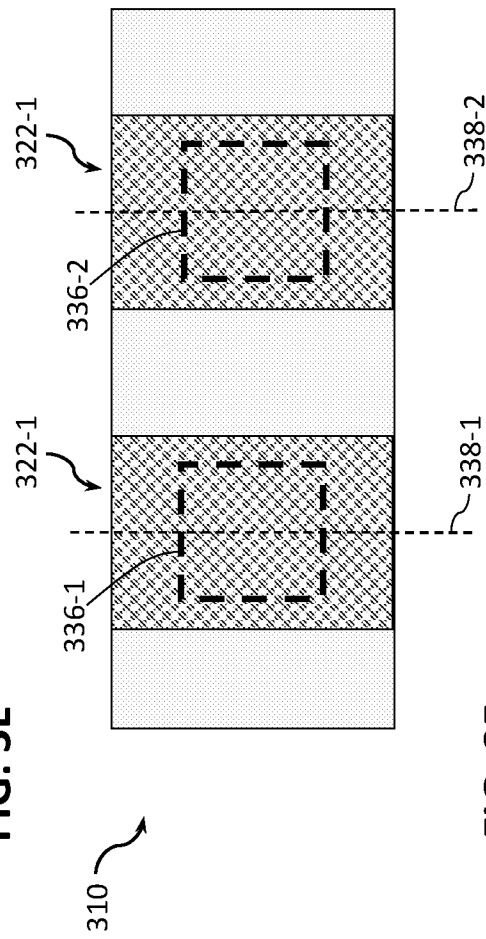
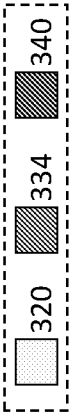
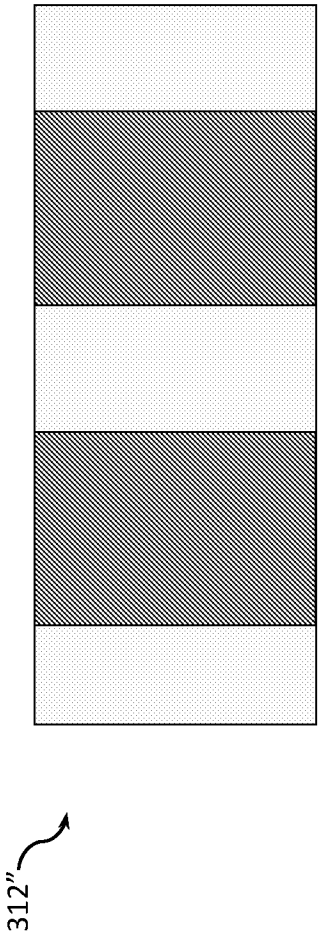
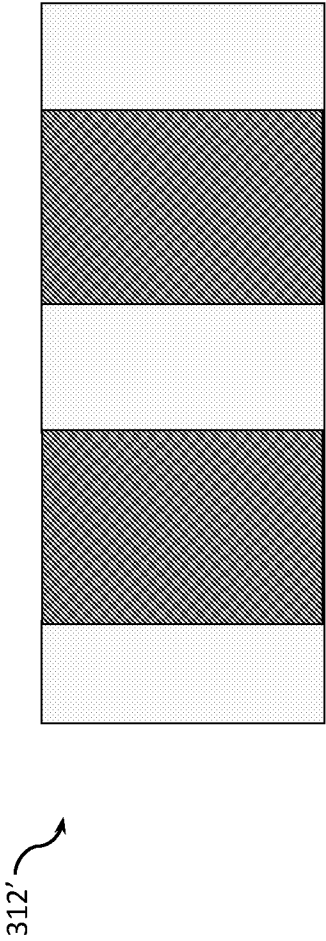


FIG. 3F





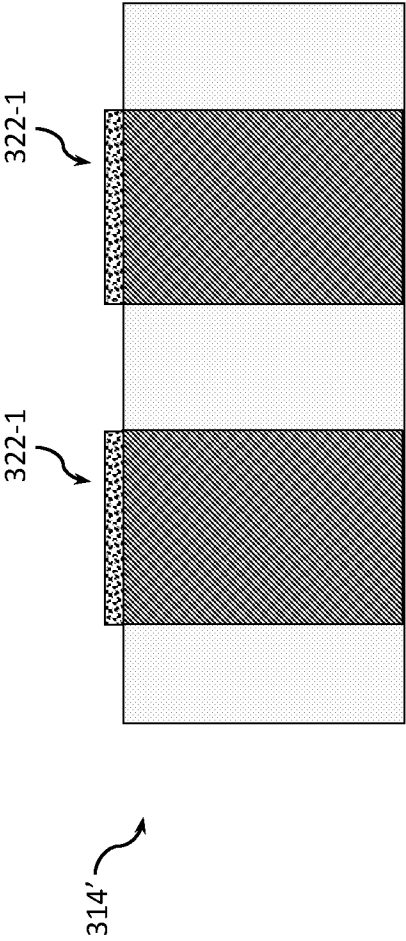


FIG. 3I

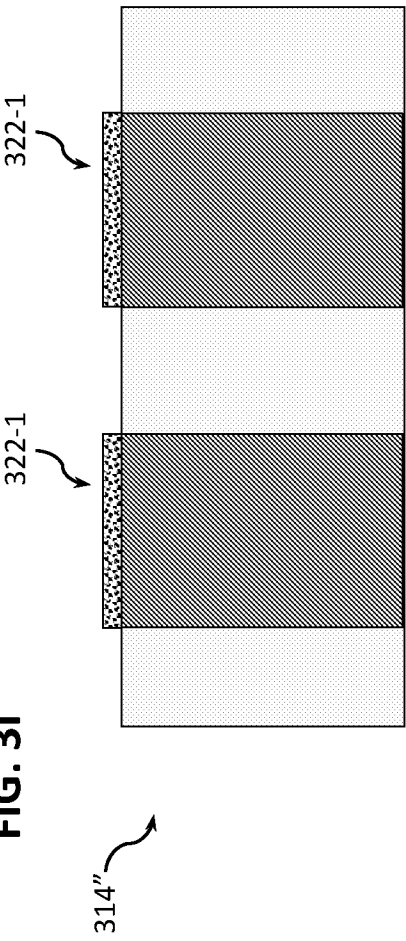
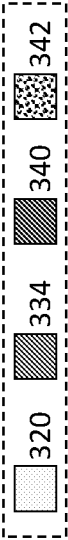


FIG. 3J



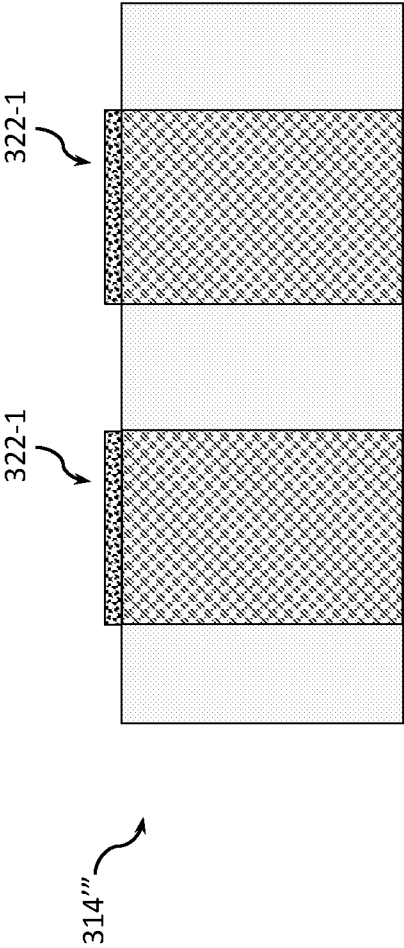


FIG. 3K

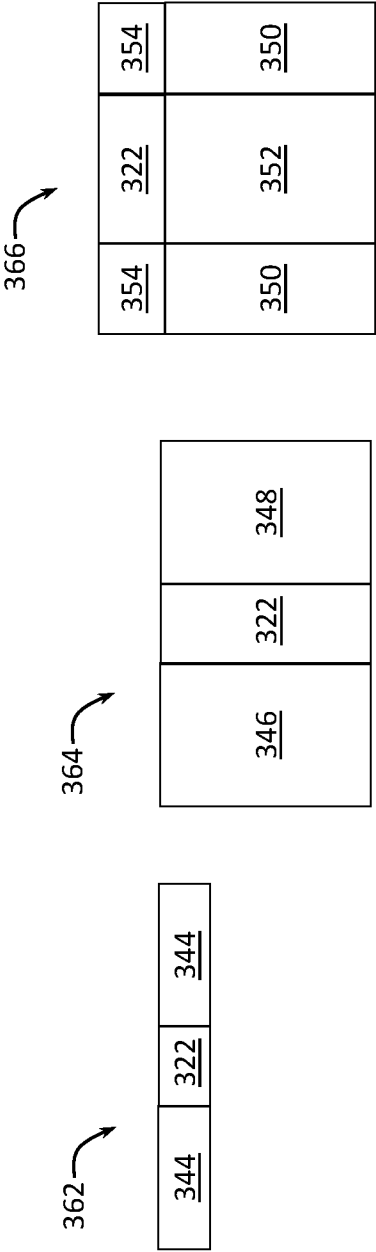


FIG. 3L



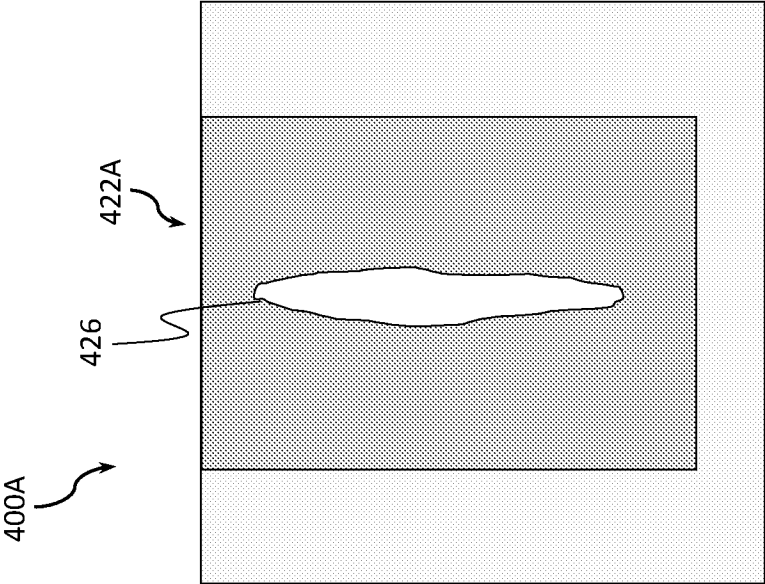


FIG. 4A

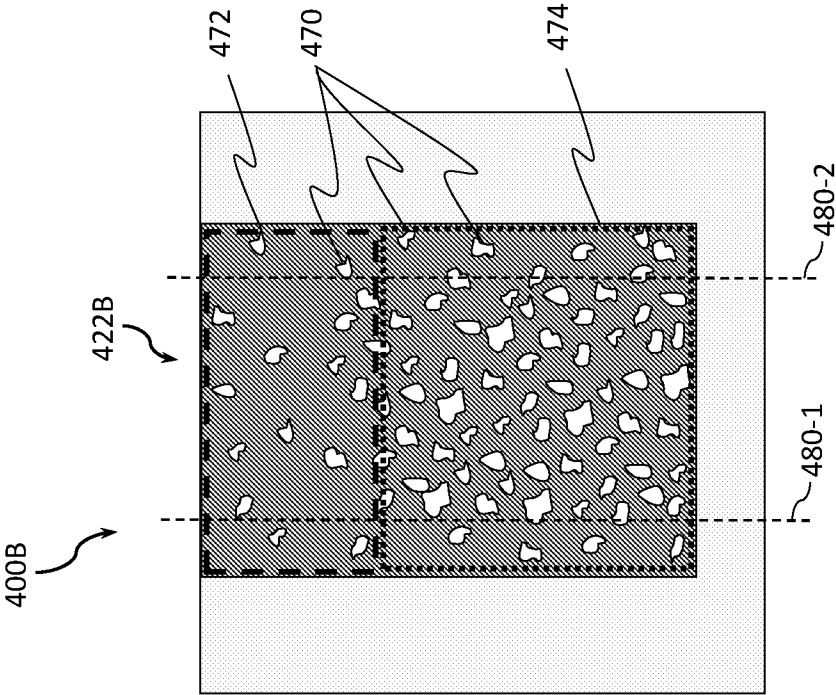
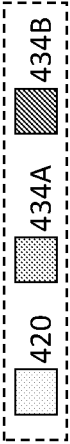


FIG. 4B



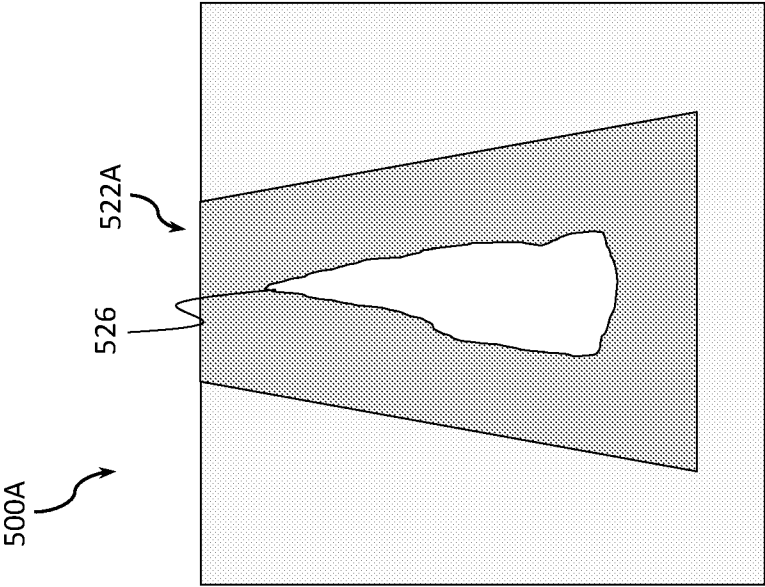


FIG. 5A

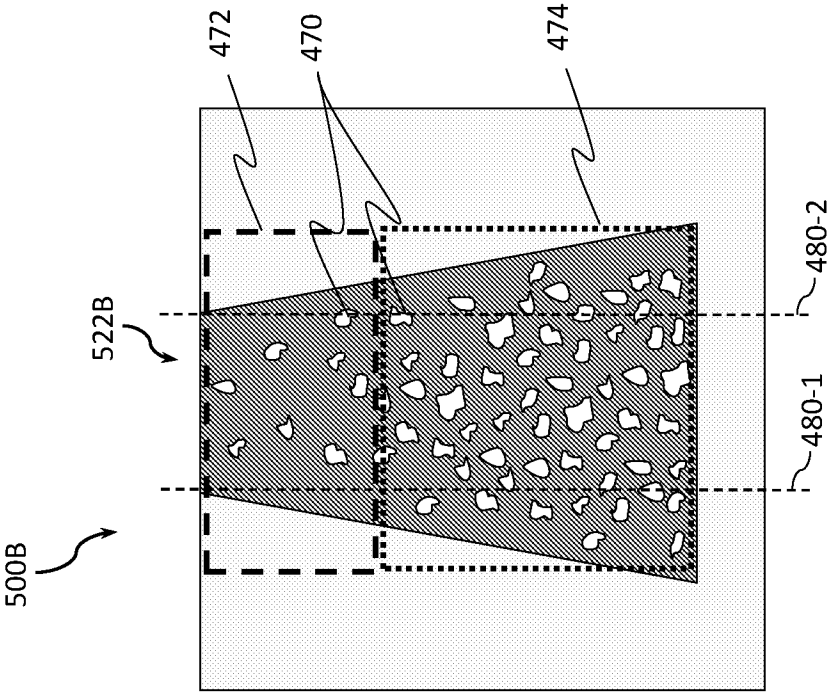
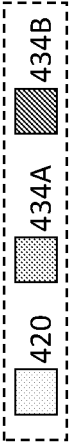


FIG. 5B



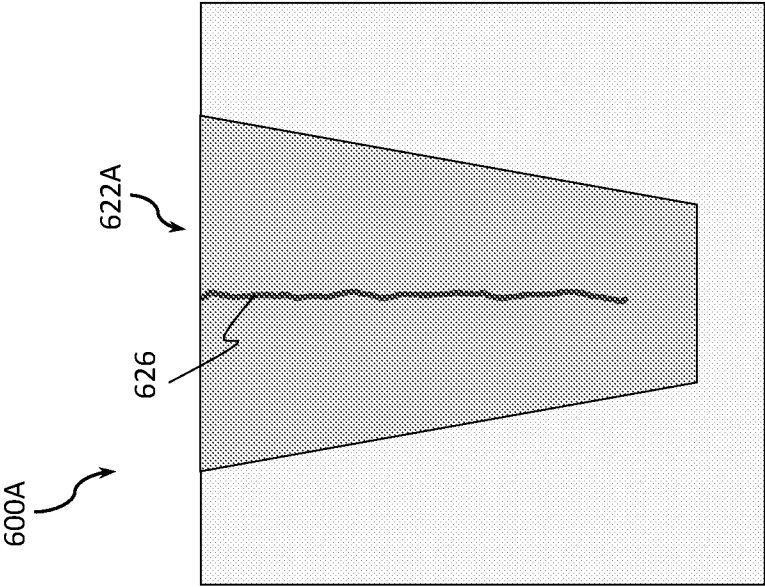


FIG. 6A

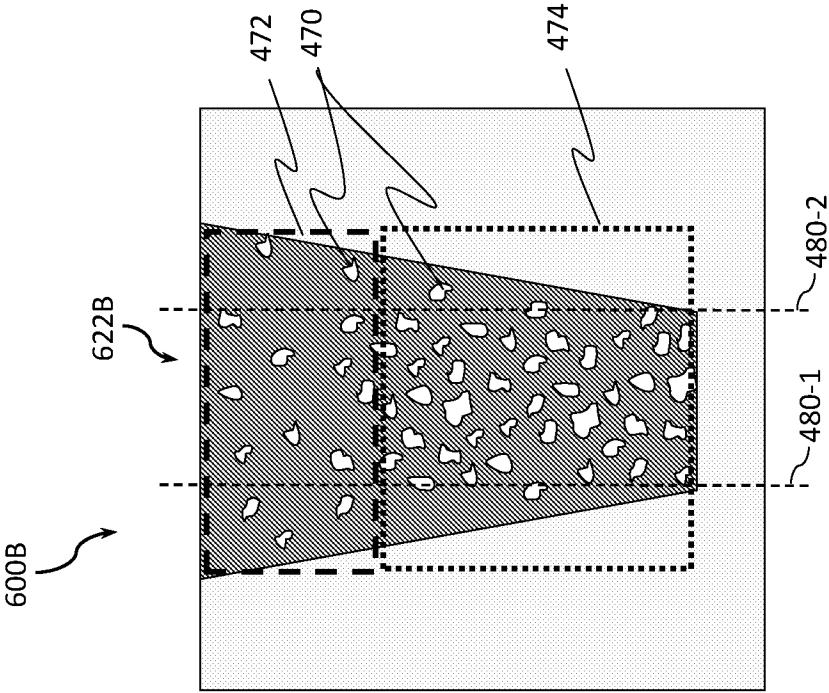
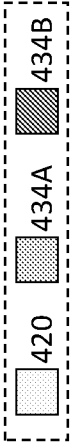


FIG. 6B



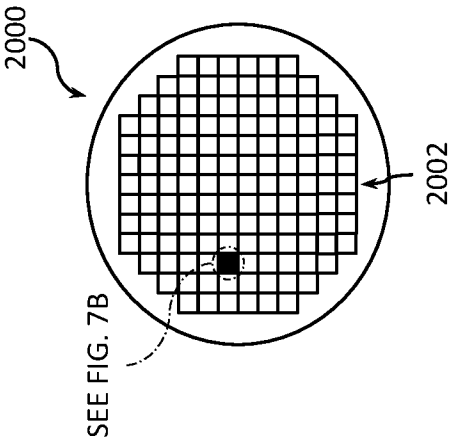


FIG. 7A

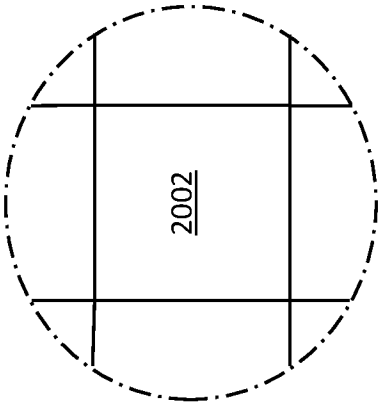


FIG. 7B

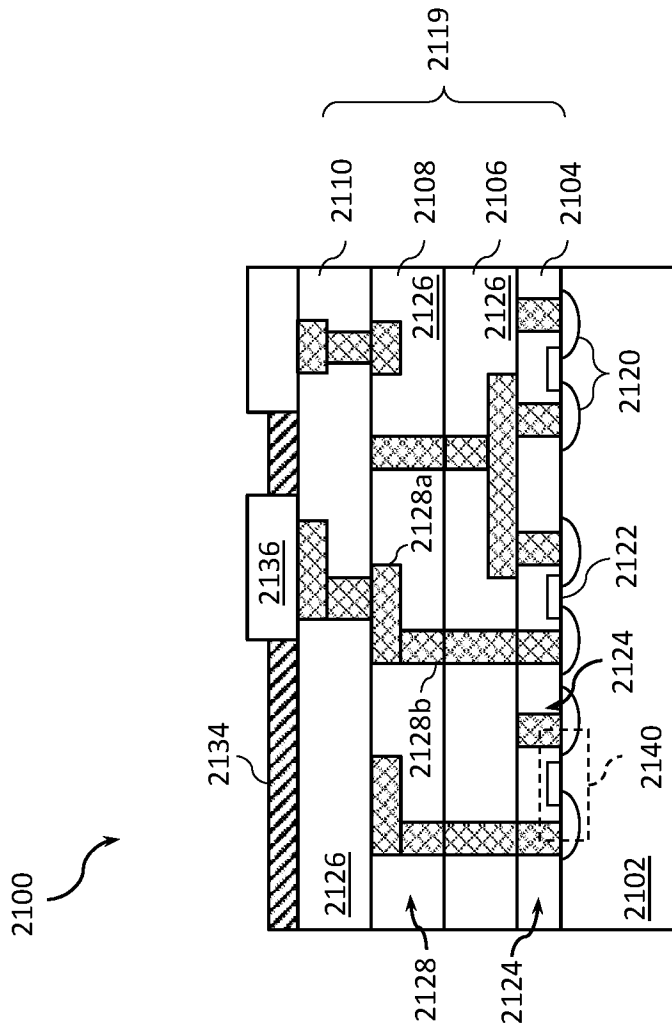


FIG. 8

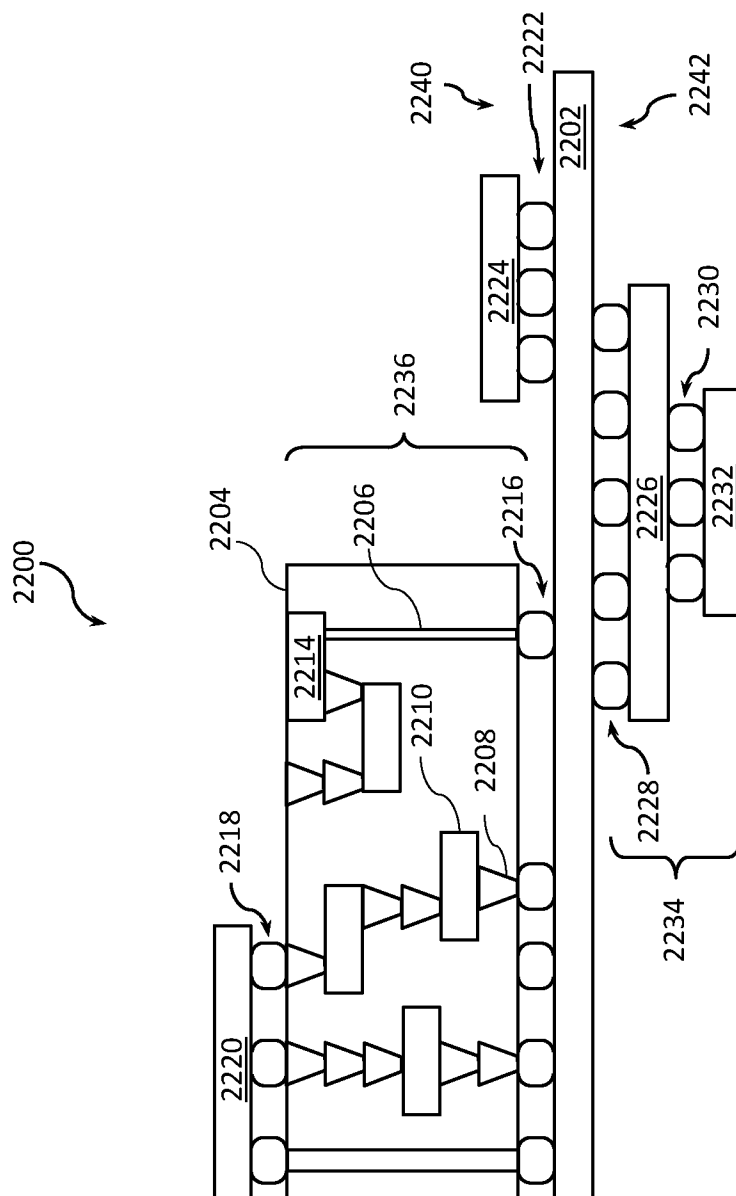


FIG. 9

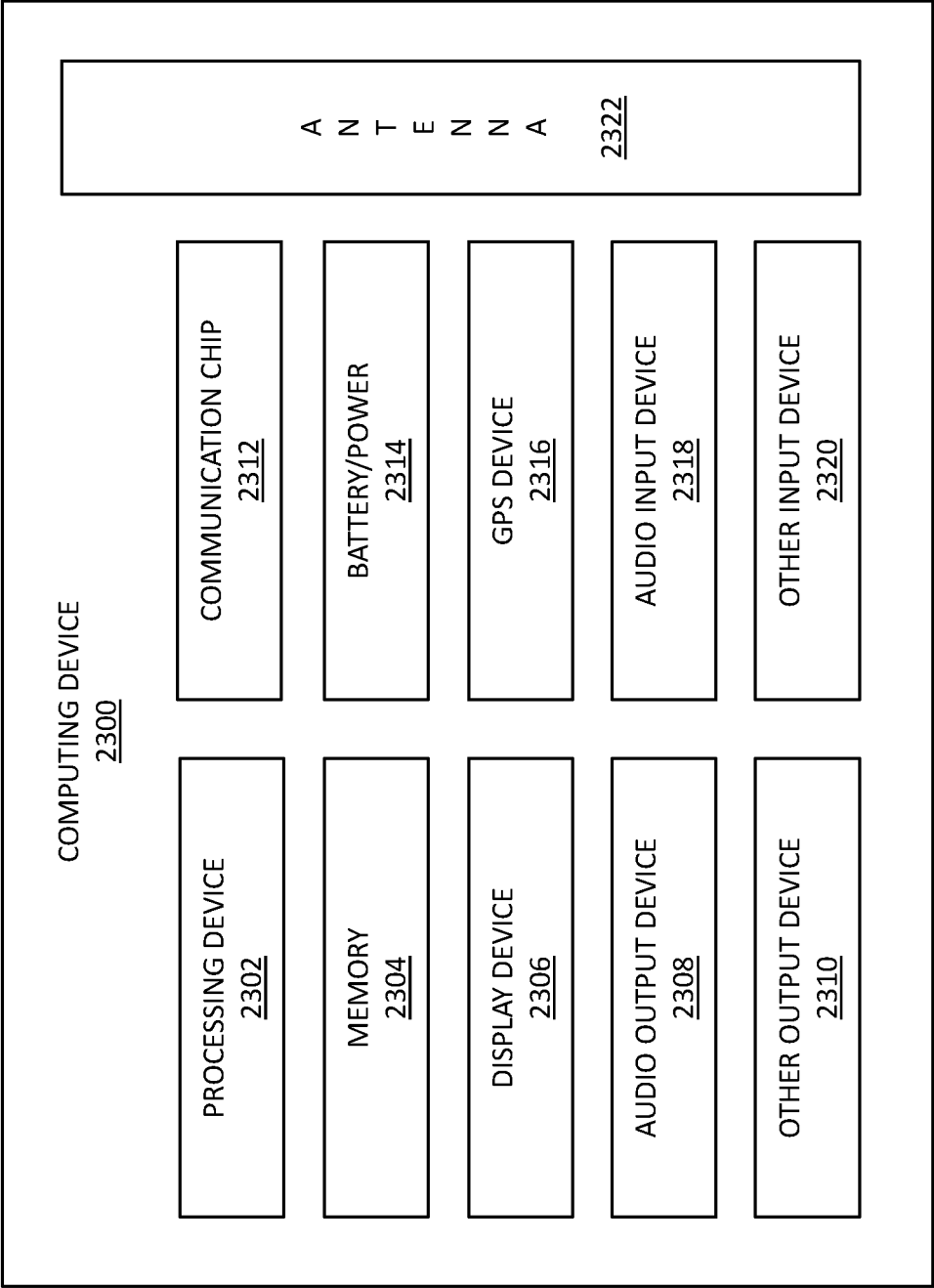


FIG. 10

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/768(2006.01)i, H01L 21/02(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
H01L 21/768; H01L 21/28; H01L 21/30; H01L 21/02; H01L 23/522; H01L 21/31; H01L 23/525Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: trimethyl aluminum, dielectric, pore, host matrix, polymer, seam**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011-0049724 A1 (BRENT A. ANDERSON et al.) 03 March 2011 See paragraph [0034] and figures 5, 5A.	14, 15, 17, 19-23
Y		18
A		1-13, 16, 24, 25
Y	US 2017-0117144 A1 (APPLIED MATERIALS, INC.) 27 April 2017 See claims 1, 9, 11.	18
A	US 2014-0239439 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 28 August 2014 See paragraph [0034] and figure 5.	1-25
A	KR 10-2014-0145469 A (SAMSUNG ELECTRONICS CO., LTD.) 23 December 2014 See claim 1.	1-25
A	US 2013-0017688 A1 (GERAUD JEAN-MICHEL DUBOIS et al.) 17 January 2013 See paragraphs [0027]-[0036] and figures 5-7.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 March 2018 (27.03.2018)

Date of mailing of the international search report

27 March 2018 (27.03.2018)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/039364

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 2013-0017688 A1	17/01/2013	US 2013-0045608 A1 US 8541301 B2 US 8871632 B2	21/02/2013 24/09/2013 28/10/2014