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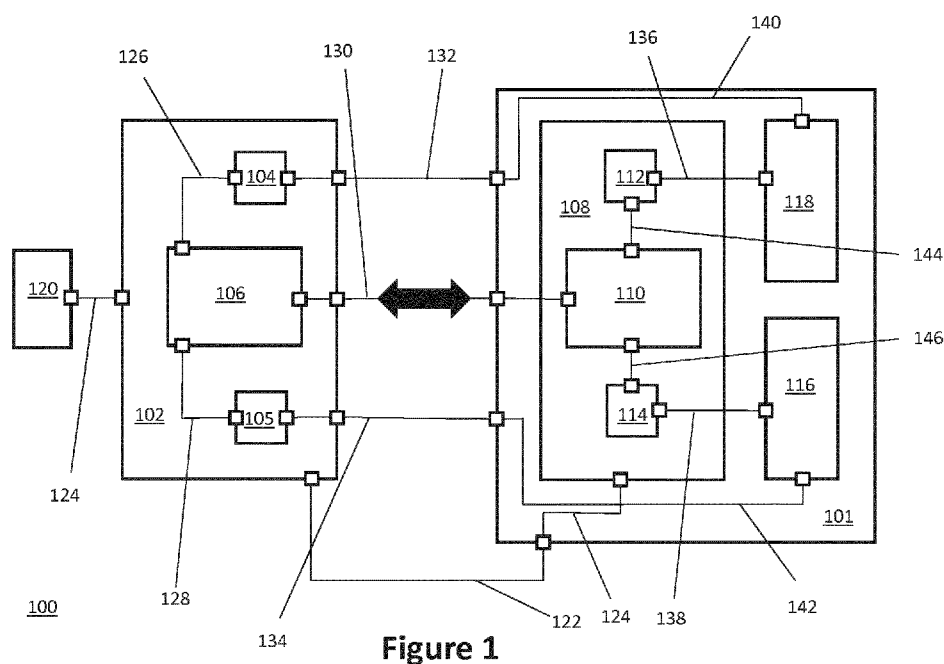


Figure 1

(57) Abstract: An electronic device (100) comprising a system on chip (101) which includes a plurality of internal subsystems (116, 118) and a power management system (108). The power management system comprises a plurality of internal voltage regulators (112, 114) arranged to supply power to the plurality of different internal subsystems, and control logic (110) which controls the supply of power from the internal voltage regulators. The electronic device further comprises an external module (102) comprising at least one external voltage regulator (104, 105). The external module is connected to the system on chip such that the external voltage regulator can selectively provide power to at least one of said internal subsystems on the system on chip.

MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
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Power Management in a System on Chip

5 This invention relates to power management systems in system on chip (SoC) arrangements, and particularly management of the power supplied to internal subsystems within the system on chip.

10 SoC's such as the Applicant's highly popular nRF series typically include a microprocessor, memory, and wireless communication functionality on a single integrated circuit. They are used in a large variety of portable electronic devices to provide compact, power efficient general purpose data handling and communication. In order to provide long battery life, an SoC will typically include a complex power management system which hosts and controls the various on-chip regulators associated with different power domains to ensure that power is only
15 provided when absolutely necessary to meet the requirements of internal subsystems within the SoC.

20 High manufacturing costs of SoCs, particularly in the production of silicon wafers, make it desirable to manufacture a single design in large quantities as opposed to a variety of different SoCs. The Applicant has appreciated the necessity for a single SoC design capable of implementation in a number of different electronic devices serving different purposes.

25 When viewed from a first aspect, the invention provides an electronic device comprising:

a system on chip, including a plurality of internal subsystems, and a power management system comprising a plurality of internal voltage regulators arranged to supply power to the plurality of different internal subsystems, and control logic which controls the supply of power from the internal voltage regulators;

30 an external module comprising at least one external voltage regulator and connected to the system on chip such that the external voltage regulator can selectively provide power to at least one of said internal subsystems on the system on chip,

wherein the control logic of the power management system is arranged to
35 control the at least one external voltage regulator.

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When viewed from a second aspect the invention provides a method of operating an electronic device comprising:

5 a system on chip, including a plurality of internal subsystems, and a power management system comprising a plurality of different internal voltage regulators arranged to supply power to the plurality of internal subsystems and control logic which controls the supply power from the internal voltage regulators;

10 an external module comprising at least one external voltage regulator; wherein the method comprises the external voltage regulator selectively providing power to at least one of said internal subsystems on the system on chip,

wherein the control logic of the power management system controls the at least one external voltage regulator.

15 Thus it will be seen by those skilled in the art that in accordance with at least embodiments of the invention, an external module may supplement the internal power management system e.g. to provide additional and/or alternative voltage and current ratings to the SoC. This is advantageous as it allows internal subsystems on the SoC to be added, or utilized, in new ways without having to redesign the existing power management system. By providing a facility for providing additional
20 power to the SoC it is possible for example to run more power hungry applications on the same SoC design.

In a set of embodiments the external module comprises a plurality of external voltage regulators.

25 The control logic of the power management system controls the at least one external voltage regulator. This removes the need for the external module to include control logic to determine the output of the at least one external voltage regulator, reducing the number of components necessary. However, in a preferred set of
30 embodiments the device further comprises external control logic separate from the SoC. Whilst the Applicant appreciates that such external control logic may not be utilized in all situations, such as when the power management system controls the at least one external voltage regulator, in a preferred set of embodiments the external control logic is arranged to control at least the external voltage regulator(s)

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at least partially. This may be beneficial in allowing regulators and the control logic therefor to be developed and provided together.

5 Typically the external module is arranged to provide power only to a portion of the internal subsystem in the system on chip. The external module would not therefore provide power to the whole system on chip.

10 In a potentially overlapping set of embodiments the external control logic controls the internal voltage regulators. This configuration allows the external logic to override the power management system's control logic and control the power supplied to the system on chip's subsystems. In such a configuration the control logic of the power management system may be in a 'sleep' state i.e. it exerts no control over the internal voltage regulators. This removes dependence on the control logic of the power management system. Advantageously this allows greater flexibility in the functionality of an SoC, as the external module can implement new features without the necessity to redesign the power management system, i.e. allowing the existing chip to be re-used.

20 Whilst it is preferred, it is not essential for the external voltage regulator(s) and the external logic (where provided) to be provided by a single module; in alternative embodiments a further module could provide the external control logic.

25 It will be appreciated from the foregoing that the external logic can, in some circumstances, control the internal voltage regulators on the SoC. This would typically be in addition to the external voltage regulator but this is not essential. In other words the device could operate in a mode in which the external control logic simply controls the internal voltage regulators without employing the external voltage regulator(s).

30 It will be seen that where external control logic is provided, it allows for a great flexibility in how the overall system is implemented, for example the external control logic could control a subset of a plurality of external voltage regulators, with the power management system controlling the remaining external voltage regulators. For example, this would allow the power management system to control the external voltage regulator(s) which match the voltage and current capacities of the

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internal voltage regulators, and the external control logic to control external voltage regulators which are different in voltage and current capacities to the internal voltage regulator(s).

5 In a set of embodiments the external module is connected directly to a power supply e.g. a battery. In a set of embodiments the SoC is connected to the same power supply but this is not essential and it could have its own supply e.g. a separate battery. In a set of embodiments the SoC is connected to the power supply e.g. a battery, via the external module.

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In a set of embodiments the electronic device comprises a single package with a common set of external pins. This provides the benefit of allowing new products implementing new features to be provided to customers whilst essentially re-using an existing SoC that does not have all those features.

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In a set of embodiments the system on chip further comprises a radio transmitter and receiver. This provides a system on chip capable of communicating via radio frequency transmissions.

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The SoC and power management system may have native support for a given RF protocol. In a set of embodiments the external module enables support for an alternative RF protocol e.g. an LTE, NB IoT or any other 3GPP protocol.

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In a set of embodiments the electronic device is arranged such that communications between the system on chip and the external module combine asynchronous signalling with serial interface communications.

Certain embodiments of the present invention will now be described by way of example only, with reference to the following diagrams in which:

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Figure 1 is a schematic diagram of a generic electronic device in accordance with an embodiment of the invention comprising a system on chip and a controller external to the system on chip;

Figure 2 is a schematic diagram of a generic electronic device in accordance with another embodiment of the invention comprising a system on chip

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and a controller external to the system on chip where the internal control logic controls the external voltage regulators;

Figure 3 is a schematic diagram of a generic electronic device in accordance with a third embodiment of the invention comprising a system on chip and a controller external to the system on chip where the controller external to the system on chip can control the internal voltage regulators.

The device 100 as seen in Figure 1 comprises a peripheral controller module 102 connected to a system on chip (SoC) 101. The SoC and peripheral module may be on separate silicon wafers but packaged together so that the device 100 forms a single package with a common set of external pins. As is conventional *per se*, the SoC 101 comprises a power management system 108 alongside multiple internal subsystems. In Figure 1 there are two such internal subsystems 116 and 118 illustrated as examples but typically there would be many more. The internal subsystems 116, 118 may be for example a radio transmitter/receiver and an internal processor.

The primary purpose of the power management system 108 is to provide and control the power to the internal subsystems 116, 118 as efficiently as possible. The power management system 108 therefore comprises a plurality of internal voltage regulators 112, 114 (again typically there would be more). Each internal voltage regulator in Figure 1 is connected to a different internal subsystem but in practice a voltage regulator might power a number of subsystems. One internal voltage regulator 112 is connected to the internal subsystem 118 via a connection 136, whereas the other internal voltage regulator 114 is connected to the other internal subsystem 116 via a connection 138. The internal voltage regulators 112, 114 can operate independently so that different internal subsystems 116, 118 reside in different power domains.

The power management system 108 also comprises control logic 110 which controls the outputs from the internal voltage regulators 112, 114 allowing the different internal subsystems 116, 118 to receive different power supplies and only operate when required. The control logic 110 is connected to the internal voltage regulators 112, 114 via suitable control buses 144 and 146 respectively.

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Due to the investment required in designing and manufacturing large numbers of different SoC designs to incorporate in different products, there may be internal subsystems 116, 118, perhaps developed after the original chip design, which the power management system 108 is not optimized to power. This may be because, for example, these internal subsystems require a high power to run at maximum performance. In Figure 1 and 2 the power management system 108 cannot supply the high power required due to limitations in the maximum voltage and/or current rating of the internal voltage regulators 112, 114.

In order to overcome this, the electronic device 100 also comprises the peripheral controller module 102 which is capable of supplementing the power supplied to the internal subsystems 116, 118. The peripheral controller module as seen in Figure 1 comprises two external voltage regulators 104, 105 and external control logic 106. Of course more or just one regulator could be provided.

The external control logic 106 controls the outputs of the external voltage regulators 104, 105 via control buses 126 and 128 respectively. The power from the external voltage regulators 104, 105 is supplied to the SoC 101 via connections 132, 134 respectively. In particular the output from an external voltage regulator 104 into the SoC 101 provides additional power to the internal subsystem 118 via an internal connection 140, and the output from the other external voltage regulator 105 into the SoC provides additional power to the other internal subsystem 116 via a further internal connection 142. Although independent power connections 140, 142 are shown, power could be routed through the power management system 108.

The external voltage regulators 104, 105 function separately from the internal regulators and each other, therefore can provide further, different power domains to the internal subsystems 116, 118.

The external control logic 106 and internal control logic 110 communicate via a bi-directional connection 130 in order to co-ordinate supply of the necessary power to optimize the internal subsystems 116, 118.

In all embodiments described, power is supplied by a battery 120 located off the main device. The battery 120 provides a power input to the peripheral controller

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module 102 through a connection 124. The battery 120 also provides power to the SoC 101 via a main voltage supply connection 122 between the peripheral controller module 102 and the SoC 101.

5 Figure 1 may represent a device 100 for installation in a larger product which requires support for an alternative radio frequency protocol than the one provided natively by the SoC 101. In Figure 1 the internal subsystem 116 might be say an internal subsystem (in practice comprising multiple modules) configured to provide support for a Bluetooth™ protocol. The internal subsystem 118 may be an internal
10 subsystem configured to provide support for an alternative radio frequency protocol e.g. an LTE protocol such as narrow-band internet-of-things (NB IoT). The power management system 108 is not optimized for the LTE protocol, and therefore cannot supply adequate power to support the NB IoT subsystem 118. The peripheral controller module 102 contains adequate external voltage regulator 104
15 which provide the required power for this subsystem 118 to run optimally.

The internal control logic 110 communicates with the external control logic 106 via a two-way data connection 130 to indicate to the external control logic 106 that additional power is required in order to optimize the performance of the NB IoT
20 subsystem 118. Upon receiving a signal from the external control logic 106, the external voltage regulator 104 is powered up and supplies additional power to the internal subsystem 118 via the connection 132, 140. Between the supply from the external voltage regulator 104 and the internal voltage regulator 112, the NB IoT subsystem 118 receives the required power to operate optimally.

25 There can also be envisaged situations where an existing subsystem such as the internal subsystem 116 requires increased power. Again the internal control logic 110 communicates with the external control logic 106 via the communication connection 130 to indicate to the external control logic 106 that additional power is required in order to optimize the performance of the internal subsystem 116. Upon
30 receiving a signal from the external control logic 106, the external voltage regulator 105 supplies power to the internal subsystem 116 via the connection 134, 142. Between the supply from the external voltage regulator 105 and the internal voltage regulator 114, the internal subsystem 116 receives the required power to operate at
35 an increased power.

The serial interface between the peripheral controller module 102 and the system on chip 101, which is used during normal operation of the system, may be identical to a general purpose serial interface such as a two wire interface (TWI) or serial peripheral interface (SPI) and will preferably be controlled by the control logic 110. The control logic 110 may receive interrupts either from the serial interface or from an internal power and clock system (not shown), and will then act accordingly (e.g. by sending commands to the other parts of power management system 108, relaying information from the power management system 108 to the internal power and clock system).

Figure 2 shows another device 200 embodying the invention which is similar to the device 100 shown in Figure 1. However in this device 200 the peripheral controller module 202 does not include control logic. The SoC 101 on the other hand is identical to the previous embodiments and thus the same reference numerals are used. The peripheral controller module 202 is still shown with two external voltage regulators 204, 205 one of which 204 is connected to one of the internal subsystems 118 and the other of which 205 is connected to the other internal subsystem 116. Both are connected to the internal control logic 110.

In this embodiment a signal may be sent by the internal control logic 110 via connections 206, 208 to the external voltage regulators 204, 205 respectively. The signals they receive control the outputs of the external voltage regulators 204, 205. The outputs from the external voltage regulators 204, 205 may simply provide additional power e.g. additional current required for the internal subsystems 118 and 116 to operate optimally to provide support for extra features such as new RF protocols as described for the embodiment presented in Figure 1.

Figure 3 shows a further device 300 embodying the invention which is similar to the device 100 shown in Figure 1. Again, the SoC 101 is identical to that of Figure 1. However in this embodiment the peripheral controller module 302 is able to control the outputs of the internal voltage regulators 112, 114 as well as those in the external module itself. The peripheral controller module's control logic 306 is connected to one of the internal voltage regulators 112 via a connection 308 and to the other internal voltage regulator 114 via a connection 310. This allows for the

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external control logic 306 to override internal control logic 110 so that it can operate the power requirements for the whole device.

5 To achieve this according to the embodiment seen in Figure 3, the external control logic 306 sends a signal via the bi-directional communication 330 to put the power management system 108 in a 'sleep' state i.e. the internal control logic 110 exerts no control over the internal voltage regulators. The external control logic then sends signals to the internal voltage regulators 112, 114 via connections which determine the outputs of the internal voltage regulators 112, 114 to the internal subsystem
10 116, 118, as well as controlling the outputs of the external regulators 304, 305.

In all embodiments discussed, the peripheral controller module may only be active for a portion of the time. The device would then operate as a standard SoC when the peripheral controller module is not active.

15 The embodiments described here are exemplary and non-limiting. For example, although the embodiments described have external voltage regulators located within the peripheral controller module, there may be further embodiments in which the external voltage regulators are not located within the peripheral controller device, and are instead found elsewhere within the electronic device. Furthermore
20 there may be embodiments wherein the external control logic controls a subset of a plurality of external voltage regulators, with the power management system controlling the remaining external voltage regulators. In alternative embodiments the peripheral control module and system on chip also may not be in a single package i.e. in separate packages on the same printed circuit board.

25

Claims

1. An electronic device comprising:
a system on chip, including a plurality of internal subsystems, and a power
management system comprising a plurality of internal voltage regulators arranged
to supply power to the plurality of different internal subsystems, and control logic
which controls the supply of power from the internal voltage regulators;
an external module comprising at least one external voltage regulator and
connected to the system on chip such that the external voltage regulator can
selectively provide power to at least one of said internal subsystems on the system
on chip,
wherein the control logic of the power management system is arranged to
control the at least one external voltage regulator.
2. The electronic device as claimed in claim 1, wherein the external module
comprises a plurality of external voltage regulators.
3. The electronic device as claimed in any preceding claim, further comprising
external control logic separate from the system on chip.
4. The electronic device as claimed in claim 3, wherein the external control
logic is arranged to control at least the external voltage regulator(s).
5. The electronic device as claimed in claim 3 or 4, wherein the external
control logic is arranged to control the internal voltage regulators.
6. The electronic device as claimed in any preceding claim, wherein the
external module is connected directly to a power supply.
7. The electronic device as claimed in claim 6, wherein system on chip is
connected to the same power supply.
8. The electronic device as claimed in claim 6 or 7, wherein the system on chip
is connected to the power supply via the external module.

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9. The electronic device as claimed in any preceding claim, wherein the electronic device comprises a single package with a common set of external pins.

5 10. The electronic device as claimed in any preceding claim, wherein the system on chip further comprises a radio transmitter and receiver.

10 11. The electronic device as claimed in any preceding claim, wherein communications between the system on chip and the external module combine asynchronous signalling with serial interface communications.

12. A method of operating an electronic device comprising:
a system on chip, including a plurality of internal subsystems, and a power management system comprising a plurality of different internal voltage regulators arranged to supply power to the plurality of internal subsystems and control logic
15 which controls the supply power from the internal voltage regulators;
an external module comprising at least one external voltage regulator;
wherein the method comprises the external voltage regulator selectively providing power to at least one of said internal subsystems on the system on chip,
wherein the control logic of the power management system controls the at
20 least one external voltage regulator.

13. The method of operating an electronic device as claimed in claim 12, comprising external control logic separate from the system on chip controlling the internal voltage regulators.

25 14. The method of operating an electronic device as claimed in claim 13, wherein the control logic of the power management system exerts no control over the internal voltage regulators.

30 15. The method of operating an electronic device as claimed in any of claims 13-14, comprising controlling at least one external voltage regulator using the external control logic.

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16. The method of operating an electronic device as claimed in any of claims 13-15, comprising controlling the internal voltage regulators using the external control logic.

5 17. The method of operating an electronic device as claimed in any of claims 12-16, comprising supplying power directly from a power supply to the external module.

10 18. The method of operating an electronic device as claimed in claim 17, comprising supplying power from the power supply to the system on chip.

15 19. The method of operating an electronic device as claimed in claim 18, comprising supplying power from the power supply to the system on chip via the external module.

20 20. The method of operating an electronic device as claimed in any of claims 12-19, comprising communicating between the system on chip and the external module by combining asynchronous signalling with serial interface communications.

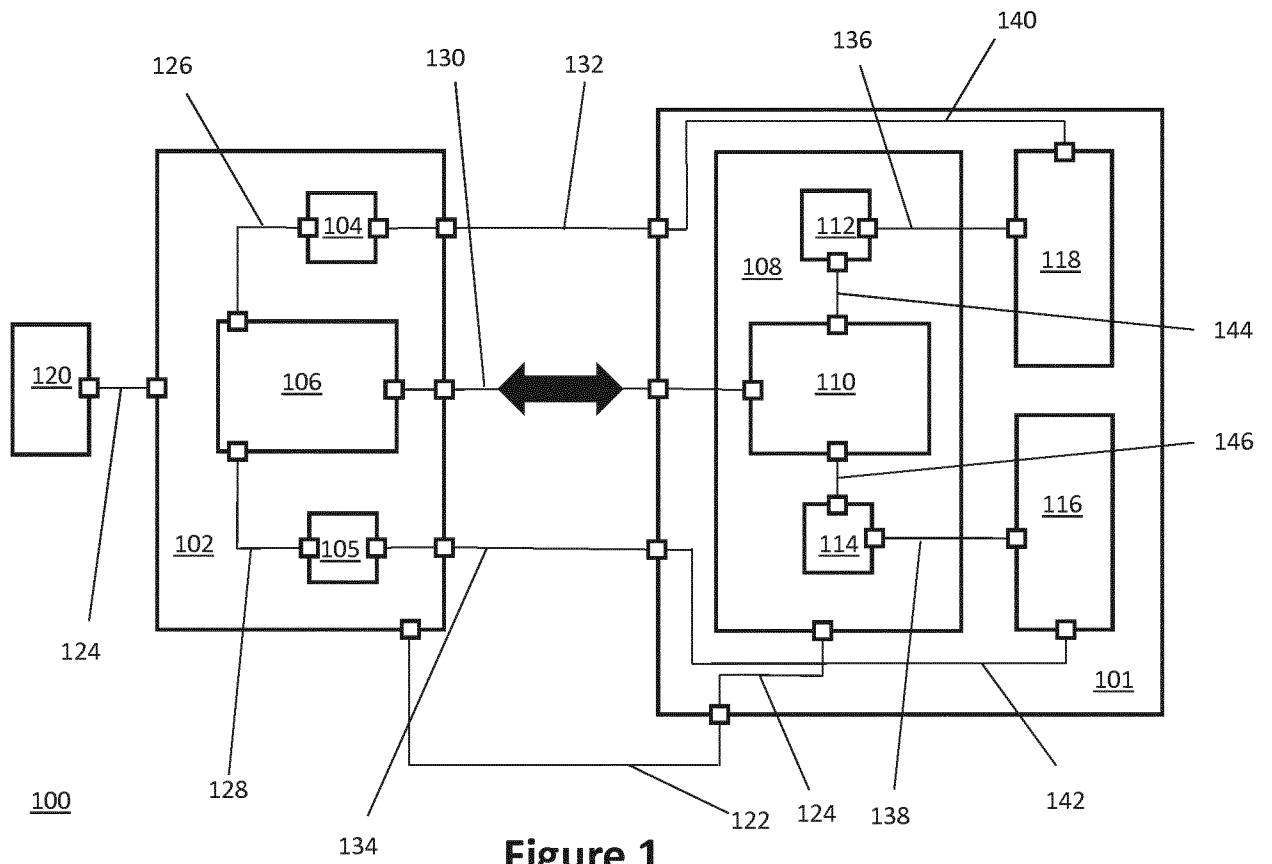


Figure 1

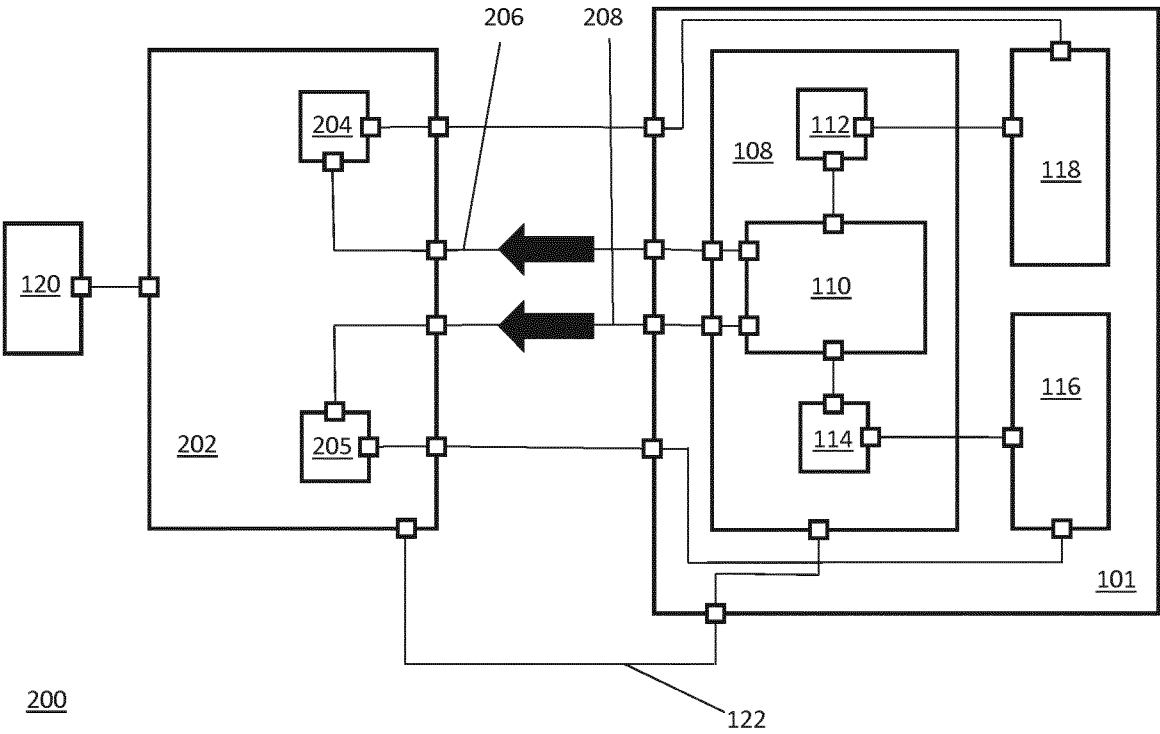


Figure 2

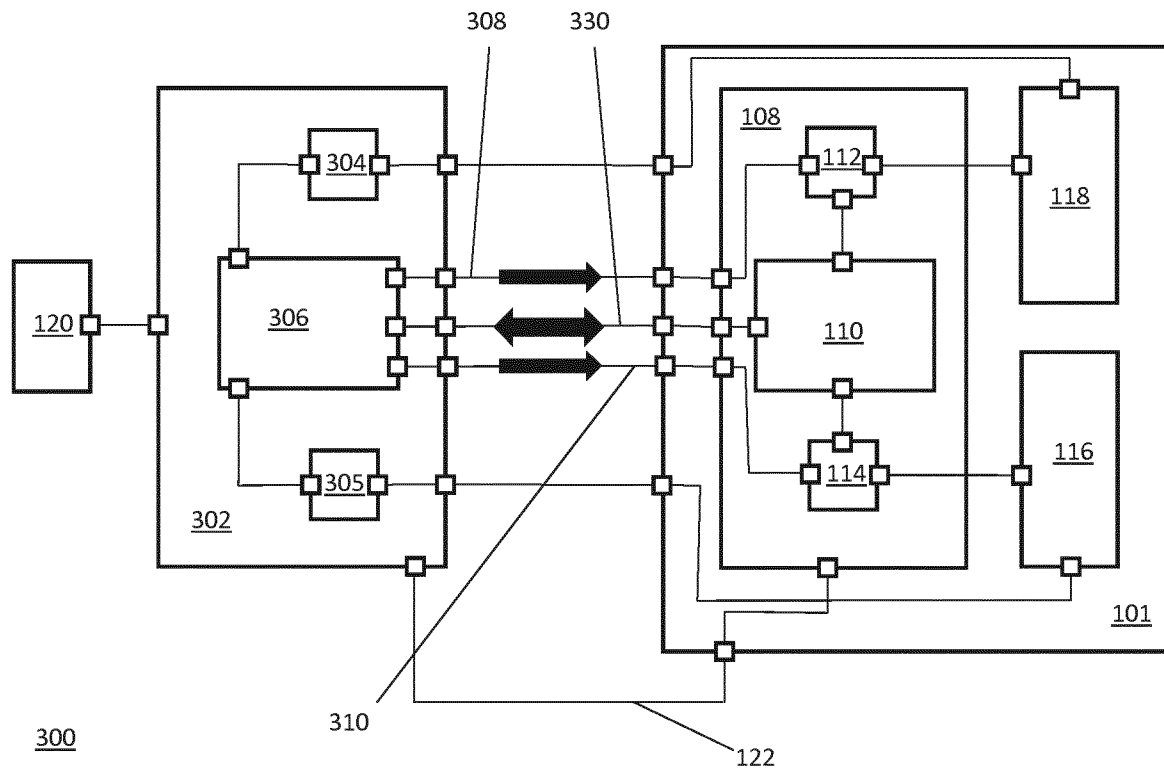


Figure 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/067249

A. CLASSIFICATION OF SUBJECT MATTER

INV. G06F1/26 G06F1/3234 G06F1/32 G05F1/46
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016/224098 A1 (GENDLER ALEXANDER [IL] ET AL) 4 August 2016 (2016-08-04) paragraph [0024] - paragraph [0027]; figure 1 paragraphs [0039], [0050], [0051]; figure 4 paragraph [0052]; figure 5 paragraph [0087] - paragraph [0092]; figure 12	1-20
A	----- WO 2010/140141 A1 (NXP BV [NL]; EVOY DAVID ROSS [US] ET AL.) 9 December 2010 (2010-12-09) page 6, line 22 - page 10, line 26; figures 1,2 page 12, line 5 - line 29; figure 7 ----- -/-	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

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Date of mailing of the international search report

06/09/2019

Name and mailing address of the ISA/

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/067249

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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