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(54) **Title**: METHODS AND DEVICES FOR AVOIDING LOWER PAGE CORRUPTION IN DATA STORAGE DEVICES

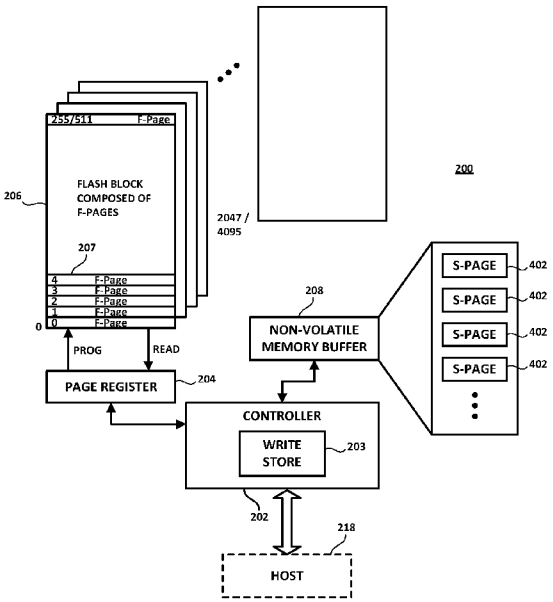

FIG. 2

(57) **Abstract**: A data storage device may comprise a plurality of Multi-Level Ceil (MLC) non- volatile memory devices comprising a plurality of lower pages and a corresponding plurality of higher-order pages. A controller may be configured to write data to and read data from the plurality of lower pages and the corresponding plurality of higher- order pages. A buffer may be coupled to the controller, which may be configured to accumulate data to be written to the MLC non-volatile memory devices, allocate space in the buffer and write the accumulated data to the allocated space, At least a portion of the accumulated data may be written in a lower page of the MLC non- volatile memory devices and the space in the buffer that stores data written to the lower page may be de-allocated when ail higher-order pages corresponding to the lower page have been written in the MLC non-volatile memory devices.

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METHODS AND DEVICES FOR AVOIDING LOWER PAGE CORRUPTION IN DATA STORAGE DEVICES

BACKGROUND

[0001] Flash memory is a non-volatile computer storage technology that can be electrically erased and reprogrammed. Flash memory is typically written in blocks and allocated, garbage collected and erased in larger super blocks or S-Blocks.

[0002] Flash memory comprises a plurality of cells, with each cell being configured to store one, two or more bits per cell. SLC is an abbreviation of "Single-Level Cell", which denotes a configuration in which each cell stores one bit. SLC is characterized not only by fast transfer speeds, low power consumption and high cell endurance, but also by relatively high cost. MLC is an abbreviation of "Multi-level Cell", which denotes a configuration in which each cell stores two or more bits per cell. The acronym MLC is often used to denote a Flash memory having cells that store two bits per cell. That same acronym MLC is also used, however, to designated Flash memory having cells configured to store three bits per cell (also called "TLC" or Triple or Three Level Cell) or even a greater number of bits per cell. When MLC is used to designate a memory that stores two bits in each cell, such an MLC Flash memory may be characterized by somewhat slower transfer speeds, higher power consumption and lower cell endurance than a Single-Level Cell memory. Such MLC memories, however, enjoy a comparatively lower manufacturing cost per bit than do SLC memories.

[0003] In MLC NAND Flash memory, the same physical page of memory cells may be used to store two or more logical pages of data, with each cell being configured to store 2 or more bits. When two bits per cell are stored, a first bit of a lower page is stored first, and then the next bit or bits of one or more higher-order pages are stored. The lower page is programmed first, followed by the higher-order page or pages. When programming the upper page, programming voltages are applied to the same cells that already store valid data in the lower page. Should power fail during the programming of the higher-order page or pages, the stored data in the lower page may be irrecoverably corrupted, as may be the data intended to be stored in the higher-order page or pages. This problem is compounded by the fact that the host may have already received an acknowledgment from the data storage

device indicating that the data stored in the lower page has already been saved to the Flash memory.

[0004] Fig. 1 is a block diagram of aspects of conventional Flash data storage device. As shown therein, the Flash data storage device 100 comprises a controller 104. The controller 104 is coupled to an array of non-volatile memory (e.g., Flash memory devices), collectively referenced at numeral 102. Conventionally, to provide power-fail protection, conventional Flash data storage devices include a backup power source, as shown at 106 in Fig. 1. As indicated at 106, super-capacitors or an array of discrete capacitors are conventionally used to maintain the controller 104 and the non-volatile memory 102 powered-up during a power loss, typically only long enough to finish programming the data to the Flash memory devices 102. Indeed, these super-capacitors or array of discrete capacitors are configured to store a sufficiently large amount of energy to enable the controller 104 to complete any firmware operation (such as a write operation) upon power loss. This is not optimal, however, because super-capacitors are large, unreliable, prone to problems and expensive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Fig. 1 is a block diagram of aspects of a conventional Flash data storage device.

[0006] Fig. 2 is a diagram showing aspects of the physical and logical data organization of a data storage device according to one embodiment.

[0007] Fig. 3 is a block diagram of an S-Block, according to one embodiment.

[0008] Fig. 4 is a block diagram of an S-Page, according to one embodiment.

[0009] Fig. 5 is a block diagram of a data storage device according to one embodiment.

[0010] Fig. 6 is a flowchart of a method of controlling a data storage device according to one embodiment.

DETAILED DESCRIPTION

[0011] Within the scope of the present disclosure, the acronym "MLC"

expressly denotes a Flash memory comprising cells that store two or more bits per cell. In the case wherein such MLC Flash memory is configured to store two bits per cell, data is stored in a lower page and a corresponding upper page. In the case wherein such MLC Flash memory is configured to store three or more bits per cell, data is stored in a lower page and one or more corresponding higher-order pages. The phrase "higher-order pages" is expressly intended to cover the upper page and/or the upper page and one or more pages of higher order.

[0012] Fig. 2 is a diagram showing aspects of the physical and logical data organization of a data storage device 200 according to one embodiment. In one embodiment, the data storage device is an SSD. In another embodiment, the data storage device is a hybrid drive including Flash memory and rotating magnetic storage media. The disclosure is applicable to both SSD and hybrid implementations, but for the sake of simplicity the various embodiments are described with reference to SSD-based implementations. A data storage device controller 202 according to one embodiment may be configured to be coupled to a host, as shown at reference numeral 218. The host 218 may utilize a logical block addressing (LBA) scheme. While the LBA size is normally fixed, the host can vary the size of the LBA dynamically. For example, the physical data storage device may be logically portioned to support partitions configured for LBAs of different sizes. However, such partitions are not required for the physical device to support LBAs of different sizes at the same time. For example, the LBA size may vary by interface and interface mode. Indeed, while 512 bytes is most common, 4 KB is also becoming more common, as are 512+ (520, 528 etc.) and 4 KB+ (4 KB+8, 4K+16 etc.) formats. As shown therein, the data storage device controller 202 may comprise or be coupled to a page register 204. The page register 204 may be configured to enable the controller 202 to read data from and store data to the data storage device 200. The controller 202 may be configured to program and read data from an array of Flash memory devices responsive to data access commands from the host 218. While the description herein refers to Flash memory generally, it is understood that the array of memory devices may comprise one or more of various types of non-volatile memory devices such as Flash integrated circuits, Chalcogenide RAM (C-RAM), Phase Change Memory (PC-RAM or PRAM), Programmable Metallization Cell RAM (PMC-RAM or PMCm), Ovonic Unified

Memory (OUM), Resistance RAM (RRAM), NAND memory (e.g., single-level cell (SLC) memory, multi-level cell (MLC) memory, or any combination thereof), NOR memory, EEPROM, Ferroelectric Memory (FeRAM), Magnetoresistive RAM (MRAM), other discrete NVM (non-volatile memory) chips, or any combination thereof.

[0013] The page register 204 may be configured to enable the controller 202 to read data from and store data to the array. According to one embodiment, the array of Flash memory devices may comprise a plurality of non-volatile memory devices in die (e.g., 128 dies), each of which comprises a plurality of blocks, such as shown at 206 in Fig. 2. Other page registers 204 (not shown), may be coupled to blocks on other die. A combination of Flash Blocks, grouped together, may be called a Superblock or S-Block. In some embodiments, the individual blocks that form an S-Block may be chosen from one or more dies, planes or other levels of granularity. An S-Block, therefore, may comprise a plurality of Flash Blocks, spread across one or more die, that are combined together. In this manner, the S-Block may form a unit on which the Flash Management System (FMS) operates. In some embodiments, the individual blocks that form an S-Block may be chosen according to a different granularity than at the die level, such as the case when the memory devices include dies that are sub-divided into structures such as planes (i.e., blocks may be taken from individual planes). According to one embodiment, allocation, erasure and garbage collection may be carried out at the S-Block level. In other embodiments, the FMS may perform data operations according to other logical groupings such as pages, blocks, planes, dies, etc.

[0014] According to one embodiment, the array of MLC non-volatile memory devices may comprise a plurality of lower pages and a corresponding plurality of higher-order pages. That is, each lower page may be associated with a corresponding single upper page or with a corresponding plurality (i.e., two or more) of higher-order pages. The MLC non-volatile memory devices may be organized in Flash Blocks 206, with each Flash Block comprising a plurality of Flash Pages (F-Pages) 207, as shown in Fig. 2. Alternatively, a different physical organization may be employed. An F-Page, according to one embodiment, may be the size of the minimum unit of program of the non-volatile memory devices. The controller 202 may be coupled to the plurality of non-volatile memory devices and may be

configured to write data to and read data from the plurality of lower pages and to one or more corresponding higher-order pages. To address the lower-page corruption problem afflicting conventional data storage devices, one embodiment of a data storage device 200 comprises a buffer 208. In one embodiment, the buffer comprises a non-volatile memory. As write commands are received from the host 218 and executed by the controller 202, the data to be written to the MLC non-volatile memory devices (i.e., Flash Blocks 206) may be accumulated. According to one embodiment, the data to be written may be accumulated within a write store 203. The write store 203 may be coupled to the controller 202. In one embodiment, the write store 203 is a store that is internal to the controller 202. Contemporaneously with the accumulation of the data in the write store 203 (or at least shortly before or after such accumulation), the controller 202 may allocate memory space in the buffer 208 and may write the accumulated data to the allocated space in the buffer 208. According to one embodiment, the data to be written to the MLC non-volatile memory devices may be stored in both the write store 203 and the buffer 208, such that the buffer 208 and the write store 203 mirror or substantially mirror each other. Indeed, according to one embodiment, the controller 202 may be configured to accumulate data to be written in the write store 203 and in the buffer 208 until a complete F-page is constructed. According to one embodiment, a partial F-Page may be packed with a predetermined coded value and considered to be complete. Completed F-Pages may be written to the MLC non-volatile memory devices. That is, at least a portion of the accumulated data may be written to a lower page of the MLC non-volatile memory devices. According to one embodiment, previously-allocated space in the buffer 208 may be de-allocated when all higher-order pages corresponding to the lower page have been written in the MLC non-volatile memory devices. That is, the controller 202 may be configured to keep lower page data in the buffer 208 until the upper page or high-order pages corresponding to the lower page have been programmed. This ensures that a power-safe copy of the write data is maintained in the buffer 208 until both the lower and higher-order page or pages have been programed, after which the data may be considered to be power-fail and corruption safe.

[0015] According to one embodiment, in the normal course of operation of the data storage device 200, as complete F-Pages are constructed (and

accumulated in the write store 203 and written out to the buffer 208), they may be written out to the MLC non-volatile memory devices. According to one embodiment, it is the completed F-Pages stored in the write store 203 that are written out to the MLC non-volatile memory devices. Indeed, it may be preferable to write the completed F-Pages out from the write store 203 rather than from the buffer 208, as the write store 203 may be able to support a greater bandwidth than the buffer 208.

[0016] According to one embodiment, the buffer 208 may comprise non-volatile memory. For example, the buffer 208 may comprise memory that is non-volatile and that is characterized as having high access, read and write speeds. According to one embodiment, the buffer 208 may comprise Magnetic Random Access Memory (MRAM). Other memory types may also be used. MRAM may exhibit performance that is similar to that of SRAM, a density comparable to DRAM and low power consumption. Moreover, MRAM is not known to degrade over time. Although relatively costly, MRAM is well suited to the task of the buffer 208; namely, to store a power-safe copy of lower page data at least until the corresponding higher-order page(s) have been safely stored in the Flash Blocks 206. It is to be noted, however that, as of this writing, the cost of implementing the buffer 208 in MRAM is still less costly than the conventional use of super-capacitors or the use of an array of discrete capacitors. In the implementation in which the buffer 208 comprises non-volatile memory such as MRAM, the data written thereto that has not yet been safely stored in the Flash Blocks 206 (such as lower page data whose corresponding higher-order page(s) were not stored to Flash before a power-fail event) may be read out from the buffer 208 by the controller 202 and stored in the Flash Blocks 206 upon restoration of the power to the data storage device 200. That is, the controller 202 may be further configured to read data from the buffer 208 and write at least a portion of the read data to the non-volatile memory devices of the Flash Blocks 206, after power is restored to the data storage device 200 subsequent to a loss of power thereto.

[0017] According to one embodiment, the buffer 208 may be configured to be at least sufficiently large to enable recovery from lower page corruption after a power loss to the data storage device. The size of the buffer 208, therefore, may vary with, for example, the number of pages between lower and higher-order pages, the size of the F-Pages, the number of planes and dies of the data storage device.

For example, the size of the buffer 208 may vary from a few MB to a few hundreds of MB, although other implementations may utilize other sizes to good effect. According to one embodiment, the buffer 208 may comprise a plurality of buffers for each die, as each die completes its programming at a different time. This enables multiple pages per die to be managed independently, leading to an efficient configuration of the buffer 208. The buffer 208 may, for example, be implemented as a plurality of buffers from which the controller 202 allocates space, stores data and de-allocates space, as the higher-order page(s) of corresponding lower pages are stored in the Flash Blocks 206. Such a buffer configuration is well suited to buffering the stream of write data from host write commands until the probability of lower page corruption upon power fail is acceptably small or zero. According to one embodiment, the controller 202 may be configured to generate and send a write acknowledgement to the host 218 after (e.g., as soon as) the accumulated data is written to the allocated space in the buffer. That is, from the host's perspective, the data may be considered to have been safely stored in Flash as soon as it is stored in the buffer 208. According to one embodiment, the MLC non-volatile devices may be run in lower-page only mode or in "SLC" mode. In that case, since there are no higher-order pages to contend with, de-allocation of space in the buffer 208 may be carried out as soon as the page in MLC lower-page only mode or the page in SLC mode is programmed and need not be delayed while waiting for any higher-ordered pages to be programmed.

[0018] Fig. 3 is a block diagram of an S-Block, according to one embodiment. As shown therein, an S-Block 302 may comprise one Flash block (F-Block) 206 per die. An S-Block, therefore, may be thought of as a collection of F-Blocks, one F-Block per die, that are combined together to form a unit of the Flash Management System (FMS) of the data storage device. According to one embodiment, allocation, erasure and GC may be managed at the S-Block level. Each F-Block 206, as shown in Fig. 3, may comprise a plurality of Flash pages (F-Page) such as, for example, 256 or 512 F-Pages. An F-Page, according to one embodiment, may be the size of the minimum unit of program for a given non-volatile memory device. Fig. 4 shows a super page (S-page), according to one embodiment. As shown therein, an S-page 402 may comprise one F-Page per F-Block of an S-Block, meaning that an S-page spans across an entire S-Block. According to one

embodiment shown in Fig. 2, the data may be accumulated, written and stored in units of S-Pages 402. The buffer 208 may be configured to store write data organized differently than S-Pages 402, depending upon the specific implementation.

[0019] Fig. 5 is a block diagram of another data storage device 500, according to one embodiment. With reference to Fig. 2, like reference numerals denote like elements and the description of such like elements omitted for brevity. In this embodiment, the controller 502 need not (but may) comprise a write store, such as write store 203 in Fig. 2. A volatile memory buffer 504 (or a plurality of such volatile memory buffers) may be coupled to the controller 502. For example, the volatile memory buffer 504 may comprise or be configured in a Dynamic Random Access Memory (DRAM). The volatile memory buffer 504 is shown in Fig. 5 as being external to the controller 502. However, the volatile memory buffer 504 may also be internal to the controller 502, which may translate into faster access times by the controller 502. However, size and/or other considerations may recommend that the volatile memory buffer 504 be configured as an external memory buffer coupled to the controller 502. The data storage device 500 of Fig. 5 may also comprise a backup source of power such as shown at 506 and a non-volatile memory, as shown at 508. The backup source of power 506 may be coupled to the volatile memory buffer 504, to the controller 502 and to the non-volatile memory 508. The backup source of power 506 may be configured to keep at least the volatile memory buffer 504, the controller 502 and/or the non-volatile memory 508 powered-up for a period of time upon a power fail event, without loss of data in the volatile memory 504 (at least until the contents thereof can be saved to the non-volatile memory 508). According to one embodiment, the backup power source 506 may be configured to power at least portions of the data storage device of Fig. 5 at least as long as necessary for the controller 502 to write the data from the volatile buffer 504 to the non-volatile memory 508. The backup power source 506 may comprise capacitors, super-capacitors and/or any energy storage elements. In one embodiment where the data storage device is a hybrid disk drive or a solid state drive coupled with a hard disk drive, the power source 506 may be provided by the BEMF (back electromotive force) generated from the spindle motor of the hard disk drive.

[0020] Indeed, during normal operation, as write commands are

received from the host 218 and executed by the controller 502, the data to be written to the MLC non-volatile memory devices (i.e., Flash Blocks 206) may be written to both the volatile memory buffer 504 and to the MLC non-volatile memory devices. According to one embodiment, the controller 502 may be configured to accumulate data to be written (as directed by write commands issued by the host 218, for example) internally (in a write store 203, for example) until a complete F-page is constructed. Alternatively and according to one embodiment, a partial F-Page may be packed with a predetermined coded value and considered to be complete. Completed F-Pages may then be written both to the volatile memory buffer 504 and to the MLC non-volatile memory devices. According to one embodiment, the data may also be accumulated, written and stored in units of S-Pages 402 or any other data organization unit. Indeed, the volatile memory buffer 504 may be configured to store write data organized differently than S-Pages 402, depending upon the specific implementation. According to one embodiment, therefore, in addition to writing the accumulated data (or a portion thereof) to volatile memory buffer 504, the accumulated data (or a portion thereof) may be written to one or more lower and/or upper pages of the MLC non-volatile memory devices (the Flash Blocks 206). According to one embodiment, previously-allocated space in the volatile memory buffer 504 may be de-allocated and the de-allocated space therein reused for new write data when all higher-order pages corresponding to a previously-programmed lower page have been written in the MLC non-volatile memory devices and thus may be considered to be effectively corruption-safe. That is, the controller 202 may be configured to keep lower page data in the volatile memory buffer 504 at least until the upper page or high-order pages corresponding to the lower page have been programmed in the MLC non-volatile memory devices.

[0021] In the event of a power loss, the backup power source 506 may supply power at least to the controller 502, the volatile memory buffer 504 and/or the non-volatile memory 508. During the time the controller 502, the volatile memory buffer 504 and/or the non-volatile memory 508 are powered by the backup power source 506, the controller 502 may cause data stored in the volatile memory buffer 504 to be copied to the non-volatile memory 508, thereby saving the data that has not yet been saved to the MLC non-volatile memory devices in a corruption safe manner, thereby enabling the controller to acknowledge the write to the host 218.

When power to the MLC non-volatile memory devices is restored, the data saved in the non-volatile memory 508 may be programmed into the MLC non-volatile memory devices.

[0022] It is to be noted that the non-volatile memory 508 may, according to one embodiment, be written to only in the event of a power failure. Moreover, by powering only the controller 502, the volatile memory buffer 504 and the non-volatile memory 508 in the event of a power failure, comparatively less power is required than would be required to also power the dies of the MLC non-volatile memory devices (e.g., Flash Blocks 206). It is to be noted that the non-volatile memory 508 may draw its power from the controller 502 that is powered by the backup power source 506. According to one embodiment, the non-volatile memory 508 may comprise MRAM. According to one embodiment, the backup power source 506 need only be coupled to the controller 502 and to the volatile memory buffer 504. In addition, by using the volatile memory buffer 504 as the primary write location in the data path and the non-volatile memory 508 in the event of a power failure, the wear on the non-volatile memory 508 is reduced.

[0023] Fig. 6 is a flowchart of a method of controlling a data storage device according to one embodiment. The data storage device may comprise a buffer and a plurality of Multi-Level Cell (MLC) non-volatile memory devices (comprising, e.g., the Flash Blocks 206). The MLC non-volatile memory devices may comprise, as described herein, a plurality of lower pages and a corresponding plurality of higher-order pages. A controller, such as shown at 502, may be configured to write and read data to and from the plurality of lower pages and the corresponding plurality of higher-order pages. According to one embodiment and as shown in Fig. 6, the method may comprise accumulating data to be written to the MLC non-volatile memory devices, as shown at Block B61. Block B62 calls for allocating space in a buffer 208, 504 and writing the accumulated data to the allocated space in the buffer 208, 504. As shown at B63, at least a portion of the accumulated data may be written to one or more lower pages of the MLC non-volatile memory devices. It is understood that a portion of the accumulated data may also be written to one or more upper pages of the MLC non-volatile memory devices. When all higher-order pages corresponding to the lower page have been written in the MLC non-volatile memory devices, space in the buffer that stores data written to

the lower page may be safely de-allocated, as called for in Block B64.

[0024] According to one embodiment and as shown in Fig. 2, the buffer may comprise or be configured as a non-volatile memory such as, for example, Magnetic Random Access Memory (MRAM). As described relative to Fig. 2 and as shown at B65 in Fig. 5, the method may also comprise reading data from the buffer 208 and writing at least a portion of the read data to the MLC non-volatile memory devices, after power is restored to the data storage device subsequent to a loss thereof. As described relative to Fig. 5, the method may also comprise reading data from the volatile memory buffer 504 and writing at least a portion of the read data to the non-volatile memory 508, after power is restored (e.g., by the backup power source 506) to the data storage device after a power loss, as shown at B65 in Fig. 6. According to one embodiment, the buffer 208, 504 may be at least sufficiently large to enable recovery from a possible lower page corruption after a power loss to the data storage device. According to one embodiment, the buffer 208, 504 may be configured as one or more buffers. A write acknowledgment to the host 218 may be generated and sent after the accumulated data is written to the allocated space in the buffer 208, 504, as the data may be considered, from that point in time forward, to be corruption-safe. According to one embodiment, the MLC non-volatile memory devices may be configured to comprise a plurality of blocks, each of which comprising a plurality of physical pages. A collection of such blocks may define a superblock (S-Block). A collection of physical pages with one physical page per block in an S-Block may define a superpage (S-Page), which may be the unit by which the controller 202 accumulates, writes and stores host and/or other data. Other data organizations and units may be implemented within the present context.

[0025] As shown in and described relative to Fig. 5, the method may also comprise providing a backup source of power 506 and a non-volatile memory, such as a non-volatile memory, such as shown at 508. The buffer 504, in this embodiment, may comprise volatile memory. The method may, according to one embodiment, further comprise powering at least a portion of the data storage device 500 for at least as long as necessary for the controller 502 to write the data from the buffer 504 to the non-volatile memory 508. According to one embodiment, after power is restored to the data storage device after a loss thereof, at least a portion of the data in the non-volatile memory 508 may be written to the MLC non-volatile

memory devices. A write store (203 in Figs. 2 and 5) may be provided, and the controller 202, 502 may be configured to write the accumulated data to the write store 203 as the accumulated data is written to the allocated space in the buffer 208, 504. According to one embodiment, the controller 202, 502 may also be configured to de-allocate space, in the buffer 208, 504, that stores data written to the higher-order pages when all higher-order pages corresponding to the lower page have been written in the MLC non-volatile memory devices, as such data may be considered to be corruption-safe.

[0026] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the present disclosure. Indeed, the novel methods, devices and systems described herein may be embodied in a variety of other forms. Furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the present disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the present disclosure. For example, those skilled in the art will appreciate that in various embodiments, the actual structures may differ from those shown in the figures. Depending on the embodiment, certain of the steps described in the example above may be removed, others may be added. Also, the features and attributes of the specific embodiments disclosed above may be combined in different ways to form additional embodiments, all of which fall within the scope of the present disclosure. Although the present disclosure provides certain preferred embodiments and applications, other embodiments that are apparent to those of ordinary skill in the art, including embodiments which do not provide all of the features and advantages set forth herein, are also within the scope of this disclosure. Accordingly, the scope of the present disclosure is intended to be defined only by reference to the appended claims.

CLAIMS:

1. A data storage device, comprising:

a plurality of Multi-Level Cell (MLC) non-volatile memory devices comprising a plurality of lower pages and a corresponding plurality of higher-order pages;

a controller coupled to the plurality of MLC non-volatile memory devices and configured to write data to and read data from the plurality of lower pages and the corresponding plurality of higher-order pages; and

a buffer coupled to the controller;

wherein the controller is configured to:

accumulate data to be written to the MLC non-volatile memory devices;

allocate space in the buffer and write the accumulated data to the allocated space in the buffer;

write at least a portion of the accumulated data in a lower page of the MLC non-volatile memory devices; and

de-allocate space in the buffer that stores data written to the lower page when all higher-order pages corresponding to the lower page have been written in the MLC non-volatile memory devices.

2. The data storage device of claim 1, wherein the buffer comprises non-volatile memory.

3. The data storage device of claim 2, wherein the non-volatile memory comprises Magnetic Random Access Memory (MRAM).

4. The data storage device of claim 1, wherein the controller is further configured to read data from the buffer and write at least a portion of the read data to the MLC non-volatile memory devices, after power is restored to the data storage device after a loss of power.

5. The data storage device of claim 1, wherein the buffer is at least sufficiently large to enable recovery from lower page corruption after a power loss to the data storage device.

6. The data storage device of claim 1, wherein the MLC non-volatile devices are configured to operate in lower page only mode or in Single Level Cell (SLC) mode.

7. The data storage device of claim 1, wherein the controller is further configured to generate and send a write acknowledgement to a host after the accumulated data is written to the allocated space in the buffer.

8. The data storage device of claim 1, wherein the MLC non-volatile memory devices comprise a plurality of blocks, each of the plurality of blocks comprising a plurality of physical pages, a collection of blocks defining a superblock (S-Block), a collection of physical pages with one physical page per block in an S-Block defining a superpage (S-Page), and wherein the data is accumulated, written and stored in units of S-Pages.

9. The data storage device of claim 1, further comprising a backup source of power and a non-volatile memory, wherein the buffer comprises volatile memory and wherein the backup source of power is configured to power at least a portion of the data storage device at least as long as necessary for the controller to write the data from the buffer to the non-volatile memory.

10. The data storage device of claim 9, wherein the non-volatile memory comprises Magnetic Random Access Memory (MRAM).

11. The data storage device of claim 9, wherein the controller is further configured to write at least a portion of the data in the non-volatile memory to the MLC non-volatile memory devices, after power is restored to the data storage device after a loss of power.

12. The data storage device of claim 1, further comprising a write store and wherein the controller is further configured to write the accumulated data to the write store as the accumulated data is written to the allocated space in the buffer.

13. The data storage device of claim 1, wherein controller is further configured to also de-allocate space in the buffer that stores data written to the higher-order pages when all higher-order pages corresponding to the lower page have been written in the MLC non-volatile memory devices.

14. A data storage device controller, comprising:

a processor configured to couple to a buffer and to a plurality of Multi-Level Cell (MLC) non-volatile memory devices that comprise a plurality of lower pages and a corresponding plurality of higher-order pages, the processor being further configured to:

read data from the plurality of lower pages and the corresponding plurality of higher-order pages; and

write data to the plurality of lower pages and the corresponding plurality of higher-order pages by at least:

accumulating data to be written to the MLC non-volatile memory devices;

allocating space in the buffer and writing the accumulated data to the allocated space in the buffer;

writing at least a portion of the accumulated data in a lower page of the MLC non-volatile memory devices; and

de-allocating space in the buffer that stores data written to the lower page when all higher-order pages corresponding to the lower page have been written in the MLC non-volatile memory devices.

15. The data storage device controller of claim 14, wherein the buffer comprises non-volatile memory.

16. The data storage device controller of claim 15, wherein the non-volatile memory comprises Magnetic Random Access Memory (MRAM).

17. The data storage device controller of claim 14, wherein the processor is further configured to read data from the buffer and write at least a portion of the read data to the MLC non-volatile memory devices, after power is restored to the

data storage device after a loss of power.

18. The data storage device controller of claim 14, wherein the buffer is at least sufficiently large to enable recovery from lower page corruption after a power loss to the data storage device.

19. The data storage device controller of claim 14, wherein the MLC non-volatile devices are configured to operate in lower page only mode or in Single Level Cell (SLC) mode.

20. The data storage device controller of claim 14, wherein the processor is further configured to generate and send a write acknowledgement to a host after the accumulated data is written to the allocated space in the buffer.

21. The data storage device controller of claim 14, wherein the MLC non-volatile memory devices comprise a plurality of blocks, each of the plurality of blocks comprising a plurality of physical pages, a collection of blocks defining a superblock (S-Block), a collection of physical pages with one physical page per block in an S-Block defining a superpage (S-Page), and wherein the data is accumulated, written and stored in units of S-Pages.

22. The data storage device controller of claim 14, further comprising a backup source of power and a non-volatile memory, wherein the buffer comprises volatile memory and wherein the backup source of power is configured to power at least a portion of the data storage device at least as long as necessary for the controller to write the data from the buffer to the non-volatile memory.

23. The data storage device controller of claim 22, wherein the non-volatile memory comprises Magnetic Random Access Memory (MRAM).

24. The data storage device controller of claim 22, wherein the processor is further configured to write at least a portion of the data in the non-volatile memory to the MLC non-volatile memory devices, after power is restored to the data storage

device after a loss of power.

25. The data storage device controller of claim 14, further comprising a write store and wherein the processor is further configured to write the accumulated data to the write store as the accumulated data is written to the allocated space in the buffer.

26. The data storage device controller of claim 14, wherein processor is further configured to also de-allocate space in the buffer that stores data written to the higher-order pages when all higher-order pages corresponding to the lower page have been written in the MLC non-volatile memory devices.

27. A method of controlling a data storage device, the data storage device comprising a buffer and a plurality of Multi-Level Cell (MLC) non-volatile memory devices that comprise a plurality of lower pages and a corresponding plurality of higher-order pages, the method comprising:

reading data from the plurality of lower pages and the corresponding plurality of higher-order pages; and

writing data to the plurality of lower pages and the corresponding plurality of higher-order pages by at least:

accumulating data to be written to the MLC non-volatile memory devices;

allocating space in the buffer and writing the accumulated data to the allocated space in the buffer;

writing at least a portion of the accumulated data in a lower page of the MLC non-volatile memory devices; and

de-allocating space in the buffer that stores data written to the lower page when all higher-order pages corresponding to the lower page have been written in the MLC non-volatile memory devices.

28. The method of claim 27, wherein the buffer comprises non-volatile memory.

29. The method of claim 28, wherein the non-volatile memory comprises Magnetic Random Access Memory (MRAM).

30. The method of claim 27, further comprising reading data from the buffer and writing at least a portion of the read data to the MLC non-volatile memory devices, after power is restored to the data storage device after a loss of power.

31. The method of claim 27, wherein the buffer is at least sufficiently large to enable recovery from lower page corruption after a power loss to the data storage device.

32. The method of claim 27, wherein the MLC non-volatile devices are configured to operate in lower page only mode or in Single Level Cell (SLC) mode.

33. The method of claim 27, further comprising generating and sending a write acknowledgement to a host after the accumulated data is written to the allocated space in the buffer.

34. The method of claim 27, wherein the MLC non-volatile memory devices comprise a plurality of blocks, each of the plurality of blocks comprising a plurality of physical pages, a collection of blocks defining a superblock (S-Block), a collection of physical pages with one physical page per block in an S-Block defining a superpage (S-Page), and accumulating, writing and storing is carried out in units of S-Pages.

35. The method of claim 27, further comprising a backup source of power and a non-volatile memory, wherein the buffer comprises volatile memory and wherein the method further comprises the backup source of power powering at least a portion of the data storage device at least as long as necessary for the controller to write the data from the buffer to the non-volatile memory.

36. The method of claim 35, wherein the non-volatile memory comprises Magnetic Random Access Memory (MRAM).

37. The method of claim 35, further comprising writing at least a portion of the data in the non-volatile memory to the MLC non-volatile memory devices, after power is restored to the data storage device after a loss of power.

38. The method of claim 27, wherein the data storage device further comprises a write store and wherein writing data further comprises writing the accumulated data to the write store as the accumulated data is written to the allocated space in the buffer.

39. The method of claim 27, further comprising de-allocating space in the buffer that stores data written to the higher-order pages when all higher-order pages corresponding to the lower page have been written in the MLC non-volatile memory devices.

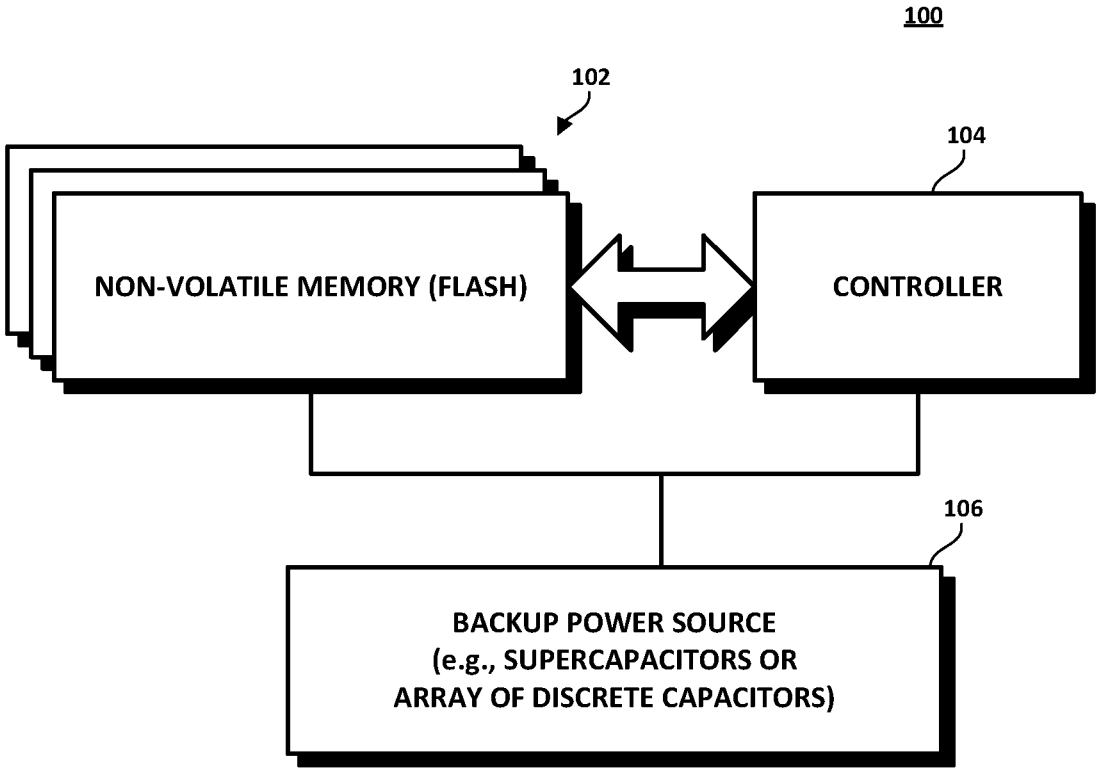


FIG. 1

(Prior Art)

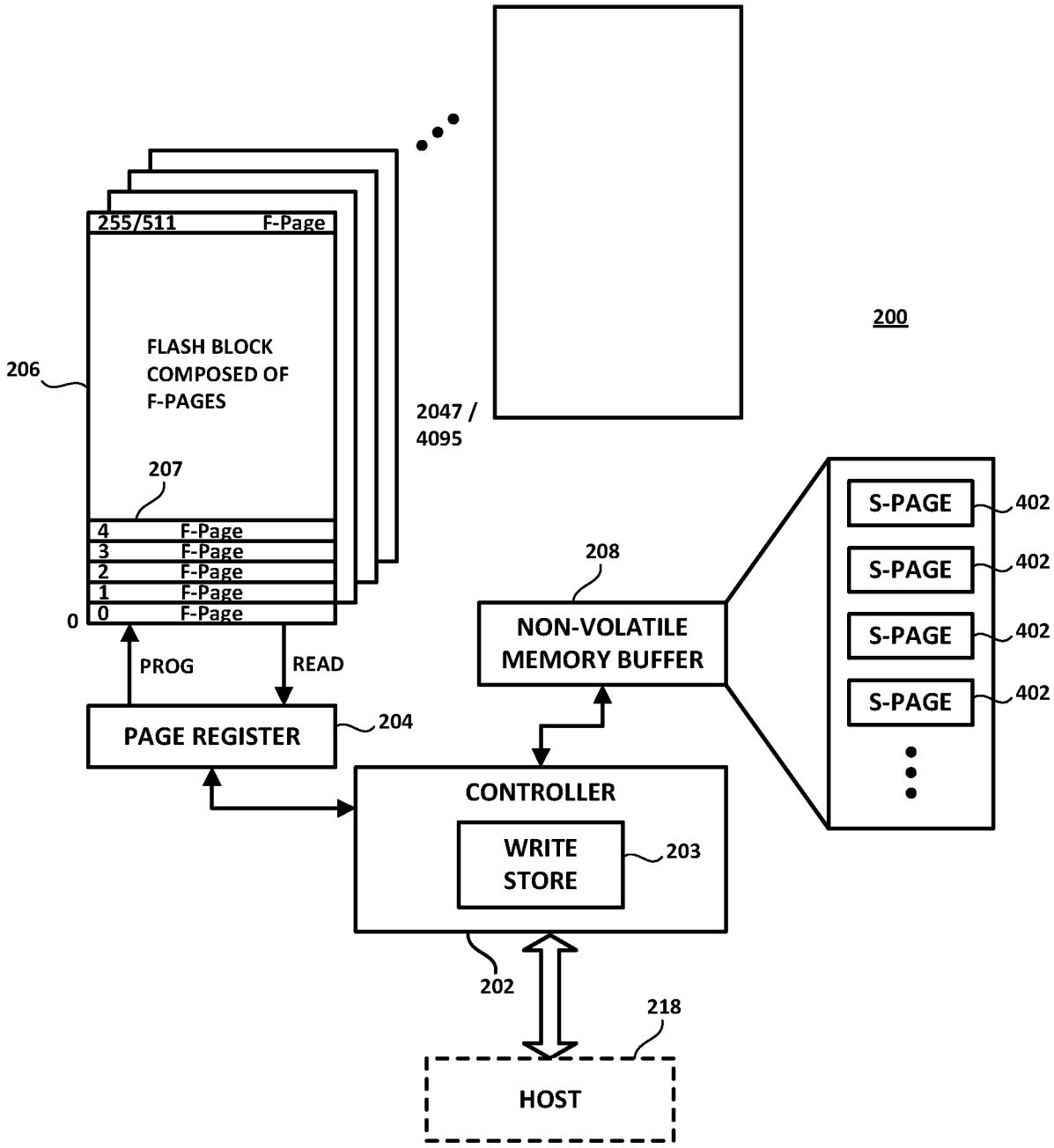
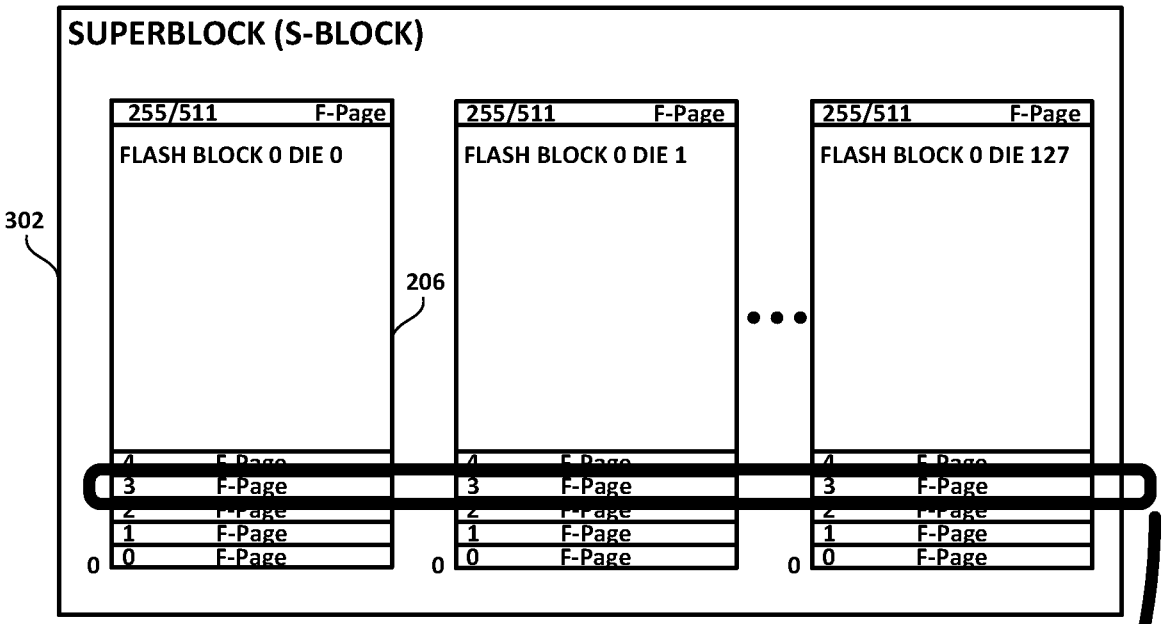

200
2047 / 4095
255/511 F-Page
FLASH BLOCK COMPOSED OF F-PAGES
206
207
4 F-Page
3 F-Page
2 F-Page
1 F-Page
0 F-Page
0
PROG
READ
PAGE REGISTER
204
208
NON-VOLATILE MEMORY BUFFER
S-PAGE
S-PAGE
S-PAGE
S-PAGE
402
402
402
402
CONTROLLER
WRITE STORE
203
202
218
HOST

FIG. 2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FLASH BLOCK 0 DIE 0
FLASH BLOCK 0 DIE 1
FLASH BLOCK 0 DIE 127
302
206
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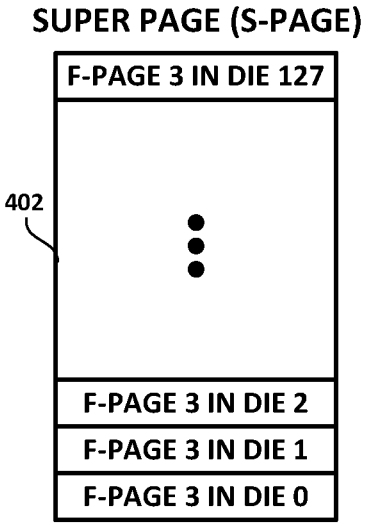
1 F-Page
0 F-Page
0
0
0

FIG. 3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F-PAGE 3 IN DIE 127
402
F-PAGE 3 IN DIE 2
F-PAGE 3 IN DIE 1
F-PAGE 3 IN DIE 0

FIG. 4

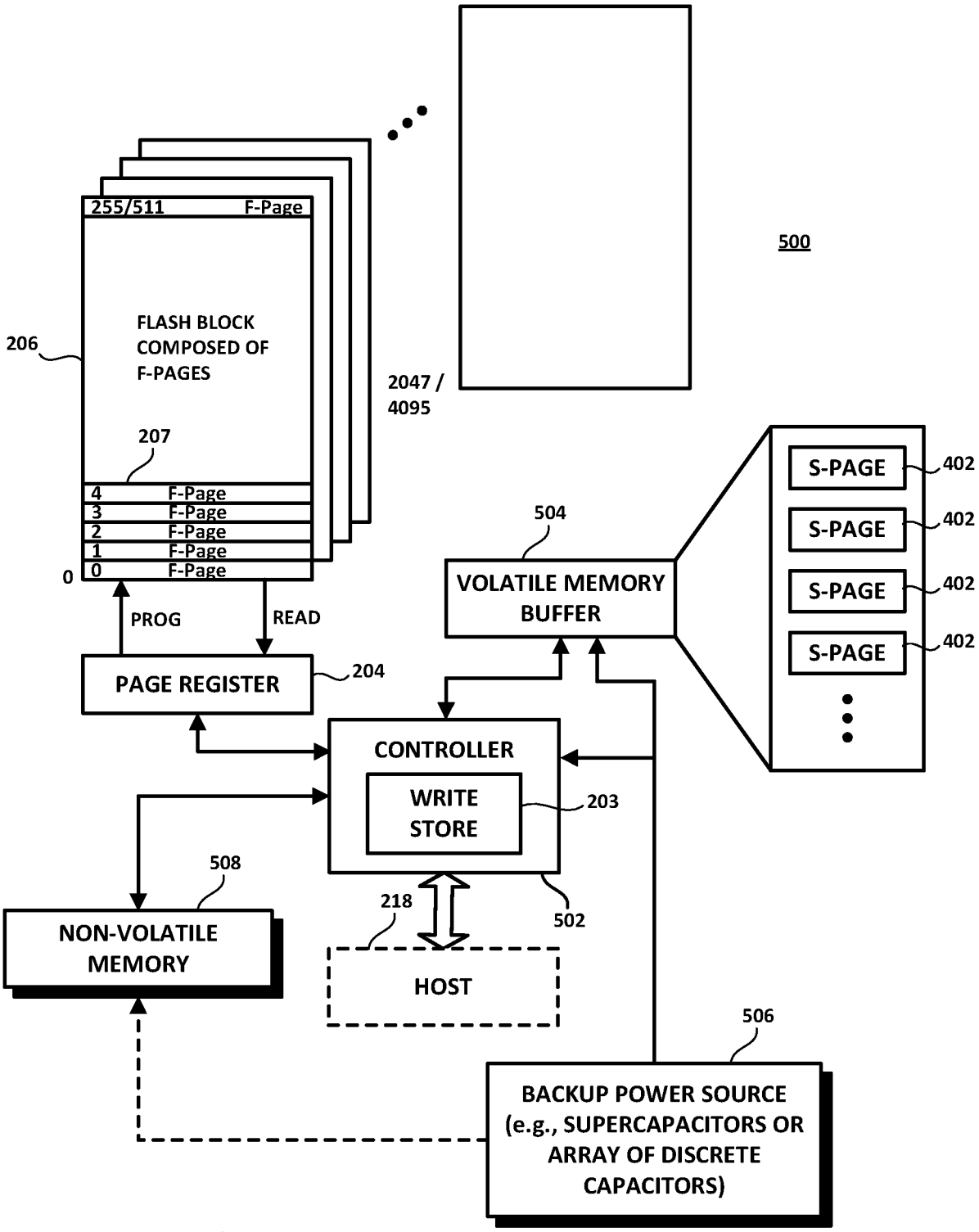
500
2047 / 4095
255/511 F-Page
FLASH BLOCK COMPOSED OF F-PAGES
206
207
4 F-Page
3 F-Page
2 F-Page
1 F-Page
0 F-Page
0
PROG
READ
PAGE REGISTER
204
504
VOLATILE MEMORY BUFFER
S-PAGE
S-PAGE
S-PAGE
S-PAGE
402
402
402
402
CONTROLLER
WRITE STORE
203
508
NON-VOLATILE MEMORY
218
502
HOST
506
BACKUP POWER SOURCE (e.g., SUPERCAPACITORS OR ARRAY OF DISCRETE CAPACITORS)

FIG. 5

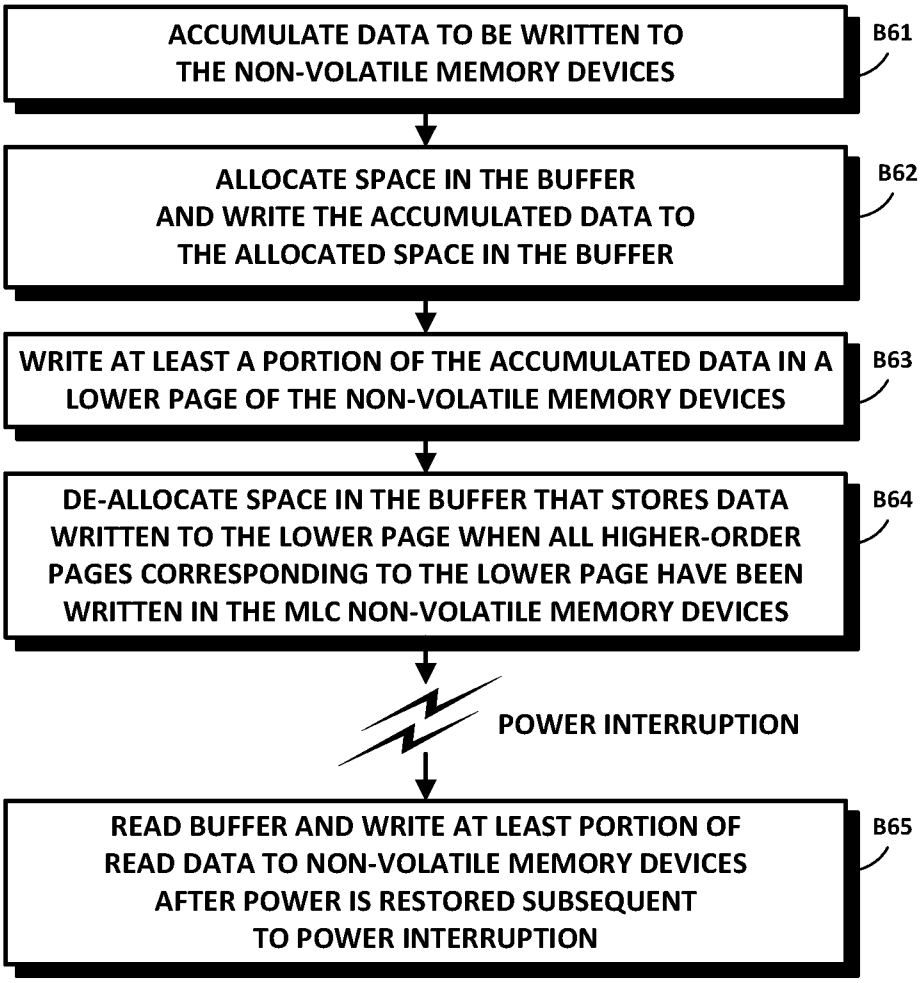
ACCUMULATE DATA TO BE WRITTEN TO THE NON-VOLATILE MEMORY DEVICES
B61
ALLOCATE SPACE IN THE BUFFER AND WRITE THE ACCUMULATED DATA TO THE ALLOCATED SPACE IN THE BUFFER
B62
WRITE AT LEAST A PORTION OF THE ACCUMULATED DATA IN A LOWER PAGE OF THE NON-VOLATILE MEMORY DEVICES
B63
DE-ALLOCATE SPACE IN THE BUFFER THAT STORES DATA WRITTEN TO THE LOWER PAGE WHEN ALL HIGHER-ORDER PAGES CORRESPONDING TO THE LOWER PAGE HAVE BEEN WRITTEN IN THE MLC NON-VOLATILE MEMORY DEVICES
B64
POWER INTERRUPTION
READ BUFFER AND WRITE AT LEAST PORTION OF READ DATA TO NON-VOLATILE MEMORY DEVICES AFTER POWER IS RESTORED SUBSEQUENT TO POWER INTERRUPTION
B65

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/062725

A. CLASSIFICATION OF SUBJECT MATTER

G06F 12/00(2006.01)i, G06F 12/08(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F 12/00; G06F 12/02; H03M 13/05; G06F 11/10; G06F 11/14; G06F 12/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: multi level cell, buffer, memory, power, loss, corrupt, interrupt, allocate, lower, higher, page, read, write, space, accumulate, and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012-0054582 A1 (MATTHEW BYOM et al.) 01 March 2012 See paragraphs [0021]-[0047] and [0061]-[0076]; claims 9 and 18; and figures 1-2 and 6.	1-39
A	US 2011-0202710 A1 (QUN ZHAO et al.) 18 August 2011 See paragraphs [0018]-[0023]; claims 1-2; and figures 1-2.	1-39
A	US 2010-0318839 A1 (CHRIS NGA YEE AVILA et al.) 16 December 2010 See paragraphs [0044]-[0046]; claim 12; and figures 6A-6C.	1-39
A	US 2008-0189473 A1 (MICHAEL MURRAY) 07 August 2008 See paragraphs [0038]-[0039]; claim 26; and figures 6-7.	1-39
A	US 2012-0166720 A1 (FRANKIE F. ROOHPARVAR) 28 July 2012 See paragraphs [0015]-[0018] and figure 1.	1-39

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 January 2014 (27.01.2014)	**28 January 2014 (28.01.2014)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/062725

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0054582 A1	01/03/2012	US 8341500 B2	25/12/2012
US 2011-0202710 A1	18/08/2011	CN 102792381 A	21/11/2012
		US 8549214 B2	01/10/2013
		WO 2011-103168 A1	25/08/2011
US 2010-0318839 A1	16/12/2010	US 8307241 B2	06/11/2012
US 2008-0189473 A1	07/08/2008	CN 101641679 A	03/02/2010
		KR 10-2009-0117787 A	12/11/2009
		TW 200847170 A	01/12/2008
		TW I395223 B	01/05/2013
		WO 2008-097617 A2	14/08/2008
		WO 2008-097617 A3	19/03/2009
US 2012-0166720 A1	28/06/2012	US 2007-288702 A1	13/12/2007
		US 2009-327594 A1	31/12/2009
		US 7586784 B2	08/09/2009
		US 8134872 B2	13/03/2012

(19)中华人民共和国国家知识产权局

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2015.06.15
(86)PCT国际申请的申请数据
PCT/US2013/062725 2013.09.30
(87)PCT国际申请的公布数据
WO2014/077962 EN 2014.05.22
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代理人 刘瑜 王英
(51)Int.Cl.
G06F 12/00(2006.01)
G06F 12/08(2006.01)

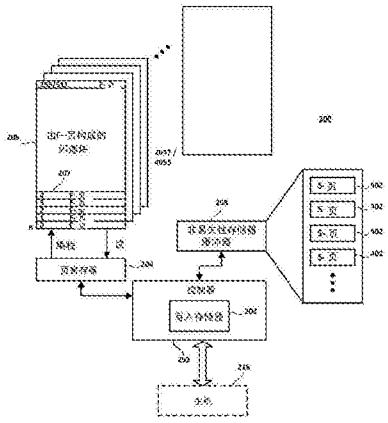
权利要求书4页 说明书7页 附图5页

(54)发明名称

用于避免数据存储设备中较低页讹误的方法和设备

(57)摘要

数据存储设备可以包括多个多层单元(MLC)非易失性存储器设备,所述多层单元(MLC)非易失性存储器设备包括多个较低页以及相对应的多个较高序页。控制器可以被配置为将数据写到多个较低页和相对应的多个较高序页以及从多个较低页和相对应的多个较高序页读取数据。缓冲器可以与控制器耦合,缓冲器可以被配置为对要写到MLC非易失性存储器设备的数据进行累积,分配缓冲器中的空间,以及将累积的数据写到分配的空间。累积的数据的至少一部分可以被写到MLC非易失性存储器设备的较低页中,并且当在MLC非易失性存储器设备中与较低页相对应的所有较高序页已经被写入时,可以将存储要被写到较低页的数据的缓冲器中的空间解除分配。



CN 105051703 A

1. 一种数据存储设备，包括：

多个多层单元 (MLC) 非易失性存储器设备，其包括多个较低页以及相对应的多个较高序页；

控制器，其与所述多个 MLC 非易失性存储器设备耦合并且被配置为将数据写到所述多个较低页和所述相对应的多个较高序页以及从所述多个较低页和所述相对应的多个较高序页读取数据；以及

耦合到所述控制器的缓冲器；

其中，所述控制器被配置为：

对要被写到所述 MLC 非易失性存储器设备的数据进行累积；

分配所述缓冲器中的空间并且将所累积的数据写到所述缓冲器中所分配的空间；

将所累积的数据的至少一部分写到所述 MLC 非易失性存储器设备的较低页中；以及

当所述 MLC 非易失性存储器设备中与所述较低页相对应的所有较高序页已经被写入时，对存储被写到所述较低页的数据的所述缓冲器中的空间解除分配。

2. 如权利要求 1 所述的数据存储设备，其中，所述缓冲器包括非易失性存储器。

3. 如权利要求 2 所述的数据存储设备，其中，所述非易失性存储器包括磁性随机存取存储器 (MRAM)。

4. 如权利要求 1 所述的数据存储设备，其中，所述控制器进一步被配置为：在对掉电后的所述数据存储设备恢复供电之后，从所述缓冲器读取数据并且将所读取的数据的至少一部分写到所述 MLC 非易失性存储器设备。

5. 如权利要求 1 所述的数据存储设备，其中，所述缓冲器至少足够大以在所述数据存储设备掉电之后能够从较低页讹误中恢复。

6. 如权利要求 1 所述的数据存储设备，其中，所述 MLC 非易失性设备被配置为在仅较低页模式中或者在单层单元 (SLC) 模式中进行操作。

7. 如权利要求 1 所述的数据存储设备，其中，所述控制器进一步被配置为：在所累积的数据被写到所述缓冲器中所分配的空间之后，生成写确认并且将所述写确认发送到主机。

8. 如权利要求 1 所述的数据存储设备，其中，所述 MLC 非易失性存储器设备包括多个块，所述多个块中的每一个都包括多个物理页，块的集合限定超级块 (S- 块)，S- 块中每块一个物理页的物理页的集合限定超级页 (S- 页)，并且其中，所述数据以 S- 页为单位被累积、写和存储。

9. 如权利要求 1 所述的数据存储设备，还包括备用电源和非易失性存储器，其中，所述缓冲器包括易失性存储器，并且其中，所述备用电源被配置为对所述数据存储设备的至少一部分供电至少长达所述控制器将所述数据从所述缓冲器写到所述非易失性存储器所需的时间。

10. 如权利要求 9 所述的数据存储设备，其中，所述非易失性存储器包括磁性随机存取存储器 (MRAM)。

11. 如权利要求 9 所述的数据存储设备，其中，所述控制器被进一步配置为：在对掉电之后的所述数据存储设备恢复供电之后，将所述非易失性存储器中的数据的至少一部分写到所述 MLC 非易失性存储器设备。

12. 如权利要求 1 所述的数据存储设备，还包括写存储装置，并且其中，所述控制器被

进一步配置为在所累积的数据被写到所述缓冲器中所分配的空间时将所累积的数据写到所述写存储装置。

13. 如权利要求 1 所述的数据存储设备，其中，控制器被进一步配置为：当所述 MLC 非易失性存储器设备中与所述较低页相对应的所有较高序页已经被写入时，还对存储被写到所述较高序页的数据的所述缓冲器中的空间解除分配。

14. 一种数据存储设备控制器，包括：

处理器，其被配置为与缓冲器和多个多层单元 (MLC) 非易失性存储器设备耦合，所述多个多层单元 (MLC) 非易失性存储器设备包括多个较低页以及相对应的多个较高序页，所述处理器被进一步配置为：

从所述多个较低页和所述相对应的多个较高序页读取数据；以及

至少通过如下处理将数据写到所述多个较低页以及所述相对应的多个较高序页：

对要写到所述 MLC 非易失性存储器设备的数据进行累积；

分配所述缓冲器中的空间并且将所累积的数据写到所述缓冲器中所分配的空间；

将所累积的数据的至少一部分写到所述 MLC 非易失性存储器设备的较低页中；以及

当所述 MLC 非易失性存储器设备中与所述较低页相对应的所有较高序页已经被写入时，对存储被写到所述较低页的数据的所述缓冲器中的空间解除分配。

15. 如权利要求 14 所述的数据存储设备控制器，其中，所述缓冲器包括非易失性存储器。

16. 如权利要求 15 所述的数据存储设备控制器，其中，所述非易失性存储器包括磁性随机存取存储器 (MRAM)。

17. 如权利要求 14 所述的数据存储设备控制器，其中，所述处理器被进一步配置为：在对掉电之后的所述数据存储设备恢复供电之后，从所述缓冲器中读取数据并且将所读取的数据的至少一部分写到所述 MLC 非易失性存储器设备。

18. 如权利要求 14 所述的数据存储设备控制器，其中，所述缓冲器至少足够大以使得在所述数据存储设备掉电之后能够从较低页讹误中恢复。

19. 如权利要求 14 所述的数据存储设备控制器，其中，所述 MLC 非易失性设备被配置为在仅较低页模式中或者在单层单元 (SLC) 模式中进行操作。

20. 如权利要求 14 所述的数据存储设备控制器，其中，所述处理器被进一步配置为在所累积的数据被写到所述缓冲器中所分配的空间之后，生成写确认并且将所述写确认发送到主机。

21. 如权利要求 14 所述的数据存储设备控制器，其中，所述 MLC 非易失性存储器设备包括多个块，所述多个块中的每一个包括多个物理页，块的集合限定超级块 (S- 块)，S- 块中的每块一个物理页的物理页的集合限定超级页 (S- 页)，并且其中，所述数据以 S- 页为单位被累积、写和存储。

22. 如权利要求 14 所述的数据存储设备控制器，还包括备用电源和非易失性存储器，其中，所述缓冲器包括易失性存储器，并且其中，所述备用电源被配置为对所述数据存储设备的至少一部分供电至少长达所述控制器将所述数据从所述缓冲器写到所述非易失性存储器所需的时间。

23. 如权利要求 22 所述的数据存储设备控制器，其中，所述非易失性存储器包括磁性

随机存取存储器 (MRAM)。

24. 如权利要求 22 所述的数据存储设备控制器，其中，所述处理器被进一步配置为：在对掉电后的所述数据存储设备恢复供电之后，将所述非易失性存储器中的数据的至少一部分写到所述 MLC 非易失性存储器设备。

25. 如权利要求 14 所述的数据存储设备控制器，还包括写存储装置，并且其中，所述处理器被进一步配置为在所累积的数据被写到所述缓冲器中所分配的空间时将所累积的数据写到所述写存储装置。

26. 如权利要求 14 所述的数据存储设备控制器，其中，处理器被进一步配置为：当所述 MLC 非易失性存储器设备中与所述较低页相对应的所有较高序页已经被写入时，还对存储被写到所述较高序页的数据的所述缓冲器中的空间解除分配。

27. 一种控制数据存储设备的方法，所述数据存储设备包括缓冲器以及多个多层单元 (MLC) 非易失性存储器设备，所述多个多层单元 (MLC) 非易失性存储器设备包括多个较低页以及相对应的多个较高序页，所述方法包括：

从所述多个较低页和所述相对应的多个较高序页中读取数据；以及

至少通过如下处理将数据写到所述多个较低页和所述相对应的多个较高序页：

对要写到入所述 MLC 非易失性存储器设备的数据进行累积；

分配所述缓冲器中的空间并且将所累积的数据写到所述缓冲器中所分配的空间；

将所累积的数据的至少一部分写到所述 MLC 非易失性存储器设备的较低页中；以及

当所述 MLC 非易失性存储器设备中与所述较低页相对应的所有较高序页已经被写入时，对存储被写到所述较低页的数据的所述缓冲器中的空间解除分配。

28. 如权利要求 27 所述的方法，其中，所述缓冲器包括非易失性存储器。

29. 如权利要求 28 所述的方法，其中，所述非易失性存储器包括磁性随机存取存储器 (MRAM)。

30. 如权利要求 27 所述的方法，还包括：在对掉电后的所述数据存储设备恢复供电之后，从所述缓冲器读取数据以及将所读取的数据的至少一部分写到所述 MLC 非易失性存储器设备。

31. 如权利要求 27 所述的方法，其中，所述缓冲器至少足够大以使得在所述数据存储设备掉电之后能够从较低页讹误中恢复。

32. 如权利要求 27 所述的方法，其中，所述 MLC 非易失性设备被配置为在仅较低页模式中或在单层单元 (SLC) 模式中进行操作。

33. 如权利要求 27 所述的方法，还包括：在所累积的数据被写到所述缓冲器中所分配的空间之后，生成写确认并且将所述写确认发送到主机。

34. 如权利要求 27 所述的方法，其中，所述 MLC 非易失性存储器设备包括多个块，所述多个块中的每一个都包括多个物理页，块的集合限定超级块 (S- 块)，S- 块中每块一个物理页的物理页的集合限定超级页 (S- 页)，并且以 S- 页为单位实施累积、写和存储。

35. 如权利要求 27 所述的方法，还包括备用电源和非易失性存储器，其中，所述缓冲器包括易失性存储器，并且其中，所述方法还包括：所述备用电源对所述数据存储设备的至少一部分供电至少长达所述控制器将所述数据从所述缓冲器写到所述非易失性存储器所需的时间。

36. 如权利要求 35 所述的方法，其中，所述非易失性存储器包括磁性随机存取存储器(MRAM)。

37. 如权利要求 35 所述的方法，还包括：在对掉电后的所述数据存储设备恢复供电之后，将所述非易失性存储器中的数据的至少一部分写到所述 MLC 非易失性存储器设备。

38. 如权利要求 27 所述的方法，其中，所述数据存储设备还包括写存储装置，并且其中，写数据还包括在所累积的数据被写到所述缓冲器中所分配的空间时将所累积的数据写到所述写存储装置。

39. 如权利要求 27 所述的方法，还包括：当所述 MLC 非易失性存储器设备中与所述较低页相对应的所有较高序页已经被写入时，将存储被写到所述较高序页的数据的所述缓冲器中的空间解除分配。

用于避免数据存储设备中较低页讹误的方法和设备

背景技术

[0001] 闪速存储器是一种能够进行电擦除以及重编程的非易失性计算机存储技术。闪速存储器通常按块写，以及按较大的超级块或 S- 块进行分配、垃圾收集和擦除。

[0002] 闪速存储器包括多个单元，其中每一个单元被配置为每单元存储一位、两位或更多位。SLC 是“单层单元 (Single-Level Cell)”的缩写，其表示每一个单元存储一位的配置。SLC 的特征不仅在于快速的传送速度、低功率消耗以及高的单元持久性，而且还在于相对高的成本。MLC 是“多层单元 (Multi-level Cell)”的简称，其表示每一个单元每单元存储两位或更多位的配置。首字母缩略词 MLC 通常用来表示具有每单元存储两位的单元的闪速存储器。但是，该相同的首字母缩略词 MLC 还用于指定的闪速存储器，所述指定的闪速存储器具有被配置为每单元存储三位（也称为“TLC”或三元组或三层单元）或者每单元甚至更多位数的单元。当 MLC 用来指定在每一个单元中存储两位的存储器时，这样的 MLC 闪速存储器的特征可以在于与单层单元存储器相比较慢的传输速度、较高的功耗以及较低的单元持久性。但是，与 SLC 存储器相比，这样的 MLC 存储器享有每比特相对较低的制造成本。

[0003] 在MLC NAND闪速存储器中，存储器单元的相同的物理页可以用来存储数据的两个或更多个逻辑页，每一个单元被配置为存储 2 位或更多位。当每单元存储两位时，首先存储较低页 (lower page) 的第一位，以及然后存储一个或多个较高序页 (higher-order page) 的下一位或多位。首先对较低页进行编程，然后对较高序的一页或多页进行编程。当对上页进行编程时，编程电压被施加到已经在较低页中存储有效数据的相同的单元。如果在对较高序的一页或多页进行编程期间发生电力故障，则较低页中存储的数据可能不可恢复地讹误，想要存储在较高序的一页或多页中的数据可能也是如此。该问题由于主机可能已经接收到来自数据存储设备的、指示存储在较低页中的数据已经保存到闪速存储器的确认的事实而复杂化。

[0004] 图 1 是常规闪速数据存储设备的各方面的框图。如其中所示，闪速数据存储设备 100 包括控制器 104。控制器 104 与统一以数字 102 指代的非易失性存储器（例如，闪速存储器设备）的阵列相耦合。常规地，为了提供电力故障保护，常规的闪速数据存储设备包括备用电源，如图 1 中的 106 所示。如 106 所指示的，超级电容器或离散电容器的阵列常规地用于在掉电期间保持控制器 104 和非易失性存储器 102 加电，通常仅足够长以结束将数据编程到闪速存储器设备 102 中。事实上，这些超级电容器或离散电容器阵列被配置为存储充分大量的能量来使控制器 104 能够在掉电时完成任何固件操作（例如写操作）。但是，这不是最优的，因为超级电容器很大、不可靠、易出现问题，而且昂贵。

附图说明

[0005] 图 1 是常规闪速数据存储设备的方面的框图。

[0006] 图 2 是根据一个实施例的示出了数据存储设备的物理的和逻辑的数据组织的方面的图。

[0007] 图 3 是根据一个实施例的 S- 块的框图。

[0008] 图 4 是根据一个实施例的 S- 页的框图。

[0009] 图 5 是根据一个实施例的数据存储设备的框图。

[0010] 图 6 是根据一个实施例的控制数据存储设备的方法的流程图。

具体实施方式

[0011] 在本公开的范围内，首字母缩略词“MLC”明确地表示包括每单元存储两位或更多位的单元的闪速存储器。在其中这样的 MLC 闪速存储器被配置为每单元存储两位的情况下，数据被存储在较低页和相对应的上页中。在其中这样的 MLC 闪速存储器被配置为每单元存储三位或更多位的情况下，数据被存储在较低页以及一个或多个相对应的较高序页中。术语“较高序页”是要明确地涵盖上页和 / 或上页以及较高序的一个或多个页。

[0012] 图 2 是根据一个实施例的示出了数据存储设备 200 的物理和逻辑数据组织方面的图。在一个实施例中，数据存储设备是 SSD。在另一实施例中，数据存储设备是包括闪速存储器和旋转磁性存储介质的混合驱动器。本公开能够应用于 SSD 和混合实现二者，但是为了简单起见，将参考基于 SSD 的实现来描述各个实施例。根据一个实施例的数据存储设备控制器 202 可以被配置为与主机耦合，主机如附图标记 218 所示。主机 218 可以利用逻辑块寻址 (LBA) 方案。虽然 LBA 尺寸通常是固定的，但是主机能够动态地改变 LBA 的尺寸。例如，可以对物理数据存储设备进行逻辑划分，以支持被配置用于不同尺寸的 LBA 的分区。但是，物理设备不需要这样的分区来同时支持不同尺寸的 LBA。例如，LBA 尺寸可以根据接口和接口模式而不同。事实上，虽然 512 字节是最常见的，但是 4KB 也变得更加普遍，512+(520, 528, 等）以及 4KB+(4KB+8, 4K+16, 等）格式也是如此。如其中所示，数据存储设备控制器 202 可以包括或者耦合到页寄存器 204。页寄存器 204 可被配置以使控制器 202 能够从数据存储设备 200 读取数据以及将数据存储到数据存储设备 200 中。控制器 202 可以被配置为响应于来自主机 218 的数据存取指令来对数据进行编程并且从闪速存储器设备的阵列读取数据。虽然此处的说明一般性地指闪速存储器，但是应当理解存储器设备的阵列可以包括一个或多个各种类型的非易失性存储器设备，例如，闪速集成电路、硫属化物 RAM(C-RAM)、相变存储器 (PC-RAM 或 PRAM)、可编程金属化单元 RAM(PMC-RAM 或 PMCm)、双向统一存储器 (OUM)、电阻式 RAM(RRAM)、NAND 存储器（例如，单层单元 (SLC) 存储器、多层单元 (MLC) 存储器、或其任意组合）、NOR 存储器、EEPROM、铁电存储器 (FeRAM)、磁阻式 RAM(MRAM)、其他离散的 NVM（非易失性存储器）芯片、或其任意组合。

[0013] 页寄存器 204 可以被配置为使控制器 202 能够从阵列读取数据以及将数据存储到阵列中。根据一个实施例，闪速存储器设备的阵列可以在管芯（例如，128 个管芯）上包括多个非易失性存储器设备，其中的每一个都包括多个块，例如图 2 中的 206 所示。其他的页寄存器 204（未示出）可以与其它管芯上的块耦合。成组在一起的闪速块的组合可以被称为超级块或 S- 块 (S-Block)。在一些实施例中，形成 S- 块的单独的块可以从一个或多个管芯、平面或其他粒度级选出。因此，S- 块可以包括分散在一个或多个管芯上的、被组合在一起的多个闪速块。以这种方式，S- 块可以形成闪速管理系统 (FMS) 在其上进行操作的单元。在一些实施例中，形成 S- 块的单独的块可以根据与管芯级不同的粒度级来选出，例如，当存储器设备包括被细分成例如平面的结构的管芯时的情况（即，可以从单独的平面取得块）。根据一个实施例，可以在 S- 块级上实施分配、擦除和垃圾收集。在其他实施例中，FMS

可以根据其他逻辑分组（例如，页、块、平面、管芯等）来执行数据操作。

[0014] 根据一个实施例，MLC 非易失性存储器设备的阵列可以包括多个较低页和相对应的多个较高序页。也即，每一个较低页可以与相对应的单个上页或者与相对应的多个（即，两个或更多个）的较高序页相关联。MLC 非易失性存储器设备可以组织在闪速块 206 中，每一个闪速块包括多个闪速页 (F- 页)207，如图 2 所示。可替代地，可以采用不同的物理组织。根据一个实施例，F- 页可以是非易失性存储器设备的最小程序单元的尺寸。控制器 202 可以与多个非易失性存储器设备耦合并且可以被配置为将数据写到多个较低页和一个或多个相对应的较高序页以及从多个较低页和一个或多个相对应的较高序页读取数据。为了解决困扰常规数据存储设备的较低页讹误问题，数据存储设备 200 的一个实施例包括缓冲器 208。在一个实施例中，缓冲器包括非易失性存储器。在写命令从主机 218 接收并且由控制器 202 执行时，可以对要写到 MLC 非易失性存储器设备（即，闪速块 206）的数据进行累积。根据一个实施例，要写入的数据可以累积在写存储装置 203 中。写存储装置 203 可以与控制器 202 耦合。在一个实施例中，写存储装置 203 是控制器 202 内部的存储装置。与在写存储装置 203 中累积数据同时进行（或者至少紧接在这样的累积之前或之后），控制器 202 可以分配缓冲器 208 中的存储器空间并且可以将所累积的数据写到缓冲器 208 中所分配的空间中。根据一个实施例，要写到 MLC 非易失性存储器设备的数据可以存储在写存储装置 203 和缓冲器 208 中，使得缓冲器 208 和写存储装置 203 彼此镜像或者彼此基本镜像。事实上，根据一个实施例，控制器 202 可以被配置为对要写到写存储装置 203 和缓冲器 208 中的数据进行累积，直到构造出完整的 F- 页。根据一个实施例，部分 F- 页可以与预定的编码值封装在一起并且被视为完整的。完整的 F- 页可以写到 MLC 非易失性存储器设备。也即，所累积的数据的至少一部分可以写到 MLC 非易失性存储器设备的较低页。根据一个实施例，当与较低页相对应的所有较高序页已写 MLC 非易失性存储器设备时，可以将缓冲器 208 中先前分配的空间解除分配。也即，控制器 202 可以被配置为将较低页数据保存在缓冲器 208 中，直到已经对与较低页相对应的上页或高序页进行编程。这确保了写数据的电力安全副本被维持在缓冲器 208 中，直到较低页和较高序页或多个页二者已被编程，此后数据可以被视为防电力故障或讹误。

[0015] 根据一个实施例，在数据存储设备 200 的正常操作过程中，随着构造出完整的 F- 页（并且在写存储装置 203 中累积以及写出到缓冲器 208），它们可以写出到 MLC 非易失性存储器设备。根据一个实施例，写出到 MLC 非易失性存储器设备的是存储在写存储装置 203 中的完整的 F- 页。事实上，由于写存储装置 203 能够支持比缓冲器 208 更大的带宽，所以优选的是将完整的 F- 页从写存储装置 203 中而不是从缓冲器 208 中写出。

[0016] 根据一个实施例，缓冲器 208 可以包括非易失性存储器。例如，缓冲器 208 可以包括这样的存储器 ：其为非易失性的，以及特征为具有高的存取速度、读速度和写速度。根据一个实施例，缓冲器 208 可以包括磁性随机存取存储器 (MRAM)。还可以使用其他存储器类型。MRAM 可以展现出与 SRAM 类似的性能，相当于 DRAM 的密度以及低功耗。而且，MRAM 不随时间而降级。虽然成本相对高，但是 MRAM 非常适合于缓冲器 208 的任务 ；也即，适合于存储较低页数据的电力安全副本，至少直到相对应的较高序页已经安全地存储在闪速块 206 中。但是，值得注意的是，由于该写入，在 MRAM 中实现缓冲器 208 的成本仍比常规的超级电容器的使用或者离散电容器阵列的使用更廉价。在缓冲器 208 包括例如 MRAM 的非易失

性存储器的实现中，尚未安全地存储在闪速块 206 中的写到非易失性存储器中的数据（例如，在电力故障事件之前其相对应的较高序页未存储到闪速存储器中的较低页数据）可以在对数据存储设备 200 恢复供电时，由控制器 202 从缓冲器 208 读出并且存储在闪速块 206 中。也即，控制器 202 可以进一步被配置为，在对掉电之后的数据存储设备 200 恢复供电之后，从缓冲器 208 中读取数据以及将读取的数据的至少一部分写到闪速块 206 的非易失性存储器设备。

[0017] 根据一个实施例，缓冲器 208 可以被配置为至少足够大以使得在数据存储设备掉电之后能够从较低页讹误恢复。因此，缓冲器 208 的尺寸可以随着例如较低页与较高序页之间的页数、F- 页的尺寸、平面的数量以及数据存储设备的管芯数而不同。例如，缓冲器 208 的尺寸可以从几 MB 到几百 MB 不同，但是其他实现可以利用其他尺寸而达到良好效果。根据一个实施例，缓冲器 208 可以包括用于每一个管芯的多个缓冲器，因为每一个管芯在不同的时间完成其编程。这使得能够独立地管理每管芯的多个页，产生高效的缓冲器 208 的配置。缓冲器 208 可以例如被实现为多个缓冲器，当相对应的较低页的较高序页存储在闪速块 206 中时，控制器 202 从所述多个缓冲器分配空间，存储数据，以及对空间解除分配。这样的缓冲器配置非常适合于缓存来自主机写命令的写数据流，直到在电力故障时较低页讹误的概率可接受地小或者为零。根据一个实施例，控制器 202 可以被配置为在累积的数据被写缓冲器中的分配空间之后（例如，一旦累积的数据被写缓冲器中的分配空间）就生成写确认，并且将该写确认发送到主机 218。也即，从主机的视角看，当数据存储在缓冲器 208 中时，数据就可以被视为已经安全地存储在闪速存储器中。根据一个实施例，MLC 非易失性设备可以在仅较低页模式或者“SLC”模式下运行。在该情况下，由于没有要处理的较高序页，所以一旦对仅 MLC 较低页模式下的页或者 SLC 模式中的页进行编程，就可以实施对缓冲器 208 中的空间进行解除分配，并且在等待要被编程的任何较高序页的同时无需被延迟。

[0018] 图 3 是根据一个实施例的 S- 块的框图。如其中所示，S- 块 302 可以每管芯包括一个闪速块 (F- 块)206。因此，S- 块可以被视为 F- 块的集合，每个管芯上一个 F- 块，这些 F- 块组合在一起而形成数据存储设备的闪速管理系统 (FMS) 的单元。根据一个实施例，可以在 S- 块级上管理分配、擦除和 GC。如图 3 所示，每一个 F- 块 206 可以包括多个闪速页 (F- 页)，例如，256 或 512 个 F- 页。根据一个实施例，F- 页可以为用于给定的非易失性存储器设备的最小程序单元的尺寸。图 4 示出了根据一个实施例的超级页 (S- 页)。如其中所示，S- 页 402 可以每 S- 块的 F- 块包括一个 F- 页，意味着 S- 页跨越整个 S- 块。根据图 2 所示的一个实施例，数据可以 S- 页 402 为单位进行累积、写和存储。缓冲器 208 可以被配置为取决于具体的实现来存储以与 S- 页 402 不同的方式组织的写数据。

[0019] 图 5 是根据一个实施例的另一数据存储设备 500 的框图。参考图 2，类似的附图标记表示类似的元件，并且为简要起见省略了对这样的类似元件的说明。在该实施例中，控制器 502 无需（但是可以）包括写存储装置，例如图 2 中的写存储装置 203。易失性存储器缓冲器 504（或者多个这样的易失性存储器缓冲器）可以与控制器 502 耦合。例如，易失性存储器缓冲器 504 可以包括动态随机存取存储器 (DRAM) 或者被配置在动态随机存取存储器 (DRAM) 中。易失性存储器缓冲器 504 在图 5 中示出为位于控制器 502 的外部。但是，易失性存储器缓冲器 504 还可以位于控制器 502 的内部，其可以通过控制器 502 来变换为更快

的存取时间。但是，尺寸和/或其他考量可以推荐的是，将易失性存储器缓冲器 504 配置为与控制器 502 耦合的外部存储器缓冲器。图 5 的数据存储设备 500 还可以包括例如 506 所示的备用电源以及如 508 所示的非易失性存储器。备用电源 506 可以与易失性存储器缓冲器 504、控制器 504 和非易失性存储器 508 耦合。备用电源 506 可以被配置为在电力故障事件发生时至少保持易失性存储器缓冲器 504、控制器 502 和/或非易失性存储器 508 在一段时间内加电，而不会丢失易失性存储器 504 中的数据（至少直到其内容能够被保存到非易失性存储器 508 中）。根据一个实施例，备用电源 506 可以被配置为对图 5 的数据存储设备的至少部分加电，至少长达控制器 502 将数据从易失性缓冲器 504 写到非易失性存储器 508 所需的时间。备用电源 506 可以包括电容器、超级电容器和/或任何能量存储元件。在一个实施例中，其中数据存储设备是与硬盘驱动器耦合的混合磁盘驱动器或者固态驱动器，电源 506 可以由根据硬盘驱动器的主轴电动机生成的 BEMF（反向电动势）来提供。

[0020] 事实上，在正常操作期间，由于写命令是从主机 218 接收并且由控制器 502 执行的，所以要写到 MLC 非易失性存储器设备（即，闪速块 206）的数据可以写到易失性存储器缓冲器 504 和 MLC 非易失性存储器设备二者。根据一个实施例，控制器 502 可以被配置为累积待在内部（例如，在写存储装置 203 中）写（如例如由主机 218 发出的写命令所引导）的数据，直到构造了完整的 F- 页。可替代地以及根据一个实施例，部分 F- 页可以与预定的编码值封装在一起并且被视为完整的。然后，完整的 F- 页可以写到易失性存储器缓冲器 504 和 MLC 非易失性存储器设备二者。根据一个实施例，数据还可以以 S- 页 402 为单位或者以任何其他数据组织单元为单位来进行累积、写以及存储。实际上，易失性存储器缓冲器 504 可以被配置为取决于具体的实现来存储以与 S- 页 402 不同的方式组织的写数据。因此，根据一个实施例，除了将累积的数据（或其部分）写到易失性存储器缓冲器 504 中之外，所累积的数据（或其部分）可以写到 MLC 非易失性存储器设备（闪速块 206）的一个或多个较低页和/或上页。根据一个实施例，当与之前编程的较低页相对应的所有较高序页已经写到 MLC 非易失性存储器设备中，并且因此可以被视为有效地防讹误时，可以将易失性存储器缓冲器 504 中的先前分配的空间解除分配，其中解除分配的空间重新用于新的写数据。也即，控制器 202 可以被配置为将较低页数据保存在易失性存储器缓冲器 504 中至少直到与较低页相对应的上页或较高序页已被编程在 MLC 非易失性存储器设备中。

[0021] 在发生掉电的事件中，备用电源 506 可以至少向控制器 502、易失性存储器缓冲器 504 和/或非易失性存储器 508 供电。在控制器 502、易失性存储器缓冲器 504 和/或非易失性存储器 508 由备用电源 506 供电期间，控制器 502 可以使存储在易失性存储器缓冲器 504 中的数据被复制到非易失性存储器 508，从而以防讹误方式将尚未保存到 MLC 非易失性存储器设备中的数据进行保存，从而使控制器能够确认写到主机 218。当恢复对 MLC 非易失性存储器设备供电时，保存在非易失性存储器 508 中的数据可以被编程到 MLC 非易失性存储器设备中。

[0022] 值得注意的是，根据一个实施例，可以仅在发生电力故障的事件中，写非易失性存储器 508。而且，通过仅在发生电力故障的事件中对控制器 502、易失性存储器缓冲器 504 和非易失性存储器 508 供电，与还对 MLC 非易失性存储器设备（例如，闪速块 206）的管芯进行供电所需的电力相比，需要相对较少的电力。值得注意的是，非易失性存储器 508 可以从由备用电源 506 供电的控制器 502 汲取其电力。根据一个实施例，非易失性存储器 508 可

以包括 MRAM。根据一个实施例，备用电源 506 仅需要与控制器 502 和易失性存储器缓冲器 504 耦合。另外，通过在发生电力故障的事件中，使用易失性存储器缓冲器 504 作为数据路径和非易失性存储器 508 中的主写位置，降低了非易失性存储器 508 的磨损。

[0023] 图 6 是根据一个实施例的控制数据存储设备的方法的流程图。数据存储设备可以包括缓冲器以及多个多层单元 (MLC) 非易失性存储器设备（包括例如闪速块 206）。如本文所描述的，MLC 非易失性存储器设备可以包括多个较低页以及相对应的多个较高序页。例如 502 所示的控制器可以被配置为将数据写到多个较低页和相对应的多个较高序页以及从多个较低页和相对应的多个较高序页读取数据。根据一个实施例，以及如图 6 所示，该方法可以包括 :对要写到 MLC 非易失性存储器设备的数据进行累积，如块 B61 所示。块 B62 要求分配缓冲器 208、504 中的空间以及将累积的数据写到缓冲器 208、504 中分配的空间。如在 B63 所示，累积的数据的至少一部分可以写到 MLC 非易失性存储器设备的一个或多个较低页。应当理解的是，所累积的数据的一部分还可以写到 MLC 非易失性存储器设备的一个或多个上页。当与较低页相对应的所有较高序页已经写到 MLC 非易失性存储器设备中时，正如在块 B64 中所要求的，可以安全地对存储要被写到较低页的数据的缓冲器中的空间解除分配。

[0024] 根据一个实施例并且如图 2 所示，缓冲器可以包括或被配置为非易失性存储器，例如，磁性随机存取存储器 (MRAM)。如关于图 2 所描述的，以及如图 5 中的 B65 所示，该方法还可以包括 :在对掉电之后的数据存储设备恢复供电之后，从缓冲器 208 读取数据以及将所读取的数据的至少一部分写到 MLC 非易失性存储器设备。如关于图 5 所描述的，该方法还可以包括 :在对掉电之后的数据存储设备恢复供电（由备用电源 506）之后，从易失性存储器缓冲器 504 读取数据，以及将所读取的数据的至少一部分写到非易失性存储器 508，如图 6 中的 B65 所示。根据一个实施例，缓冲器 208、504 可以至少足够大以使得能够在数据存储设备掉电之后从可能的较低页讹误中恢复。根据一个实施例，缓冲器 208、504 可以被配置为一个或多个缓冲器。在累积的数据写到缓冲器 208、504 中的分配的空间之后，可以生成写确认并将所述写确认发送到主机 218，因为从该时间点向前，数据可以被视为是防讹误的。根据一个实施例，MLC 非易失性存储器设备可以被配置为包括多个块，多个块中的每一个包括多个物理页。这些块的集合可以限定超级块 (S- 块）。S- 块中的每块一个物理页的物理页的集合可以限定超级页 (S- 页），所述 S- 页可以是控制器 202 累积、写和存储主机和 / 或其他数据的单位。可以在当前的上下文中实现其他的数据组织和单位。

[0025] 如关于图 5 所示出和描述的，该方法还可以包括 :提供备用电源 506 和非易失性存储器，例如，如 508 所示的非易失性存储器。在该实施例中，缓冲器 504 可以包括易失性存储器。根据一个实施例，该方法还可以包括 :对数据存储设备 500 的至少一部分供电至少长达控制器 502 将数据从缓冲器 504 写到非易失性存储器 508 所需的时间。根据一个实施例，在对掉电之后的数据存储设备恢复供电之后，非易失性存储器 508 中的数据的至少一部分可以写到 MLC 非易失性存储器设备。可以提供写存储装置（图 2 和图 5 中的 203），并且控制器 202、502 可以被配置为在所累积的数据写到缓冲器 208、504 中所分配的空间时将所累积的数据写到写存储装置 203 中。根据一个实施例，控制器 202、502 还可以配置为 :当与较低页相对应的所有较高序页已经写到 MLC 非易失性存储器设备中时，对存储要被写到较高序页的数据的缓冲器 208、504 中的空间解除分配，因为这样的数据可以被视为防讹误的。

[0026] 虽然已经描述了一些实施例，但是这些实施例仅通过示例的方式提供，并且并不是要限制本发明的范围。事实上，本文所描述的新颖的方法、设备和系统可以通过各种的其他形式来具体实现。此外，可以在不偏离本公开精神的情况下做出对本文所描述的方法和系统的形式的各种省略、替代和变化。随附的权利要求书及其等效物是要涵盖落在本公开的范围和精神内的这样的形式或改进。例如，本领域的技术人员将意识到，在各个实施例中，实际的结构可能与图中所示的那些不同。根据实施例，在上述示例中描述的一些步骤可以去除，可以添加其他步骤。而且，上文公开的具体实施例的特征和属性可以通过不同方式组合而形成额外的实施例，所有这些落在本公开范围内。虽然本公开提供了一些优选的实施例和应用，但是对于本领域普通技术人员而言显而易见的是，其他实施例，包括不提供本文阐述的全部特征和优点的实施例，也在本公开的范围内。因此，本公开的范围是要仅由随附的权利要求书来限定。

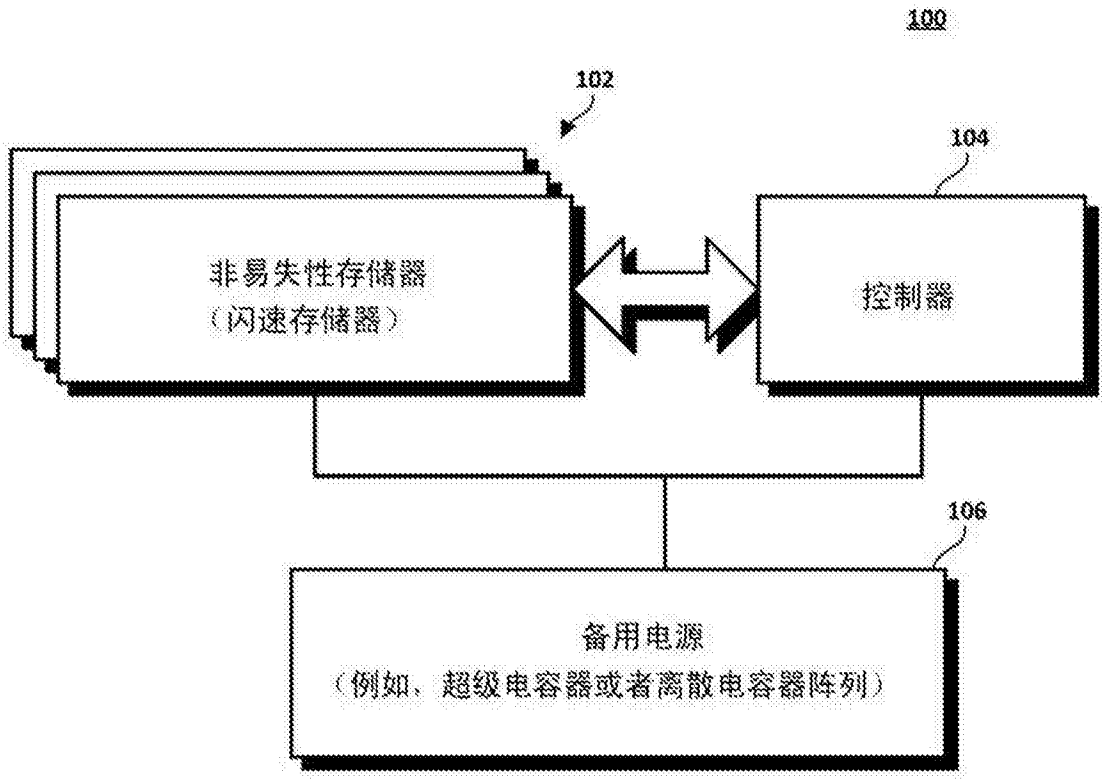


图 1（现有技术）

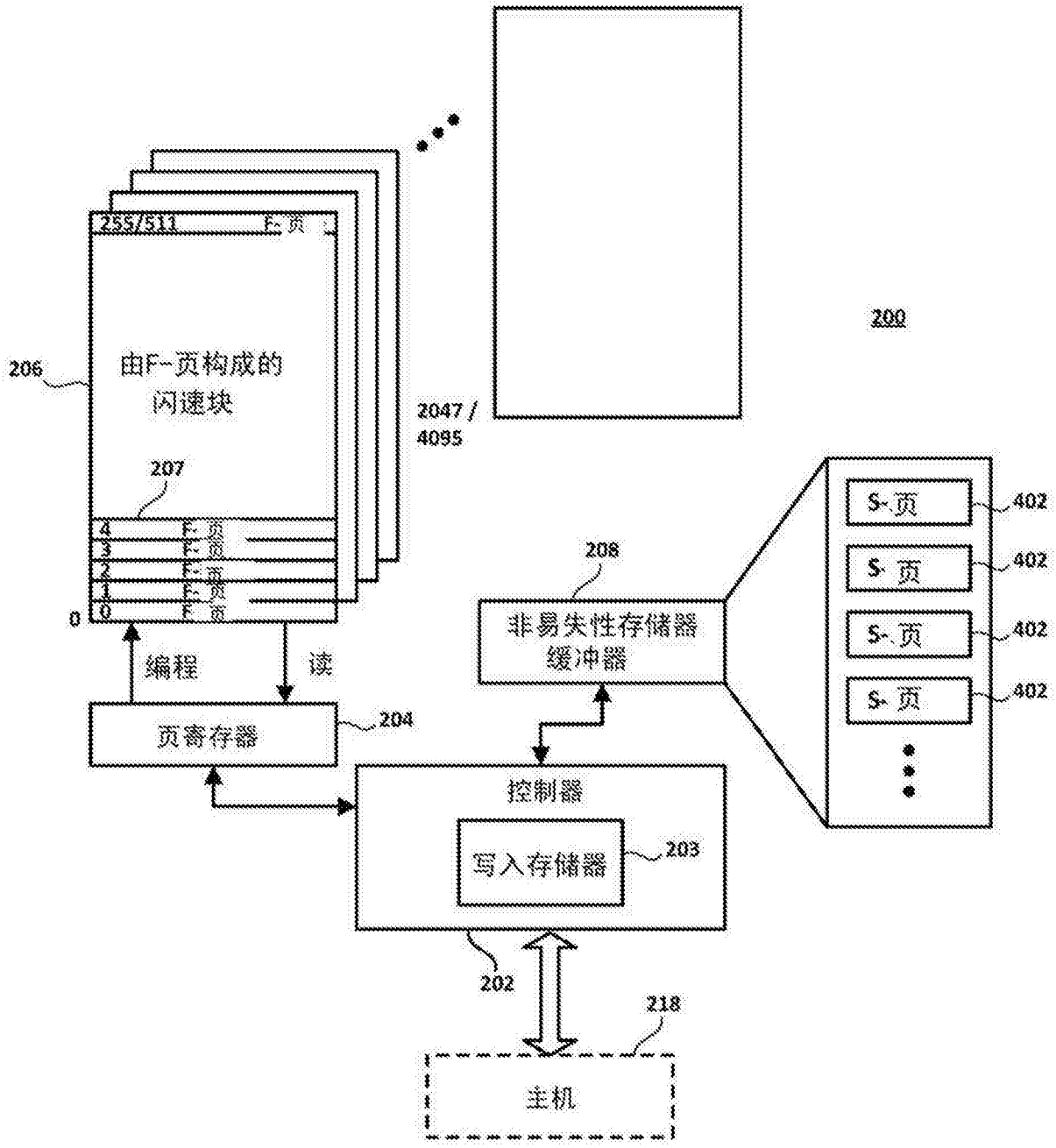

200
206
由F-页构成的
闪速块
255/511
F-页
2047 /
4095
207
4
3
2
1
0
F-页
编程
读
页寄存器
204
208
非易失性存储器
缓冲器
S-页
402
控制器
写入存储器
203
202
218
主机

图 2

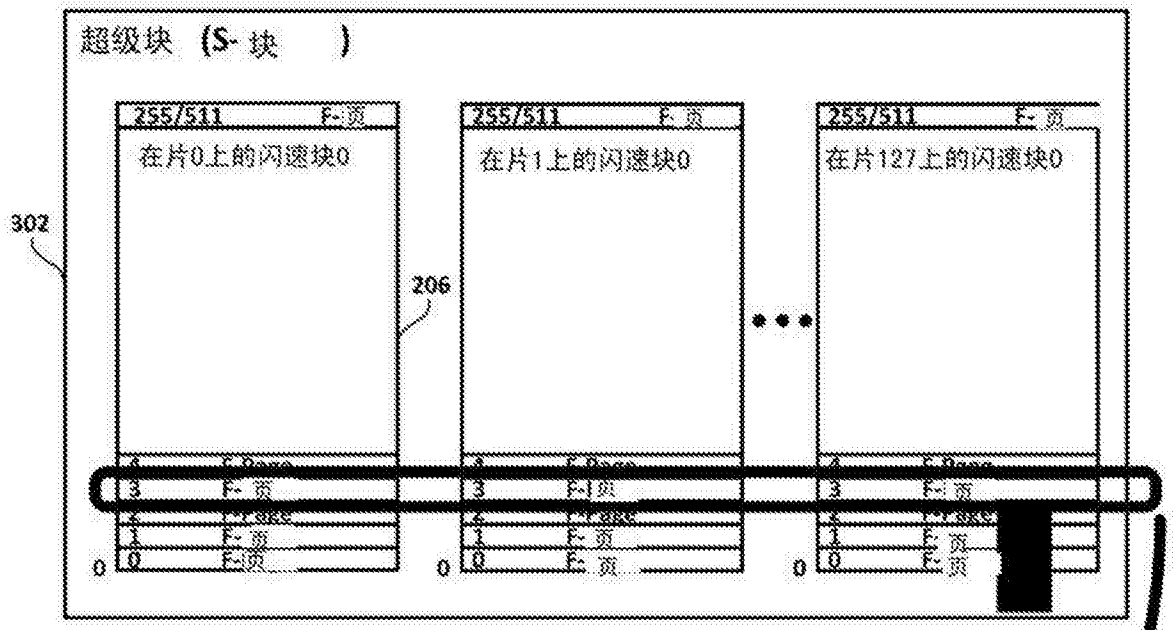

超级块 (S-块)
255/511 F-页
在片0上的闪速块0
在片1上的闪速块0
在片127上的闪速块0
302
206
3 F-页
1 F-页
0 F-页

图3

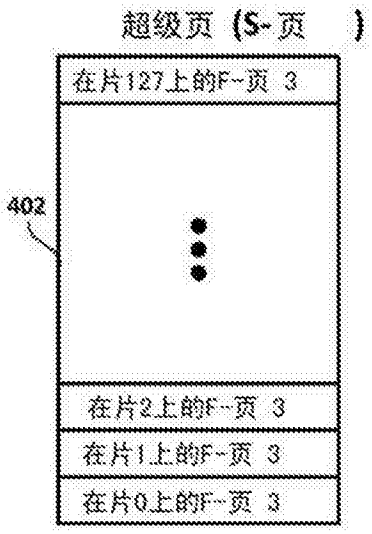

超级页 (S-页)
在片127上的F-页 3
402
在片2上的F-页 3
在片1上的F-页 3
在片0上的F-页 3

图4

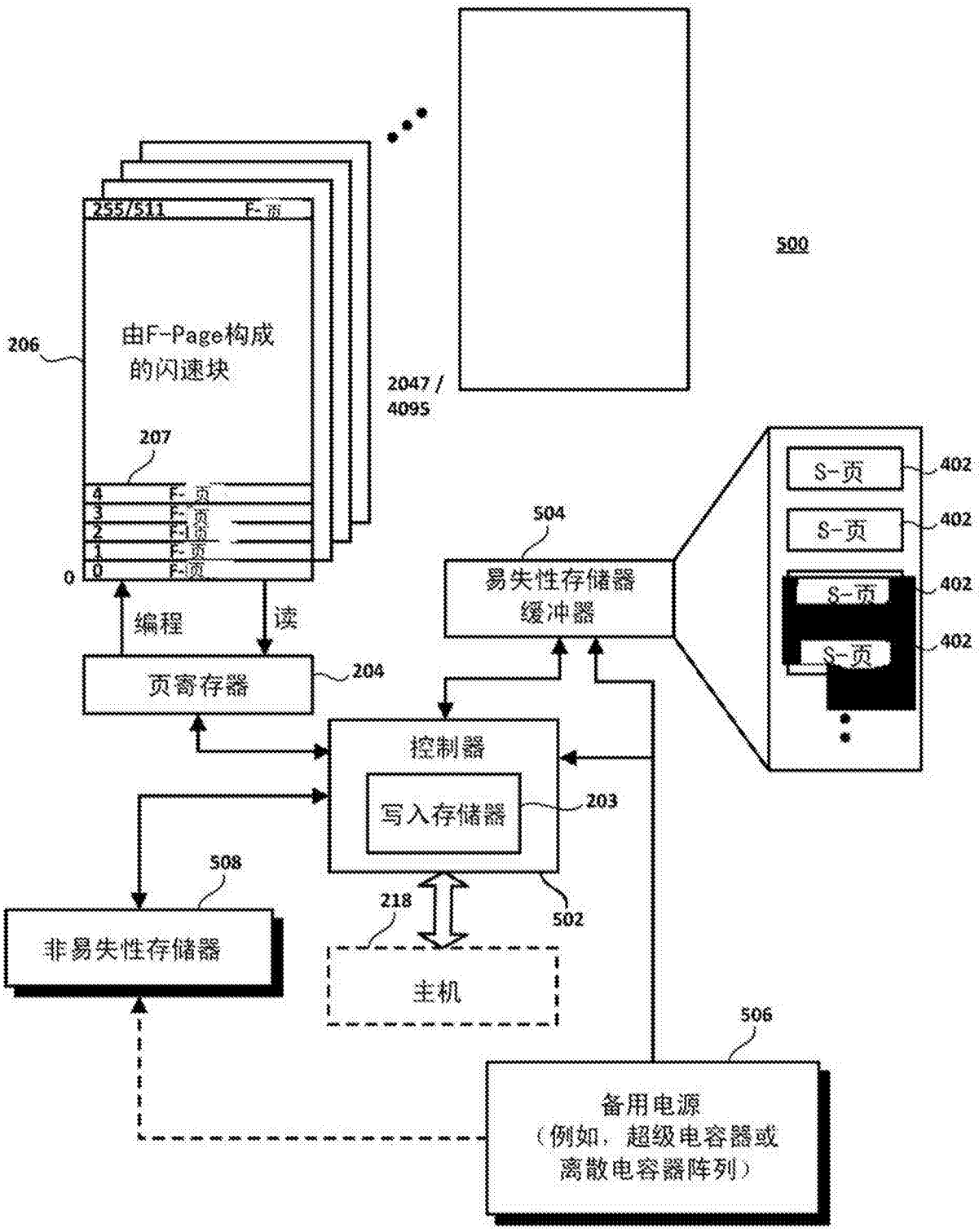

500
206
由F-Page构成
的闪速块
255/511
F-页
2047 /
4095
207
4
3
2
1
0
F-页
编程
读
页寄存器
204
504
易失性存储器
缓冲器
S-页
402
控制器
写入存储器
203
508
非易失性存储器
218
502
主机
506
备用电源
（例如，超级电容器或
离散电容器阵列）

图 5

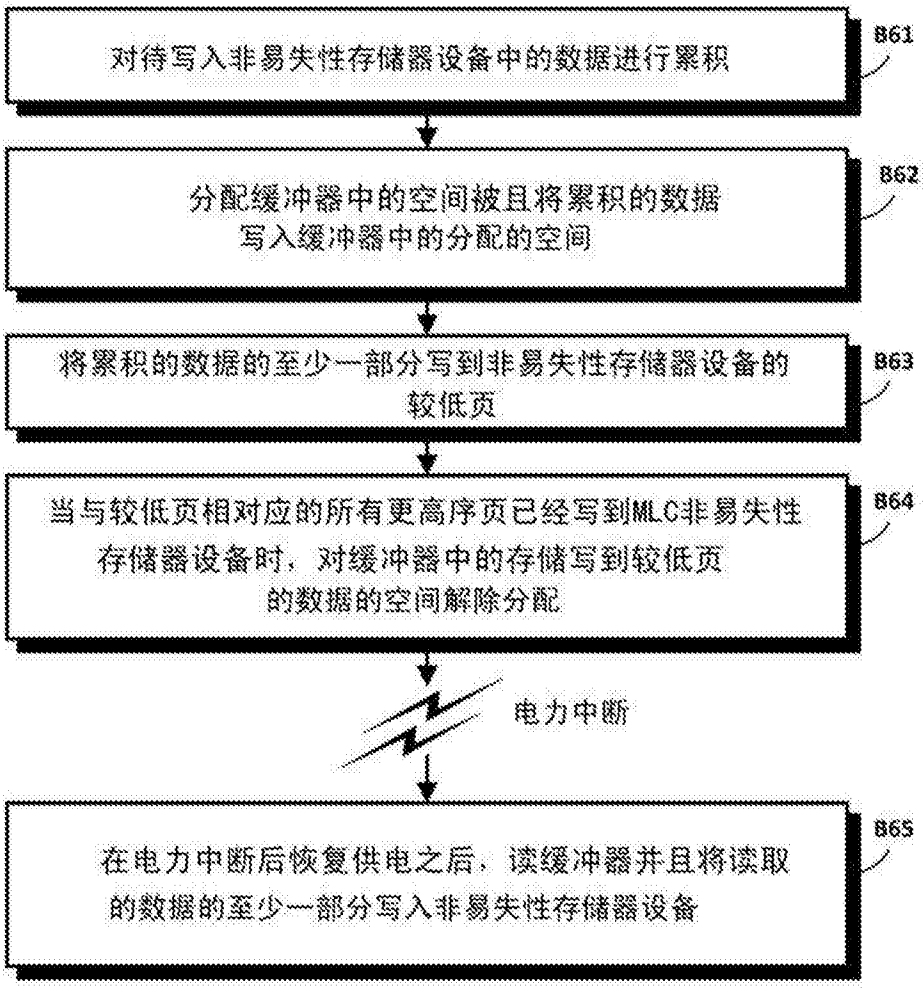

对待写入非易失性存储器设备中的数据进行累积
B61
分配缓冲器中的空间被且将累积的数据写入缓冲器中的分配的空间
B62
将累积的数据的至少一部分写到非易失性存储器设备的较低页
B63
当与较低页相对应的所有更高序页已经写到MLC非易失性存储器设备时，对缓冲器中的存储写到较低页的数据的空间解除分配
B64
电力中断
在电力中断后恢复供电之后，读缓冲器并且将读取的数据的至少一部分写入非易失性存储器设备
B65

图 6

Abstract

A data storage device may comprise a plurality of Multi-Level Cell (MLC) non-volatile memory devices comprising a plurality of lower pages and a corresponding plurality of higher-order pages. A controller may be configured to write data to and read data from the plurality of lower pages and the corresponding plurality of higher-order pages. A buffer may be coupled to the controller, which may be configured to accumulate data to be written to the MLC non-volatile memory devices, allocate space in the buffer and write the accumulated data to the allocated space. At least a portion of the accumulated data may be written in a lower page of the MLC non-volatile memory devices and the space in the buffer that stores data written to the lower page may be de-allocated when all higher-order pages corresponding to the lower page have been written in the MLC non-volatile memory devices.