United States Patent [19]

Warren

[11] **3,875,519**

[45] **Apr. 1, 1975**

[54] **RATIO COMPUTING CIRCUIT**

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[22] Filed: **Dec. 17, 1973**

[21] Appl. No.: **425,256**

[52] **U.S. Cl.** ..... **328/161**, 235/196, 307/229, 324/140 D, 328/127

[51] **Int. Cl.** **G06g 7/16**

[58] **Field of Search** ..... 328/161, 145, 127; 307/229; 235/196; 324/140 D

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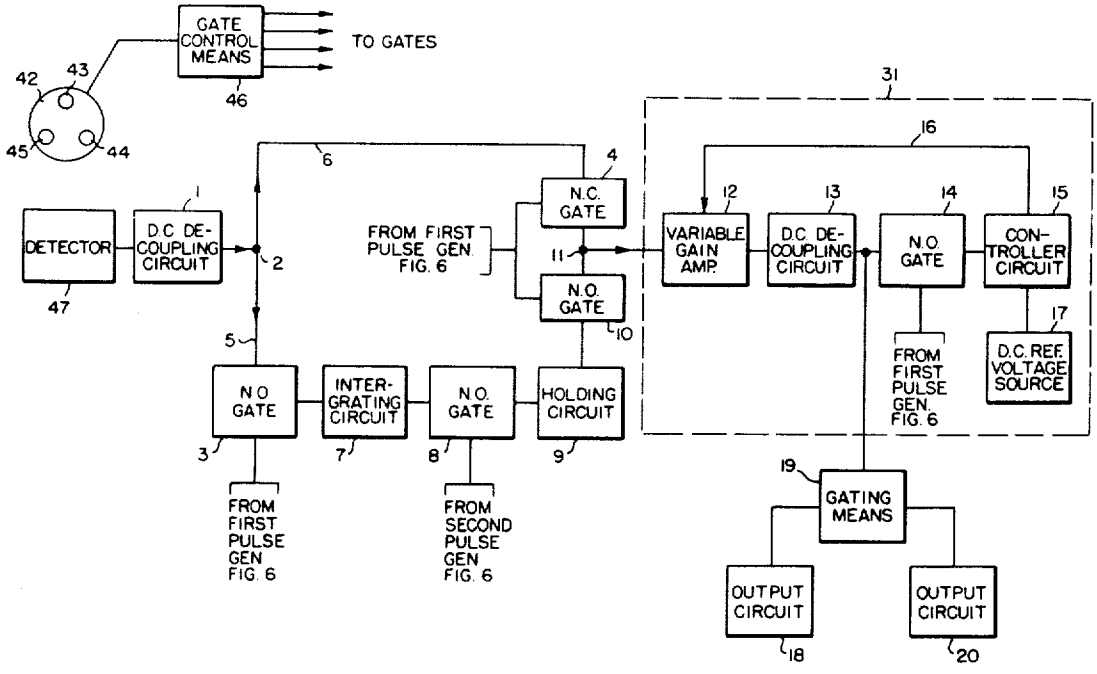
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Attorney, Agent, or Firm—Theodore B. Roessel; J. Stephen Yeo

[57] **ABSTRACT**

A ratio computer serially accepts a reference signal pulse and two condition indicating signal pulses from a detector. The computer selects the reference pulse, which is then integrated. The resulting voltage represents the energy in the reference signal pulse. The two condition indicating signal pulses are divided by the integral of the reference signal pulse to obtain the desired ratios.

8 Claims, 6 Drawing Figures



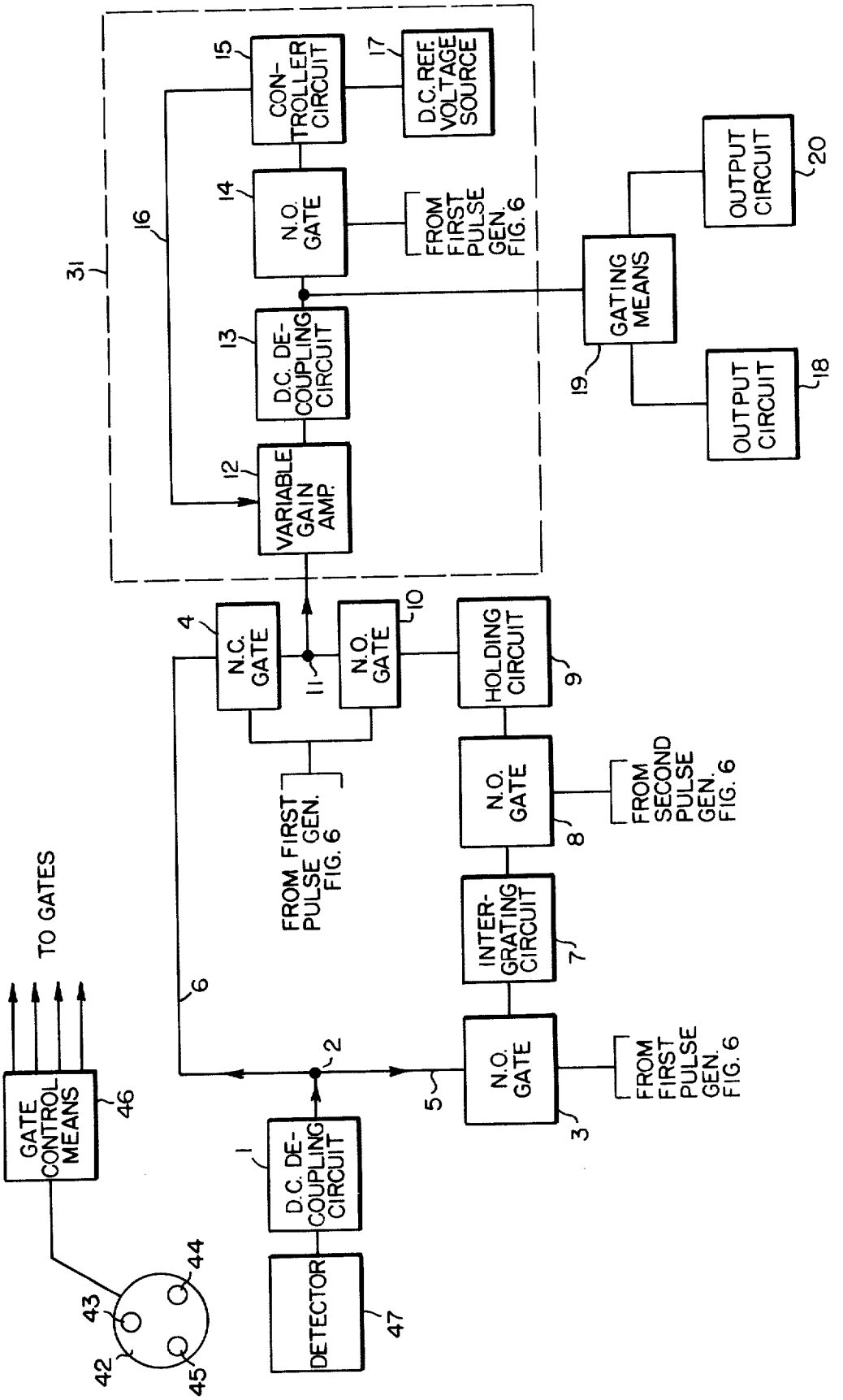

CONTROLLER CIRCUIT
D.C. REF. VOLTAGE SOURCE
N.O. GATE
FROM FIRST PULSE GEN. FIG. 6
D.C. DE-COUPLING CIRCUIT
VARIABLE GAIN AMP.
GATING MEANS
OUTPUT CIRCUIT
OUTPUT CIRCUIT
N.C. GATE
N.O. GATE
HOLDING CIRCUIT
FROM FIRST PULSE GEN. FIG. 6
N.O. GATE
FROM SECOND PULSE GEN. FIG. 6
INTER-GRATING CIRCUIT
N.O. GATE
FROM FIRST PULSE GEN. FIG. 6
TO GATES
GATE CONTROL MEANS
D.C. DE-COUPLING CIRCUIT
DETECTOR
31
16
15
17
14
13
12
20
19
18
4
10
11
9
8
7
6
2
5
3
1
46
47
42
43
44
45

FIG. 1

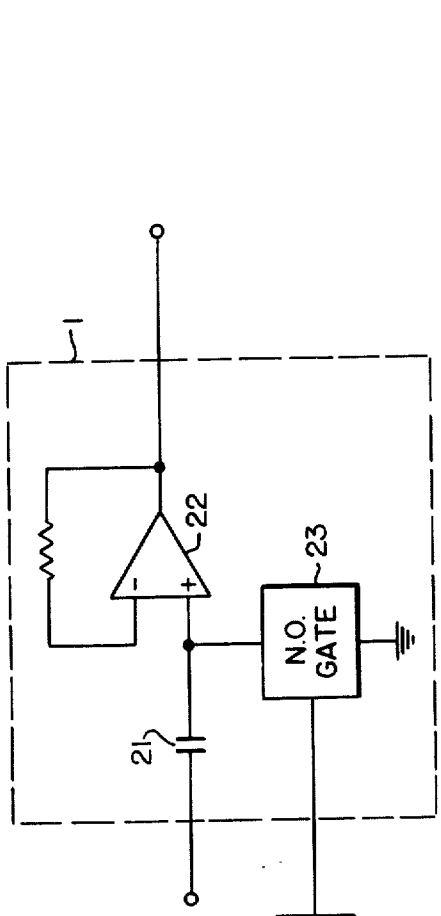

1
22
23
N.O. GATE
21
FROM NOR GATE FIG. 6

FIG. 2

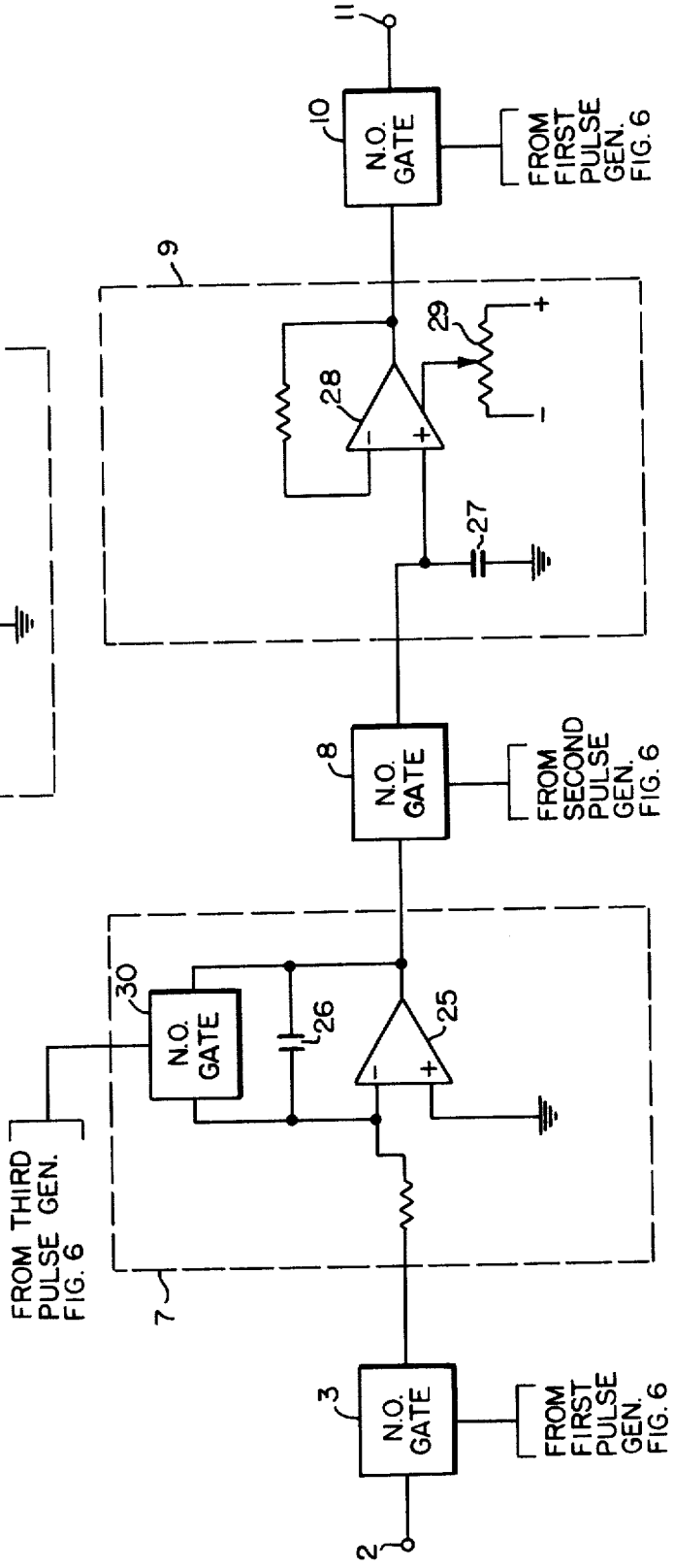

11
10
N.O. GATE
FROM FIRST PULSE GEN. FIG. 6
9
29
28
27
8
N.O. GATE
FROM SECOND PULSE GEN. FIG. 6
30
N.O. GATE
26
25
FROM THIRD PULSE GEN. FIG. 6
7
3
N.O. GATE
FROM FIRST PULSE GEN. FIG. 6
2

FIG. 3

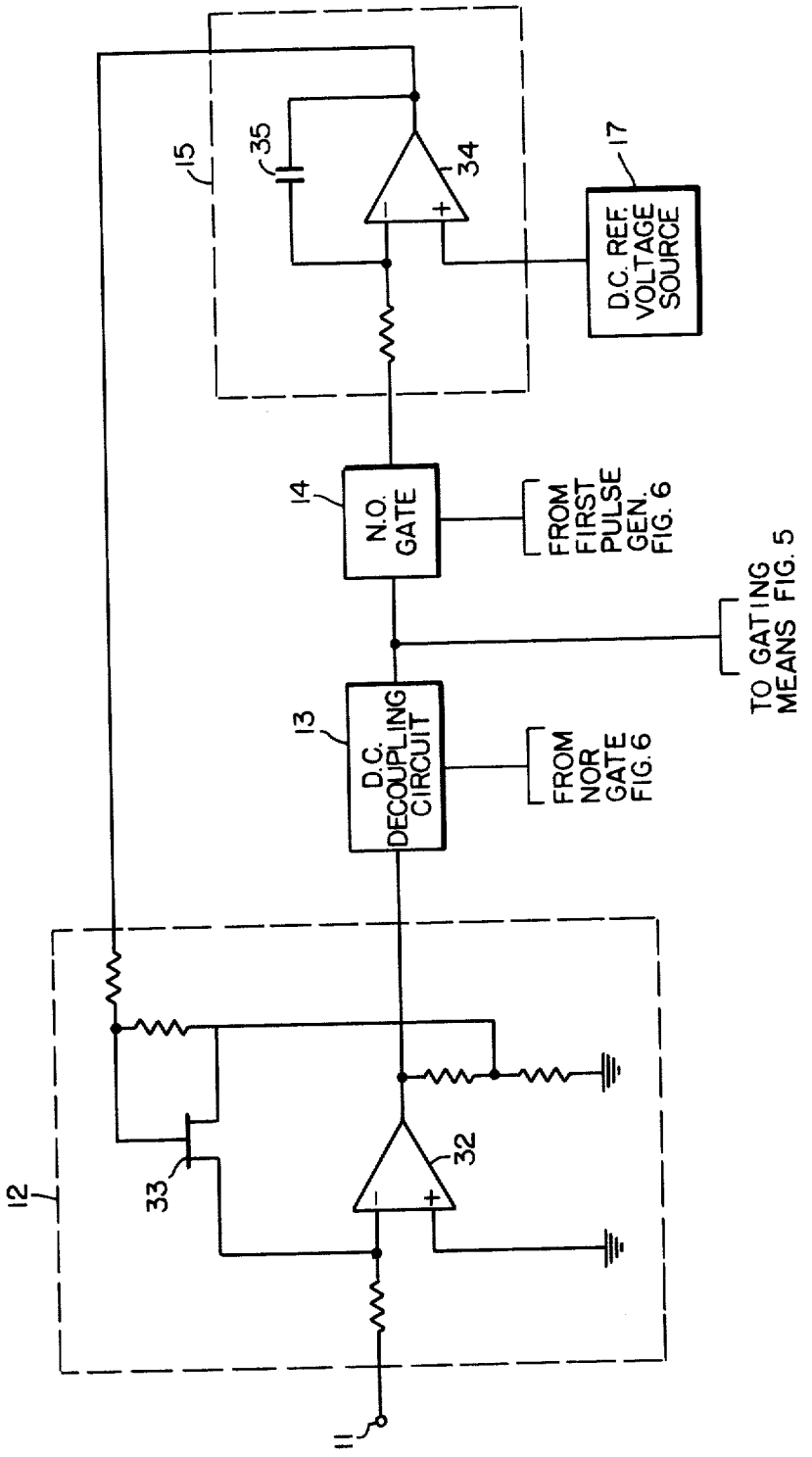

15
35
34
17
D.C. REF. VOLTAGE SOURCE
14
N.O. GATE
FROM FIRST PULSE GEN. FIG. 6
TO GATING MEANS FIG. 5
13
D.C. DECOUPLING CIRCUIT
FROM NOR GATE FIG. 6
12
33
32
11

FIG. 4

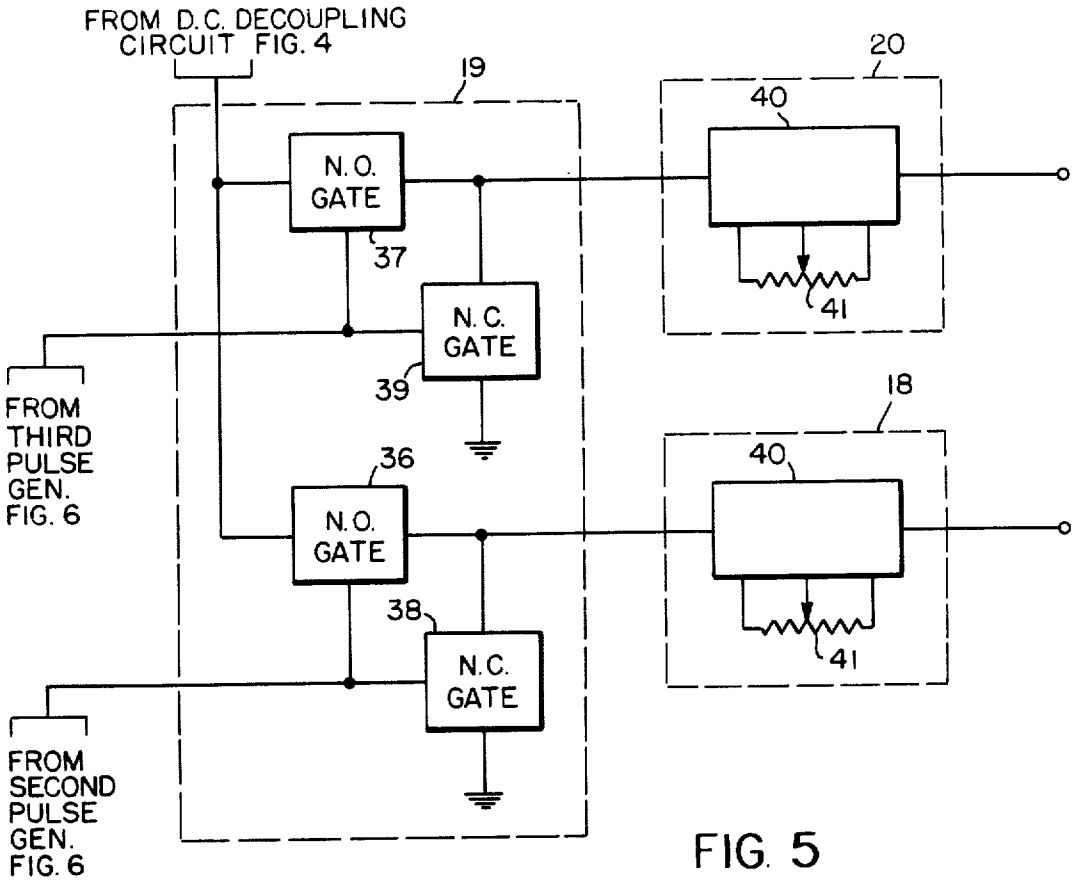

FROM D.C. DECOUPLING CIRCUIT FIG. 4
19
20
40
N.O. GATE
37
N.C. GATE
39
41
FROM THIRD PULSE GEN. FIG. 6
18
36
40
N.O. GATE
38
N.C. GATE
41
FROM SECOND PULSE GEN. FIG. 6

FIG. 5

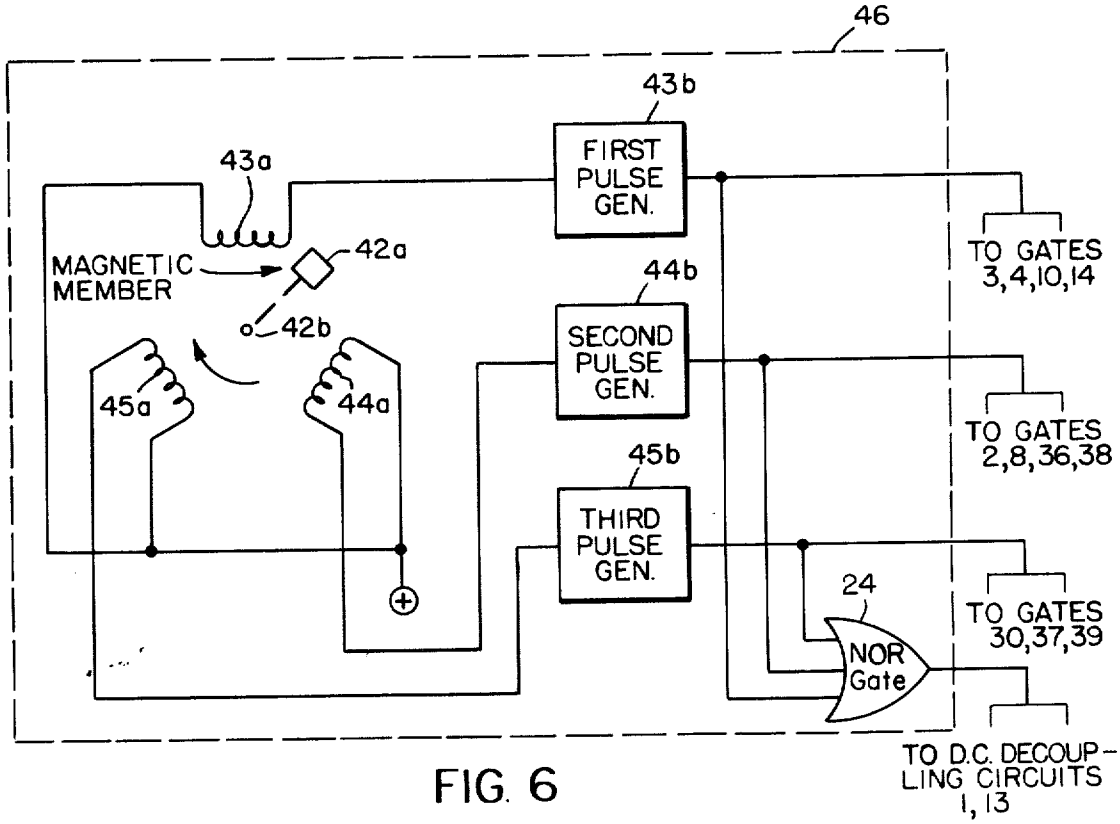

46
43b
FIRST PULSE GEN.
43a
MAGNETIC MEMBER
42a
42b
TO GATES 3,4,10,14
44b
SECOND PULSE GEN.
45a
44a
TO GATES 2,8,36,38
45b
THIRD PULSE GEN.
24
NOR Gate
TO GATES 30,37,39
TO D.C. DECOUPLING CIRCUITS 1, 13

FIG. 6

RATIO COMPUTING CIRCUIT

BACKGROUND OF THE INVENTION

This invention relates to computing ratios and more particularly concerns measuring the moisture content of paper and like materials.

The predominant constituent of paper is cellulose in the form of wood and other fibers whose natural form and substance has been altered mechanically and/or chemically and which are held together mainly by direct molecular bonding between cellulose molecules. Bonding is sometimes reinforced by an adhesive impregnant of the fibrous structure, and a mechanical interwining of fibers, and friction, also contribute a little to holding the fibers together.

Mositure (that is, liquid water) is also generally present in the fibrous structure, and various of an enormous range of other substances usually may be found impregnating the fibrous structure and/or coating the paper surface. These structural and compositional characteristics affect radiation, determine the functional properties of the end product of the paper manufacturing process, and are varied in manufacturing to obtain the practically numberless variety of papers.

When a beam of radiation is projected on paper, or on a material of analogous structure and composition, a number of interactions between the material and the radiation will occur.

A U.S. Pat. No. 3,551,678 entitled "Material Parometer Measurement Using Infrared Radiation" of Richard L. Mitchell, assigned to the assignee of the present application discloses a non-contacting instrument for continuous "on line" measurement of paper moisture. It utilizes infrared transmittance measurements at three wavelengths for the moisture determination. One wavelength is in a water absorption band, one is in a cellulose absorption band and one is at a nearby wavelength not in an absorption band and thus useful as a reference. The ratio of the transmittance in the moisture band to the transmittance at the reference wavelength is an indication of sheet moisture. This is only a relative indication however, since the relationship of the transmittance ratio to the moisture is a function of filter and paper characteristics (bandpass filters) are used to select the three wavelengths). No two bandpass filters are identical and sensitivity to moisture therefore varies from set to set. With a given of filters, the relationship of the transmittance ratio to total sheet moisture varies with both basis weight and chemical composition, (but not density or surface texture), of the paper. The ratio of transmittance in the water absorption band to transmittance just outside the band (reference wavelength) is used to eliminate such "common mode" effects as scattering of the beam by the paper or foreign material on the windows, or signal variations caused by movement of the paper web. The transmittance ratio can be measured accurately on line, while the absolute transmittance cannot.

The ratio of transmittance in the cellulose absorption band to that at the reference wavelength is a similar indication of the cellulose content of the sheet, and thus infers the basis weight. Again, the relationship is dependent on filter and paper characteristics. It is also affected somewhat by moisture content, as the two absorption bands are close together, and by the chemical composition.

The moisture gauge in the Mitchell patent consists of source and detector heads and an electronic circuitry package to process the detector signal. The source contains a infrared lamp arranged with an optical system, a motor and filter disk (containing the three bandpass filters), and three pickup coils to indicate the position of the filter disk. In operation, the disk spins and the approach of each filter to the output port is indicated by a synch pulse from the appropriate pickup coil. The source output is a beam in infrared bursts at the three wavelengths.

The detector contains an infrared sensitive cell having output signals which are fed through an amplifier. A ratio computer computes the two aforementioned ratios from the detector signals. The ratios are used to derive the moisture content of the paper. An improved ratio computer is the subject of this invention.

A U.S. Pat. No. 3,514,700, entitled "Voltage Rate Computer" of Walter F. Kalin et al. assigned to the assignee of the present application, disclosed a ratio computer. The circuit disclosed by Kalin includes a variable gain amplifier having an input disposed to receive signal voltage pulses from a detector. The output on the variable gain amplifier was gated to a holding circuit during the duration of a reference pulse. The holding circuit compared the output of the variable again amplifier to a reference voltage. The output of the holding circuit was a question of the difference between the said output of the variable gain amplifier and the said reference voltage. The output voltage of the holding circuit control of the gain of the variable gain amplifier by means of a gated feedback loop. The property of the loop is to adjust the gain of the variable gain amplifier until the amplitude of its output is equal to that of the DC reference voltage. The gain is then held constant for the remainder of the cycle. The variable gain amplifier and feedback loop acts as a dividing circuit. Subsequent signal pulses pass through the amplifier and are effectively divided by the magnitude of the reference pulse. The output of the amplifier is gated into individual holding circuits for further process of the ratios.

While this circuit has found successful application, the stability of the system may be guaranteed only when the time constant of the loop exceeds a minimum time constant which is related to the sample rate. The minimum time constant limitation has adverse effects on tracking between actual ratios and measured ratios if the changes in the perimeters are less than the time constant. It is, therefore, highly desirable to obtain ratios by means of a more stable circuit.

It is, therefore, an object of this invention to provide a new and improved ratio computer circuit for paper moisture gauges and the like.

It is a further object of this invention to provide a new and improved stable ratio computing circuit for paper moisture gauges.

It is still another object of this invention to provide a new and improved ratio computing circuit for paper moisture gauges having minimum tracking error.

It is an additional object of this invention to provide a new and improved ratio computing cicuit for paper moisture gauges having a high speed of reference.

SUMMARY OF THE INVENTION

A ratio computer that computes the ratio of at least one periodic input signal to a periodic reference signal. The input of the computer during the presence of the

reference signal is applied to circuitry which holds a function of the reference signal until a subsequent cycle. The computer includes an automatic gain control circuit. The automatic gain control circuit is in a closed loop configuration during receipt of a reference signal from a prior cycle. The gain of the automatic gain control circuit is set to be a function of the reference signal. The gain control loop is then opened so that the gain of the circuitry remains a constant for the remainder of the cycle. Subsequent input signals are amplified by the automatic gain control circuitry. The output of the automatic gain control circuit represents the ratio of a particular input signal relative to a function of the reference signal of a prior cycle. The output of the automatic gain control circuit is connected during the presence of an input signal to a computer output circuit corresponding to the input signal. A feature of this invention is that the reference signal is converted to a DC level before introduction to the automatic gain control circuit. The DC level is held until a subsequent cycle. Any transients occurring as a result of the DC conversion will have decayed to negligible amplitude during the holding period, so that the input of the automatic gain control circuit sees a DC level at all times. The time constant of the circuit is thereby kept at a minimum as most of the system transients have been eliminated.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon the reading the following detailed description and reference to the drawings in which:

FIG. **1** is a block diagram of the computing circuitry according to the present invention.

FIG. **2** is a diagram of a DC decoupling circuit.

FIG. **3** represents a first branch of the disclosed circuit.

FIG. **4** is a detailed diagram of a dividing circuit.

FIG. **5** represents the means to select and store the computed ratios.

FIG. **6** is a diagram of gate control circuitry providing a gating sequence.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In FIG. **1**, disk **42**, is the filter disk of the above identified Mitchell application including the three filters **43**, 44 and **45** mounted thereon. The filters in **43**, **44** and **45**, pass through a beam or radiation and transmit different wave lengths actually narrow spectrum bands). The filtered radiation is projected on a sheet of paper, and those portions thereof which emerge from the paper are detected by suitable means providing an output corresponding to the intensity of the detected radiation, this output being transformed by suitable means, such as electrical circuitry, represented by the detector circuit **47** into signal preferably electrical quantities such as voltage, whose magnitude are proportional to said intensities, and which are suitable for use in the systems about to be described.

In practice, disk **42** is rotated a uniform rate of speed. In each revolution, each filter is in the radiation path for less than third of the cycle. The dimensions of disk in filters in the radio in angular positions of the filters are such that in each revolution, not more than **1** filter is wholly or partly in the path of the radiation in a continuous interval. For DC decoupling circuit **1** the output signal from the detector **47**. The output signal accepts from the detector appears as a series of negative going voltage pulses, each having the same duration, but the amplitude being representative of conditions. The series of pulses consist of cycles of three signal pulses, a reference indicating signal pulse and two condition indicating signal pulses. Each of said cycles correspond to a rotation to disk body **42**.

For each of the three signal pulses there is provided by gate control means **46**, an individual synchronizing pulse.

Singal pulses are passed through the DC coupling circuit to a first node **2**, DC components of the signal pulses being removed by the DC decoupling circuit. The output of the DC coupling circuit **1** has a zero volt base line with a negative pulse representing each signal pulse. The output of the DC coupling circuit is directed in one of two branches **5** and **6** selected by series gates **3** and **4**. Series gate **3** is normally open and is closed during the presence of the first synchronizing pulse. Series gate **4** is normally closed and is opened during the presence of the first synchronizing pulse. It is, therefore, seen that during the first signal pulse, from the detector **47** which is considered the reference pulse, the output of the DC decoupling circuit is gated into branch **5**. At all other times during the cycle, the output of the DC coupling circuit **1** is gated through branch **6**. Considering, now, a reference signal pulse; the output of the DC decoupling circuit **1** is gated into branch **5**. The output of the DC coupling circuit **1** is integrated by the integrator circuit **7**. The process of integration assures fast measurement of the reference pulse. During the second signal pulse a series gate **8** at the output of the integrating circuit **7** is closed. The integral of the reference signal pulse is transferred by a gate **8** to holding circuit **9**. The integral is held in the holding circuit **9** for the remainder of the cycle. At the beginning of the next subsequent cycle, during the reference signal pulse, series gate **10** is closed allowing the integral to appear at a second node load **11**. The integral of the reference signal passes through the variable gain amplifier **12** through a DC decoupling circuit **13** through a series gate **14** to controller circuit **15**. Controller circuit **15** is in communication with the variable gain amplifier **12** by a feedback loop **16**. The controller circuit **15** is also in a communication with a reference voltage source **17**. The property of this loop is for the controller circuit to adjust the gain of the variable gain amplifier **12** such that the output of variable gain amplifier **12** is substantially equal in amplitude to that of the reference voltage source **17**. The result is at the gain of the variable gain amplifier **12** is inversely proportional to the amplitude of the integral of the reference signal pulse. The gain is maintained as a constant for the remainder of the cycle.

During the second signal pulse, the output of the DC decoupling circuit **1** is gated to branch **6** through gate **4** to the second node **11**. The output is then amplified by the variable gain amplifier **12**. As aforementioned, the gain of variable gain amplifier **12** is inversely proportional to the integral of reference signal pulse. This operation, therefore, is equivalent of dividing the second signal pulse by the integral of the reference signal pulse. The output of variable gain amplifier **12** passes through DC decoupling circuit **13**. During the second signal pulse, the output of DC decoupling circuit **13** is

in communication with holding circuit **18** by a gating means **19.** During the third signal pulse, the output of DC decoupling circuit **1** is also gated through branch **6** by a gate **4,** through the variable gain amplifier **12,** through the DC decoupling circuit **13.** During the third signal pulse, the output of DC decoupling circuit **13** is connected to output holding circuit **20** by the gating means **19.** Output holding circuit **18** holds until the next cycle, the ratio of the second signal pulse divided by the integral of the first reference signal pulse. Output holding circuit **20** holds the signal representative of the ratio of third signal pulse divided by the integral of the reference signal pulse. Strictly speaking, the integral is that of the reference pulse of the previous cycle. However, because of the fast repetition rate, of the cycle, this should introduce little error.

FIG. **2** is a detail of the DC decoupling circuit **1.** This circuit is also used for the DC decoupling circuit **13.** At the input of the decoupling circuit, there is a series DC blocking decapacitor **21.** In series with the output, of the blocking capacitor **21** and the output on a DC circuit there is interposed a non-inverting operational amplifier **22.** The purpose of a non-invering operational amplifier **22** is to prevent the discharge of a blocking capacitor for the duration of a signal pulse. The output of the amplifier **22** has a zero volt base line with a negative pulse representing each signal pulse. Interposed between the blocking capacitor **21** and the non-inverting operational amplifier **22** there is a normally open shunt gate **23** to ground. The gate **23** is turned on inbetween signal pulses by means of a gating signal from a nor-gate **24** to the shut gate **23.** The nor-gate **24** generates this gating signal in the absence of any of the three synchronizing pulses. In this manner, any DC component across the DC blocking capacitor **21** is discharged between each synchronizing pulse.

FIG. **3** is a more detailed diagram of branch **5** which extends from the first node **2** to the second node **11.** Series gate **3** closes during the reference signal pulse and allows the DC decoupled reference signal pulse to be integrated by integrating circuit **7.** Integrating circuit **7** includes an inverting operational amplifer **25** having a feedback capacitor **26.** During the second signal pulse, gate **9** closes to store the resulting DC level on capacitor **27** of the holding circuit **9.** The output on the holding circuit **9** includes a non-inverting buffer amplifier **28** which prevents a discharge of capacitor **27.** Buffer amplifier **28** may include a variable voltage source **29** which is used for calibration purposes. This is used to adjust the zero offset of amplifier **28** to match the combined zero offsets amplifiers **25** and **28** to amplifier **22.** During the third signal pulse, a normally open gate **30** discharges the feedback capacitor **26** of the integrating circuit **7.** At the beginning of the next cycle, during the first signal pulse, gate **10** closes which allow the output of holding circuit **9** to appear at node **11.** The output of the holding circuit **9** is a DC level representing the energy in last reference signal pulse.

FIG. **4** is a detailed diagram of a dividing circuit **31** first seen in FIG. **1.** We will first consider the operation of the circuit during the first signal pulse which is considered the reference signal pulse. At node **11,** there exists a positive DC level representing the energy in the last energy signal pulse. This level is amplified by a variable gain amplifier **12.** The variable gain amplifier **12** includes an inverting variable gain amplifier **32** whose gain is controlled by an N channel field-effect transistor **33.** This transistor **33** is used as a voltage controlled feedback resistor. The transistor **33** is operated at millivolt levels in order to utilize its purely resistive characteristics. The output of the variable gain amplifier **12** is connected by a DC decoupling circuit **13** through the series gate **14** to the controller circuit **15.** The DC decoupling circuit **13** has been described in detail by FIG. **2.** The controller circuit **15** includes an inverting integrator amplifier **34** having two inputs, one of which accepts the output of the variable gain amplifier **12.** The other input is connected to the reference voltage source **17.** The output of the controller circuit **15,** is connected by a feedback line **16** to the transistor **33** of the variable gain amplifier **12.** A characteristic of an operational amplifier in a close loop configuration, such as is used in the controller's circuit **15,** is for the difference of its inputs to approach zero. It follows the output of the controller circuit **15** adjusts the gain of the variable gain amplifier **12** until the output of the variable gain amplifier **12** is substantially equal to the level of the reference voltage **17** coming into controller circuit **15.** This loop settles completely before gate **14** opens and the resulting output control voltage from the controller circuit **15** is held by the capacitor **35** until the gate **14** closes again during the next cycle. Again, with amplifier **12** has now been set equal to the reference voltage from source **17** divided by the reference signal pulse energy. Thus, the gain of the variable gain amplifier **12** is inversely proportional to the reference pulse signal and is held constant for the duration of the cycle. upon the completion of a reference signal pulse, gate **14** opens up. Subsequent signal pulses form branch **6** appears at node **11** and are amplified by the variable gain amplifier **12.** The output appears through the DC coupling circuit **13** and represents the ratio of the subsequent signal pulse divided by the integral of the references signal pulse. For each cycle, there will appear two ratios which are individually gated to holding circuits.

FIG. **5** diagrams the details of gating means **19,** and the output circuits **18** and **20.** During the second signal pulse the output from the DC decoupling circuit appears across the normally open gates **36** and **37.** Gate **36** is closed by the second synchronizing pulse. The output is thereby connected to holding circuit **18.** At the end of the second synchronizing pulse, normally closed shut gate **38** is closed discharging any offset at the input of holding circuit **18.** During the third signal pulse, gate **37** is closed by action of the third synchronizing pulse thereby applying the output from the DC decoupling circuit **13** through the gate **37** to the holding circuit **20.** At the end of the third pulse, normally closed shut gate **39** is closed discharging any offset in the input of holding circuit **20.** Holding circuits **18** and **20** are identical in design. A high order active filter **40** may be used to convert pulse outputs to DC levels by attenuating frequencies at the pulse repetition rate, while still allowing first response. The external gain adjust **41** is provided. Alternatively, the active filter may be replaced by an integrating type sample and hold scheme similar to that used in branch **5** of FIG. **1** for faster response.

In FIG. **6,** gate control means **46** is depicted as having a magnetic member **42A** mounted for rotation about an axis **42B.** Conveniently, member **42A** is mounted on the periphery of disk **42,** making that axis **42B** the axis of rotation of disk **42** (not shown in FIG. **6**). Pick up

coils **43A**, **44A** and **45A** are equally spaced about and closely adjacent to the path of member **42A**. As member **42A** rotates, its passing a pick up coil to generate a pulse therein. Each such pulse is coupled to a corresponding one of pulse generators **43B**, **44B** and **45B** of convenient construction, as for example, mono stable vibrators constructed of predetermined duration. These pulses are transmitted to the gates indicated in the figure. Each pulse starts just before the associated detector signal pulse and end just after the associated detector signal pulse. These pulses are also feed to a NOR gate whose output is a pulse occurring in the interval between detector signal pulse. The output pulse from the NOR right gate is feed to the DC decoupling circuits **1** and **13** to obtain the device DC outputs representation of the ratios.

A feature of this invention is that the reference signal is converted to a DC level before introduction to the automatic gain control circuit. The DC level is held until a subsequent cycle. Any transients occurring as a result of the DC conversion will have decayed to negligible amplitude during the holding period, so that the input of the automatic gain control circuit sees a DC level at all times. The time constant of the circuit is thereby kept at a minimum as most of the system transients have been eliminated.

The disclosed ratio computer has exceptionally stable circuitry and provides a good correlation between actual ratio and measured ratios independent of sample rate.

Although the invention has been described above in the form of a ratio computer for computing the ratio of the amplitude of a input signal relative to the amplitude of a reference signal, it is to be understood, that the invention would also apply to other parameters of the input and refernce signals such as, for example, pulse width. In the case of pulse width ratio circuits, the block diagram of FIG. **1** can be modified by including a pulse width to analog convertor circuit between the output of the DC decoupling circuit **1** and the node **2.** Such pulse width to analog convertor circuits are well known in the art such as, for example, the type disclosed in the U.S. Pat. No. 3,590,250 issued on June 29, 1971, to Richard L. Witkover and entitled "Valve and Pulse-Width Modulated Data Link Using Infrared Light To Control and Monitor Power Supply For Modulator For High-Energy Accelerator." In such a case, the signals at the output circuits **18** and **20** will be a ratio of the duration of the input signals relative to the duration of the reference signals of the prior periodic signal.

I claim:

1. A ratio computer comprising:

automatic gain control circuit means having a signal input circuit, a signal output circuit, and a gain control input circuit;

circuit means for receiving periodically recurring cycles of signals, each cycle including a reference signal and at least one input signal;

a computer output circuit;

first gating circuit means synchronized to said periodic signals for alternately connecting the signal output circuit to said gain control input circuit and to said computer output circuit;

second gating circuit means receiving said periodic signal and synchronized thereto, for storing a signal that is a function of the magnitude of a parameter of the received reference signal and applying the stored signal to said signal input circuit during a subsequent cycle of said periodic signals while said first gating circuit means connects said signal output circuit to said gain control input circuit, and

third gating circuit means receiving said periodic signals and synchronized thereto for applying said input signal to said signal input circuit while said first gating circuit means connects said signal output circuit to said computer output circuit so that the signal at the computer output circuit is a ratio of the magnitude of the parameter of said input signal that corresponds to said reference signal parameter relative to the magnitude of said reference signal parameter of the prior cycle to the periodic signals.

2. A ratio computer as defined in claim **1** wherein:

said parameter of said input signal is a function of the amplitude of said input signal and;

said parameter of said reference signal is a function of the amplitude of said reference signal.

3. A ratio computer as defined in claim **2** wherein:

said second gating circuit means includes a converting circuit means for converting the amplitude of the reference signal to a DC signal.

4. A ratio computer as defined in claim **3** wherein said converting circuit means:

includes an integrating circuit for integrating the received reference signal and a holding circuit for storing the integrated reference signal for an additional cycle.

5. A ratio computer as defined in claim **2** wherein second said gating circuit means includes:

an integrating circuit means;

an input gate synchronized to said periodic signals for translating the reference signals to said integrating means;

a holding circuit;

circuit means for transferring an integrated output signal from said integrating circuit means to said holding circuit, and

an output gate, synchronized to said periodic signals, for translating an output signal from said holding circuit to said signal input circuit.

6. A ratio computer as defined in claim **5** wherein:

said transferring circuit means includes a gating circuit, synchronized to said periodic signals for translating the output of said integrating circuit means to said holding circuit during the absence of the reference signal.

7. A ratio computer as defined in claim **6** wherein:

said periodic signals comprise the reference signal and a plurality of input signals, in consecutive sequence;

said computer circuit output includes a plurality of output circuits, a separate one for each of said plurality of input signals; and

said first gating circuit means includes a plurality of gates, a separate one connected between said signal output circuit and each of said plurality of output circuits, said plurality of gates being synchronized to said input signals to translate their respective output signals from said output circuits to the appropriate one of the plurality output circuits.

8. A method for computing the ratio of the amplitude of a periodic input signal as a function of the amplitude of a periodic reference signal, wherein said input and

reference signals are periodically reoccurring signals, said method comprising:

integrating said periodic reference signal to obtain the integral of the amplitude of said periodic reference signal;

holding said integral until the subsequent cycle of the reoccurring signals;

adjusting the gain of a variable gain amplifier in an inverse proportion to said integral during said subsequent cycle, and

amplifying said periodic input signals by said variable gain amplifier so that the output signal of said variable gain amplifier is representative of the ratio of the amplitude of said reoccurring input signals to the integral of said periodic reference signal.

* * * * *