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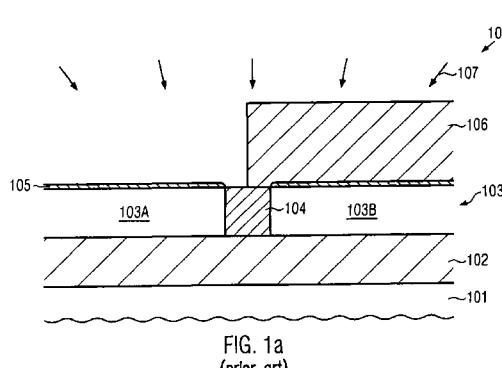
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(54) Title: REDUCTION OF THRESHOLD VOLTAGE VARIATION IN TRANSISTORS COMPRISING A CHANNEL SEMICONDUCTOR ALLOY BY REDUCING DEPOSITION NON-UNIFORMITIES



(57) Abstract: A threshold adjusting semiconductor material, such as a silicon/germanium alloy may be provided selectively for one type of transistors on the basis of enhanced deposition uniformity. For this purpose, the semiconductor alloy may be deposited on the active regions of any transistors and may subsequently be patterned on the basis of a highly controllable patterning regime. Consequently, threshold variability may be reduced.

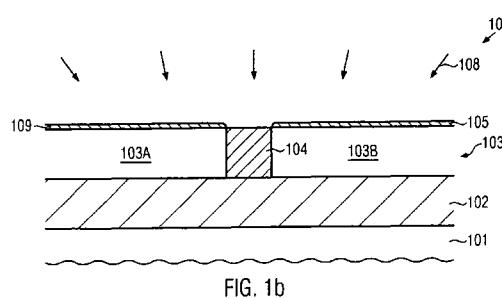


FIG. 1b  
(prior art)



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**REDUCTION OF THRESHOLD VOLTAGE VARIATION IN TRANSISTORS  
COMPRISING A CHANNEL SEMICONDUCTOR ALLOY BY REDUCING  
DEPOSITION NON-UNIFORMITIES**

**FIELD OF THE PRESENT DISCLOSURE**

Generally, the present disclosure relates to sophisticated integrated circuits including advanced transistor elements that comprise highly capacitive gate structures including a metal containing electrode and a high-k gate dielectric of increased permittivity compared to gate dielectrics, such as silicon dioxide and silicon nitride.

**DESCRIPTION OF THE PRIOR ART**

The fabrication of advanced integrated circuits, such as CPUs, storage devices, ASICs (application specific integrated circuits), and the like, requires a large number of circuit elements to be formed on a given chip area according to a specified circuit layout, wherein field effect transistors represent one important type of circuit elements that substantially determine performance of the integrated circuits. Generally, a plurality of process technologies are currently practiced, wherein for many types of complex circuitry including field effect transistors, MOS technology is currently one of the most promising approaches due to the superior characteristics in view of operating speed and/or power consumption and/or cost efficiency. During the fabrication of complex integrated circuits using, for instance, MOS technology, millions of transistors, e.g., n-channel transistors and/or p-channel transistors, are formed on a substrate including a crystalline semiconductor layer. A field effect transistor, irrespective of whether an n-channel transistor or a p-channel transistor is considered, typically comprises so-called pn-junctions that are formed by an interface of highly doped regions, referred to as drain and source regions, with a slightly doped or non-doped region, such as a channel region, disposed adjacent to the highly doped regions. In a field effect transistor the conductivity of the channel region, i.e., the drive current capability of the conductive channel, is controlled by a gate electrode formed adjacent to the channel region and separated therefrom by a thin insulating layer. The conductivity of the channel region upon formation of a conductive channel due to the application of an appropriate control voltage

to the gate electrode, depends on the dopant concentration, the mobility of the charge carriers, and – for a given extension of the channel region in the transistor width direction – on the distance between the source and drain regions, which is also referred to as channel length. Hence, in combination with the capability of rapidly creating a conductive channel below the insulating layer upon application of the control voltage to the gate electrode, the conductivity of the channel region substantially affects the performance of MOS transistors. Thus, as the speed of creating the channel, which depends on the conductivity of the gate electrode, and the channel resistivity substantially determine the transistor characteristics, the scaling of the channel length – and associated therewith the reduction of channel resistivity and reduction of gate resistivity – is a dominant design criterion for accomplishing an increase in the operating speed of the integrated circuits.

Presently, the vast majority of integrated circuits is fabricated on the basis of silicon due to the substantially unlimited availability thereof, the well-understood characteristics of silicon and related materials and processes and the experience gathered over the last 50 years. Therefore, silicon will likely remain the material of choice in the foreseeable future for circuit generations designed for mass products. One reason for the importance of silicon in fabricating semiconductor devices, has been the superior characteristics of a silicon/silicon dioxide interface that allows reliable electrical insulation of different regions from each other. The silicon/silicon dioxide interface is stable at high temperatures and thus, allows the performance of subsequent high temperature processes, as are required for example for anneal cycles to activate dopants and to cure crystal damage without sacrificing the electrical characteristics of the interface.

For the reasons pointed out above, silicon dioxide is preferably used as a gate insulation layer in field effect transistors that separates the gate electrode, frequently comprised of polysilicon or other metal containing materials, from the silicon channel region. In steadily improving device performance of field effect transistors, the length of the channel region has continuously been decreased to improve switching speed and drive current capability. Since the transistor performance is controlled by the voltage supplied to the gate electrode to invert the surface of the channel region to a sufficiently high charge density for providing the desired drive current for a given supply voltage, a certain degree of

capacitive coupling, provided by the capacitor formed by the gate electrode, the channel region and the silicon dioxide disposed therebetween, has to be maintained. It turns out that decreasing the channel length requires an increased capacitive coupling to avoid the so-called short channel behavior during transistor operation. The short channel behavior may lead to an increased leakage current and to a pronounced dependence of the threshold voltage on the channel length. Aggressively scaled transistor devices with a relatively low supply voltage and thus reduced threshold voltage may suffer from an exponential increase of the leakage current while also requiring enhanced capacitive coupling of the gate electrode to the channel region. Thus, the thickness of the silicon dioxide layer has to be correspondingly decreased to provide for the required capacitance between the gate and the channel region. For example, a channel length of approximately  $0.08\mu\text{m}$  may require a gate dielectric made of silicon dioxide as thin as approximately 1.2nm. Although generally usage of high speed transistor elements having an extremely short channel may be restricted to high speed applications, whereas transistor elements with a longer channel may be used for less critical applications, such as storage transistor elements, the relatively high leakage current caused by direct tunneling of charge carriers through an ultra thin silicon dioxide gate insulation layer may reach values for an oxide thickness in the range of 1-2nm that may no longer be compatible with requirements for performance driven circuits.

Therefore, replacing silicon dioxide, or at least a part thereof, as the material for gate insulation layers has been considered, particularly for extremely thin silicon dioxide gate layers. Possible alternative dielectrics include materials that exhibit a significantly higher permittivity so that a physically greater thickness of a correspondingly formed gate insulation layer nevertheless provides for a capacitive coupling that would be obtained by an extremely thin silicon dioxide layer. Commonly, a thickness required for achieving a specified capacitive coupling with silicon dioxide is referred to as capacitance equivalent thickness (CET). Thus, at a first glance, it appears that simply replacing the silicon dioxide with high-k materials is a straight forward way to obtain a capacitance equivalent thickness in the range of 1nm and less.

It has been thus suggested to replace silicon dioxide with high permittivity materials such as tantalum oxide ( $Ta_2O_5$ ) with a  $k$  of approximately 25, strontium titanium oxide ( $SrTiO_3$ ) having a  $k$  of approximately 150, hafnium oxide ( $HfO_2$ ),  $HfSiO$ , zirconium oxide ( $ZrO_2$ ), and the like.

When advancing to sophisticated gate architecture based on high- $k$  dielectrics additionally, transistor performance may also be increased by providing an appropriate conductive material for the gate electrode so as to replace the usually used polysilicon material, since polysilicon may suffer from charge carrier depletion at the vicinity of the interface to the gate dielectric, thereby reducing the effective capacitance between the channel region and the gate electrode. Thus, a gate stack has been suggested in which a high- $k$  dielectric material provides for enhanced capacitance even at a less critical thickness compared to a silicon dioxide layer, while additionally maintaining leakage currents at an acceptable level. On the other hand metal containing non-polysilicon material, such as titanium nitride, aluminum oxide and the like, may be formed so as to directly connect to the high- $k$  dielectric material, thereby substantially avoiding the presence of a depletion zone. Since typically a low threshold voltage of the transistor, which represents the voltage at which a conductive channel forms in the channel region, is desired to obtain the high drive currents, commonly the controllability of the respective channel requires sophisticated lateral dopant profiles and dopant gradients, at least in the vicinity of the pn-junctions. Therefore, so-called halo regions are usually formed by ion implantation in order to introduce a dopant species whose conductivity type corresponds to the conductivity type of the remaining channel and semiconductor region so as to "reinforce" the resulting pn-junction dopant gradient after the formation of respective extension and deep drain and source regions. In this way, the threshold voltage of the transistor significantly determines the controllability of the channel, wherein a significant variance of the threshold voltage may be observed for reduced gate lengths. Hence, by providing an appropriate halo implantation region the controllability of the channel may be enhanced, thereby also reducing the variance of the threshold voltage, which is also referred to as threshold roll off, and also reducing significant variations of transistor performance with a variation in gate length. Since the threshold voltage of the transistors is significantly affected by the work function of the gate material that is in contact with the gate dielectric material, an appropriate adjustment of the effective work function with respect to the conductivity type of the transistor under consideration has to be guaranteed.

For example, appropriate metal-containing gate electrode materials such as titanium nitride, aluminum oxide and the like may frequently be used, wherein the corresponding work function may be adjusted so as to be appropriate for one type of transistor, such as n-channel transistors, while p-channel transistors may require a different work function and thus a differently treated metal containing electrode material in order to obtain the desired threshold voltage. In this case, complex and sophisticated manufacturing regimes may be required so as to provide different gate electrode materials in order to comply with the requirements of different transistor types. For this reason it has also been proposed to appropriately adjust the threshold voltage of transistor devices by providing a specifically designed semiconductor material at the interface between the high-k dielectric material and the channel region of the transistor device, in order to appropriately "adapt" the band gap of the specifically designed semiconductor material to the work function of the metal-containing gate electrode material, thereby obtaining the desired low threshold voltage of the transistor under consideration. Typically, a corresponding specifically designed semiconductor material, such as silicon/germanium and the like, may be provided by an epitaxial growth technique, which may also present an additional complex process step, which however may provide for reduced overall process complexity compared to the provision of the different metal-containing gate electrode materials or which may provide for increased flexibility in obtaining appropriate transistor characteristics.

It turns out, however, that the manufacturing sequence for providing the threshold adjusting semiconductor alloy may have a significant influence on threshold variability across semiconductor die or substrates, as will be explained in more detail with reference to figures 1A to 1D.

Figure 1A schematically illustrates a cross-sectional view of a semiconductor device 100 comprising a substrate 101, above which is formed a silicon-containing semiconductor material 103 having an appropriate thickness for forming therein and thereabove transistor elements. In the example shown, a buried insulating layer 102, for instance in the form of a silicon dioxide material, is positioned between the substrate 101 and the silicon-containing semiconductor layer 103. Moreover, an isolation structure 104, such as a shallow trench isolation, is formed in the semiconductor layer 103 so as to define a first crystalline "active" region 103A and a second active region 103B. In this context, an

active region is to be understood as a semiconductor material, in which an appropriate dopant profile is created so as to form pn-junctions for one or more transistor elements. In the example shown, the first active region 103A may correspond to a p-channel transistor, while the second active region 103B may correspond to an n-channel transistor. Furthermore, a mask layer 105, for instance in the form of a silicon dioxide material, and the like, may be formed so as to at least cover the first and second active regions 103A, 103B, while the isolation structure 104 may be exposed, depending on the process for forming the mask layer 105. Additionally, an etch mask 106 is provided, for instance in the form of a resist mask, which covers the second active region 103B and exposes the first active region 103A.

The semiconductor device 100 as illustrated in figure 1A may typically be formed on the basis of the following process techniques. First, the isolation structure 104 is formed on the basis of well-established lithography, etch, deposition, planarization and anneal techniques, in which, for instance, a trench is formed in the semiconductor layer 103 on the basis of a lithography process, which is subsequently to be filled with an appropriate insulating material, such as silicon dioxide, silicon nitride, and the like. After removing excess material and planarizing the surface topography, the further processing is typically continued by performing active implantation sequences using an appropriate mask regime in order to introduce the corresponding dopant species for generating the basic dopant concentration in the active regions 103A, 103B corresponding to the type of transistors to be formed therein and thereabove. After activating the dopant species and recrystallizing implantation induced damage, the further processing may be continued by forming the mask layer 105, for instance on the basis of an oxidation process, and the like. Next, the resist mask 106 is formed by using lithography techniques in order to expose a portion of the mask layer 105 that is to be removed during the etch process 107, which may be performed as a wet chemical etch step using, for instance, hydrofluoric acid (HF), when the mask layer 105 is comprised of silicon dioxide. Furthermore, after removing the etch mask 106, the exposed surface area may be treated in order to prepare the first active region 103A for the selective deposition of a silicon/germanium alloy that is appropriately designed for adjusting the threshold voltage or band gap energy in combination with a metal-containing electrode material to be formed in a later manufacturing stage.

Figure 1B schematically illustrates the semiconductor device 100 during a selective epitaxial growth process 108, in which process parameters are selected in accordance with well established recipes such that significant material deposition may be restricted to the exposed active region 103A, while material deposition on dielectric surface areas may be negligible. Consequently, during the selected epitaxial growth process 108 a silicon/germanium alloy 109 may selectively be formed on the active region 103A, while a deposition thereof on the isolation structure 104 and on the mask layer 105 may be suppressed. For instance, in sophisticated applications, the silicon/germanium alloy 109 may be provided with a thickness of approximately 10nm and less, while a germanium concentration may be approximately 25 atomic percent. It should be appreciated that the material composition of the silicon/germanium alloy 109 as well as the thickness thereof may have a significant influence on the finally-obtained threshold voltage and thus on the finally-obtained transistor characteristics.

Figure 1C schematically illustrates the semiconductor device 100 in a further advanced manufacturing stage. As illustrated, the device 100 is exposed to an etch ambient 110, for instance provided in the form of a wet chemical etch ambient, in which the mask layer 105 (cf. figure 1B) is selectively removed with respect to material of the active region 103B and the previously-deposited silicon/germanium alloy 109. For instance, the etch process 110 is performed on the basis of hydrofluoric acid, which may remove silicon dioxide material with a high degree of selectivity with respect to the materials 103B and 109. Thereafter, the further processing may be continued by forming gate electrode structures and completing the basic transistor configuration.

Figure 1D schematically illustrates the semiconductor device 100 in an advanced manufacturing stage. In this stage, a p-channel transistor 150A is formed in and above the active region 103A and an n-channel transistor 150B is formed in and above the active region 103B. The transistors 150A, 150B both comprise an electrode structure 151 including a gate insulation layer 151B, comprising a high-k dielectric material, as previously explained. Furthermore, a metal-containing electrode material, such as aluminum oxide, titanium nitride, and the like, may be formed on the gate insulation layer 151B, followed by a further electrode material, such as polysilicon 151C. As illustrated, in the p-channel transistor 150A, the gate insulation layer 151B is formed on the silicon/germanium alloy 109 so that a threshold voltage of the transistor 150A, i.e. the voltage at which a conductive channel forms in a channel region 153, may be determined

by the characteristics of the alloy 109 and the materials 151B and 151A, in combination with the corresponding characteristics of drain and source regions 154, which may also be formed on the basis of sophisticated dopant profiles, as previously explained. On the other hand, the band gap configuration of the channel region 153 of the transistor 150B is appropriate for the bonding materials 151B, 151A.

The transistors 150A, 150B may be formed on the basis of well-established manufacturing techniques including the deposition of the gate insulation layers 151B, the electrode materials 151A and the polysilicon material 151C and the patterning thereof using sophisticated lithography and etch techniques. Thereafter, corresponding implantation sequences may be performed in combination with a manufacturing sequence for forming a spacer structure 152 in order to appropriately define the vertical and lateral dopant profile for the drain and source regions 154. After corresponding anneal processes for activating the dopants and recrystallizing implantation-induced damage, the basic transistor configuration may be completed, if required, by forming metal silicide regions (not shown) in the drain and source regions 154 and the polysilicon material 151C.

Also the threshold voltage of the p-channel transistor 150A may efficiently be adjusted by providing the silicon/germanium alloy 109, a significant variability of the threshold voltages of p-channel transistors may be observed, in particular a significant deviation of the threshold voltage of p-channel transistors in densely packed device regions and the device areas may be observed. Consequently, for sophisticated applications requiring highly-scaled transistor elements having a gate length of 50 nm and less, the conventional strategy for adjusting the threshold voltage of transistors comprising a sophisticated high-k metal gate electrode structure may be less than desirable due to the high threshold variability obtained in the conventional process flow.

In view of the situation described above, the present disclosure relates to manufacturing techniques and semiconductor devices, in which an efficient threshold adjustment may be achieved on the basis of a semiconductor alloy provided in the channel region while avoiding or at least reducing the effects of one or more of the problems identified above.

## SUMMARY OF THE PRESENT DISCLOSURE

Generally, the present disclosure provides semiconductor devices and manufacturing techniques, in which threshold variability of transistors including a threshold adjusting semiconductor alloy may significantly be reduced by reducing process non-uniformities during the deposition of the threshold adjusting semiconductor material. To this end, the degree of "pattern loading" during the epitaxial growth process for depositing the threshold adjusting semiconductor material may be reduced, thereby obtaining a high degree of uniformity across individual semiconductor die and also entire substrates. In this respect, the term "pattern loading" may be understood as the effect of variability of layer thickness and/or material composition during a deposition process depending on the "neighborhood" of the area, on which the corresponding material is to be deposited. That is, typically, the deposition behavior may depend on the local deposition conditions, which in turn may be determined by the neighborhood of a deposition area, wherein, in particular, a significant difference between densely packed device regions and non-densely packed device regions may be observed. Consequently, according to the principles disclosed herein, the corresponding local deposition conditions may be made more uniform by depositing the threshold adjusting material in a more "global" manner and patterning the same in a subsequent uniform and well-controllable patterning sequence.

One illustrative method disclosed herein comprises forming a layer of a silicon-containing semiconductor alloy on a first silicon-containing crystalline semiconductor region and a second silicon-containing crystalline semiconductor region. The method further comprises removing the layer of silicon-containing semiconductor alloy selectively from the second silicon-containing crystalline semiconductor region. Furthermore, the method comprises forming a first gate electrode structure of a first transistor on the layer of silicon-containing semiconductor alloy, wherein the first gate electrode structure comprises a high-k dielectric gate insulation layer and a metal-containing gate electrode material formed on high-k dielectric gate insulation layer. Finally, the method comprises forming a second gate electrode structure of a second transistor above the second silicon-containing crystalline semiconductor region, wherein the second gate electrode structure comprises a high-k dielectric gate insulation layer and a metal-containing gate electrode material formed thereon.

A further illustrative method disclosed herein comprises forming a threshold adjusting semiconductor material on first and second silicon-containing semiconductor regions. Furthermore, a dopant species is introduced into the second silicon-containing semiconductor regions by using an implantation mask that covers the first silicon-containing semiconductor region. The method further comprises removing the threshold adjusting semiconductor material selectively from the second silicon-containing semiconductor region on the basis of the implantation mask. Finally, the method comprises forming a first gate electrode structure of a first transistor on the threshold adjusting semiconductor material and a second gate electrode structure of a second transistor on the second silicon-containing semiconductor region, wherein the first and second gate electrode structures comprise a high-k dielectric material and a metal-containing electrode material formed on the high-k dielectric material.

One illustrative semiconductor device disclosed herein comprises a first device region comprising a plurality of densely packed first p-channel transistors that define a pitch of approximately 100nm or less. Each of the first p-channel transistors is formed in and above a first silicon-containing semiconductor region and comprises a first layer of a threshold adjusting semiconductor alloy in a channel region of each of the first p-channel transistors. The semiconductor device further comprises a second device region comprising a plurality of second p-channel transistors that define a pitch of more than 100 nm, wherein each of the second p-channel transistors is formed in and above a second silicon containing semiconductor region and comprises a second layer of the threshold adjusting semiconductor alloy in a channel region of each of the second p-channel transistors. Furthermore, a degree of uniformity of a material composition and/or a layer thickness of the first and second layers of the threshold adjusting semiconductor alloy is approximately  $\pm 2\%$ .

#### BRIEF DESCRIPTION OF THE DRAWINGS

Further embodiments of the present disclosure are defined in the appended claims and will become more apparent with the following detailed description when taken with reference to the accompanying drawings, in which:

Figures 1A to 1D schematically illustrate cross-sectional views of a sophisticated semiconductor device including p-channel and an n-channel transistor during various manufacturing stages in providing a threshold adjusting silicon/germanium alloy according to conventional strategies;

Figures 2A to 2E schematically illustrate cross-sectional views of a semiconductor device during various manufacturing stages in selectively forming a threshold adjusting semiconductor alloy above a corresponding semiconductor region with enhanced uniformity according to illustrative embodiments;

Figure 2F schematically illustrates a cross-sectional view of the semiconductor device, in which a threshold adjusting semiconductor alloy may be formed prior to forming corresponding isolation structures according to still further illustrative embodiments;

Figures 2G to 2K schematically illustrate cross-sectional views of a semiconductor device during various manufacturing stages, in which the threshold adjusting semiconductor alloy may be formed on the basis of an implantation mask used for defining the basic doping in an active region according to illustrative embodiments;

Figure 2L schematically illustrates the semiconductor device according to an illustrative embodiment in which an isolation structure may be formed after providing the threshold adjusting semiconductor alloy; and

Figure 2M schematically illustrates a cross-sectional view of the semiconductor device in a further advanced manufacturing stage, in which a plurality of p-channel transistors may have a threshold adjusting semiconductor alloy with a reduced degree of variability with respect to material composition and/or layer thickness according to illustrative embodiments.

## DETAILED DESCRIPTION

While the present disclosure is described with reference to the embodiments as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the subject matter disclosed herein to the particular illustrative embodiments disclosed, but rather the described illustrative embodiments merely exemplify the various aspects of the present disclosure, the scope of which is defined by the appended claims.

Generally, the present disclosure provides semiconductor devices and techniques, in which sophisticated gate electrode structures may be formed in an early manufacturing stage on the basis of a high-k dielectric material and an electrode containing electrode material. In this case, the threshold voltage of one type of transistors may be adjusted by providing an appropriate semiconductor material in the channel region of the corresponding transistor, which may be accomplished on the basis of a manufacturing process with enhanced uniformity, thereby reducing threshold variability, which may be caused by even small deviations in layer thickness and/or material composition of approximately  $\pm 5\%$ . That is, as previously explained with reference to the semiconductor device 100, in conventional manufacturing strategies the provision of a silicon/germanium alloy with a variability of approximately 5% with respect to layer thickness and/or germanium concentration with respect to a corresponding target value may result in significant threshold variations, which may not be compatible with requirements of sophisticated integrated circuits, in which transistors may be formed on the basis of critical dimensions of approximately 50 nm and less. It has been recognized that pattern-related non-uniformities during the deposition process for forming the threshold adjusting semiconductor alloy may have a significant influence on the resulting threshold variability, in particular with respect to device areas including densely packed transistor element and device areas with a less critical packing density. Consequently, according to some illustrative embodiments, the critical epitaxial deposition process for forming the threshold adjusting semiconductor alloy may be performed on the basis of advanced surface conditions, i.e. with an increased

degree of uniformity with respect to deposition surface areas and non-deposition areas so that the resulting degree of uniformity of the semiconductor alloy may be enhanced. In this respect, a degree of uniformity may be understood as a deviation of approximately  $\pm 3\%$  of a given target value of the corresponding parameters. For example, the material composition of the threshold adjusting semiconductor material may vary by approximately 3% or less, i.e.  $\pm 3\%$  compared to a target value, which may be defined an average value taken from a large number of corresponding material samples. In other cases, the layer thickness may deviate by approximately  $\pm 3\%$  or less with respect to the corresponding target thickness.

The enhanced degree of uniformity may in some illustrative embodiments be accomplished by depositing the threshold adjusting semiconductor alloy in a "non-selective" manner, wherein semiconductor alloy may be deposited on active regions of any type of transistors and may subsequently be removed from one type of transistors, such as n-channel transistors on the basis of a well-controllable etch process. It should be appreciated that the term "non-selective" deposition may also refer to cases, in which nevertheless a degree of selectivity may be achieved between crystalline semiconductor surfaces and dielectric surface areas, which may be provided in the form of isolation structure, and the like. Thus, even if a deposition of semiconductor alloy may be restricted to crystalline semiconductor surfaces, significantly improved deposition conditions may be achieved across the entire semiconductor die or the substrate including a plurality of semiconductor die, since on a local scale very similar deposition conditions may be achieved as typically both types of transistors may be positioned in close proximity, irrespective of whether densely packed or non-densely packed device regions are considered. In other illustrative embodiments, the isolation structures may be formed after depositing the semiconductor alloy in a highly non-selective manner, thereby even further enhancing uniformity of the deposition conditions. In some illustrative embodiments disclosed herein, the patterning of the semiconductor alloy may be accomplished without requiring an additional lithography step, thereby providing for a highly efficient overall manufacturing flow.

With reference to figures 2A to 2N, further illustrative embodiments will now be described in more detail, wherein also reference may be made to figures 1A to 1D, if required.

Figure 2A schematically illustrates a cross-sectional view of a semiconductor device 200 comprising a substrate 201 and a silicon-containing semiconductor layer 203. Furthermore, in some illustrative embodiments, as is for instance shown in figure 2A, at least a portion of the device 200 may comprise an SOI architecture, in which a buried insulating layer 202 may be positioned between the substrate 201 and the silicon containing semiconductor layer 203. It should be appreciated, however, that the principles disclosed herein may also readily be applied to "bulk" configurations, in which the buried insulating layer 202 may be omitted, at least in some device areas of the device 200. Furthermore, an isolation structure 204, such as a shallow trench isolation, may be provided in the semiconductor layer 203, thereby defining a first active region 203A and a second active region 203B. In the embodiment shown, the active regions 203A, 203B may comprise a basic doping for defining the conductivity type of corresponding transistors still to be formed in and above the active regions 203A, 203B. In one illustrative embodiment, the active region 203A may represent an n-doped region in order to form a p-channel transistor. Similarly, the active region 203B may represent the active region of an n-channel transistor. In the following, a manufacturing sequence will be discussed, in which a threshold adjusting semiconductor alloy may selectively be formed on the active region 203A in order to provide a corresponding threshold voltage for the transistor to be formed therein. It should be appreciated, however, that also corresponding mechanisms for adjusting the threshold voltage may be applied to the transistor to be formed in the active region 203B or to both transistors, depending on the overall device and process requirements.

Furthermore, with respect to the components described so far and with respect to any manufacturing techniques for forming the same, the same criteria may apply as previously explained with reference to the semiconductor device 100. In the embodiment shown, after forming the isolation structure 204 and defining the basic doping in the active regions 203A, 203B the device 200 may be subjected to a cleaning process 200, which may be performed on the basis of well-

established wet chemical recipes. For example, any native oxides may be removed, which may have formed during the preceding manufacturing steps.

Figure 2B schematically illustrates the semiconductor device 200 during an epitaxial growth process 208, in which a semiconductor alloy 209, for instance in the form of a silicon/germanium material, and the like may be deposited on the basis of surface conditions of enhanced uniformity compared to conventional strategies. That is, in one illustrative embodiment, the epitaxial growth process 208 may be performed on the basis of well-established process parameters, such as a “selective” deposition recipe, in which material adhesion may occur substantially on exposed crystalline surface areas, such as the regions 203A, 203B, while a pronounced material deposition on dielectric surface areas, such as the isolation structure 204 may be suppressed. In this sense, the process 208 may be referred to as a selective epitaxial growth process, wherein, however, the semiconductor alloy 209 may be formed in a non-selective manner with respect to the active regions 203A, 203B. That is, contrary to the conventional approach the deposition rate and/or the presence of any precursor materials immediately at the surface areas of the regions 203A, 203B may be very similar even for the entire substrate 201, since the local neighborhood for the deposition of the active region 203A may be similar irrespective of the overall packing density in a corresponding device region, since typically one or more further transistor elements or active regions are positioned in close proximity to the region 203A, such as the region 203B, over which a deposition of the material 209 is conventionally suppressed. Consequently, the corresponding “edge conditions” may be similar for any of the active regions corresponding to the transistor type, for which the deposition of the material 209 is required. Consequently, a thickness 209T of the material 209 may have a high degree of uniformity and may vary by approximately  $\pm 3\%$  or less compared to the corresponding representative average value taken across the entire substrate 201. In other illustrative embodiments, the thickness variability may even be approximately 2% and less. For instance, the semiconductor alloy 209 may represent a silicon/germanium alloy having a thickness of approximately 10 nm and less, for instance 9 nm while a germanium concentration may be approximately 25 at. % and less, depending on the diode band gap off-set to be provided in combination with a corresponding metal-containing electrode material. Thus, due to the

enhanced uniformity of the gas flow during the deposition process 208, also the variability of the material composition, may be enhanced, i.e. the fraction of the various components, such as silicon, germanium and the like, depending on the type of semiconductor alloy 209 used, may be reduced and may be within approximately  $\pm 3\%$  or less relative to a representative mean value or target value.

Figure 2C schematically illustrates a cross-sectional view of the semiconductor device 200 in a further advanced manufacturing stage. As illustrated, a mask layer 205 is formed on the semiconductor layer 209 and may be comprised of any appropriate material, such as silicon dioxide, silicon nitride, and the like. In some illustrative embodiments, the mask layer 205 may be formed of an oxide of the material 209 and hence corresponding components may also be deposited in the mask layer 205. The layer 205 may be formed on the basis of well established deposition techniques, such as plasma-assisted CVD (chemical vapor deposition) thermally activated CVD and the like. In other cases, an oxidation process may be performed, for instance a thermal oxidation, a plasma-assisted oxidation, a wet chemical oxidation, and the like, wherein a high degree of controllability of the corresponding oxidation process may enable a precise control of material consumption of the initial layer 209. That is, due to the well known and stable oxidation rates for a plurality of oxidation recipes, the degree of material consumption may be determined in advance and may be taken into consideration upon depositing the layer 209 with an appropriate initial thickness. Due to the high degree of uniformity of corresponding oxidation processes, the oxidation of the mask layer 205 on the basis of these oxidation processes may substantially not contribute to additional overall process non-uniformity.

Figure 2D schematically illustrates the semiconductor device 200 in a manufacturing stage, in which a mask 206 may be provided so as to cover the active region 203A and the corresponding material layers 209 and 205 formed thereon, while exposing the active region 203B and the corresponding materials formed thereon to an etch ambient 207 that is designed so as to remove material of at least the mask layer 205. In the embodiment shown, the etch process 207 may be performed so as to selectively remove the material 205 with respect to the material 209, which may be accomplished, for instance on the basis of

hydrofluoric acid, when the mask layer 205 is comprised of silicon dioxide. In other cases, any other selective etch recipe may be used in order to selectively remove the exposed portion of the layer 205.

Figure 2E schematically illustrates the semiconductor device 200 when exposed to a further etch ambient 212, which may be established on the basis of an appropriate etch chemistry for removing material of the layer 209 selectively with respect to at least the mask layer 205. In one illustrative embodiment, the etch process 212 may be performed as a wet chemical etch process on the basis of a chemical agent that enables the removal of the material 209, such as a silicon/germanium alloy selectively to the mask layer 205 that may be comprised of silicon dioxide, silicon nitride and the like. During the etch process 212 process parameters, such as concentration of chemical agents, process time and the like may appropriately be selected so as to not unduly consume material of the action region 203B. In one illustrative embodiment, the etch process 212 may be performed on the basis of tetramethyl ammonium hydroxide (TMAH), which is a well-known chemical for removing resist material, which, however, may also efficiently remove silicon-based materials and provided in higher concentrations and at elevated temperatures. Furthermore, TMAH may also exhibit a pronounced selectivity with respect to silicon dioxide and silicon nitride material. Consequently, the layer 209 may be removed with a high degree of controllability without compromising integrity of the material layer 209 above the active region 203A, even if the resist mask 206 (cf. figure 2D) may be removed during the etch process 212. In other cases, the resist mask may be removed prior to initiating the etch process 212 in order to further enhance overall process uniformity. Consequently, the overall integrity of the material 209 during the patterning sequence for exposing the action region 203B may be maintained on the basis of the mask layer 205. Thereafter, the mask layer 205 may be removed from above the active region 203A, wherein similar process techniques may be applied, as previously explained with reference to the semiconductor device 100 when referring to the etch process 110 (cf. figure 1C). After exposing the semiconductor alloy 209, the further processing may be continued on the basis of well-established process techniques for forming sophisticated gate electrode structures as previously explained.

Figure 2F schematically illustrates a semiconductor device 200 according to further illustrative embodiments, in which the basic doping for the regions 203A, 203B may have been established prior to forming an isolation structure. Furthermore, the device 200 may be exposed to the epitaxial growth process 208 in order to form the semiconductor alloy 209 on the basis of any appropriate deposition recipe, wherein a further enhanced degree of deposition conditions may be achieved due to the missing isolation structures. Consequently, also in this case the material 209 may be provided with a high degree of uniformity with respect to material composition and layer thickness, as previously explained. After forming the semiconductor alloy 209, the further processing may be continued by patterning the layer 209 and forming isolation structures, wherein appropriate manufacturing strategies for maintaining enhanced process uniformity may be described later on with reference to figure 2L.

With reference to figures 2G to 2J, further illustrative embodiments will now be described, in which the patterning of the threshold adjusting semiconductor alloy may be accomplished on the basis of an implantation mask that is used for defining the basic dopant concentration in one of the active regions.

Figure 2G schematically illustrates the semiconductor device 200 in a manufacturing stage, in which in one illustrative embodiment, the isolation structure 204 may be formed so as to separate the active regions 203A, 203B, while, however, a corresponding basic doping level may not be established yet. In other illustrative embodiments, the isolation structure 204 may not be formed in this manufacturing stage, as indicated by the dashed lines, and may be formed in a later manufacturing stage, as previously explained with reference to figure 2F and as will also be explained in more detail with reference to figure 2L. Moreover, device 200 is exposed to the deposition ambient of the process 208 so as to form the semiconductor alloy 209 with superior uniformity, as is previously explained. It should be appreciated that the semiconductor alloy 209 may not be formed above the isolation structure 204, if already present in this manufacturing stage.

Figure 2H schematically illustrates the semiconductor device 200 in a further advanced manufacturing stage. As illustrated, the mask layer 205 may be

formed on the semiconductor alloy 209, wherein the mask layer 205 may be comprised of any appropriate material, as previously explained. Furthermore, an implantation mask 214A may be provided in the form of a resist mask so as to expose the active region 203A, i.e. the mask layer 205 formed thereon, while covering the active region 203B. Moreover, the device 200 is subjected to an ion implantation process 213A designed to introduce a dopant species into the active region 203A, which may be accomplished on the basis of well-established implantation recipes, wherein, however, corresponding process parameters, such as implantation energy, and the like may appropriately be adjusted with respect to the presence of the semiconductor alloy 209 and the mask layer 205. However, typically both material layers may be provided with a moderately small layer thickness so that a corresponding adaptation may readily be accomplished on the basis of conventional strategies.

Figure 2I schematically illustrates the semiconductor device 200 in a further advanced manufacturing stage, in which after removal of the implantation mask 214A (cf. figure 2H) a further implantation mask 214B may expose the active region 203B, i.e. the material layers 205, 209 formed thereon, while covering the corresponding material layers formed above the active region 203A. Furthermore, an implantation process 213B may be performed so as to introduce the dopant species into the active region 203B in accordance with the overall device requirement.

Figure 2J schematically illustrates the semiconductor device 200 when exposed to the etch ambient 207, for instance provided in the form of a wet chemical etch ambient, in which the mask layer 205 may be patterned on the basis of the implantation mask 214B. Consequently, any additional lithography steps for patterning the mask layer 205 may be avoided, thereby contributing to a very efficient overall process flow.

Figure 2K schematically illustrates the semiconductor device 200 when exposed to the etch ambient 212 for removing the exposed portion of the semiconductor alloy 209 from above the active region 203B on the basis of the mask layer 205. With respect to any process recipes for the etch process 212, the same criteria may apply, as previously explained. Also in this case, the semiconductor alloy

209 may be provided with a high degree of uniformity on the basis of the highly efficient manufacturing flow without requiring any additional lithography steps. After the etch process 212, the further processing may be continued, as previously described, i.e. the mask layer 205 may be removed and the further processing may be continued by forming sophisticated gate electrode structures as is also previously explained with reference to the transistor elements 150A, 150B (cf. figure 1D).

Figure 2L schematically illustrates the semiconductor device 200 according to further illustrative embodiments, in which the isolation structure 204 after patterning the semiconductor alloy 209. For example, in the process sequence described above with reference to figures 2G to 2K, the semiconductor alloy 209 may be patterned on the basis of an implantation mask prior to forming the isolation structure, while in other cases, the semiconductor alloy 209 may be patterned after having formed the basic dopant concentration in the regions 203A, 203B, as is described with reference to figure 2F. In any of these cases, the further processing may be continued on the basis of the remaining portions of the semiconductor alloy 209 and the mask layer 205, which may be maintained so as to enhance integrity of the material 209 so as to reduce any process non-uniformities that may exist during the manufacturing sequence for providing the isolation structure 204. In one illustrative embodiment, as illustrated in figure 2L a stop layer 215, i.e. an etch stop material and/or a CMP (chemical mechanical polishing) stop material may be formed, such as a silicon nitride material, which may be deposited on the basis of any appropriate deposition recipe. Depending on the overall process strategy, the surface topography of the device 200 may be planarized, if required, while in other cases, the further processing may be continued on the basis of the layer 215 without further surface treatment. Consequently, the layer 215 may be used as a platform for the further processing, i.e. a sequence for defining an etch mask and etching a trench into the semiconductor layer 203 and filling the same on the basis of well-established deposition recipes. Thereafter, any excess material may be removed, for instance by CMP, wherein the layer 215 may act as a stop layer. Thereafter, residues of the layers 215 may be removed, wherein the mask layer 205 may still maintain integrity of the semiconductor alloy 209. Thereafter, the mask layer 205 may be removed, for instance on the basis of any process techniques, as

previously described, and thereafter the further processing may be continued with forming sophisticated gate electrode structures.

Figure 2M schematically illustrates the semiconductor device 200 in an advanced manufacturing stage. As illustrated, the device 200 may comprise a first device region 270A including a plurality of first transistors 250A, such as p-channel transistors, and one or more n-channel transistors, 250B. Furthermore, a second device region 270B may be provided, in which a plurality of third transistors 250C such as p-channel transistors, may be formed, possibly in combination with one or more n-channel transistors (not shown). In the embodiment shown, the transistors 250A, 250C may represent sophisticated transistor elements having formed therein the threshold adjusting semiconductor alloy 209 in order to provide for the desired transistor characteristics, as previously discussed. On the other hand, the transistor 250B may represent a transistor, for which a corresponding threshold adjustment on the basis of semiconductor alloy may not be required. The transistors 250A, 250B and 250C may each comprise a gate electrode structure 251, which may in turn comprise a gate insulation layer 251A formed on the basis of a high-k dielectric material, as previously explained. Furthermore, a metal-containing electrode material 251A, such as aluminum oxide, titanium nitride and the like may be formed on the corresponding gate insulation layers 251B, wherein, if required, an additional electrode material, such as a polysilicon material, and the like 251C may be formed on the electrode material 251A. Furthermore sophisticated drain and source regions 254 may be provided in order to obtain the desired overall transistor characteristics, as also previously discussed.

The transistors 250A, 250B and 250C may be formed on the basis of any appropriate manufacturing strategy, for instance as previously discussed, wherein the enhanced uniformity of the semiconductor alloy 209 in each of the transistors 250A, 250C may provide for superior uniformity of the resulting transistor characteristics. For example, in the device 270A, a distance or pitch 250P between adjacent transistors 250A may correspond to a minimum critical distance in order to obtain a desired high packing density. For example, in sophisticated application, the pitch 250P may be approximately 100 nm and less, while a gate length, i.e. in figure 2M the horizontal extension of the electrode

material 251A may be approximately 50 nm and less. On the other hand, a corresponding distance or pitch between adjacent transistors 250C may significantly be higher, depending on the overall device requirements, while nevertheless the enhanced degree of uniformity of the corresponding semiconductor alloys 209 may provide a reduced transistor variability irrespective of the corresponding distances 250P, 250Q. As previously explained, this may be accomplished on the basis of enhanced process conditions during the deposition of the semiconductor alloy 209, since in a local sense, a very similar neighborhood for each of the transistors 250C, 250A may be accomplished. For example, the transistor 250B may represent a "next" neighbor for respective ones of the transistor 250A, 250C, thereby providing for a similar local neighborhood during the deposition process for forming the material 209, as previously explained.

As a result, the present disclosure provides semiconductor devices and manufacturing techniques, in which deposition-related non-uniformities for forming a threshold adjusting semiconductor alloy may be reduced by depositing the material on active regions for each type of transistor and subsequently patterning the semiconductor alloy on the basis of a highly controllable patterning sequence. Consequently, sophisticated gate electrode structures including a high-k dielectric material and a metal-containing electrode material may be formed in an early manufacturing stage, i.e. prior to forming drain and source regions, on the basis of a threshold adjusting semiconductor alloy, such as a silicon/germanium material, wherein the enhanced uniformity during the selective formation of the threshold adjusting material may result in a reduced threshold variability, even if extremely scaled semiconductor devices are considered.

Further modifications and variations of the present disclosure will be apparent to those skilled in the art in view of this description. Accordingly, this description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the teaching provided herein. It is to be understood that the forms of the subject matter shown and described herein are to be taken as the presently preferred embodiments.

## CLAIMS

## 1. A method comprising:

forming a layer of a silicon containing semiconductor alloy on a first silicon containing crystalline semiconductor region and a second silicon containing crystalline semiconductor region;

removing said layer of silicon containing semiconductor alloy selectively from said second silicon containing crystalline semiconductor region;

forming a first gate electrode structure of a first transistor on said layer of a silicon containing semiconductor alloy, said first gate electrode structure comprising a high-k dielectric gate insulation layer and a metal containing gate electrode material formed on said high-k dielectric gate insulation layer; and

forming a second gate electrode structure of a second transistor above said second silicon containing crystalline semiconductor region, said second gate electrode structure comprising a high-k dielectric gate insulation layer and a metal containing gate electrode material formed on said high-k dielectric gate insulation layer of said second gate electrode structure.

2. The method of claim 1, wherein removing said layer of silicon containing semiconductor alloy comprises forming a hardmask layer selectively above said first silicon containing crystalline semiconductor region and performing an etch process on the basis of said hardmask layer.
3. The method of claim 2, wherein performing said etch process comprises applying a wet chemical etch recipe.
4. The method of claim 3, wherein performing said etch process comprises applying a wet chemical etch recipe on the basis of tetra methyl ammonia hydroxide (TMAH).

5. The method of claim 1, further comprising performing a further etch process so as to remove said hardmask layer.
6. The method of claim 1, wherein forming said layer of silicon containing semiconductor alloy comprises performing a selective epitaxial growth process so as to suppress material deposition on an isolation structure that laterally separates said first and second silicon containing crystalline semiconductor regions.
7. The method of claim 1, further comprising forming an isolation structure prior to forming said layer of silicon containing semiconductor alloy, wherein said isolation structure laterally separates said first and second silicon containing crystalline semiconductor regions.
8. The method of claim 1, further comprising forming an isolation structure after forming said layer of silicon containing semiconductor alloy, wherein said isolation structure laterally separates said first and second silicon containing crystalline semiconductor regions.
9. The method of claim 1, further comprising introducing a first dopant species in said first silicon containing crystalline semiconductor region and a second dopant species in said second silicon containing crystalline semiconductor region after forming said layer of silicon containing semiconductor alloy.
10. The method of claim 9, further comprising forming a mask layer above said layer of silicon containing semiconductor alloy prior to introducing said first and second dopant species.
11. The method of claim 10, further comprising removing said mask layer from above said second silicon containing crystalline semiconductor region on the basis of an implantation mask used for introducing said first dopant species.

12. The method of claim 11, further comprising forming an isolation structure laterally between said first and second silicon containing crystalline semiconductor regions prior to forming said layer of silicon containing semiconductor alloy.
13. The method of claim 11, further comprising forming an isolation structure laterally between said first and second silicon containing crystalline semiconductor regions after forming said layer of silicon containing semiconductor alloy.
14. The method of claim 1, wherein said semiconductor alloy comprises a silicon/germanium alloy.
15. A method comprising:
  - forming a threshold adjusting semiconductor material on first and second silicon containing semiconductor regions;
  - introducing a dopant species in said second silicon containing semiconductor region by using an implantation mask covering said first silicon containing semiconductor region;
  - removing said threshold adjusting semiconductor material selectively from said second silicon containing semiconductor region on the basis of said implantation mask; and
  - forming a first gate electrode structure of a first transistor on said threshold adjusting semiconductor material and a second gate electrode structure of a second transistor on said second silicon containing semiconductor region, said first and second gate electrode structures comprising a high-k dielectric material and a metal containing electrode material formed on said high-k dielectric material.
16. The method of claim 15, wherein removing said threshold adjusting semiconductor material selectively from said second silicon containing

semiconductor region comprises forming a mask layer, patterning said mask layer by using said implantation mask and etching said threshold adjusting semiconductor material by using said patterned mask layer as an etch mask.

17. The method of claim 16, wherein etching said threshold adjusting material comprises performing a wet chemical etch process.
18. The method of claim 17, wherein said wet chemical etch process is performed on the basis of tetra methyl ammonia hydroxide (TMAH).
19. The method of claim 15, further comprising forming an isolation structure laterally between said first and second silicon containing semiconductor regions prior to forming said threshold adjusting semiconductor material.
20. The method of claim 15, further comprising forming an isolation structure laterally between said first and second silicon containing semiconductor regions after forming said threshold adjusting semiconductor material.
21. The method of claim 15, wherein said threshold adjusting semiconductor material comprises a silicon/germanium alloy.
22. A semiconductor device comprising:

a first device region comprising a plurality of densely packed first p-channel transistors defining a pitch of approximately 100 nanometer or less, each of said first p-channel transistors being formed in and above a first silicon containing semiconductor region and comprising a first layer of a threshold adjusting semiconductor alloy in a channel region of each of said first p-channel transistors;

a second device region comprising a plurality of second p-channel transistors defining a pitch of more than 100 nanometer, each of said second p-channel transistors being formed in and above a second silicon containing semiconductor region and comprising a second layer of said

threshold adjusting semiconductor alloy in a channel region of each of said second p-channel transistors, wherein a degree of uniformity of at least one a material composition and a layer thickness of said first and second layers of said threshold adjusting semiconductor alloy is approximately plus/minus 2 percent.

23. The semiconductor device of claim 22, wherein said gate electrode structures of said first and second p-channel transistors comprise a high-k dielectric material formed above said first and second layers of threshold adjusting semiconductor material, respectively, and a metal containing electrode material formed on said high-k dielectric material.
24. The semiconductor device of claim 22, wherein a target thickness of said layer of threshold adjusting semiconductor material is approximately 10 nanometer or less.
25. The semiconductor device of claim 24, wherein said threshold adjusting semiconductor alloy comprises a silicon/germanium alloy with a germanium concentration of approximately 20 atomic percent or more.

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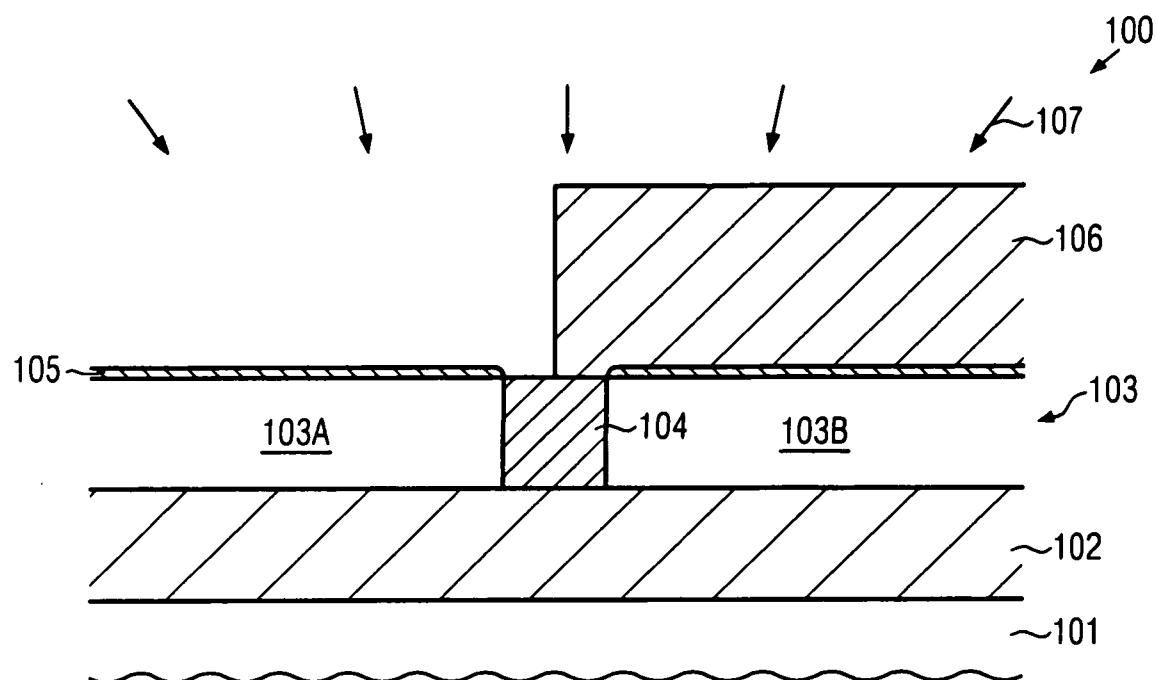


FIG. 1a  
(prior art)

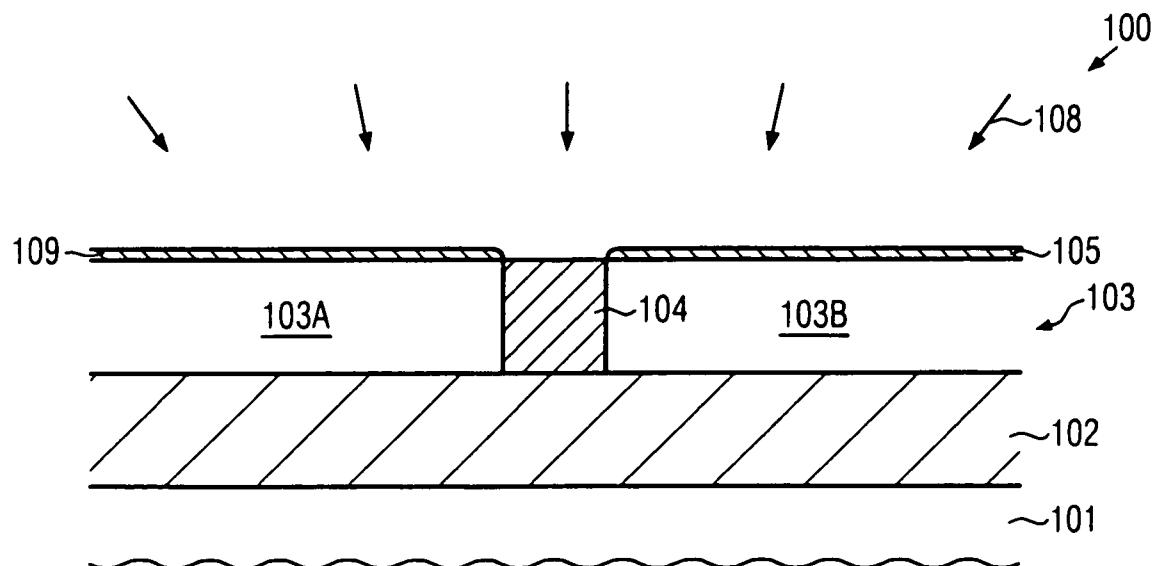


FIG. 1b  
(prior art)

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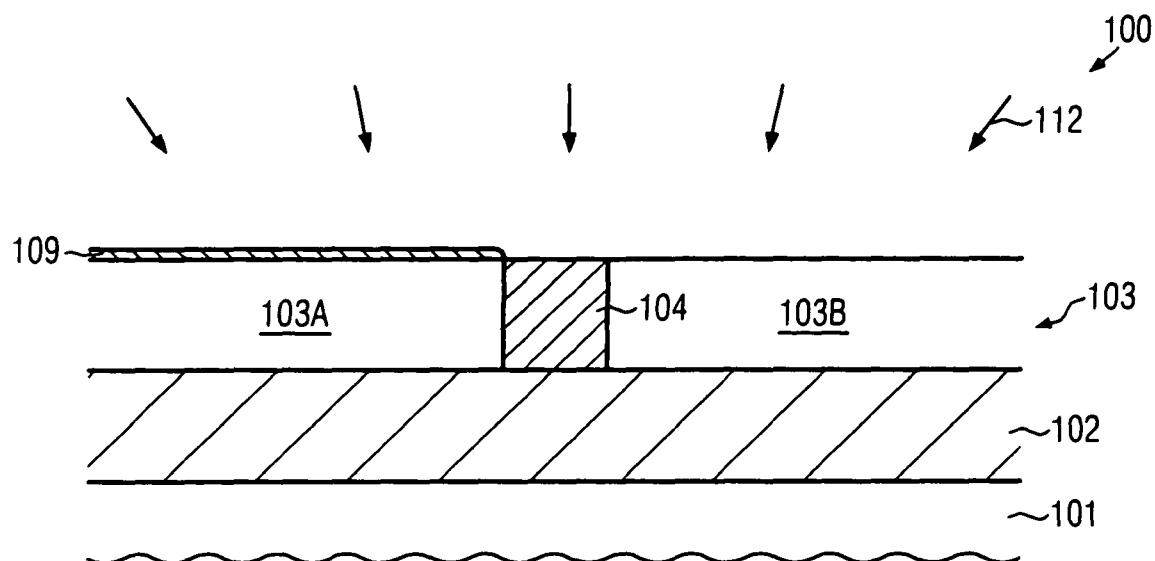


FIG. 1c  
(prior art)

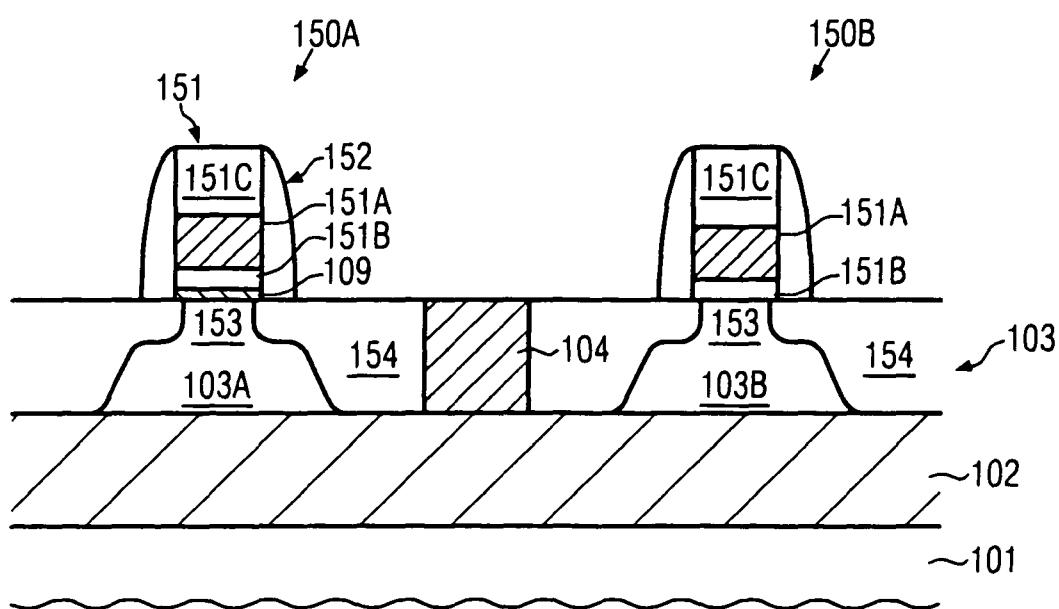


FIG. 1d  
(prior art)

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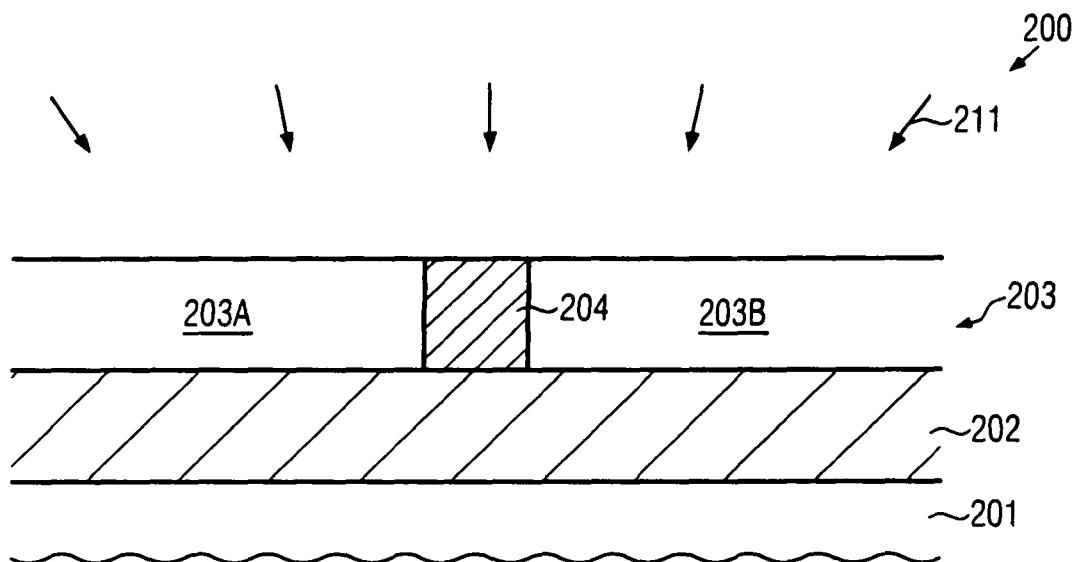


FIG. 2a

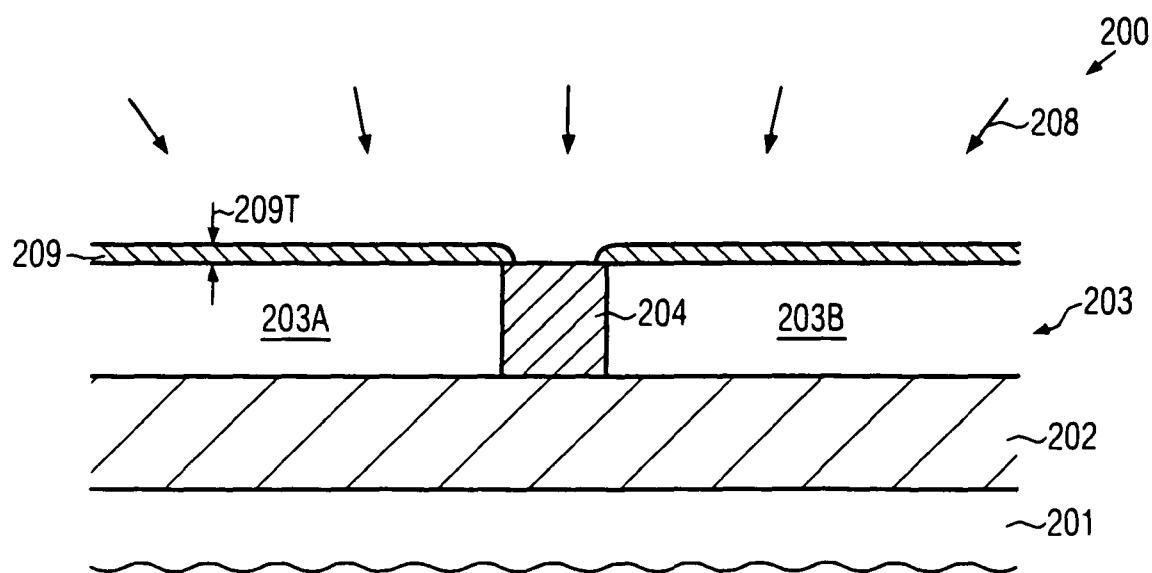


FIG. 2b

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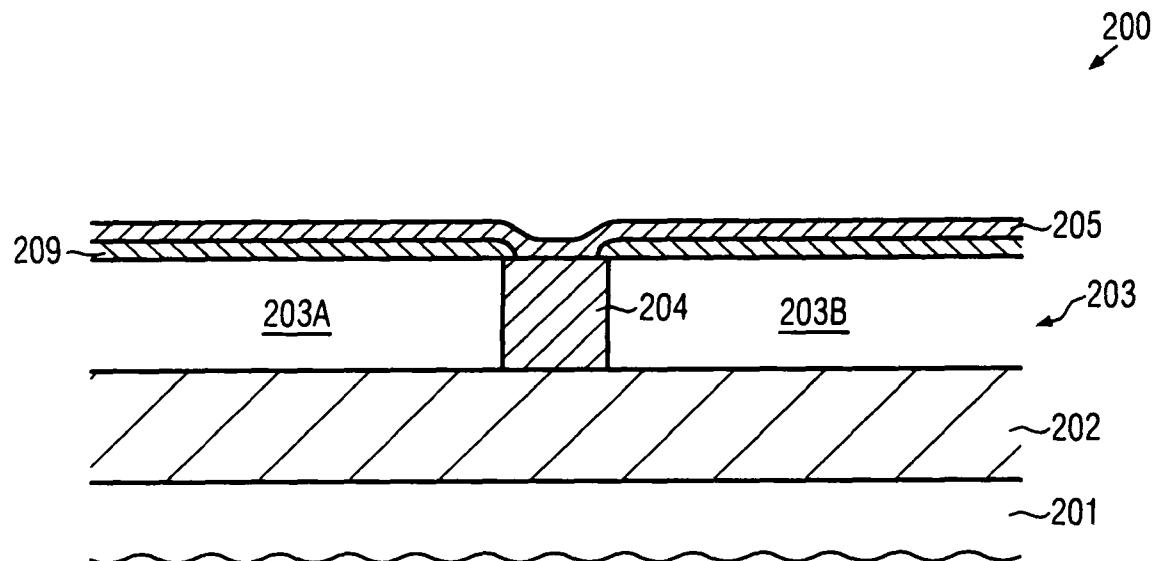


FIG. 2c

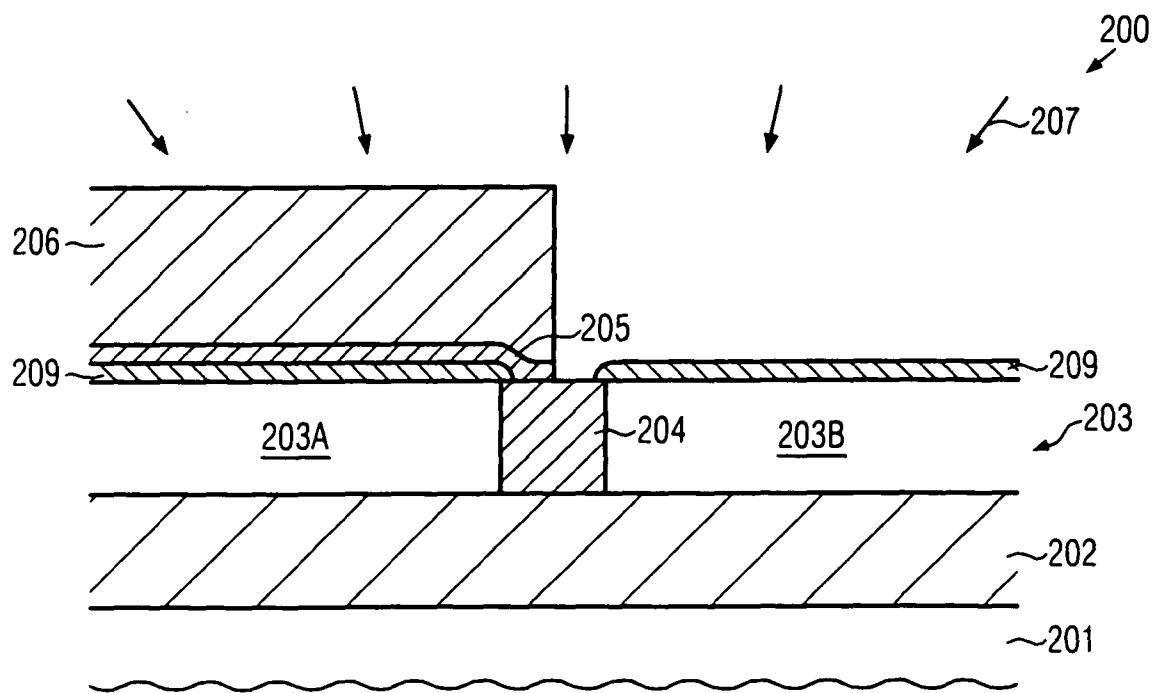


FIG. 2d

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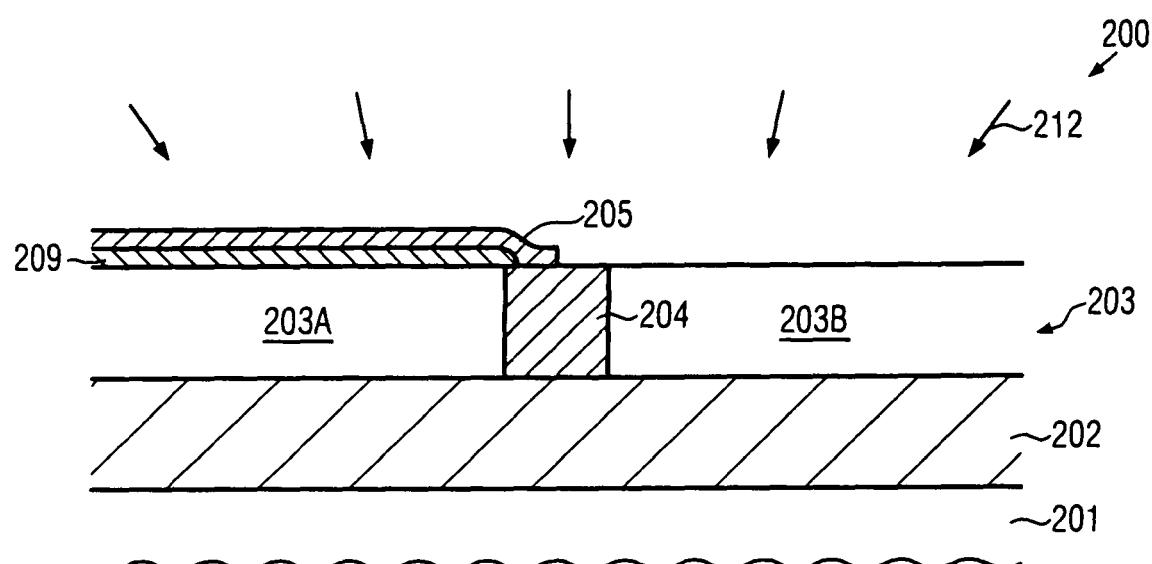


FIG. 2e

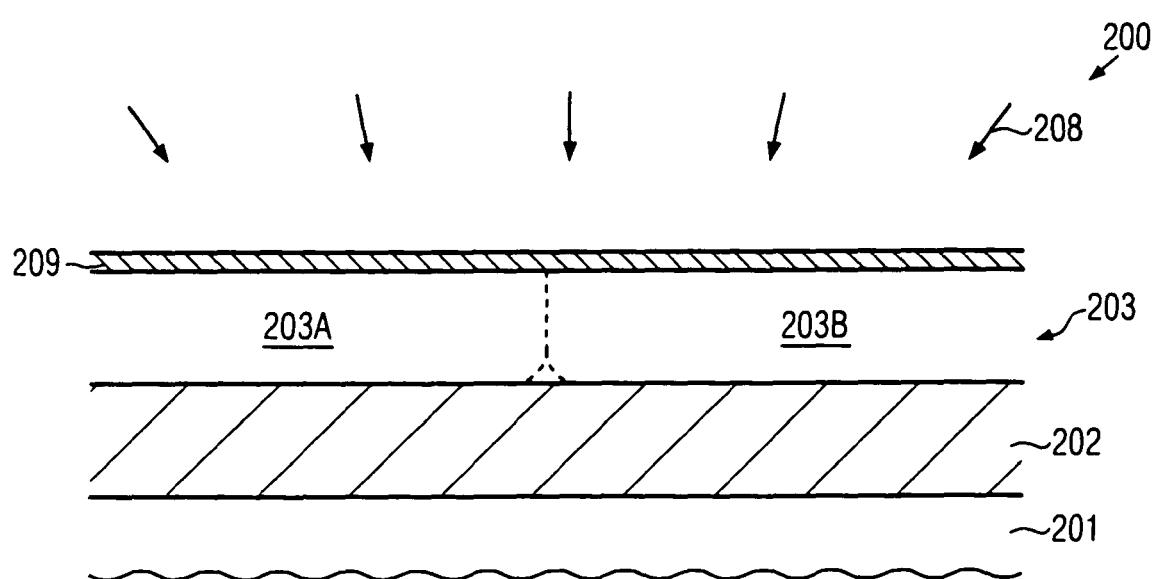


FIG. 2f

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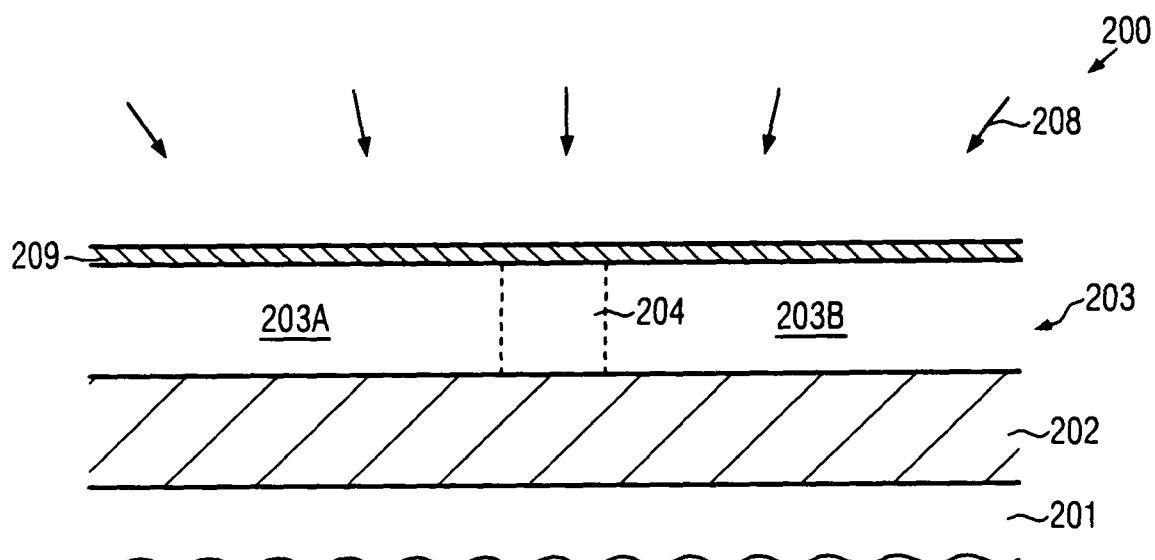


FIG. 2g

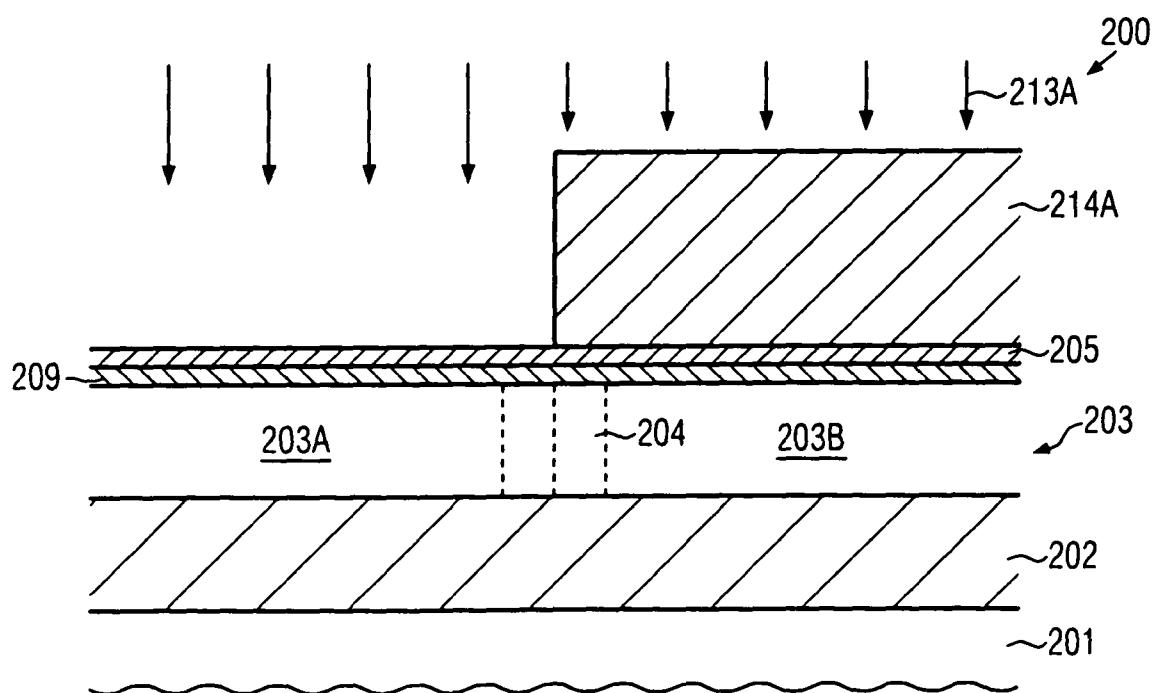


FIG. 2h

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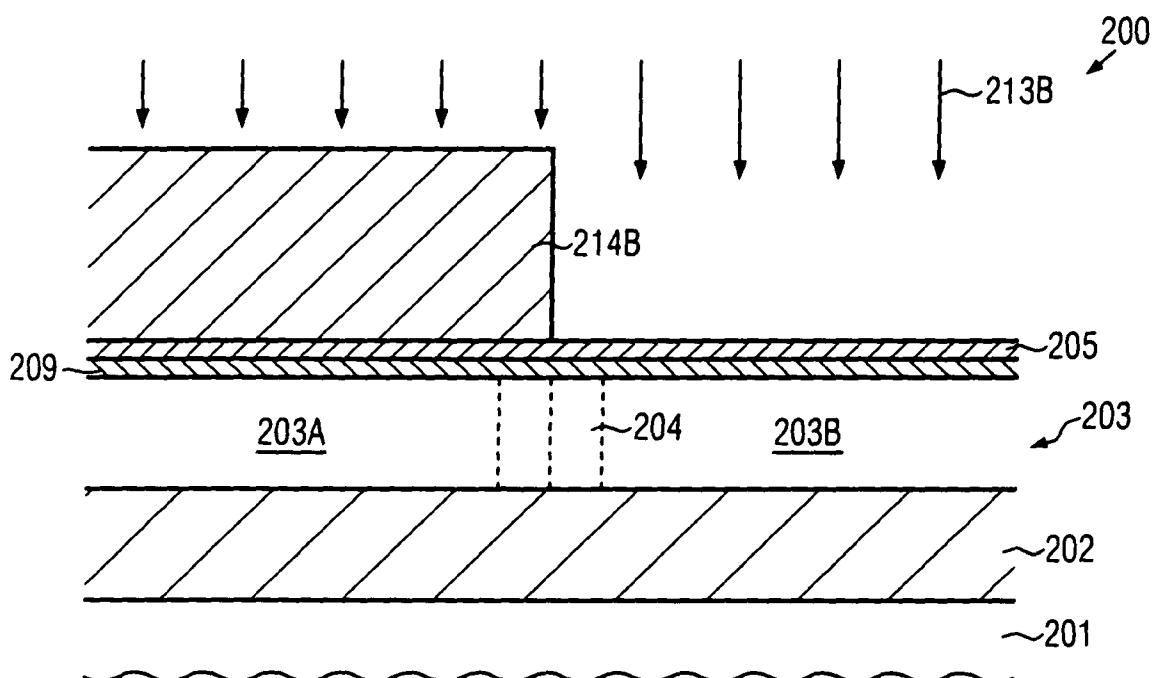


FIG. 2i

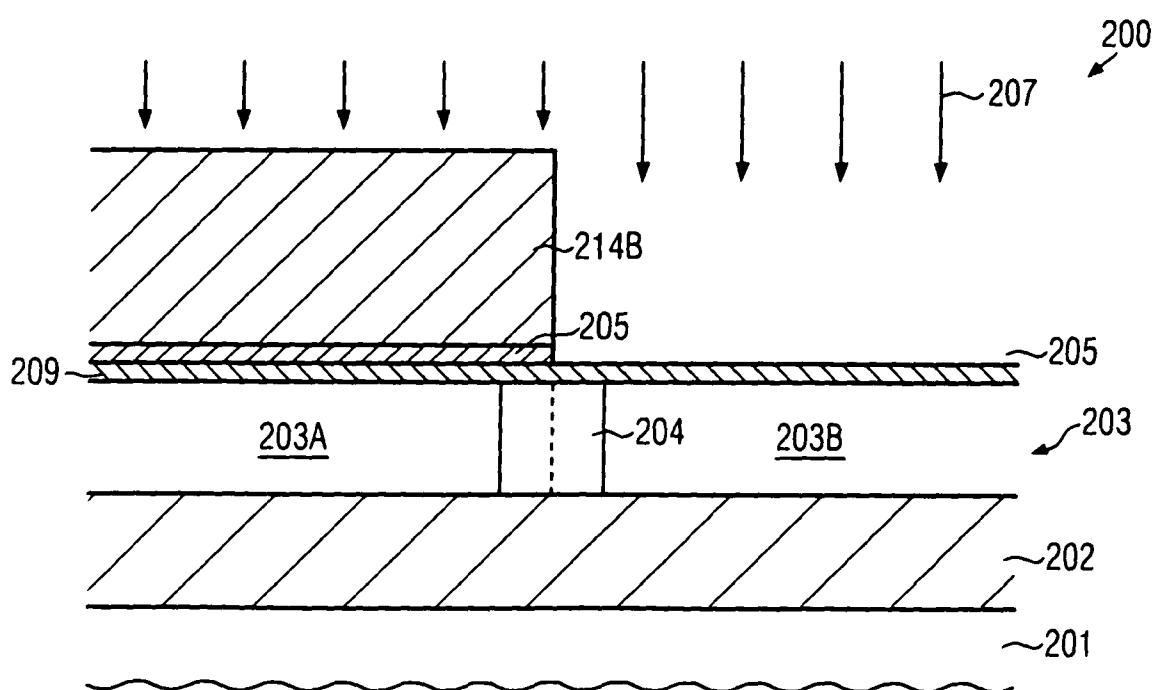


FIG. 2j

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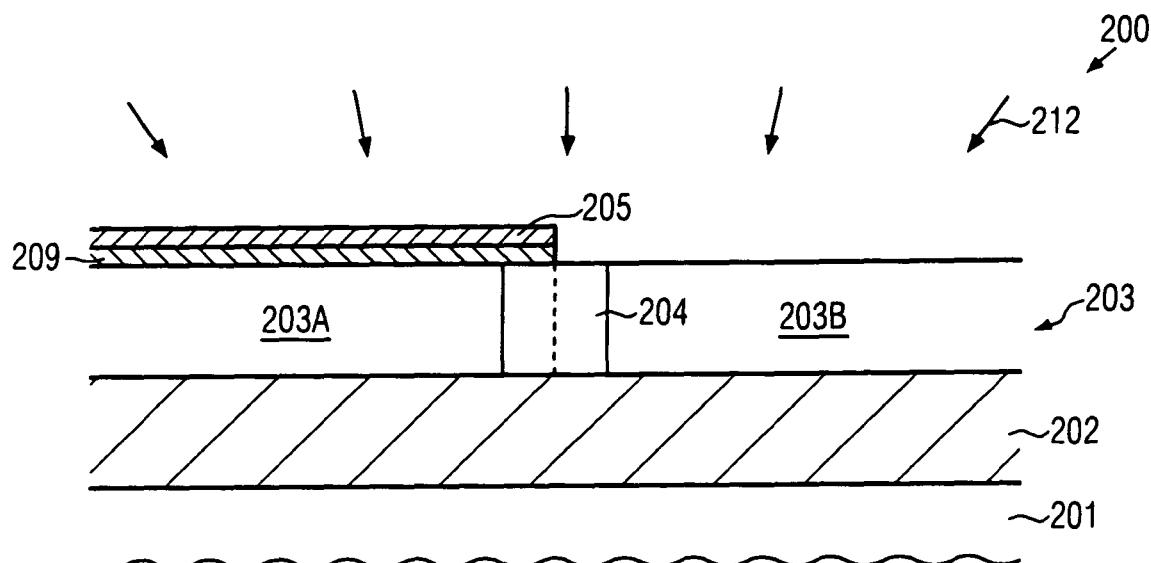


FIG. 2k

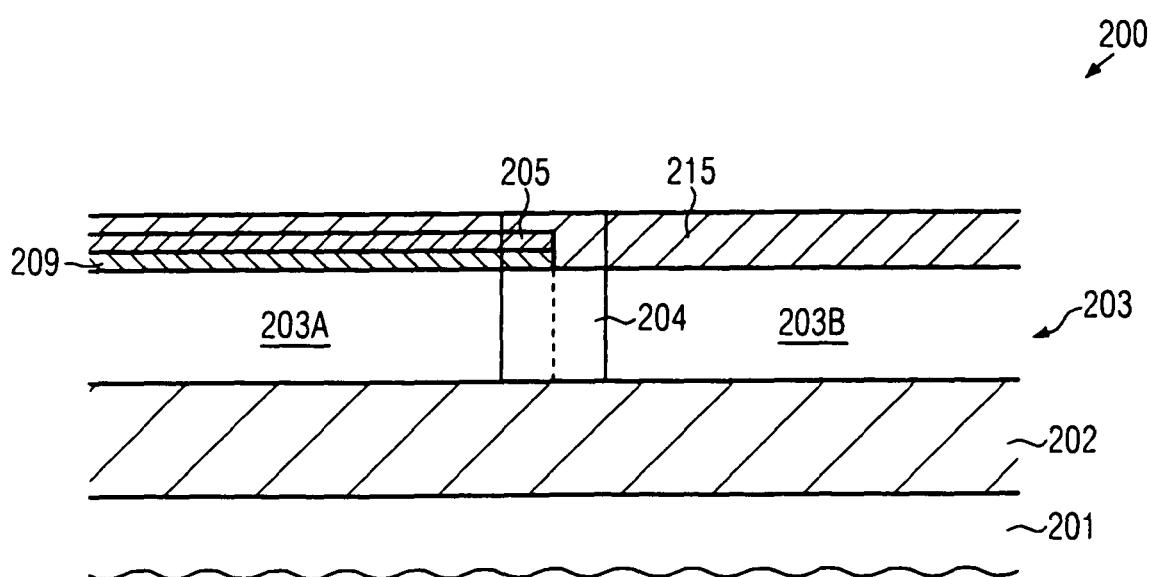


FIG. 2l

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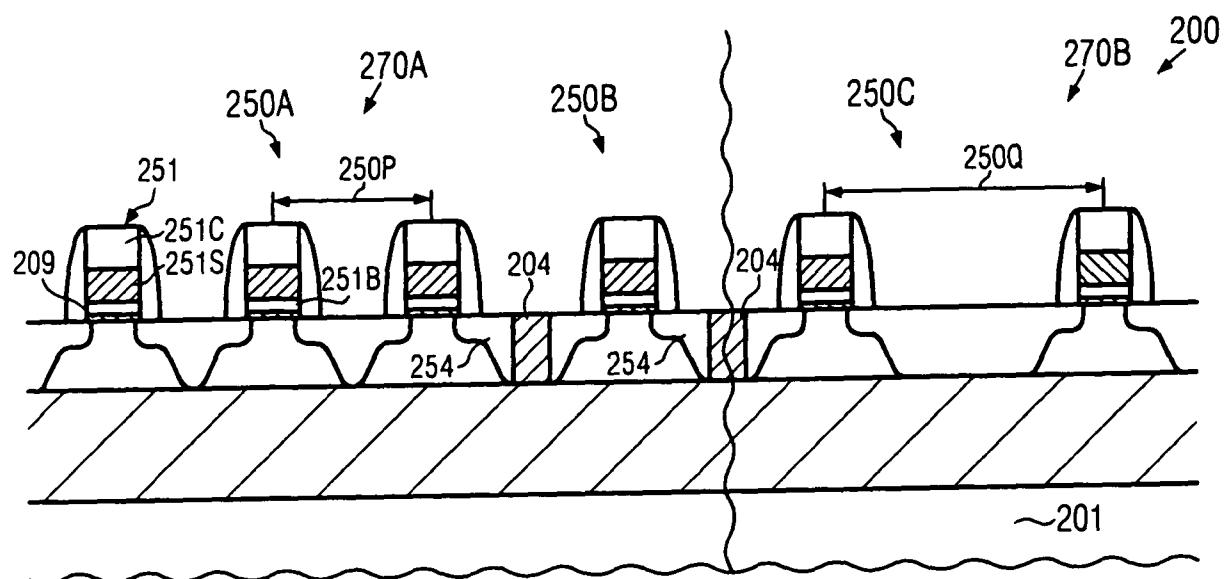


FIG. 2m

# INTERNATIONAL SEARCH REPORT

International application No  
PCT/EP2009/009307

**A. CLASSIFICATION OF SUBJECT MATTER**  
INV. H01L21/8234 H01L21/8238

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EP0-Internal, WPI Data, INSPEC, IBM-TDB

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/224451 A1 (CHEN JIA [US] ET AL) 11 November 2004 (2004-11-11) abstract; figure 1 -----	1-5, 9-14
Y	EP 1 298 722 A2 (TEXAS INSTRUMENTS INC [US]) 2 April 2003 (2003-04-02) abstract; figure 1 paragraph [0014] - paragraph [0029] -----	6-8
X	JP 2006 108251 A (ROHM CO LTD) 20 April 2006 (2006-04-20) abstract; figures -----	1-5, 9-14
Y	JP 2006 108251 A (ROHM CO LTD) 20 April 2006 (2006-04-20) abstract; figures -----	6-8
Y	US 2003/203560 A1 (RYU HYUK-JU [KR] ET AL) 30 October 2003 (2003-10-30) abstract; figures -----	15-21
Y	US 2003/203560 A1 (RYU HYUK-JU [KR] ET AL) 30 October 2003 (2003-10-30) abstract; figures -----	15-21
		-/-

Further documents are listed in the continuation of Box C.

See patent family annex.

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- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- "&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 March 2010	01/04/2010
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer  Wirner, Christoph

## INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/009307

## C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 7 132 322 B1 (GREENE BRIAN J [US] ET AL GREENE BRIAN JOSEPH [US] ET AL) 7 November 2006 (2006-11-07) abstract; figures -----	15-21
Y	JP 2003 332458 A (FUJITSU LTD) 21 November 2003 (2003-11-21) abstract; figures -----	22-25
Y	US 2008/113186 A1 (KOUVETAKIS JOHN [US] ET AL) 15 May 2008 (2008-05-15) abstract; figures -----	22-25
Y	US 2008/116487 A1 (LEE BYEONG-CHAN [KR] ET AL SOO ET AL) 22 May 2008 (2008-05-22) abstract; figures -----	6-8
A	US 2006/068557 A1 (OCHIMIZU HIROSATO [JP] ET AL) 30 March 2006 (2006-03-30) abstract; figure 1 -----	1-25
A	JP 2004 006959 A (MATSUSHITA ELECTRIC IND CO LTD) 8 January 2004 (2004-01-08) abstract; figures -----	1-25
A	"PLANAR FULLY-INTEGRATED BULK/SOI SIGE CMOS FABRICATION PROCESS" IBM TECHNICAL DISCLOSURE BULLETIN, INTERNATIONAL BUSINESS MACHINES CORP. (THORNWOOD), US, vol. 34, no. 10A, 1 March 1992 (1992-03-01), pages 128-129, XP000302251 ISSN: 0018-8689 abstract; figures -----	1-25
X,P	US 2009/152637 A1 (CARTER RICK [US] ET AL) 18 June 2009 (2009-06-18) abstract; figures -----	1,15
X,P	US 2009/108294 A1 (CHOI CHANGHWAN [US] ET AL) 30 April 2009 (2009-04-30) abstract; figures -----	1,15

**INTERNATIONAL SEARCH REPORT**

Information on patent family members

 International application No  
**PCT/EP2009/009307**

Patent document cited in search report	Publication date	Patent family member(s)			Publication date
US 2004224451	A1 11-11-2004	CN 1551333 A	JP 2004336056 A	TW 272669 B	01-12-2004 25-11-2004 01-02-2007
EP 1298722	A2 02-04-2003	JP 2003179155 A			27-06-2003
JP 2006108251	A 20-04-2006	NONE			
US 2003203560	A1 30-10-2003	CN 1453850 A	DE 10323013 A1	JP 4313065 B2	05-11-2003 20-11-2003 12-08-2009
		JP 2003318283 A	KR 20030084144 A		07-11-2003 01-11-2003
US 7132322	B1 07-11-2006	NONE			
JP 2003332458	A 21-11-2003	NONE			
US 2008113186	A1 15-05-2008	JP 2008513979 T	KR 20090053866 A		01-05-2008 27-05-2009
US 2008116487	A1 22-05-2008	NONE			
US 2006068557	A1 30-03-2006	CN 1788354 A	WO 2005013375 A1	JP 4322255 B2	14-06-2006 10-02-2005 26-08-2009
		US 2009039391 A1			12-02-2009
JP 2004006959	A 08-01-2004	NONE			
US 2009152637	A1 18-06-2009	CN 101504933 A			12-08-2009
US 2009108294	A1 30-04-2009	NONE			