A reference bias regulator utilizes both NPN and PNP transistors supplying a reference bias for constant current sources to be used as load devices in low voltage integrated circuits thus eliminating the necessity to use large ohmic value external resistors. The regulator effectively maintains a current independent of source and load variation.

8 Claims, 8 Drawing Figures
REGULATOR WITH BIPOLAR TRANSISTORS

This is a continuation of application Ser. No. 263,819, filed June 19, 1972, and now abandoned.

Low powered electronically controlled timekeeping devices have been described in the literature. For example, one such device is described in U.S. Pat. No. 3,560,998 and another in U.S. Pat. No. 3,505,804.

There have been proposals which suggest utilizing CMOS (complementary metal oxide semiconductor) technology in combination with liquid crystal displays primarily due to the power savings capability of such a configuration. Certain advantages, however, may be obtained utilizing bipolar technology for implementing the circuit logic of electronic watches; however, readily available battery sources provide on the order of one volt and it is exceedingly difficult to implement logic with bipolar integrated circuits using such voltage levels. Additional limitations are imposed due to integration requirements, these primarily being that it is difficult to obtain large resistances in integrated circuit format.


Briefly, in accordance with that invention, a timekeeping device is provided which includes a battery operated bipolar integrated circuit for regulating display of the time, including means for displaying and independently setting the calendar date. A crystal controlled oscillator generates a master frequency. This frequency is applied to a frequency divider comprising a ripple counter of toggle flip-flops effective to produce a one hertz system clock signal. The toggle flip-flops respectively comprise bipolar transistors in a circuit configuration effective to operate from voltage sources which provide on the order of one volt. The system clock is applied to a series of counters and decoder logic to effect generation of signals to drive circuitry for application to a liquid crystal display. Circuit means are provided for producing current sources as load devices in these circuits in lieu of high value external resistors. The current sources receive a regulated reference bias current and thus are independent of supply voltage fluctuations and load changes.

The regulator of the present invention provides such a regulated reference bias current source. Therefore it is a principal object of the present invention to provide a regulator circuit suitable for incorporation into integrated circuits to establish a regulated reference bias for constant current sources.

Other objects and advantages of the invention will be apparent upon reading the following detailed description of illustrative embodiments in conjunction with the drawings wherein:

FIG. 1 schematically illustrates a regulator in accordance with the present invention to insure that the constant current sources do not fluctuate;
FIG. 1A is the circuit of FIG. 1 redrawn;
FIG. 2 schematically illustrates a constant current source;
FIG. 3 schematically illustrates a plurality of current sources;
FIG. 4 is a plan view of a current source in accordance with the present invention;
FIG. 4A schematically depicts the current source of FIG. 4;
FIG. 5 is a cross-sectional view of the current source illustrated in FIG. 4;
FIG. 6 schematically illustrates a slave regulator which may be utilized in accordance with the present invention;

In the disclosure of the above-referenced Williams and Schnurr application the regulator 16A of FIG. 2 is the system master regulator and in the illustrated two-chip embodiment is connected to a slave regulator 16B. That is, as illustrated in FIG. 2 of that application, the seconds and minutes counters, decoders, and drivers are defined on one integrated circuit chip while the remaining circuitry is on a second integrated circuit chip. Since device parameters may vary from chip to chip, a master/slabs regulator system is provided.

The regulator of the present invention is suitable for use as such a master/slave regulator.

The regulator circuitry in accordance with the present invention is described with reference to FIGS. 1–6.

The basic operation of a current source is depicted in FIG. 2. Transistor T1 defines a reference along with resistor R. Transistor T1 has its base and collector tied together and forms a diode. The current through this diode forms a voltage reference. The assumption is made that the base drive required in transistor T1 is small compared to its emitter current. When transistor T2 is connected as shown in FIG. 2, the potential established by the base-emitter drop of transistor T1 is placed across the base-emitter of T2. Therefore, the current that flows in the emitter of transistor T2 will be the same as that which flows in the emitter of transistor T1. It is assumed that currents I1 and I2 are much smaller than the emitter currents I1 and I2. Therefore, the assumption is that the sum of I1 and I2, i.e., I3, is much smaller than the current I3. Thus, the current I3 is determined by the value of resistor R. If transistors T1 and T2 are well-matched, then the collector current Ic of T2 will be essentially identical to the current that flows through the resistor R. The practical limitations of this type circuit are apparent in FIG. 3. When the basic current source is extended to have many current sources connected to it, then the assumption which was made above that the base current is small compared to the collector current in the reference section no longer holds. Also, the current that is established by the resistor R is directly dependent upon the supply voltage V.

In accordance with the present invention, a circuit is provided which sets a current I3 in the reference that is independent of supply voltage and also which is independent of the base current from the current sources I2 (FIG. 3). The regulator circuit of the present system is illustrated in FIG. 1, wherein a fixed current flows in the emitter of transistor 5.

Operation of the regulator circuit of FIG. 1 is as follows. The current I3 in FIG. 1 is set to be about 15 times as large as the current I1. This ratio is established by the geometries of transistors 1, 2, 3 and 4. This ratio is not critical. Because of the ratio between the currents I1 and I3, the base-emitter voltages of transistor 6 and 7 are different. This voltage difference appears across the external resistor which is connected to ground and IC chip bonding 23. This resistor may, for example, be on the order of 68K ohms. Three-fourths of the collector cur-
rent of reference transistor 5 flows through this resistor to ground since three of the four collectors are commonly connected thereto. If the current flowing through reference transistor 5 becomes too large, the potential across the resistor will increase. This causes more of current I1 to go to base drive for transistor 7. Therefore, more of current I2 will become collector current of transistor 7, depleting transistor 8 of its base drive. When transistor 8 begins to turn off, it reduces the base drive to all of the p-n-p transistors used as current sources. Therefore, transistor 5 loses its base drive and its current must decrease. If the current in transistor 5 decreases too much, the voltage across the resistor will drop, driving more of the current of I1 into the resistor. This depletes transistor 7 of base drive and allows more of current I1 to go to base drive for transistor 8. This increases the base drive to transistor 5 and all of the p-n-p transistors which are used as current sources. The regulator circuit has a sufficient dynamic range to adjust itself to a fixed current established solely by the external reference resistor. The current established is thus independent of supply voltage. The capacitor which is connected between the collector and the base of transistor 7 is used to compensate the regulator and keep it from oscillating. The resistor which is connected in the collector of transistor 8 is there to prevent SCR action from latching the regulator. Transistors 9, 10, and the external resistor attached to IC chip bonding pad 31 are used as a starting circuit to guarantee that the regulator will start up. One collector of transistor 5 goes to IC chips bonding pad 21. The current out of this collector is used as a reference for the slave current regulator of FIG. 6 which may be located on a different IC chip.

The circuit of FIG. 1A is the circuit of FIG. 1 redrawn in a manner that may facilitate the above explanation and better illustrate the function of the various devices. In FIG. 1A transistors 2, 3, 4 and part of 1, which are all connected in parallel in FIG. 1 are combined as a single transistor 2; the remainder of transistor 1 (i.e., the fourth collector) is shown in FIG. 1A as 1'. Likewise, the two collector circuits of transistor 5 are depicted with separate transistors 5A and 5B. Assuming that the geometries to the transistors of FIG. 1A are such that the ratios of currents I1 and I2 and currents I1A and I1B are maintained as in FIG. 1 the operation of the two circuits is exactly the same.

A schematic of the slave regulator is illustrated in FIG. 6. Transistors 13, 14 and 15 form a current source which is directly dependent upon the current from the reference node of the master regulator described in FIG. 1. Transistor 13 forms a reference base-emitter potential which then sets the emitter currents in transistors 14 and 15. Because of the difference in the number of emitters between transistors 13 and 14 and transistor 15, there is an 8 to 1 ratio between the currents that flow in the collectors of transistors 14 and 15. Transistor 12 is a reference transistor for all of the current sources controlled by slave regulator. Its current is established primarily by the collector current of transistor 15. A small amount of the current out of the collector of transistor 12 is used for base drive to transistor 16. If the current in transistor 12 becomes too large, all the excess current becomes base drive for transistor 16, which then diverts base drive from transistor 17 thereby reducing the base drive to transistor 12 and bringing its collector current back in line. If the current in transistor 12 is too small, then transistor 16 will be deprived of base drive. Transistor 17 will then receive additional base drive and it in turn will supply additional base drive for transistor 12. The capacitor between the collector and the base of transistor 16 is used to compensate the regulator and keep it from oscillating.

CURRENT SOURCE

With reference to FIGS. 4, 4A and 5, a typical four collector p-n-p transistor which is used as a current source load in accordance with the present invention is illustrated. FIG. 4 is a plan view illustrating the layout of a typical current source transistor. For the illustrated example, a substrate 91 may, by way of example, be comprised of p-type silicon. A p+ diffusion 88 defines an isolation barrier between various components on the substrate. The base region of the transistor comprises an n-type epitaxial layer 90. A DUF n+ region 92 is formed to underlie the transistor structure. An n+ region 94 is formed for the base contact. Collectors C1, C2, C3 and C4 are formed around a central p diffused emitter region 96. The transistor is schematically illustrated in FIG. 4A. Conventional integrated circuit fabrication techniques may be utilized in fabricating the transistor structure. Such techniques are well-known to those skilled in the art and need not be explained in detail herein.

While various embodiments have been described in detail herein, it will be apparent to those skilled in the art that various changes may be made without departing from the spirit or scope of the invention.

What is claimed is:

1. A reference bias regulator for a current source comprising:
a. a reference portion having a first bipolar transistor means of one type connected in emitter-collector series with a reference resistor between first and second reference nodes;
b. a differential regulator portion having second and third bipolar transistor means of said one type and fourth and fifth bipolar transistor means of the opposite type, resistance means and capacitance means, the bases of said transistor means of like types being connected together, the emitters of said transistor means of said one type being connected together and through said resistance means to the first reference node and the emitter of said fourth transistor means being connected to the second reference node, the collectors of said second and fourth transistor means being connected together and to one terminal of said capacitance means; the collectors of said third and fifth transistor means being connected together and to the bases of said fourth and fifth transistor means and to the other terminal of said capacitance means and the emitter of said fifth transistor means being connected to the junction of said reference resistor and said first transistor means; and
c. a drive portion having a sixth bipolar transistor means of said opposite type, the base of said sixth transistor means being connected to the collector of said second and fourth transistor means and the emitter of said sixth transistor means being connected to said second reference node.

2. The regulator as defined in claim 1 wherein said second, third, fourth and fifth transistor means are so
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ar ranged and constructed that the collector current of
said second transistor means is greater than about fif-
ten times the collector current of said third transistor
means.

3. The regulator as defined in claim 2 further includ-
ing a start portion comprising further bipolar transistor
means connected to said drive portion and arranged to
insure initial start up of said regulator.

4. The regulator as defined in claim 1 further having
a slave regulator portion comprising first, second, third
and fourth additional bipolar transistor means of said
one type with their emitters connected to one terminal
of a supply voltage, fifth, sixth, seventh, eighth and
ninth additional bipolar transistor means of said other
type with their emitters connected to the other terminal
of a supply voltage, and additional capacitance means;
the bases of said fifth, sixth and seventh additional tran-
sistor means and the collector of said fifth additional
transistor means being connected to the collector of
said first additional transistor means; the base of said
first additional transistor means being connected to the
base of said first transistor means; the bases of said sec-
ond and third additional transistor means being con-
ected to the collectors of said second and sixth addi-
tional transistor means; the collectors of said fourth
and seventh additional transistor means being con-
ected to the base of said eighth additional transistor
means and to one terminal of said additional capaci-
tance means; the collector of said third and eighth addi-
tional transistor means being connected to the base of
said ninth additional transistor means and to the other
terminal of said additional capacitance means; and the
collector of said ninth additional transistor means being
connected to the base of said fourth additional trans-
istor means.

5. A regulator as defined in claim 4 wherein said sec-
ond, third, fourth and fifth transistor means are so ar-
ranged and constructed that the collector current of
said second transistor means is greater than about fif-
ten times the collector current of said third transistor
means and wherein said first transistor means and said
first additional transistor means are so arranged and
constructed that the collector current of said first tran-
sistor means is more than about three times the collec-
tor current of said first additional transistor means.

6. The regulator as defined in claim 5 further includ-
ing a start portion comprising further bipolar transistor
means connected to said drive portion and arranged to
assure initial start up of said regulator.

7. In a reference bias regulator for constant current
sources wherein a master regulator output is taken
from the base of a reference bipolar transistor means
of one type connected in emitter-collector series with
a reference resistor between the terminals of a voltage
source, a slave regulator comprising:
first, second, third and further bipolar transistor means
of said one type with their emitters connected to one
terminal of the supply voltage source, fifth, sixth,
seventh, eighth and ninth bipolar transistor means of said other type with their emitters con-
ected to the other terminal of said supply voltage
source and capacitance means;
the bases of said fifth, sixth and seventh transistor
means and the collector of said fifth transistor
means being connected to the collector of said first
transistor means, the base of said first transistor
means being connected to the base of said refer-
ence transistor, the bases of said second and third
transistor means being connected to the collectors
of said second and sixth transistor means, the col-
lectors of said fourth and seventh transistor means
being connected to the base of said eighth transistor
means and to one terminal of said capacitance
means, the collectors of said third and eighth tran-
sistor means being connected to the base of said
ninth transistor means and to the other terminal of
said capacitance means, and the collector of said
ninth transistor means being connected to the base
of said fourth transistor means.

8. A regulator as defined in claim 7 wherein said first
transistor means is so arranged and constructed as to
have a collector current less than about one-third, the
collector current of said reference transistor means.

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