



AU9174262

(12) PATENT ABRIDGMENT (11) Document No. AU-B-74262/91
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 640473

- (54) Title
A METHOD OF MAKING A CIRCUIT DEVICE IN THE MANUFACTURE OF INTEGRATED CIRCUITS
- International Patent Classification(s)
(51)⁵ **H01L 021/82 H01C 017/06 H01L 027/06**
- (21) Application No. : **74262/91** (22) Application Date : **10.04.91**
- (30) Priority Data
- (31) Number (32) Date (33) Country
515854 27.04.90 US UNITED STATES OF AMERICA
- (43) Publication Date : **14.11.91**
- (44) Publication Date of Accepted Application : **26.08.93**
- (71) Applicant(s)
DIGITAL EQUIPMENT CORPORATION
- (72) Inventor(s)
BJORN K.A. ZETTERLUND
- (74) Attorney or Agent
DAVIES COLLISON CAVE , 1 Little Collins Street, MELBOURNE VIC 3000
- (56) Prior Art Documents
EP 287195
EP 272433
- (57) Claim

1. **A method of making a circuit device comprising a resistor in the manufacture of integrated circuit devices, said method comprising the step of:**

- a) **forming resistor area and transistor gates in transistor areas at a face of a semiconductor body; and being characterized by the steps of:**
- b) **depositing a conformal coating of oxide on said face;**
- c) **masking a resistor area of said face and exposing said transistor areas;**
- d) **etching said face in a directional manner to leave said oxide on said resistor area and to leave sidewall spacers adjacent said gates in said transistor areas;**
- e) **removing the mask; and**
- f) **simultaneously forming silicided areas on said face on opposite sides of said oxide on said resistor on transistor gates, and on source/drain regions adjacent said sidewall spacers.**

640473

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952

COMPLETE SPECIFICATION

NAME & ADDRESS
OF APPLICANT:

Digital Equipment Corporation
146 Main Street
Maynard Massachusetts 01754
United States of America

NAME(S) OF INVENTOR(S):

Bjorn K.A. ZETTERLUND

ADDRESS FOR SERVICE:

DAVIES & COLLISON
Patent Attorneys
1 Little Collins Street, Melbourne, 3000.

COMPLETE SPECIFICATION FOR THE INVENTION ENTITLED:

"A Method of Making a Circuit Device in the Manufacture of Integrated Circuits"

The following statement is a full description of this invention, including the best method of performing it known to me/us:-



BACKGROUND OF THE INVENTION

This invention relates generally to semiconductor devices, and more particularly to a method of forming precision resistors compatible with a self-aligned silicided CMOS process for making integrated circuits.

In high-performance, high-speed integrated circuit devices the signal paths between integrated circuit chips are effectively transmission lines. The impedances of the input and output circuits at the chip are different from the impedances of the signal paths, which causes reflections and degrade the signal. On-chip resistors to match the resistance on the chip with that of the signal path are the most effective way of reducing these signal-degrading reflections. For proper matching, the resistors preferably have selected values in the 10-50 ohm range with tolerances of $\pm 10\%$ (3 sigma). In MOS integrated circuits made by commercial processes, these resistance and tolerance requirements are best met by using resistors formed by N⁺ diffusions.

Resistors are formed in integrated circuit devices by making use of a diffused region of the proper length, width and impurity concentration to give the necessary resistance. In prior devices, the diffused regions creating the resistors are formed at the same time as source/drain regions in MOS integrated circuits. In contemporary CMOS processes using self-aligned silicided source/drain regions, however, the resistors cannot be created by previous methods without introducing unduly burdensome additional process steps, and these may have required critical alignments.

Various other methods for making resistors elements in integrated circuits have been proposed. For example, resistors may be formed in first-level or second-level polysilicon layers as set forth in U.S. Patents 4,110,776, 4,209,716, 4,291,328 or 4,416,049. Alternatively, resistor elements may be formed by implanted regions buried under field oxide as set forth in U.S. Patent 4,212,083. These prior methods are not suitable for the present purposes, however, due to the additional process steps needed, or deficiencies in the values or tolerances of the resistors, or their temperature coefficient of resistance, or other characteristics.

SUMMARY OF THE INVENTION

In accordance with the present invention there is provided a method of making a circuit device comprising a resistor, in the manufacture of integrated circuit devices,
5 said method comprising the steps of:

- a) forming a resistor area and transistor gates in transistor areas at a face of a semiconductor body; and being characterized by the steps of:
 - b) depositing a conformal coating of oxide on said face;
 - c) masking a resistor area of said face and exposing said transistor area;
 - 10 d) etching said face in a directional manner to leave said oxide on said resistor area and to leave sidewall spacers adjacent said gates in said transistor areas;
 - e) removing the mask; and
 - f) simultaneously forming silicided areas on said face on opposite sides of said oxide on said resistor, on transistor gates, and on source/drain regions adjacent said
15 sidewall spacers.

In another aspect there is provided a method of making a circuit device in the manufacture of integrated circuit devices, comprising the steps of:

- a) forming transistor gates in transistor areas at a face of a semiconductor
20 body;
- b) depositing a conformal coating of oxide on said face;
- c) masking a selected area of said face spaced from said transistor areas, and exposing said transistor areas;
- d) etching said face in a directional manner to leave said oxide on said
25 selected area and to leave sidewall spacers adjacent said gates in said transistor areas;
- e) removing the mask; and
- f) simultaneously forming silicided areas on said face on opposite sides of said oxide on said selected area on transistor gates, and on source/drain areas adjacent said sidewall spacers.

30



BRIEF DESCRIPTION OF THE DRAWINGS

A more detailed understanding of the invention may be had from the following description of a preferred embodiment, given by way of example and to be understood
5 in conjunction with the accompanying drawings wherein:

Figure 1 is an elevation view in section of a small part of a semiconductor integrated circuit containing a precision resistor according to one embodiment of the invention, along with other components, taken along the line 1-1 of Figure 1a;

10 Figure 1a is a plan view of the device of Figure 1;

20
30
40
50
60
70
80
90
100
110
120
130
140
150
160
170
180
190
200
210
220
230
240
250
260
270
280
290
300
310
320
330
340
350
360
370
380
390
400
410
420
430
440
450
460
470
480
490
500
510
520
530
540
550
560
570
580
590
600
610
620
630
640
650
660
670
680
690
700
710
720
730
740
750
760
770
780
790
800
810
820
830
840
850
860
870
880
890
900
910
920
930
940
950
960
970
980
990



Figures 2, 3, 4, 5 and 6 are elevation views in section of the device of Figures 1 and 1a at intermediate stages in the manufacture of a precision resistor according to one embodiment of the invention;

Figures 4a, 5a and 6a are plan views of the device of Figures 4, 5 and 6, respectively;

Figure 7 is an elevation view in section of a small part of a semiconductor integrated circuit containing a precision resistor according to another embodiment of the invention, taken along the line 7-7 of Figure 7a; and

Figure 7a is a plan view of the device of Figure 7.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENT

Referring to Figures 1 and 1a, a semiconductor chip 10 is shown having a precision resistor 11 constructed according to the invention in a CMOS device having an N-channel transistor 12 and a P-channel transistor 13. The chip includes a P+ substrate 14 with a P- epitaxial layer 15, and the resistor 11 and the P-channel transistor 13 are formed in separate N-wells 16 and 17. Source and drain regions 18 for the N- channel

transistor 12 are created by an N+ implant which is driven into the P- epi layer 15 to form shallow N+ areas; this same N+ implant into the N-well 16 is used to create the N-type resistive area 20 of the precision resistor 11, according to a feature of one embodiment of the invention. Source and drain regions 21 for the P-channel transistor 13 are created by a P+ implant which is driven into the N-well 17 to form shallow P+ areas. Gates 22 and 23 for the transistors 12 and 13 are polysilicon electrodes overlying thin gate oxide and overlying channel regions between the source/drain regions, with the source/drain regions self-aligned with the gates. Sidewall spacers 24 and 25 are used on the sides of the polysilicon gates 22 and 23 to provide a self-alignment feature in creating silicided areas 26 and 27 on the source/drain regions 18 and 21. Silicided areas 28 and 29 are also created on top of the polysilicon gates 22 and 23. According to a feature of one embodiment of the invention, an oxide layer 30 on top of the resistor region 20 is created at the same time as the sidewall spacers 24 and 25, and self-aligned silicided regions 31 and 32 created at the same time as the silicided areas 26, 27, 28 and 29 provide contacts to the ends of the resistor region 20. A low-temperature deposited oxide layer 33 covers the entire face of the wafer after the silicided areas are formed, and vias etched in this

oxide layer 33 allow metal-to-silicide contacts for connections 34 and 35 to both sides of the resistor 11, as well as source/drain connections 36 and 37 for the transistors 12 and 13, respectively. The metal connections 34-37 make contact to the silicided areas at contact areas 38 or 39. The areas used for the precision resistor and the N- and P-channel transistors 12 and 13 are delineated on the face of the substrate by high-temperature (thermal) field oxide areas 40. There may be second (or third) level metallization, separated from the first level metal contacts and interconnections 34-37 by interlevel oxide, not shown.

Referring to Figures 2-6, a method for manufacturing the device of Figures 1 and 1a will be described. These Figures 2-6 are at successive stages in the manufacturing process. It is understood that only a very small part of a silicon wafer is shown in these Figures, and the transistors and resistor illustrated are merely examples of devices formed in dense circuits having perhaps hundreds of thousands of such components in each chip. There are usually hundreds of such chips in a wafer of perhaps six or eight inch diameter, before breaking into individual units.

After a thermal oxidation step to create a layer 41 of silicon oxide, a photoresist mask 42 is formed over the areas where N-channel transistors are to be created, as shown in Figure 2. After an etching step to remove the silicon oxide layer 41 in the unmasked areas, a phosphorus implant is performed to create shallow regions 43 which, when driven into the silicon by subsequent high-temperature steps, create the N-wells 16 and 17, as seen in Figure 3. The field oxide layer 40 is formed by first depositing a layer 44 of silicon nitride over a thin layer of oxide on the epi layer 15 as shown in Figure 3, then patterning this oxide/nitride layer 44 using a photolithographic masking and etching step to leave oxide/nitride only where the transistors or resistor are to be created. The wafer is then subjected to a thermal oxidation step to form the field oxide 40 in areas where the oxide/nitride 44 has been removed. The oxide/nitride layer 44 is stripped off. The next step is forming the gate oxide 45, usually by thermal oxidation, then creating the gates 22 and 23 by depositing a layer of polycrystalline silicon over the entire face of the wafer and patterning the layer using photoresist masking and etching to leave only the gates 22 and 23 (as well as polysilicon interconnects) as seen in Figures 4 and 4a. The area of the P-channel transistor 13 is covered by a photoresist mask, and an arsenic implant is performed at

this point, using the polysilicon gate 22 as a mask to create the N+ source/drain regions 18 and 21; at the same time, the resistor region 20 is formed by this implant. The photoresist mask is stripped, then the area of the resistor 11 and that of the N-channel transistor 12 are covered by another photoresist mask and a P+ implant done to create the source/drain regions 21 for the P-channel transistor 13. The face of the wafer is next covered with a conformal coating 46 of low-temperature deposited oxide to be used in creating the sidewall spacers 24 and 25. This oxide is also used to define the shape of the precision resistor 11, and to this end a mask 47 of photoresist is formed over the region 20 which is to become the resistor. This mask 47 is formed by depositing photoresist over the entire top surface of the oxide 46, then exposing to light through a mask prepared for solely the purpose of defining the resistor sizes. This photoresist mask and etch step (and subsequent removal of the mask 47) is the only manufacturing step added to a standard CMOS process to produce the resistors of the invention, since all of the other steps in this method are already present in an N-well CMOS process using sidewall spacers and self-aligned silicided source/drain regions. These added steps, forming the mask 47 and then removing this mask, require no critical alignment with other geometry of the face of the wafer to define the

resistor value, since the resistor value will be determined by the width of the mask 47 (for a given resistivity of the diffused region 20). A directional etch such as a reactive ion etch is used to remove all of the deposited oxide layer 46 in the areas of the face not covered by the mask 47, but since only a given amount of oxide is removed in this step the sidewall spacers 24 and 25 are left where the thickness has built up near the vertical step of the polysilicon gates 22 and 23, seen in Figures 5 and 5a. The next step is forming the silicided areas 26, 27, 28, 29, 31 and 32, as seen in Figure 6, and this is accomplished by first stripping off the mask 47 then depositing a thin layer of cobalt or other such metal over the entire top surface of the wafer, followed by a heat treatment which forms the silicide by reaction of the metal with the silicon where the silicon is bare; in areas covered by oxide the metal does not react and is subsequently removed by cleaning. The silicide thus forms on the tops of the polysilicon gates 22 and 23, and on the source/drain regions of the transistors, as well as defining the resistor 11 by low-resistance contacts areas on both sides of the oxide layer 30. After the self-aligned silicide areas are created, the entire top surface of the wafer is coated with the low-temperature deposited oxide 33 as seen in Figure 1, and a photoresist masking and etching step is performed to

open the vias where contact is to be made to the silicided areas at contact areas 38 and 39. The metallization layer for contacts and interconnects is then formed by first laying down a coating a metal, e.g., aluminum, and patterning this metal layer using photoresist masking and etching to leave the contacts 34, 35 36 and 37, seen in Figures 1 and 1a.

In another embodiment of the invention, as illustrated in Figures 7 and 7a, the low temperature deposited oxide layer used to create the region 30 of oxide to define the resistor size (and of course to create the sidewall spacers) may also be left in place in a frame-shaped area 48 surrounding the resistor, overlying all of the inner edge of the field oxide 40 on the wafer face and spacing the silicided area away from the field oxide 40. This configuration increases the distance 49 along the surface between the N+ diffused region just beneath the silicide and the P- epitaxial region 15 and thus allows the precision resistor to withstand higher electrostatic voltages. Other than the shape of the frame area 48 of the oxide layer around the resistor, the process of making the device of Figures 7 and 7a is the same as that of Figures 1-6.

The precision resistors described above are thus seen to be manufactured by a process compatible with a standard CMOS process, without adding any process steps requiring critical alignment. The magnitude of resistance produced is in the range needed for impedance matching, i.e., 10-50 ohms. Self-aligned silicided source/drain regions may be used for the N- and P-channel transistors in the CMOS integrated circuit, but the silicided areas need not be used for the resistors; the silicided areas have a sheet resistance many times lower than that of the diffused source/drain regions, and so cannot function as resistors of moderate value.

While this invention has been described with reference to specific embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention. The reference numerals in the following claims do not in any way limit the scope of the respective claims.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A method of making a circuit device comprising a resistor in the manufacture of integrated circuit devices, said method comprising the step of:
 - 5 a) forming resistor area and transistor gates in transistor areas at a face of a semiconductor body; and being characterized by the steps of:
 - b) depositing a conformal coating of oxide on said face;
 - c) masking a resistor area of said face and exposing said transistor areas;
 - d) etching said face in a directional manner to leave said oxide on said
 - 10 resistor area and to leave sidewall spacers adjacent said gates in said transistor areas;
 - e) removing the mask; and
 - f) simultaneously forming silicided areas on said face on opposite sides of said oxide on said resistor on transistor gates, and on source/drain regions adjacent said sidewall spacers.
- 15 2. A method according to claim 1 including the step of introducing impurity into said face using said transistor gates as a mask to create source/drain regions for said transistors and to create a resistor region beneath said resistor area.
- 20 3. A method according to claim 2 wherein said step of introducing impurity includes separate steps of introducing N-type and P-type impurity to thereby create both N-channel and P-channel transistors.
4. A method according to any one of claims 1 to 3 wherein said step of masking said
- 25 resistor area includes masking a frame area surrounding said resistor area.
5. A method according to any one of claims 1 to 4 wherein said resistor area overlies an N-well in a P-type substrate.
- 30 6. A method according to claim 1 wherein said step of masking said part of said resistor area includes also masking a frame area surrounding said resistor area, whereby said silicided areas on said resistor area are spaced from field oxide.



7. A method according to claim 1 including the step of forming metal-to-semiconductor contacts on contact areas of said silicided areas.

8. A method of making a circuit device in the manufacture of integrated circuit devices, comprising the steps of:

- a) forming transistor gates in transistor areas at a face of a semiconductor body;
- b) depositing a conformal coating of oxide on said face;
- c) masking a selected area of said face spaced from said transistor areas, and
- 10 exposing said transistor areas;
- d) etching said face in a directional manner to leave said oxide on said selected area and to leave sidewall spacers adjacent said gates in said transistor areas;
- e) removing the mask; and
- f) simultaneously forming silicided areas on said face on opposite sides of
- 15 said oxide on said selected area, on transistor gates, and on source/drain areas adjacent said sidewall spacers.

9. A method according to claim 8 including the step of introducing impurity into said face using said transistor gates as a mask to create source/drain regions for said

20 transistors and to create a region beneath said selected area to provide a resistor device.

10. A method according to claim 9 wherein said step of introducing impurity includes separate steps of introducing N-type and P-type impurity to thereby create both N-channel and P-channel transistors.

11. A method according to claim 8 wherein said step of masking said selected area includes masking a frame area surrounding said selected area.

12. A method according to claim 8 wherein said selected area overlies an N-well in

30 a P-type substrate.



13. A method of making a circuit device substantially as hereinbefore described with reference to the drawings.

5

DATED this 17th day of June, 1993

DIGITAL EQUIPMENT CORPORATION

By its Patent Attorneys

10 DAVIES COLLISON CAVE

8
2
2

8
2
2



A 4x4 grid of 16 small images showing the digits 3, 5, 9, and 1 in various styles and orientations. The digits are arranged in a 2x2 grid, with each digit appearing twice in different styles and orientations.

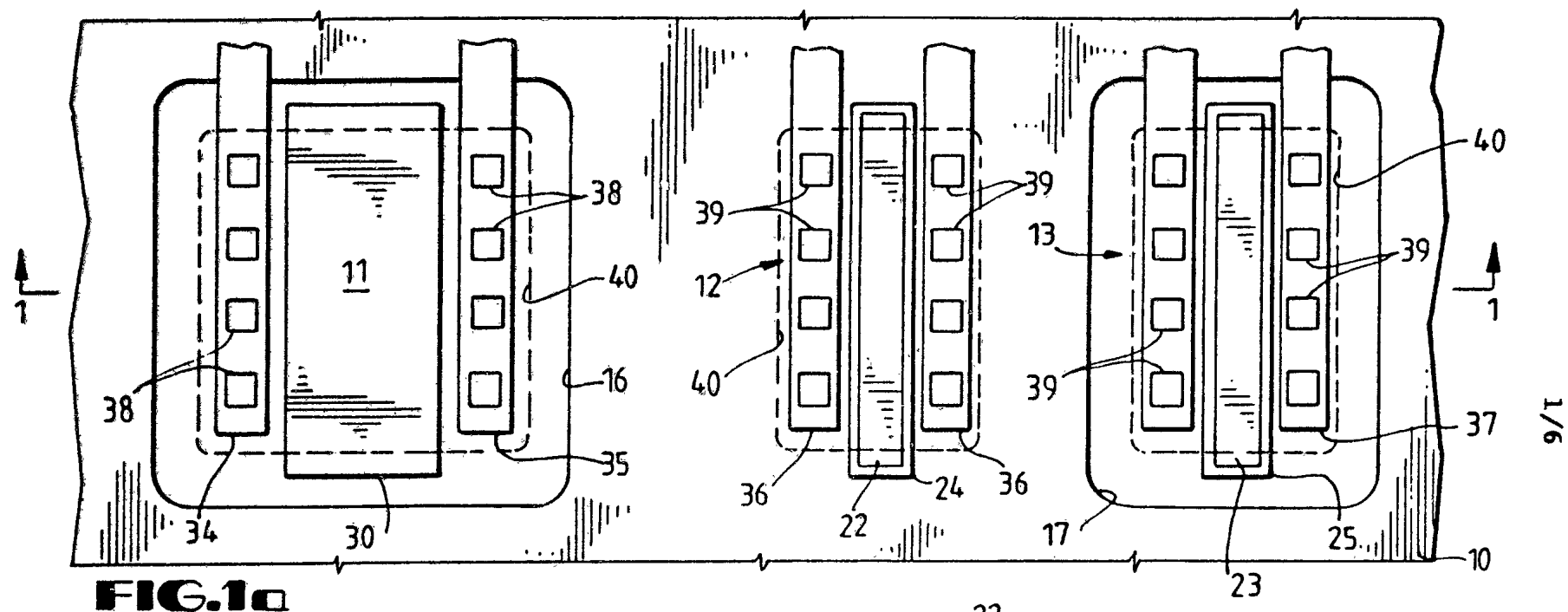


FIG.1a

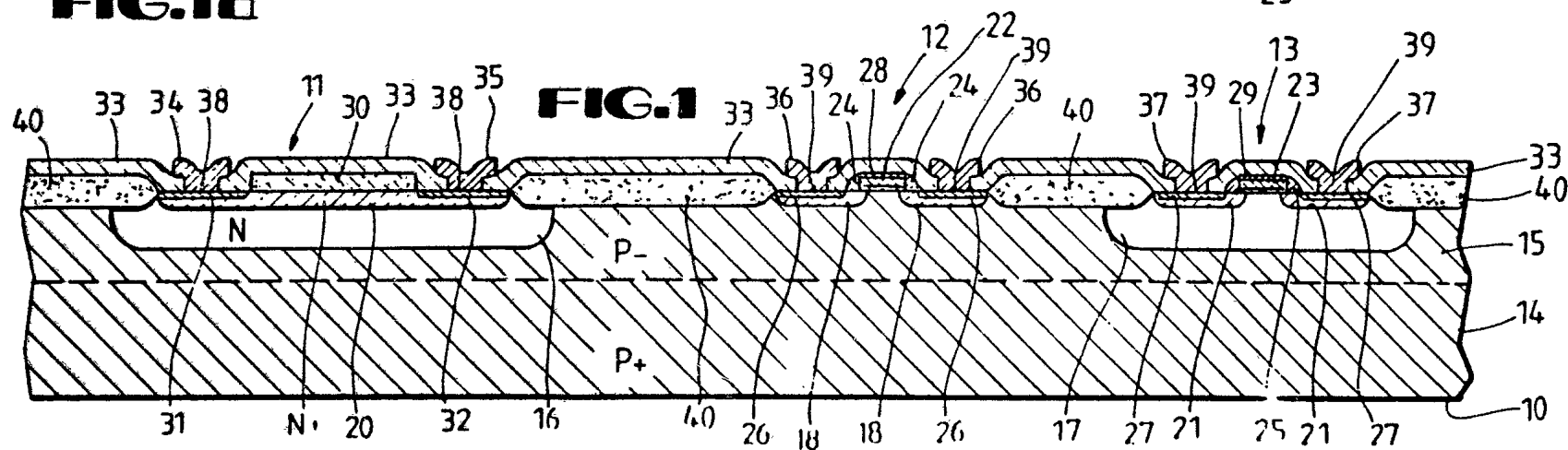


FIG.1

3 5 91 74202

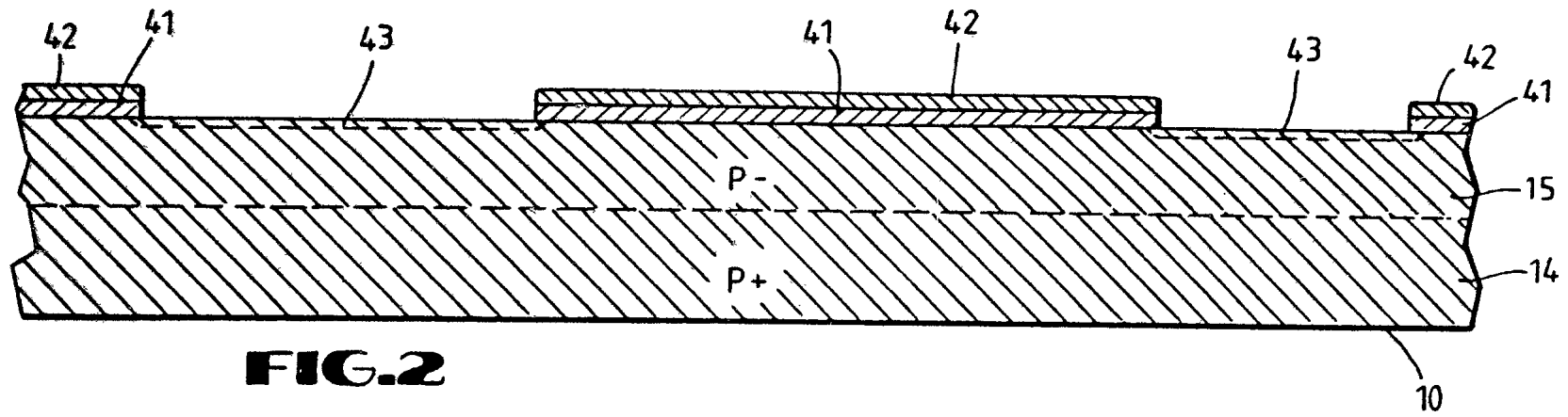


FIG. 2

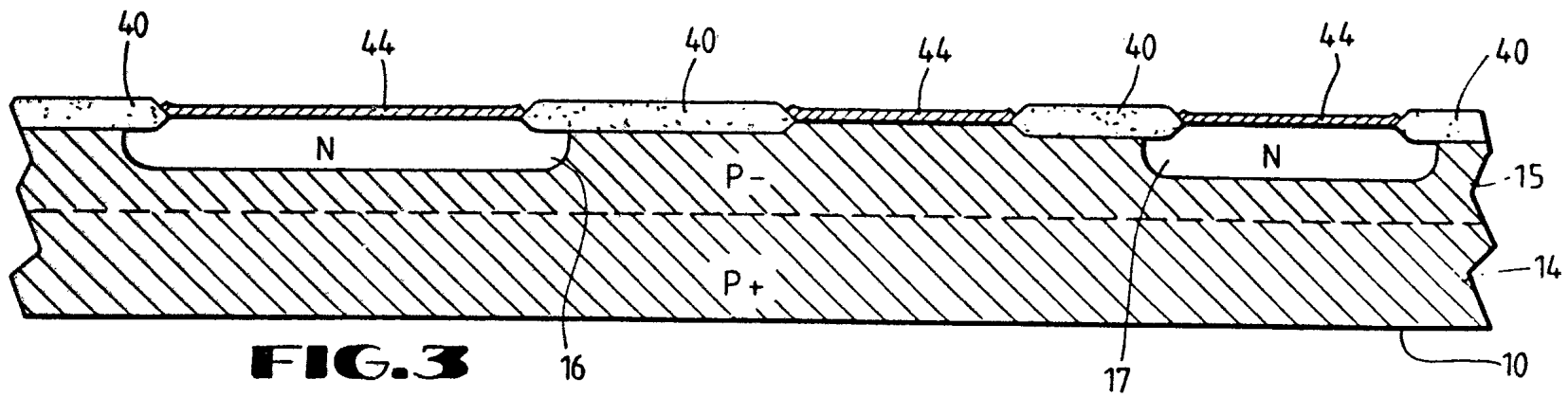


FIG. 3

3 5 91 74282

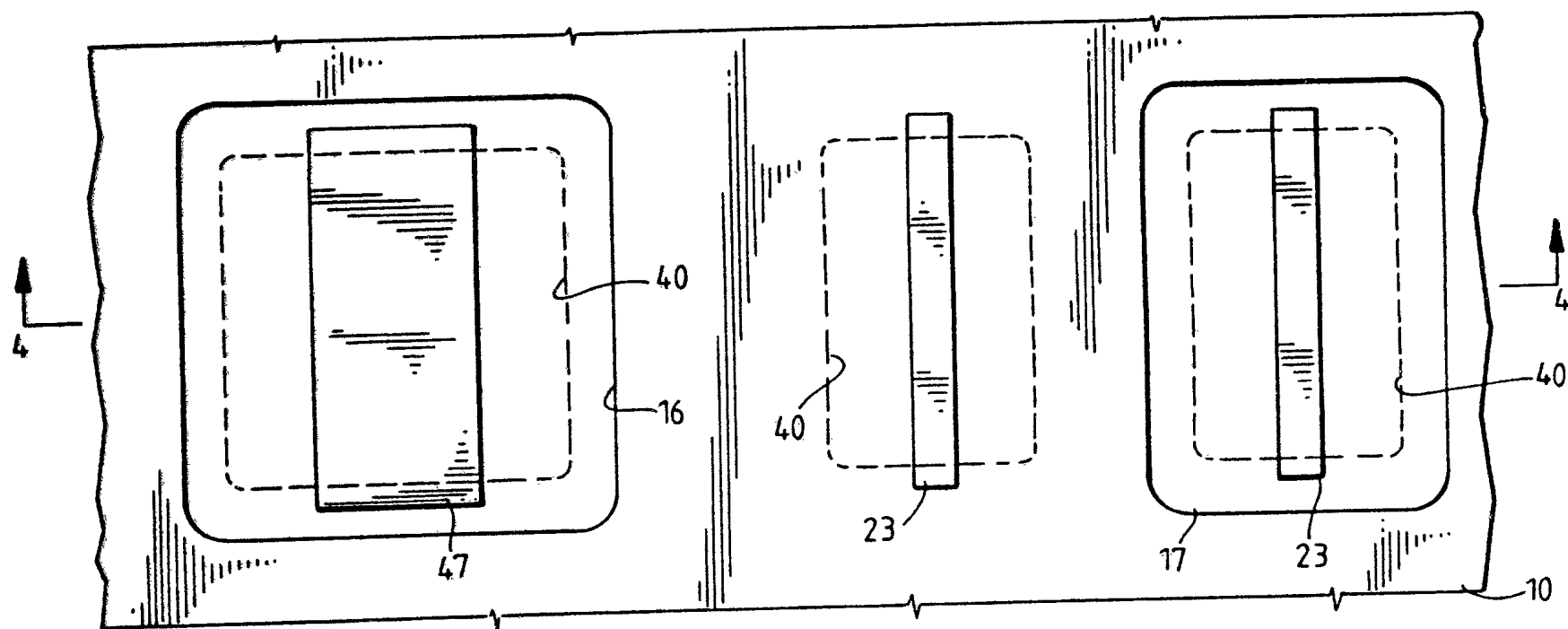


FIG. 4

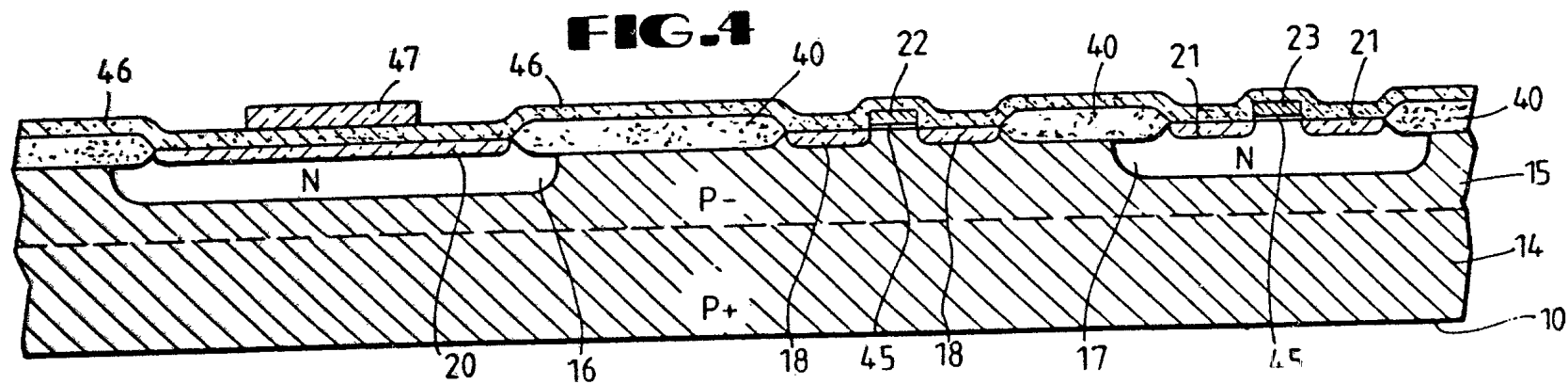


FIG. 4

3 5 91 74282

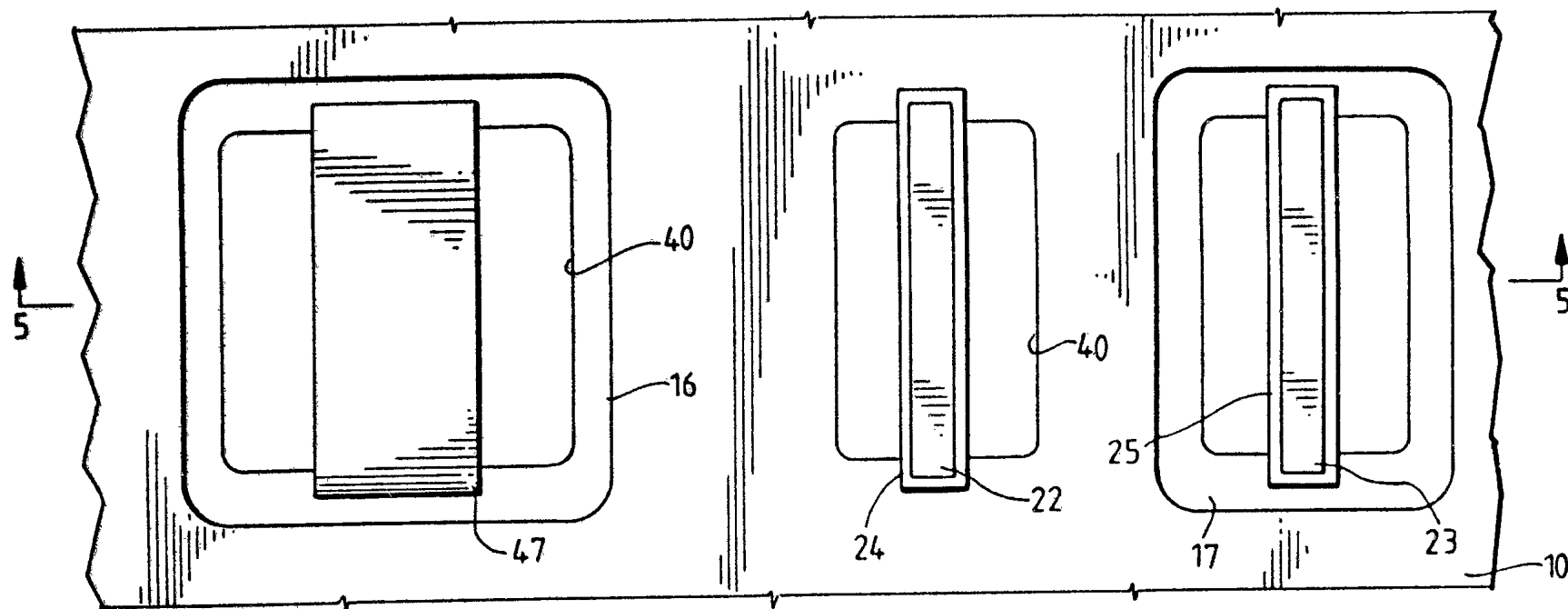


FIG. 5a

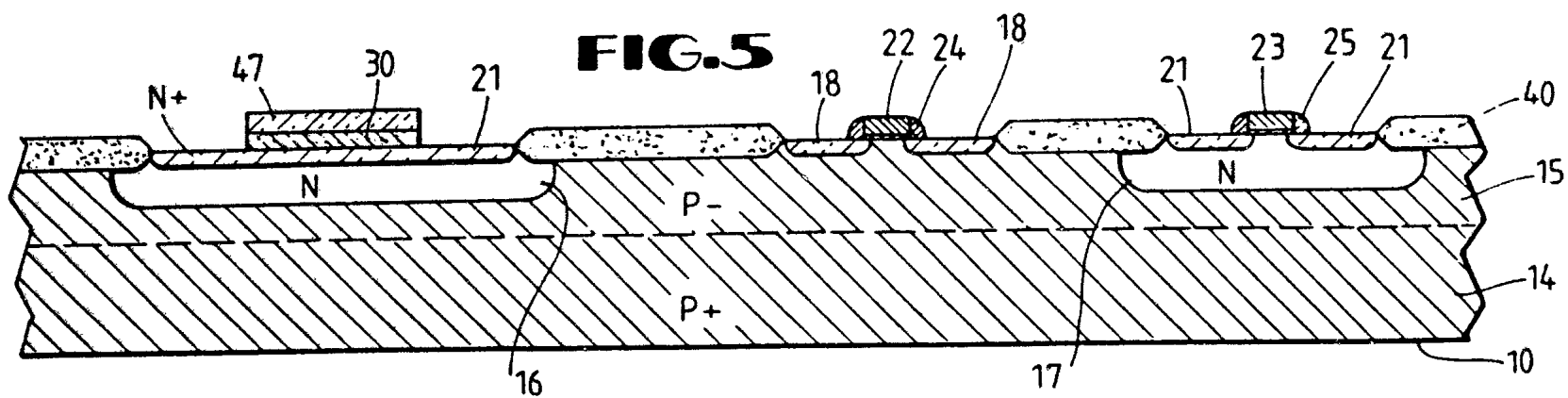


FIG. 5

3 5 91 74262

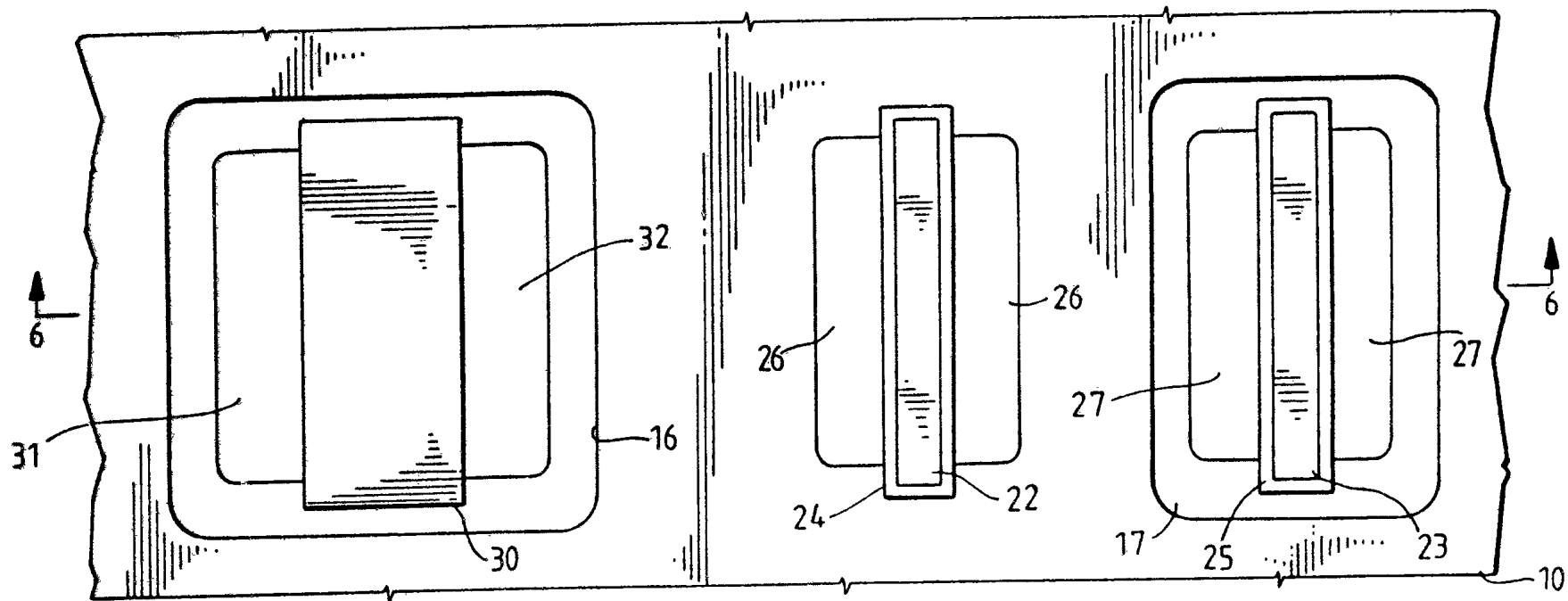


FIG. 6a

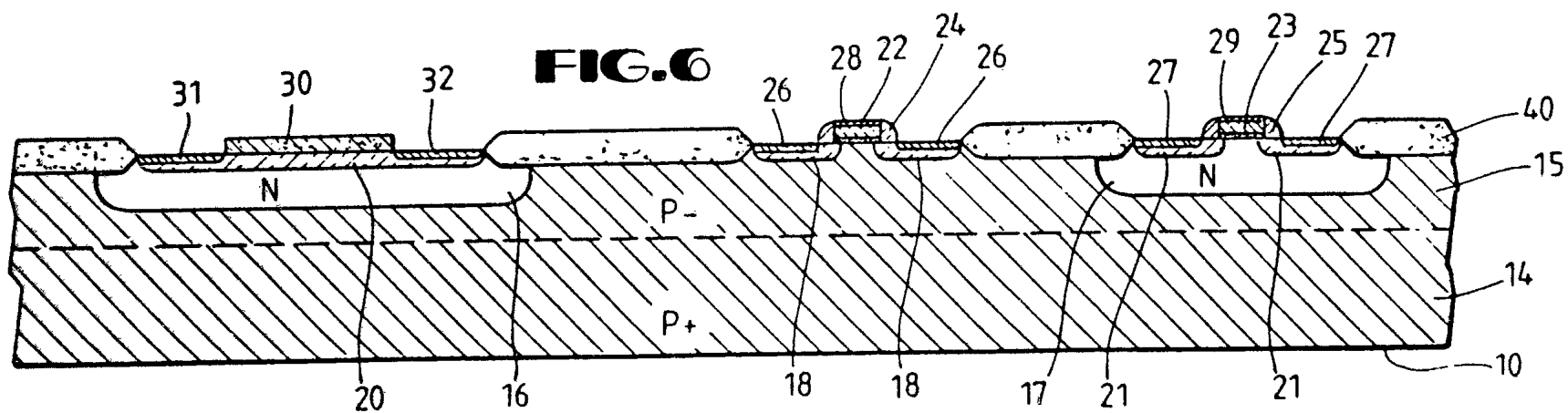
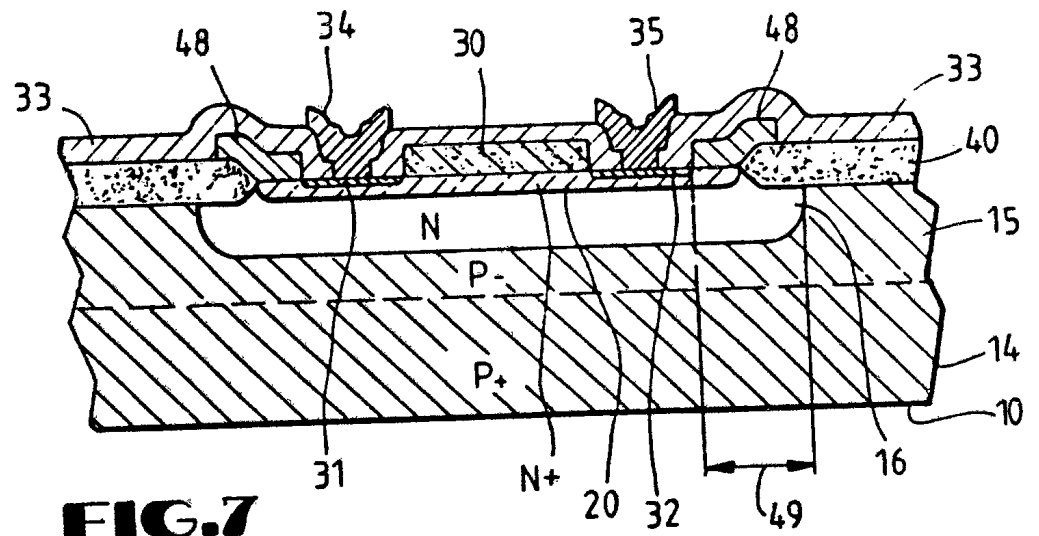
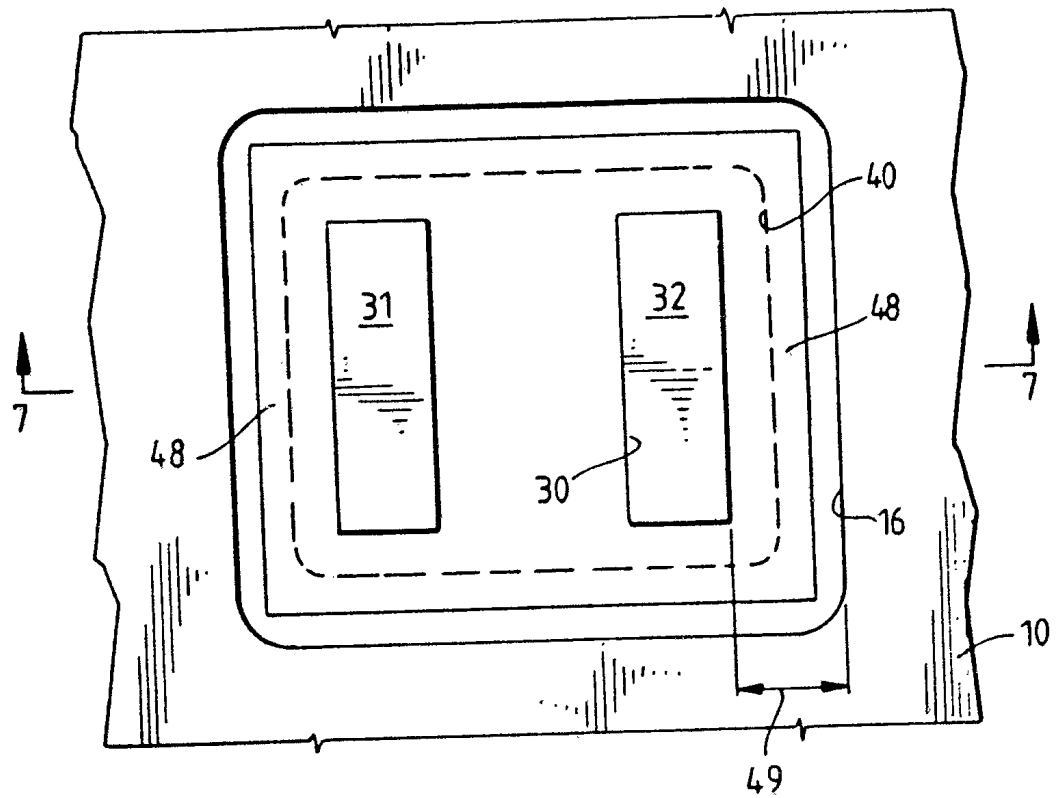


FIG. 6

FIG.7a**FIG.7**