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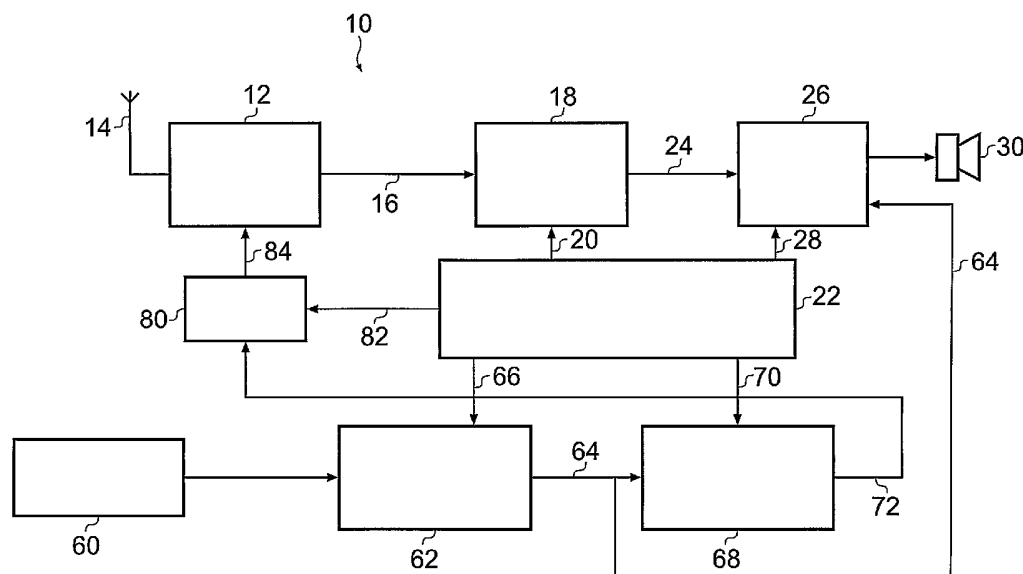
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(54) Title: AN ELECTRICAL DEVICE WITH IMPROVED IMMUNITY TO SELF GENERATED NOISE



(57) Abstract: An electrical device (10) comprising a signal source (12), a switched mode device (26, 62) and a sampling circuit (18), in which the sampling circuit is adapted to periodically sample an output (16) of the signal source during a time period when the switched mode device is not switching.

An Electrical device with Improved Immunity to Self Generated Noise

The present invention relates to an electrical device with improved immunity to self generated noise.

A typical electronic radio receiver comprises two main parts, a receiver/demodulator and an amplifier. The receiver/demodulator receives a broadcast modulated signal and recovers from it a signal containing audio information. The amplifier amplifies the recovered signal and uses it to drive, for example, a loudspeaker.

Where the radio is powered by batteries, it is desirable to extend the lifetime of the batteries as they may be expensive or inconvenient to replace. Therefore it is beneficial to reduce the power consumption of the radio. The power consumption of the amplifier can be reduced by using switched-mode techniques. In particular, a class-D amplifier can be used. The power consumption of the receiver/demodulator can be reduced by employing a switched-mode power converter to convert the variable battery voltage into exactly the minimum voltage required to drive the demodulator.

However the use of switched-mode techniques in the radio receiver circuits creates radio-frequency emissions which interfere with the incoming modulated signal or interact with sensitive parts of the receiver/demodulator, thereby degrading the performance of the receiver.

The prior art teaches that this problem can be mitigated by enclosing all switched-mode components inside a metal screening container, with input and output leads appropriately filtered, such that the emissions are substantially contained within the screening container. However, the containers tend to be physically large and expensive.

Summary of the Invention

According to a first aspect of the present invention, there is provided an electrical device comprising a signal source, a switched mode device and a sampling circuit, in which the

sampling circuit is adapted to periodically sample an output of the signal source during a time period when the switched mode device is not switching.

Thus interference from the switched mode circuit, such as a switching amplifier and/or its associated load (e.g. a loudspeaker coil) is reduced or eliminated as the sample of the output signal from the signal source, such as a receiver/demodulator is taken when the switched mode circuit is not switching.

Preferably, for a period of time herein called a “quiet time”, interference from the amplifier is reduced. This is preferably done by preventing the amplifier from switching during the “quite time”.

Alternatively, from knowledge of the amplifier’s operation it is possible to predict a time when the amplifier is not switching, and take a sample in that time.

Advantageously the signal source only receives power for a short time, called the “power-up time”, during which the sample is taken. Preferably the signal source is allowed to settle before a sample is taken. In this way the power consumption of the signal source is reduced when compared to a signal source which is running continuously. Alternatively, certain parts of the signal source circuit can be powered up earlier or continuously, in order to reduce its settling time. Thus if the signal source is a radio reciever/demodulator, then a local oscillator within the radio receiver may be powered up in advance to allow it to settle, or alternatively outside of the power up time it could be placed in a reduced power mode just sufficient to sustain oscillation.

Preferably the signal source is a radio receiver and demodulator circuit which receives a modulated signal from an antenna and demodulates it.

Preferably certain parts of the circuit are powered by a switched-mode power supply. Advantageously the sample is taken during a period when this is not switching in order to reduce the effects of switching interference on the sample. This can be done by preventing

the power supply from switching while the sample is being taken. Alternatively the circuit can predict a time when the power supply will not switch, and can take a sample in this time.

According to a second aspect of the present invention, there is provided a method of recovering a signal, comprising the steps of:

- a) periodically taking a sample of a signal source when a switching amplifier is not switching; and
- b) providing the sample to the switching amplifier.

According to a third aspect of the present invention, there is provided a compressed data decoder, comprising

- an input for receiving compressed data from a first data store;
- an output for sending decoded data to a second data store;
- wherein when it is desired to replenish decoded data within the second data store, the decoder is arranged to receive full power, decode compressed data from the first data store, output decoded data to the second data store at a faster rate than that at which the decoded data is to be used, and receive no power or partial power until it is desired to replenish decoded data again.

According to a fourth aspect of the present invention, there is provided a method of decoding compressed data stored in a first data store, comprising the steps of:

- (a) continuously using decoded data in a second data store,
- (b) when it is desired to replenish the second data store with decoded data, performing the steps of:
 - (i) providing full power to a decoder;
 - (ii) using the decoder to decode compressed data from a first data store to form the decoded data;
 - (iii) storing the decoded data in the second data store; and
 - (iv) providing no power or partial power to the decoder.

Brief Description of the Drawings

The invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 schematically shows a receiver circuit according to a first embodiment of the present invention;

Figure 2 shows an example of a class-D amplifier;

Figure 3 shows an implementation of a class-D amplifier;

Figure 4 shows a class-D amplifier including a transistor H-bridge;

Figures 5a to 5g show waveforms illustrating the behaviour of various components of figure 1;

Figure 6 shows an example of a voltage step-down converter; and

Figure 7 schematically shows a portable compressed audio player according to a further embodiment of the present invention.

Detailed Description of Embodiments of the Invention

The radio receiver 10 of Figure 1 comprises a receiver and demodulator 12 which receives a modulated signal via antenna 14. An output 16 of the receiver and demodulator 12 comprises an audio signal which has been recovered from the modulated signal in a manner which is well known to those skilled in the art. The modulated signal may comprise the audio signal modulated by a carrier using an AM, FM or another modulation method.

The output 16 of the receiver and demodulator 12 is supplied to a sample and hold circuit 18. The sample and hold circuit (a track and hold circuit could also be used) 18 takes a sample of a receiver and demodulator output signal 16 in response to a control signal 20 from a controller 22, and outputs this until it is instructed by the controller 22 to take another sample of the output signal 16.

The sampled voltage 24 is supplied to the input of a class-D amplifier 26. The amplifier 26 also receives a clock signal 28 from the controller 22.

The class D amplifier schematically illustrated in Figure 2 is efficient because the semiconductor devices Q1 and Q2 are switched between fully on and fully off, thereby reducing dissipation within these semiconductors. Furthermore, the amplifier is suitable for driving a capacitive load efficiently. Piezoelectric loudspeakers present a substantially capacitive load. These loudspeakers are available with diameters of at least 4" and have a lower cut-off frequency of 300Hz. Whilst the bass content of sound from this type of loudspeaker is not strong, the overall sound quality is quite acceptable. Additionally, a short cone can be used to load the speaker so as to emphasise the bass tones. The impedance of a piezoelectric loudspeaker is approximately 1 microfarad and the device is efficient in converting electrical energy into sound energy. However, to achieve the required displacement of the transducer element, large amounts of charge (and therefore energy) must flow in and out of the loudspeaker each cycle of the audio signal. In order to realise high overall efficiency, the amplifier used to drive the loudspeaker must be capable of recovering the energy stored in the capacitive load that the speaker presents. A class D amplifier is able to recover this energy.

It should be noted that the amplifier can also drive a permanent magnet loudspeaker having a moving coil. These loudspeakers are typically only one to two percent efficient. This is partly due to the difficulty of coupling the loudspeaker cone to the air without use of an unacceptably large horn. However, it is also due to the fact that moving coil loudspeakers appear as a resistance of approximately 8 ohms over most of their frequency range. At certain frequencies, the impedance may include a reactive element, but most of the losses are associated with the current flowing through the resistance of the coil. These losses are

proportional to the square of the current in the coil. Thus, as more current movement is required, losses increase sharply.

However, a permanent magnet loudspeaker can be used in radios constituting an embodiment of the present invention with little increase in power requirement when the radio is to be operated at low volume. However, at greater levels of loudness, the power demand rises steeply.

As shown in Figure 2, the switching elements Q1 and Q2, which can be implemented by field-effect transistors, are arranged in series and driven in anti-phase. Thus, the loudspeaker 30 is either connected to the supply rail 32 or to the 0 volt rail 34. An inductor 36 is provided in series with the loudspeaker 30 in order to smooth out switching transients which occur due to the essentially digital nature of the amplifier. A capacitor 38 is provided to block DC current flow. Diodes D1 and D2 are connected in parallel with the semiconductor switches Q1 and Q2 and act as flyback diodes, thereby shielding the semiconductor switches from inductive current flow during device switching.

The class D amplifier is driven by a pulse-width modulated signal obtained by comparing an audio signal with a reference waveform which is a sawtooth or triangular wave. Figure 3 schematically illustrates an embodiment of the amplifier. A waveform generator 40 (generating a sawtooth or triangular wave) is connected to the non-inverting input of a comparator 42. The sampled audio signal is supplied to the inverting input of the comparator. The output of the comparator is therefore a pulse-width modulated signal representing the magnitude of the audio signal. First and second field-effect transistors 44 and 46 are connected in series between the power supply rail 32 and the ground rail 34. The first field-effect transistor 44 is an N channel device, whereas the second field-effect transistor 46 is a P channel device. The gates of the field-effect transistors 44 and 46 are connected to the output of the comparator 42. An output is picked off from the junction between the field-effect transistors and is supplied via an inductor L1 to a piezoelectric speaker 48 represented as a capacitor C1. A ferrite bead 50 is included in the connection between the first field-effect transistor 44 and the power supply rail 32 in order to limit current shoot-through. Similarly, diodes D1 and D2 are provided to inhibit current

shoot-through. The diodes D1 and D2 may be externally provided Schottky diodes for efficiency, or they may be the body drain diodes internal to the MOSFET transistors.

An important feature of the class D amplifier is that power can flow in both directions. When driving a purely reactive load, there will be power flow in both directions during the complete audio cycle. The current in the DC supply will therefore vary between positive and negative during each cycle. If there were no losses anywhere in the circuit, the average value of this DC current over one audio cycle would be zero. When driving the piezoelectric loudspeaker, there will be losses in the loudspeaker and there will be losses in the transistors, the diodes and in the resistance of other components, but the overall efficiency of this combination of loudspeaker and amplifier is high compared with that of a conventional class AB amplifier and permanent magnet loudspeaker arrangement.

Since the output voltage is developed across C1 in Figure 3 (C1 representing a piezoelectric loudspeaker) or across C1 in Figure 2 (where the loudspeaker 30 is a moving coil-type), the value of the series inductance must be chosen carefully. If it is too low, the ripple current at the switching frequency will be high and the associated losses in the MOSFETs of the amplifier will be significant. If the inductance is too high, it will present significant impedance to high frequency audio currents.

In the pulse-width modulation wave form generator circuit, and in the amplifier output stages, there is a certain amount of current drawn from the supply which is independent of the power being delivered to the loudspeaker. This current is effectively the quiescent current of the amplifier. The quiescent power drain of the amplifier is therefore the quiescent current multiplied by the supply voltage. It is desirable to keep the supply voltage as low as possible in order to minimise power loss. However, the loudspeakers (whether moving coil or piezoelectric) require a certain voltage swing from the amplifier in order to obtain their dynamic performance. This can lead to unacceptably large quiescent losses. A solution to this problem is to couple two output stages together in a "H" bridge configuration. Such an arrangement is shown in Figure 4. Comparing this with Figure 3, it is seen that one plate of C1 was grounded in Figure 3 and the other plate could be switched between 0 and the supply rail. In Figure 4, either plate of the capacitor can be

connected to the ground, and either plate can be connected to the supply rail. Thus, the effective peak-to-peak voltage that can be applied to the capacitor C1 (which could represent the piezoelectric loudspeaker) is doubled. Thus, Q1 and Q4 are controlled to open and close together, and Q2 and Q3 are controlled to open and close together. Otherwise the operation of the amplifier is similar to that described in respect of Figure 3.

To ensure that each bridge operates at a fifty percent duty cycle where there is no audio input signal, and therefore that the average DC voltage is zero, the average output voltage of one leg of the H-bridge can be fed back to the modulator circuit (including the wave form generator 40 and comparator 42) to adjust the bias level in the amplifier. A more sophisticated bias scheme is to use a differential amplifier to sense the average voltage difference across the output terminals of the amplifier and feed this signal back to the pulse-width modulator wave form generator.

The class-D amplifier 26 therefore amplifies the sample 24 of the audio signal 16 and supplies it to the loudspeaker 30.

The receiver 10 of Figure 1 is driven using a power supply 60. In a typical portable radio, the power supply 60 will comprise one or more batteries. In the embodiment described herein, the power source 60 comprises a single 1.5v battery.

The voltage of the battery 60 is not constant and degrades over time. Therefore the battery voltage is supplied to a boost converter 62, which boosts and regulates the battery voltage to produce a substantially constant output voltage 64 of 2.1v, although it will be appreciated that the circuit designer has freedom to choose a different voltage. The voltage 64 is used as the power supply for the class-D amplifier 26.

The boost converter 62 receives a control signal 66 from the controller 22, and uses switched-mode techniques to boost and regulate the battery voltage. Such boost converters are well known to those skilled in the art and will not be described further herein.

The demodulator 12 typically operates with a power supply voltage less than that of the class-D amplifier 26. Therefore the output voltage 64 of the boost converter 62 is provided to the input of a voltage step-down converter 68. The voltage step-down converter 68 also receives a control signal 70 from the controller 22, and uses switched-mode techniques to halve the voltage 64 at the input. Therefore the output voltage 72 of the voltage step-down converter 68 is 1.05v.

In practice, the generated voltages 64 and 72 may comprise wave forms which switch between two output voltage levels at a high frequency, and have an average of 2.1v and 1.05v respectively. Using high-frequency switching ensures that the components which receive the switching supply voltages are not substantially affected by the switching operation. Advantageously the voltages 64 and 72 are low-pass filtered to produce substantially constant voltages.

The reduced voltage 72 is supplied to the demodulator 12 via a switch 80 which is controlled by a control signal 82 from the controller 22. The control signal 82 controls whether an output 84 of the switch 80 is equal to zero volts or the input voltage 72.

The operation of the receiver 10 will now be described with reference to component control wave forms shown in Figures 5a to 5g. Voltage is given on the vertical axis, and time is given on the horizontal axis.

Figure 5a shows the cycle number of the current clock cycle within the receiver 10. The sequence repeats every 8 cycles.

The sequence starts at time $T=0$ with cycle 1. In Figure 5b the line 100 represents the power supply 84 to the demodulator 12, as controlled by the switch 80. At the start of the cycle, the controller 22 opens the switch 80 and the power supply 84 changes from zero volts to 1.05 volts. The supply 84 remains at 1.05v for a "power up time", which is the length of the first cycle.

Whilst the demodulator 12 has power (i.e. the supply voltage 84 is 1.05v) the output 16 comprises the recovered audio signal although this may not be accurate immediately after supplying the demodulator 12 with power. Therefore the demodulator 12 is allowed to settle before a sample is taken.

Figure 5c shows the control voltage 20 for the sample and hold circuit 18. The voltage remains low for a "settle time" after power up of the receiver/demodulator 12 which allows the receiver/demodulator 12 to settle and produce an output 16 which is accurate or at least acceptable. After the settle time, the control voltage 20 is driven high for a short period. During this period, the output 24 of the sample and hold circuit 18 tracks the input voltage 16. At the end of this short period, the control voltage 20 is driven low again, and the output 24 remains constant until the control voltage is driven high in the next sequence. The voltage must be driven low before the power 84 to the receiver/demodulator 12 is deactivated by the switch 80, which occurs at the end of cycle 1.

Figure 5d of Figure 2 shows an example of the output 24 of the sample and hold circuit 18, when the output 16 of the demodulator 12 is an increasing wave form.

The receiver 10 works on the principle that a sample is taken once every 8 cycles, and that sample is supplied to the class-D amplifier for the remaining 7 cycles. In order to produce an acceptable audio output, the frequency at which a sample is taken must be at least twice that of a maximum frequency which is to be amplified (Shannon sampling criteria). In the embodiment described, it is desired to reproduce all frequencies below 10kHz, which gives an acceptable audio output quality. Therefore a sample must be taken at least at a frequency of 20kHz (once every 50 microseconds). As a sample is taken every 8 clock cycles, it follows that the clock frequency must be at least 160kHz. However these figures relate only to the present embodiment. If for example the maximum frequency to be reproduced is 20kHz, then a clock frequency of at least 320kHz would be required. Alternatively, if a sample were taken every 4 clock cycles and the maximum frequency that is to be reproduced is 10kHz, then the clock frequency could be reduced to 80 kHz. A person skilled in the art is able to select the number of cycles between samples and the clock frequency based on the particular application and the components available.

In the current embodiment the demodulator is supplied with power for 1/8 of a complete sequence. Therefore, it consumes approximately 1/8 of the power that would be consumed if it were operated continuously, although in practice it will probably consume slightly more power due to losses in powering up the demodulator 12 and in components such as the switch 80.

Figure 5e shows the switching operation of the class-D amplifier 26. The waveform switches from +1 to -1. It is assumed that the class-D amplifier includes a transistor H-bridge to which the speaker 30 is connected. Therefore, when the waveform (E) is at +1, the speaker is connected between the supply voltage and ground in a first polarity, and when the waveform is at -1 the speaker is connected in a second, opposite polarity. The waveform is at +1 at the start of each cycle and switches to -1 at some point depending on the level of the audio signal sample 24.

However, during cycle 1, which is the cycle in which a sample is taken, the class-D amplifier is inhibited, that is it is prevented from switching. The controller 22 in cycle 1 supplies a control signal to the amplifier 26 instructing it not to switch. Instead, the output voltage of the class-D amplifier is set to zero by simultaneously activating either switches Q1 and Q3 or Q2 and Q4, as shown in Figure 4. As a result, the amplifier, loudspeaker and other components do not produce radio-frequency interference.

The controller maintains the class-D amplifier in this state (shown as a shaded block 108 in Figure 5e) for a “quiet time”, which is the length of a clock cycle. Therefore, the sample is taken during a period and the class-D amplifier and/or associated load components do not generate radio frequency interference. As a result, the class-D amplifier and other components do not have to be housed within a metal screening container in order to protect other parts of the receiver 10 from interference.

At the end of the first clock cycle, normal operation of the class-D amplifier is resumed.

Figure 5f shows a switching operation of the boost converter 68. The waveform 110 represents an internal switching voltage of the boost converter. The output voltage is variable as it depends on the supply voltage from the battery 60. Therefore, the duty cycle of the waveform 110 is adjusted by a control loop to ensure that the desired 2.1.V output is obtained.

However, during cycle 1, the boost converter is prevented from switching by a control signal 66 from controller 22. As a result, the switching operation is avoided and radio frequency interference from the switching operation is not produced. This state of the boost converter is maintained for a "prevention time" which is equal to one clock cycle. The sample is taken in this time, and hence is cleaner than it would have been had the boost converter switched in this time.

For the remaining cycles 2 to 8, as shown in Figures 5a to 5f, the sample voltage is maintained constant, and the class-D amplifier provides a constant average signal to the output speaker 30 for those cycles. Because one cycle frequency is much greater than the audio output frequency, the fact that the amplifier does not switch during cycle 1 has no noticeable effect on the audio output quality. Similarly, as the sampling frequency is sufficient to reproduce the audio signal to an acceptable quality, the fact that the sample voltage is held constant for multiple clock cycles and does not continuously track the audio signal does not substantially effect output quality. This is because the sample rate is greater than twice the highest output frequency of the amplifier.

The switching operation of the voltage step-down converter 68 is shown in Figure 5g. This shows a square wave with a duty cycle of 50% and a frequency of half the clock frequency. This gives an average voltage which is half of the supply voltage to the step down converter.

Figure 6 shows a typical voltage step-down converter 68 suitable for use with the embodiment of the invention shown in Figure 1. The voltage step-down converter 68 comprises a JK flip-flop 120 wired such that with each clock signal its Q and Q' outputs alternately change between logical 1 and logical 0. A similar arrangement can be

implemented in other flip-flop architectures. Thus, the Q output of the flip-flop 120 will be a square wave at half the clock frequency. The clock is provided via control signal 70 from controller 22 as shown in Figure 1. The Q output is fed to a storage capacitor 122 via an inductor 124. The inductor capacitor combination averages the output of the flip-flop to obtain a 1.05 volt supply which constitutes the output voltage 72. A zener diode 126 provides protection for the flip-flop against inductively induced currents during the switching of the Q output.

The voltage step-down converter 68 only switches at the start of each clock cycle. Therefore, it does not produce radio frequency interference at a time when it would affect the quality of the sampled audio signal 24. As a result, it is not necessary to prevent the voltage step-down converter from switching during cycle 1 when the sample is taken.

Thus, interference can be reduced and the accuracy of the sampled signal improved by taking a sample at a time when no switching events occur within the receiver 10. This is achieved by preventing certain components from switching. However, it may not necessary to prevent all switching components from switching, as preventing each component in isolation contributes to an overall reduction in the effects of interference.

The present invention is not limited to radio receivers which have antennas and receivers/demodulators. Interference from switching components can affect many circuit components as well as a receiver and demodulator. Therefore, the present invention can be used in circuits which do not have these two components but contain switching components. For example, other types of portable audio devices such as CD and MP3 players may contain a class-D amplifier. Preventing the amplifier from switching whilst data is, for example being read from the CD into a buffer memory, may reduce the effects of interference on the sample from the class-D amplifier. The present invention can also be used within devices which include other switching components such as switched-mode power supplies when their operation can be temporarily suspended or perturbed in order to prevent switching from occurring during a sensitive moment for some signal or data processing device.

The receiver 10 constituting an embodiment of the invention also consumes less power than a receiver which includes a receiver/demodulator 12 which is powered continuously. The receiver/demodulator 12 in the present embodiment uses approximately 1/8 of the power that it would normally consume, as described above. This is not essential for reducing interference in the receiver 10, but is desirable for extending the life of the battery 60. In other devices which use other sources of power such as solar power it is still desirable to reduce power consumption.

Although in the embodiment described above the demodulator 12 receives power only for 1/8 of the time, depending on the clock frequency there may be insufficient time for the demodulator 12 to power up and settle before a sample is taken. Therefore, other approaches can be used. Firstly, the demodulator 12 can be powered up in a clock cycle before the clock cycle in which a sample is taken, and can receive power for multiple clock cycles. This increases the time in which the demodulator 12 is allowed to settle.

Alternatively or additionally, certain components inside the receiver/demodulator 12 can be arranged to receive power continuously or to be powered up earlier than the rest of the demodulator 12. Therefore components such as those which take longer to settle can be powered continuously or given longer to settle. Many receiver/demodulators contain a local oscillator (LO) which would typically take longer to settle than many other circuit components, and is therefore an example of a component which can be powered continuously or can receive power earlier. Some components, however, still receive power for shorter periods of time and therefore the receiver/demodulator 12 still consumes less power than one which is powered continuously.

In an alternative embodiment of the invention, the class-D amplifier 26 and/or the boost converter 62 do not need to be placed in a quiescent state in order to take a sample. In this embodiment, the receiver 10 predicts when a switching event is to occur, and uses this data to take a sample during a time period when a switching event will not occur.

For example, the receiver 10 can predict when the class-D amplifier will switch by monitoring the transistor control signals. In this way a switching event will be known

before the transistors are switched. Alternatively, the level of the sampled audio signal can be monitored to predict when a switching event will occur.

Similarly, a switching event of the boost converter 62 can be predicted. However, it may be difficult to predict a length of time in which a switching event will not occur in the amplifier 26 or converter 62, which is sufficiently long in order to allow the demodulator 12 to settle and to take a sample. It may therefore be advantageous to monitor only the amplifier 26 or converter 62. The other component may advantageously be prevented from switching.

In this way, reduced effects from interference is achieved, and the amplifier 26 and/or the converter 62 need not be prevented from switching.

Figure 7 schematically shows a typical portable audio device 200 which plays compressed audio files such as MP3 files. Therefore, the device 200 is an MP3 player or the like. Such devices are often powered using one or more batteries. It is therefore desirable to reduce power consumption.

The device 200 includes a permanent storage device 202 which stores the compressed audio files. The permanent storage device 202 may comprise a flash memory card, CD, hard disk or other storage device suitable for use in portable audio devices.

The device 200 also includes a decoder 204. The decoder 204 is arranged to receive compressed audio data from the storage device 202, decode the data and store the decoded data in a further storage device comprising RAM 206, although other temporary or permanent storage devices may be used. A digital-to-analogue converter (DAC) 207 is connected between the RAM 206 and amplifier 208, which converts the digital decoded audio data into an analogue waveform. The analogue signal is then provided to an amplifier 208 which amplifies the audio data appropriately and provides it to a loudspeaker or headphones 210.

Each component 202, 204, 206, 207 and 208 may receive power and/or control signals from a controller 212. The operation of the device 200 will now be described.

Data from the RAM 206 which has been decoded is provided continuously to the DAC 207 and amplifier 208. The rate at which the data is “used” is constant and does not depend on the content of the data. The data may also need to be periodically refreshed in a known manner if the storage device 206 comprises dynamic RAM. Therefore, the dynamic RAM is powered continuously. The amplifier 208 also receives power continuously as its output is continuous.

If the speed at which the decoder retrieves data from storage device 202, decodes it and stores it in the RAM is greater than the speed at which the data in the RAM is used, then the decoder does not have to be operated continuously and only needs power when the RAM 206 needs to be topped up with decoded data.

The decoder 204 need only be operated in order to “top-up” the RAM 206 when the amount of unused data in the RAM is running out. The controller 212 is arranged to power up the decoder 204, instruct it to decode a certain amount of data from the permanent storage device 202, and store it in the RAM 206. The new decoded data can overwrite used data in the RAM 206. The RAM 206 is preferably operated in a manner similar to a first-in-first-out (FIFO) stack which is known to those skilled in the art.

Therefore, the power consumption of the decoder is reduced as it only receives power for some of the time. Furthermore, the permanent storage device 202 (and/or associated controllers, not shown) need only be powered whilst the decoder 204 is decoding data, and also for a settling time if appropriate before the decoder starts to decode data. For example, if the device 202 is a CD or hard disk, the disk may be spun up to speed, used for the appropriate length of time, and depowered again. Alternatively, the disk can be spinning continuously and an associated controller which controls other parts such as a reading head can be powered only when required.

It may also be advantageous, if the amplifier 208 is a switching amplifier such as a class-D amplifier, to prevent the amplifier from switching when a digital to analog conversion is in progress. This may reduce the effects of interference from the switching action. Alternatively, a conversion can be taken when a switching event will not occur, for example, by predicting the time at which the amplifier will switch.

In an alternative embodiment, the storage devices 202 and 206 may be the same storage device which operates continuously. The decoder could be powered up when required, and could decode data from the storage device and write it back to a different area of the storage device.

The frequency and length of time for which the decoder must be in operation depends on the size of the RAM 206 amongst other things. For example, if the RAM 206 is larger, the decoder may have to run for longer to fill it, but would then be inactive for a longer length of time as the decoded data is used.

Claims

1. An electrical device (10) comprising a signal source (12), a switched mode device (26, 62) and a sampling circuit (18), in which the sampling circuit is adapted to periodically sample an output (16) of the signal source during a time period when the switched mode device is not switching.
2. A device (10) as claimed in claim 1, in which interference from the switched mode device (26, 62) is periodically reduced for a predetermined quiet time, and the sampling circuit (18) takes a sample during the quiet time.
3. A device (10) as claimed in claim 2, in which the switched mode device (26, 62) is a switching amplifier (26) and interference is reduced by preventing the switching amplifier from switching during the quiet time.
4. A device (10) as claimed in claim 1, in which the switched mode device (26, 62) is a switching amplifier (26), and the time at which the sampling circuit (18) takes a sample is adjusted to ensure that the sample is taken when the switching amplifier is not switching.
5. A device (10) as claimed in any one of the preceding claims, in which the signal source (12) is a demodulator circuit.
6. A device (10) as claimed in claim 5, in which power (84) is supplied periodically to the demodulator circuit (12) only for a predetermined power time, and the sampling circuit (18) takes a sample during the power time.
7. A device (10) as claimed in claim 3, in which the switching amplifier (26) is periodically prevented from switching for a predetermined quiet time, and the sampling circuit (18) takes a sample during the quiet time.

8. A device (10) as claimed in any one of the preceding claims, in which the signal source (12) and/or the switched mode device (26, 62) is/are powered by a switched mode power supply (62), and the sampling circuit (18) takes a sample when the switched mode power supply is not switching.
9. A device (10) as claimed in claim 7, in which the switched mode power supply (62) is periodically prevented from switching for a predetermined prevention time, and the sampling circuit takes a sample during the prevention time.
10. A method of recovering a signal, comprising the steps of:
 - a) periodically taking a sample of a signal source (12) when a switching amplifier (26) is not switching; and
 - b) providing the sample to the switching amplifier.
11. A method as claimed in claim 10, in which the step of periodically taking a sample comprises the steps of:
 - determining a time when the switching amplifier (26) will not be switching;
 - and taking the sample at that time.
12. A method as claimed in claim 10, in which the step of periodically taking a sample comprises the steps of:
 - reducing interference from the switching amplifier (26) for a predetermined quiet time; and
 - taking the sample during the quiet time.
13. A method as claimed in claim 12, in which the step of reducing interference comprises the steps of:
 - deactivating switching of the switching amplifier (26); and
 - reactivating switching after the quiet time.

14. A method as claimed in any one of claims 10 to 13, in which the signal source (12) receives power (84) only for a predetermined settle time before the sample is taken and during the step of taking the sample.
15. A controller (22) for controlling a receiver (10) to carry out the method as claimed in any one of claims 10 to 14.
16. A radio including a device (10) as claimed in any one of claims 1 to 9.
17. A compressed data decoder (204), comprising
 - an input for receiving compressed data from a first data store (202);
 - an output for sending decoded data to a second data store (206);

wherein when it is desired to replenish decoded data within the first data store, the decoder is arranged to receive full power, decode compressed data from the first data store, output decoded data to the second data store at a faster rate than that at which the decoded data is to be used, and receive no power or partial power until it is desired to replenish decoded data again.
18. A compressed audio player (200) comprising a compressed data decoder (204) as claimed in claim 17, in which the first data store (202) comprises one of a compact disc (CD), a hard disk and a flash memory card.
19. A compressed audio player (200) as claimed in claim 18, in which the second data store (206) comprises RAM.
20. A method of decoding compressed data stored in a first data store (202), comprising the steps of:
 - (a) continuously using decoded data in a second data store (206);

(b) when it is desired to replenish the second data store with decoded data, performing the steps of:

- (i) providing full power to a decoder (204);
- (ii) using the decoder to decode compressed data from the first data store to form the decoded data;
- (iii) storing the decoded data in the second data store; and
- (iv) providing no power or partial power to the decoder.

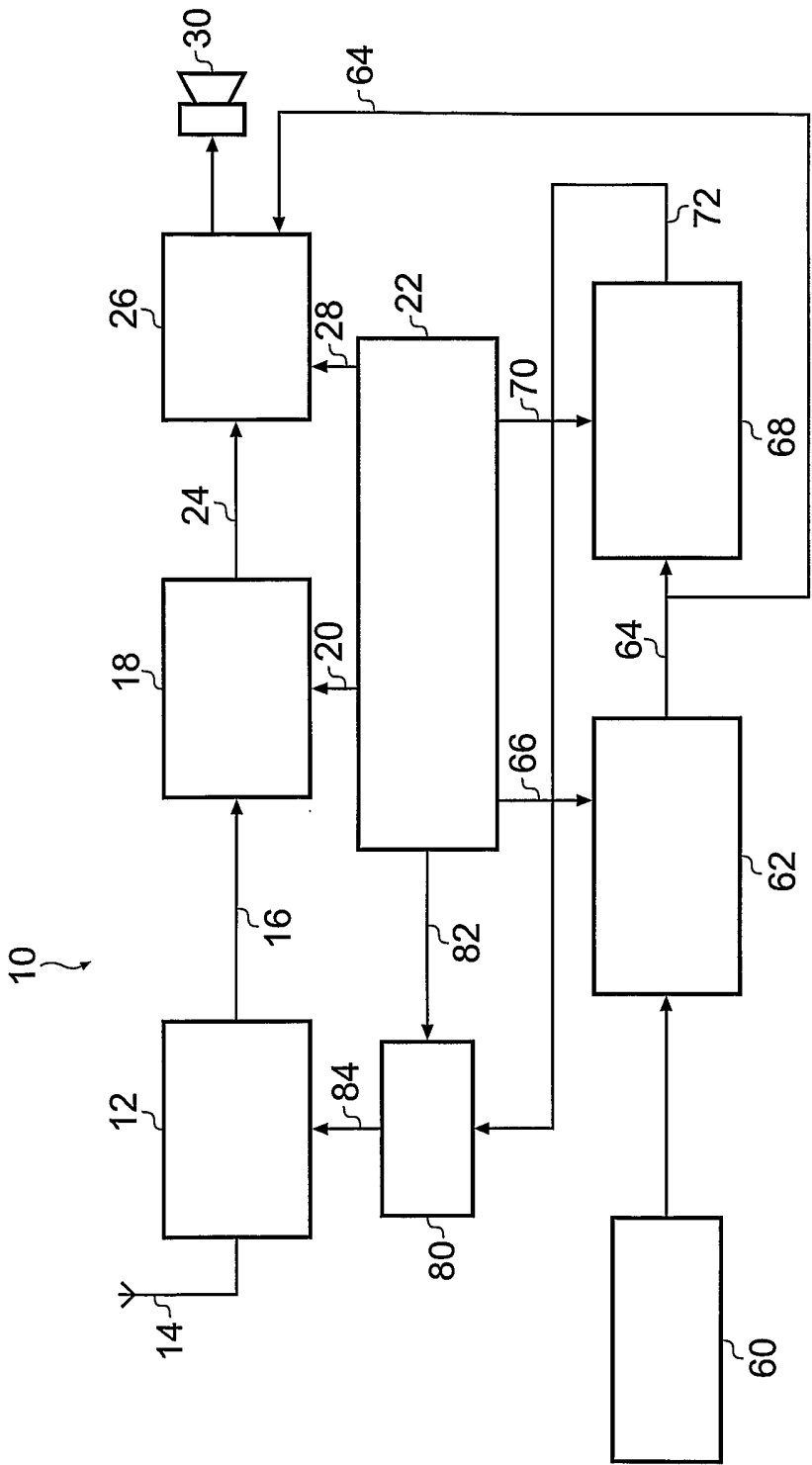


Fig. 1

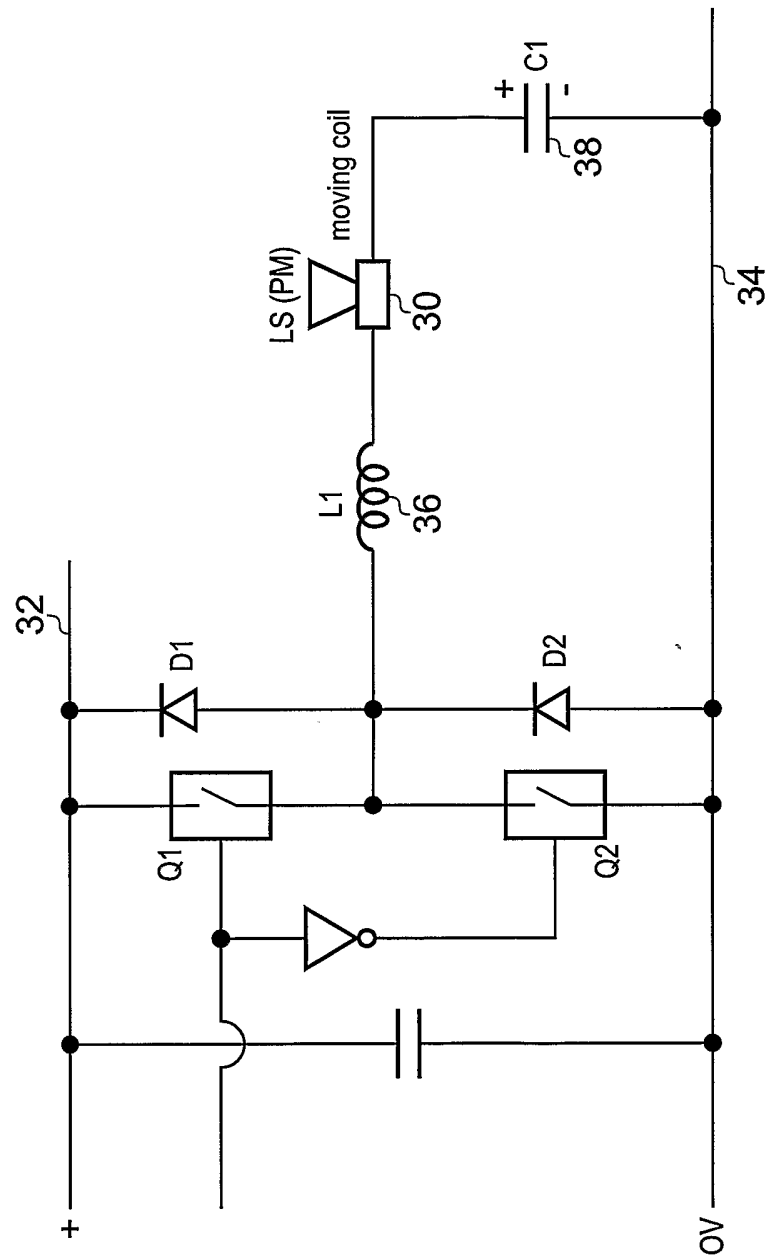


Fig. 2

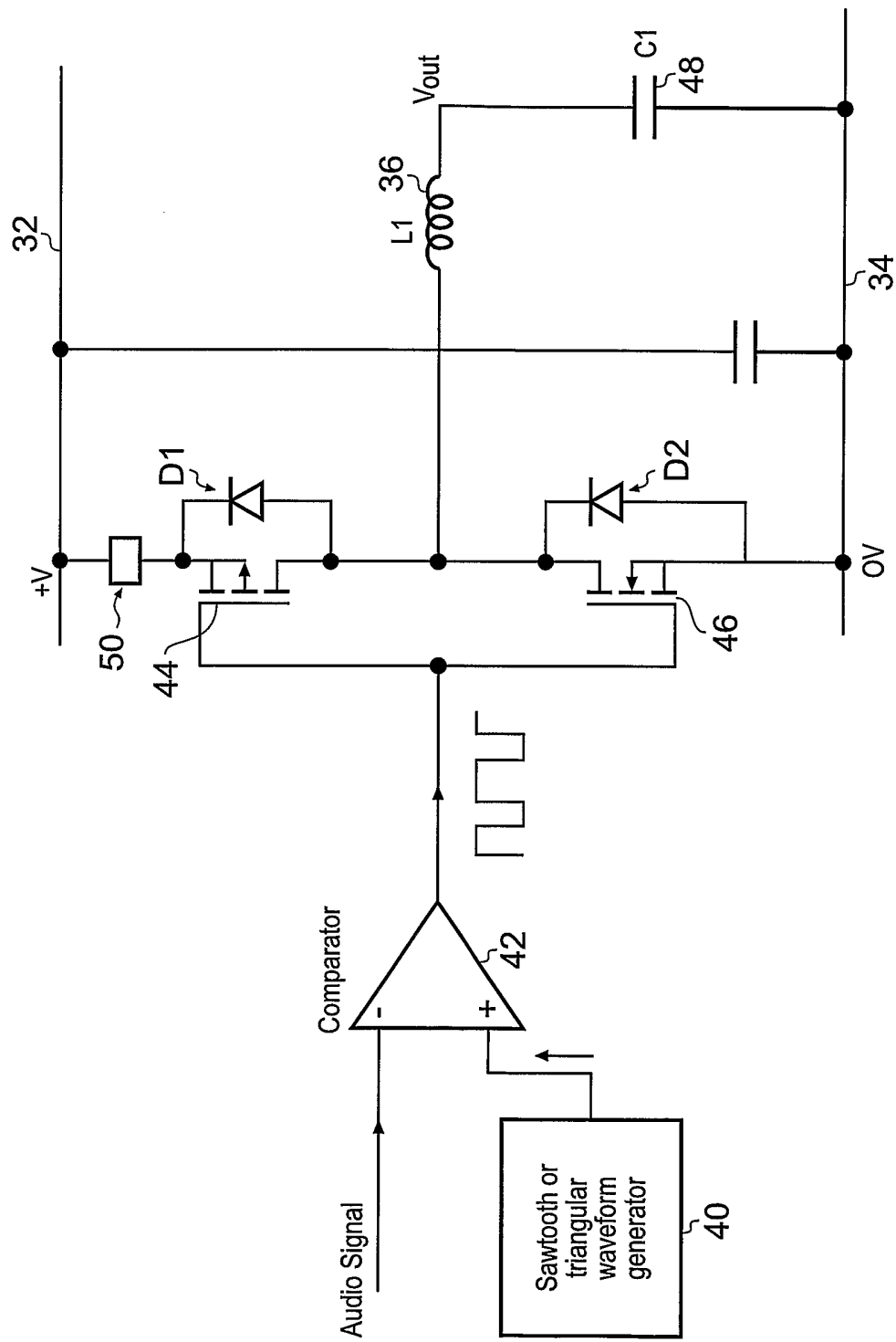


Fig. 3

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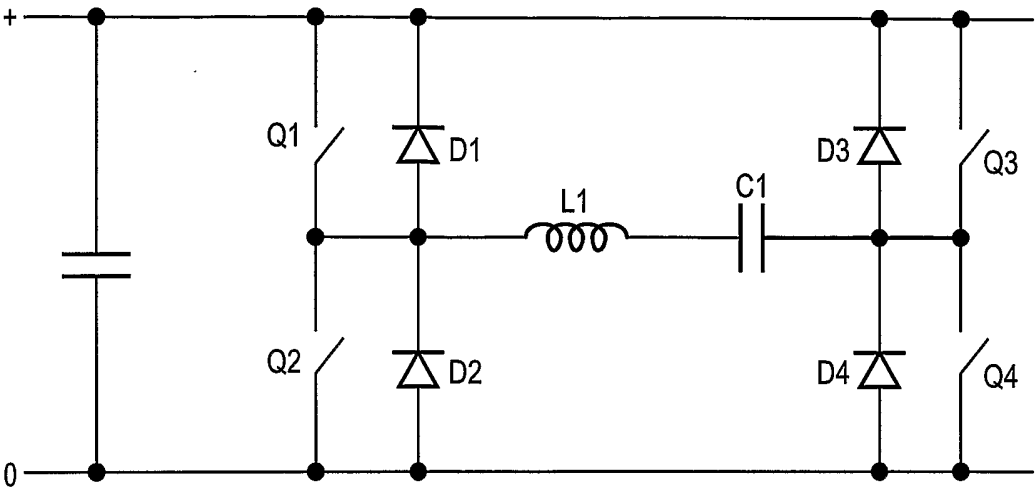


Fig. 4

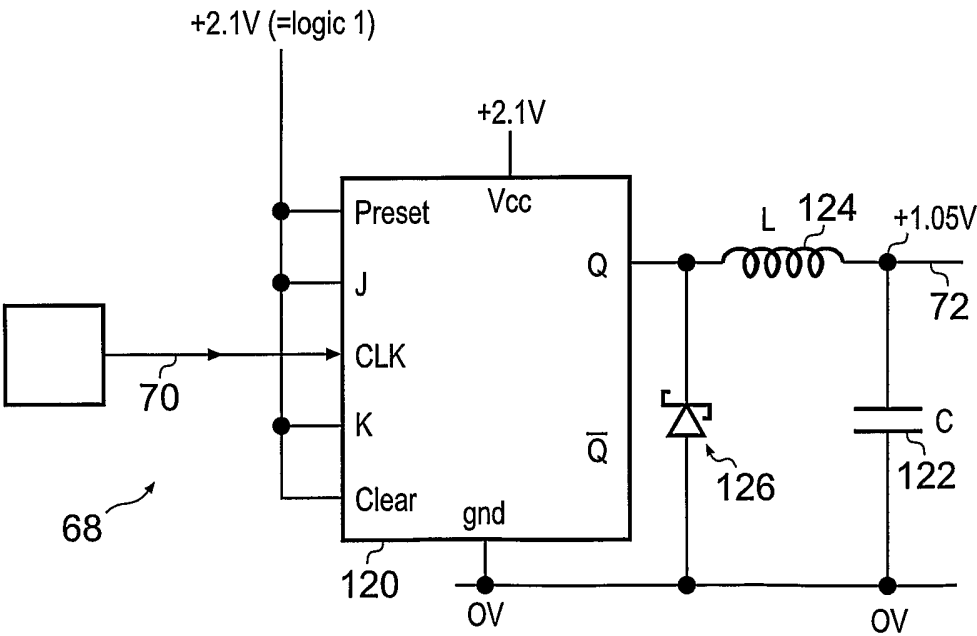


Fig. 6

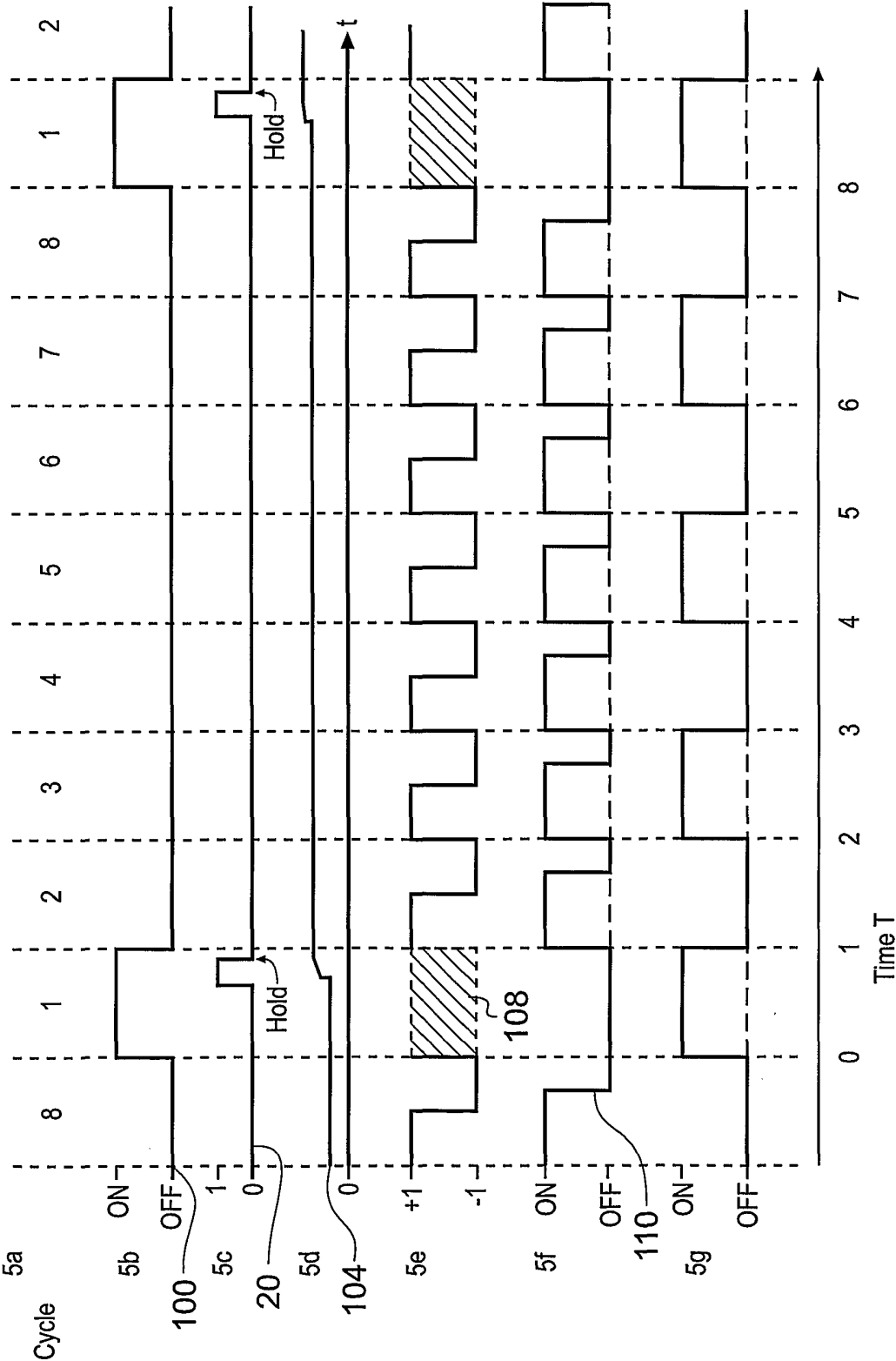


Fig. 5

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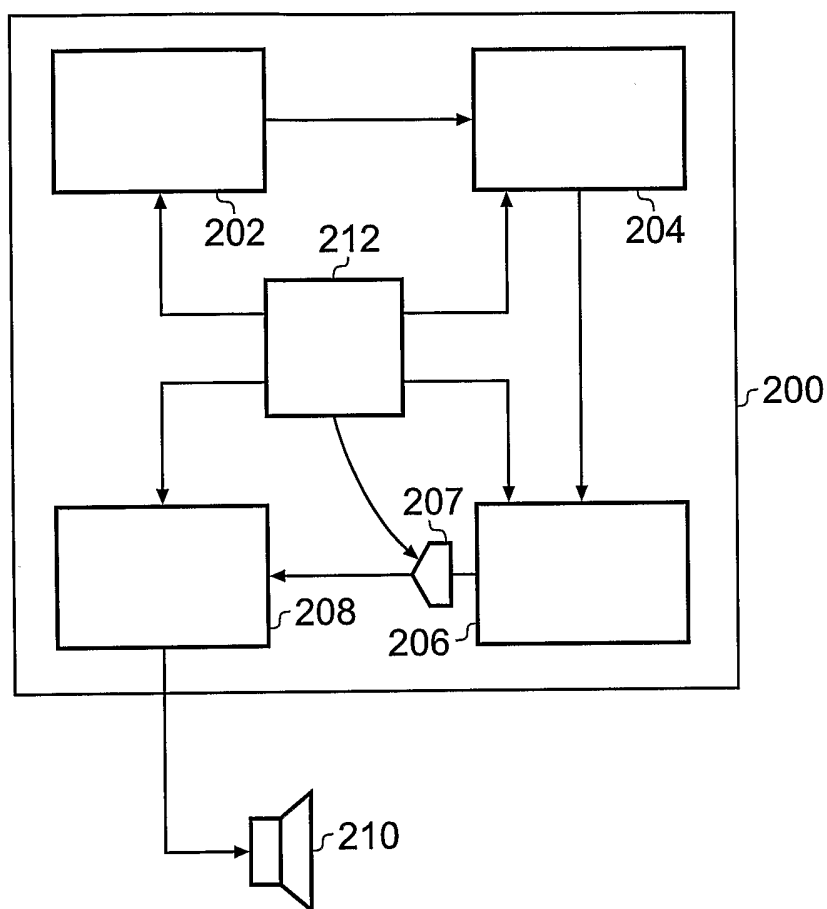


Fig. 7