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Takagi et al.

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[54] **DELAY TIMING CIRCUIT**

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[30] **Foreign Application Priority Data**

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[52] **U.S. Cl.** ..... **307/293**, 317/141 S, 328/131

[51] **Int. Cl.** **H03k 17/26**

[58] **Field of Search** ..... 307/293, 10 LS; 315/82, 315/77, 83; 317/141 S; 328/129–131

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[57] **ABSTRACT**

A timer apparatus includes a timer circuit utilizing the charging and discharging of a capacitor. The timer circuit comprises a timing capacitor adapted to charge in the direction for cutting-off a transistor at the setting time, a switch adapted to apply the voltage in the direction for discharging of said capacitor, and a transistor adapted to be turned conductive after a given time from the commencement of discharging. Said timer has excellent temperature and voltage characteristics without employing a Zener diode and FET, is hardly affected by the D.C. current amplification factor of said transistor and the open-circuit voltage of a relay and can determine a set time to be several seconds through dozens of minutes.

6 Claims, 4 Drawing Figures

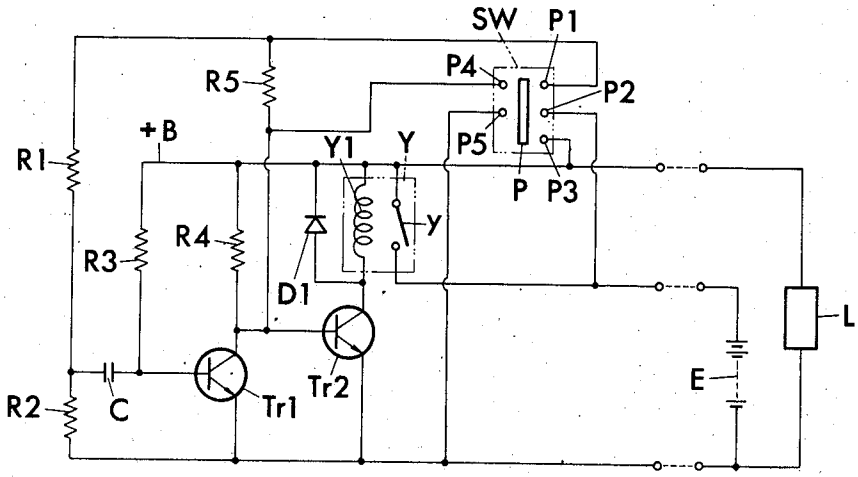
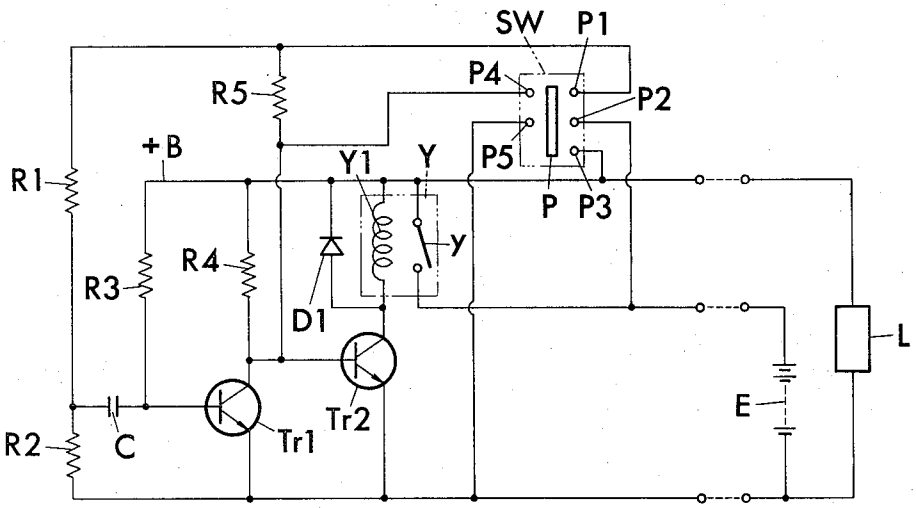


FIG.1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P1
P4
P2
R5
+B
Y1
Y
P5
P
P3
R1
y
R3
R4
D1
L
Tr2
E
Tr1
R2
C

FIG.2

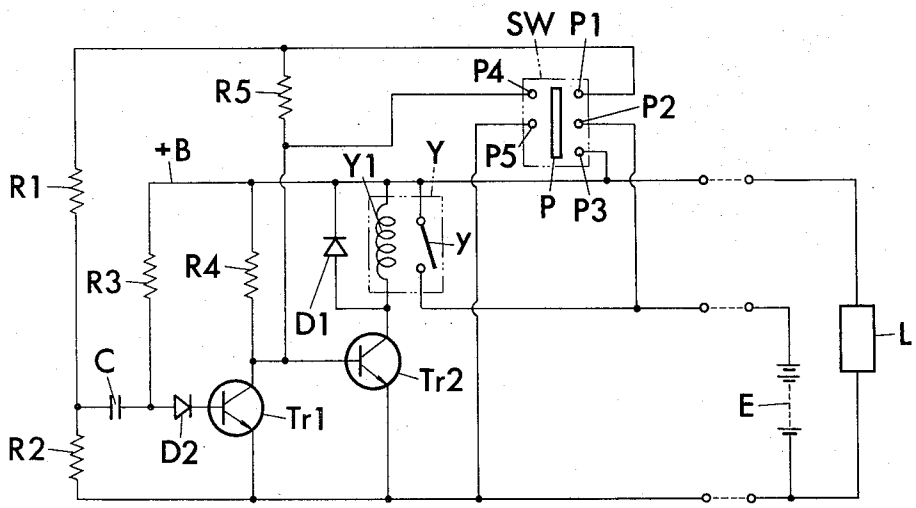
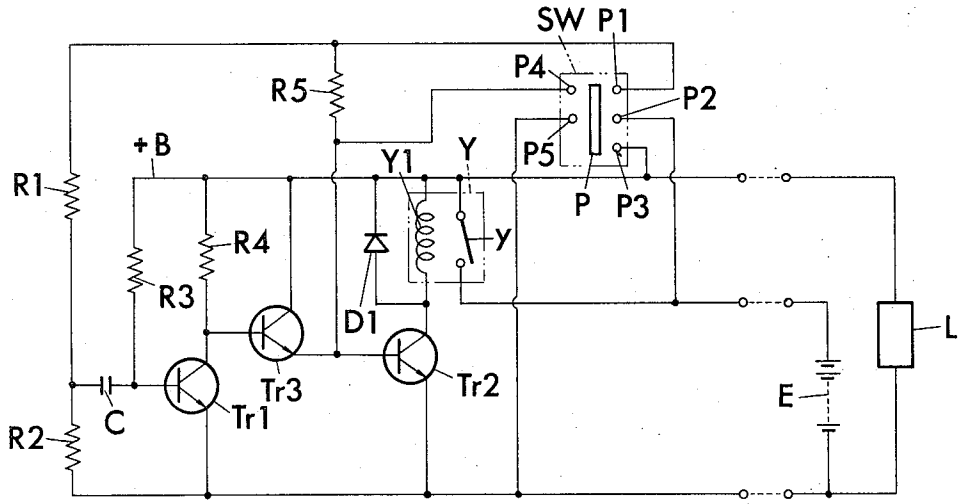

SW
P1
P4
R5
P2
+B
Y1
Y
P5
P
P3
R1
y
R3
R4
D1
L
Tr2
C
E
Tr1
R2
D2

FIG.3


SW P1
P4
P2
R5
+B
Y1
Y
P5
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P3
R1
R4
R3
y
D1
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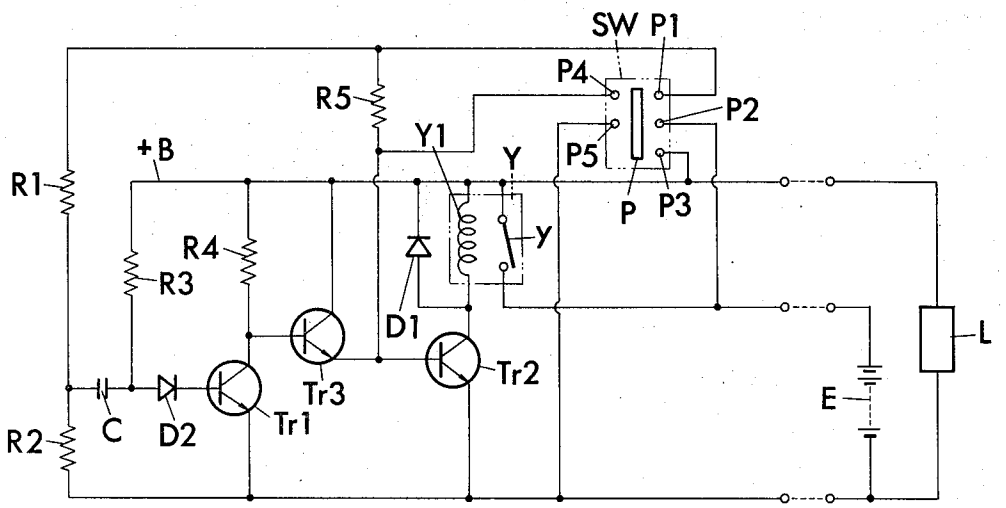
Tr3
Tr2
Tr1
E
C
R2

FIG.4


SW P1
P4
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+B
Y1
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Tr3
Tr2
Tr1
E
C
D2
R2

DELAY TIMING CIRCUIT

The present invention relates to a timer device and more particularly to a timer device capable of determining a set time to be several seconds through dozens of minutes by utilizing semiconductor circuits.

Various types of prior art timers are known; for instance, a thermal-responsive type (bimetal) timer, a motor type timer, or an electronic (a semiconductor) type timer, etc. In a timer for an automobile which utilizes a D.C. source as its power source (such as a timer for a defogger, a timer for an automatic choke, a warning timer for seatbelts, an off-delay timer for headlights and a timer for turning out a headlight after a given time of period has passed since an automobile stops), the voltage of its power source varies, so that a motor type timer cannot be utilized and a thermal-responsive timer has been used in most cases. Such conventional thermal-responsive type timers are subject to the influence of the ambient temperature and therefore apt to be inaccurate in setting a predetermined time, and it further has a disadvantage that a set time for a subsequent operation is by far shortened due to the thermal inertia in cases where sequential operation is effected.

In recent years, as the cost of the semiconductor parts has fallen, an electronic type timer device has come to be employed which enables a timer to be small-sized and lighter and capable of obtaining a set time of several seconds to dozens of minutes and increasing the reliability thereof by eliminating movable parts. Stated illustratively, in the conventional electronic type timer, a set time has been determined upon comparison of the discharge level of a parallel circuit comprised of a timing capacitor and a timing resistor, with the trip level of a Schmidt circuit or the threshold voltage between the base and the emitter of a transistor itself, or upon comparison of the charging voltage applied from a power source to a timing capacitor through a timing resistor, with the trip level of a Schmidt circuit or the threshold voltage between the base and the emitter of a transistor. However, the above-mentioned circuits are easily affected by the variation of the source voltage and therefore necessitate employment of a Zener diode to improve the voltage characteristic. Furthermore, where such a timer is constructed to have a relatively long set time, the variation of the trip level of a Schmidt circuit or the capacitor voltage in the vicinity of the threshold voltage of a transistor is made less severe, so that the circuit is not only apt to be affected by noise but is sensitive to variations in ambient temperature and source voltage, so as to be liable to produce an error in the set time. Further, in some such circuit structures, wherein the transistor for driving relays passes slowly through the active region in response to the slack variation of the capacitor voltage, the open-circuit voltage of a relay or the D.C. current amplification factor of a transistor become the elements to determine the set time. The open-circuit voltage of the relay or the D.C. current amplification factor of a transistor not only has fluctuation in the measured value, but also varies in the value with variation in the environmental temperature, thereby increasing the temperature-dependency of the set time and reducing the accuracy thereof. Another disadvantage, due to the fact that the transistor for driving a relay passes slowly through the active region is that the collector loss of this transistor is increased and it becomes necessary to provide with a transistor having such a large collector loss as can counterbalance therewith, which would raise the cost. The fact that the transistor for driving a relay passes slowly through the active region means that at first on the exciting coil of the relay is applied a full source voltage, then such voltage gradually decreases to an open-circuit voltage near the end of the set time. Therefore, when the transistor is in the active region, a sufficient exciting voltage is not applied thereto thus, even with only a slight vibration, the relay may possibly be opened, although the set predetermined time has not yet passed.

The present invention has been made to overcome the above-mentioned disadvantages. It is therefore an object of the present invention to provide a timer which has excellent temperature and voltage characteristics without employing such expensive semiconductor elements as a Zener diode or a field-effect transistor and which is not affected by the D.C. current amplification factor of the transistors employed and which is the open voltage of the relay and capable of obtaining a set time of several seconds through dozens of minutes.

Another object of the present invention is to provide a timer which is adapted to expend no electric power when operates as a timer, due to the complete interruption of the circuits and loads from power sources, and to produce no erroneous operation due to external noise even with a high impedance circuit.

A further object of the present invention is to provide a timer which employs no elements other than the fundamental circuit elements for voltage regulation and temperature compensation as a timer, and which is capable of, in its performance, being fully stable against the variation of power supply voltage or ambient temperature in normal use and which can be manufactured at reasonable cost.

The above, as well as still further objects, features and advantages of the present invention will become apparent upon consideration of the following detailed description of several specific embodiments thereof, especially when taken in conjunction with the accompanying drawings, wherein:

According to the present invention, there is provided a timer device including a timer circuit utilizing the charging and discharging of a capacitor, comprising a timing capacitor adapted to charge in the direction for cutting-off a transistor at the time of setting; a switch adapted to apply a voltage in the direction for discharging the charged electric charge of said capacitor to cause such discharge; and said transistor adapted to be turned conductive after a predetermined period of time has passed from the commencement of discharging, thereby to determine a set time.

FIG. 1 is a circuit diagram of one preferred embodiment of the present invention;

FIGS. 2 through 4 are circuit diagrams of modified embodiments in accordance with the present invention.

Referring now to the drawings, and more particularly to FIG. 1 thereof, there is illustrated a circuit of one embodiment of the invention. E designates a D.C. power source, SW a switch for setting and resetting, R_1 a charging resistor, one terminal of which is connected with a setting contact P_1 of the setting-resetting switch SW and the other terminal of which is connected with a positive electrode or a timing capacitor C. R_2 is a re-

sistor for keeping the positive electrode of said capacitor at an earth-potential while the circuit functions as a timer. One terminal of resistor R_2 is connected with the positive electrode of said timing capacitor C and the other terminal thereof is connected with a negative terminal of said power source E. R_3 is a timing resistor for charging and discharging the timing capacitor C, one terminal of which resistor is connected with a +B power supply line and the other of which is connected with the junction of the negative electrode of said timing capacitor C and a base of a first stage transistor Tr_1. R_4 is a collector resistor one terminal of which is connected with the +B power source line and the other terminal of which is connected with both a collector of the first stage transistor Tr_1 and a base of a second stage transistor Tr_2. The emitters of the first and the second stage transistors Tr_1 and Tr_2 are connected to the negative terminal of the power source E. R_5 is a base resistor, one terminal of which is connected with said contact P_1 of the setting-resetting switch SW and the other terminal of which connects with the base of the second stage transistor Tr_2. Y is a relay for controlling a load current and includes a coil Y_1, one terminal of which is connected with the +B power supply line and the other terminal of which connects with a collector of the second stage transistor Tr_2. Relay *y* further includes a contact *y*, one terminal of which is connected with a positive terminal of the power supply E and the other terminal of which connects with the +B power supply line. D_1 is a diode, for preventing a counter electro-motive force connected in parallel with the coil Y_1 of said relay Y. Concerning the setting-resetting switch SW, a setting contact P_2 is connected with the positive terminal of the power supply E and a setting contact P_3 connects with the +B power supply line, respectively, while a resetting contact P_4 is connected with the base of the second stage transistor Tr_2 and another resetting contact P_5 connects with the negative terminal of the power supply E, respectively. L is a load having a terminal connected with the negative terminal of the power supply and another terminal connected with the +B power supply line.

The operation of the above-mentioned circuit will be explained in detail as follows. When the movable contact P of the setting-resetting switch SW is turned to the setting side contacts P_1, P_2 and P_3, the positive terminal of the power supply E is connected with the +B power supply line of said circuit. Therefore, the feed to the load L is commenced and the charging current flows from the contact P_1 through the charging resistor R_1, timing capacitor C and the base-emitter of the first stage transistor Tr_1 to charge the timing capacitor C it up to the following voltage.

$$Vo = R_2/R_1 + R_2\,E - Vd$$

where Vo is the charging voltage of a timing capacitor C, Vd the base-emitter forward voltage of the transistor Tr_1 and E the power supply voltage.

Since there is determined

$$\frac{R_3}{h_{FE} \text{ of } Tr_1} \gg R_5,$$

the transistor Tr_2 is turned on even when the transistor Tr_1 is turned on.

In other words, the base current is supplied to the second stage transistor Tr_2 through the base resistor R_5 and accordingly said transistor Tr_2 is made conductive to excite the coil Y_1 of the relay Y and close the contact y. Then, when the setting-resetting switch SW is released, the movable contact P of said switch SW is returned to a neutral position and the switch side of the charging resistor R_1 is disconnected from the power supply E, so that the positive electrode side of the timing capacitor C is maintained nearly at the earth potential. At the same time, the voltage at the base of the first stage transistor Tr_1 becomes $-Vo$ and said transistor Tr_1 is cut off, while the second stage transistor Tr_2 maintains the conductive condition by the current flowing through the collector resistor R_4, even if no current flows through the base resistor R_5, thus maintaining the relay Y closed.

On the other hand, upon releasing the setting-resetting switch SW, the base potential of the first stage transistor Tr_1, which is reversely biased to $-Vo$, increases towards the power supply voltage by the current supplied from the +B power supply line through timing resistor R_3. Thus, when the base potential becomes the base-emitter threshold voltage Vd of the transistor Tr_1, said first stage transistor Tr_1 becomes conductive, and the collector of said transistor Tr_1 becomes nearly the earth potential. Resultantly, the second stage transistor Tr_2 is cut off, and the relay Y is made open to interrupt the current to the load L, thereby terminating one delay operation. When the timer operation comes to an end, the contact *y* of the relay Y is opened and both the load L and the timer circuit itself will be completely separated from the power supply E, as the movable contact P of the setting-resetting switch SW stands in the neutral position.

After the setting-resetting switch SW has been thrown into the setting side, if it is required for some reasons to reset before the set time has been passed, the movable contact P of the setting-resetting switch SW is thrown into the resetting side contacts P_4 and P_5 to short-circuit the base-emitter of the second stage transistor Tr_2 and forcibly cut-off said transistor Tr_2, thereby making the contact y of the relay Y open regardless of the operation of the first stage transistor Tr_1. Once the relay Y is opened, the power supply of the timer circuit is interrupted simultaneously and complete resetting will be made.

As is mentioned above, the delay time T in accordance with the present invention corresponds to the time that the first stage transistor Tr_1 is cut-off by means of a timing capacitor C and can be expressed as follows:

$$T = CR_3 \log\left\{1 + \frac{a}{1 - \frac{Vd_1}{E} - b\frac{Vd_2}{E}}\right\}$$

where

$$a = R_2/R_1 + R_2\,,\quad b = R_2/R_1 + R_2 + R_5$$

Vd_1 = the base-emitter threshold voltage of the first stage transistor Tr_1

Vd_2 = the base-emitter voltage of the second stage transistor Tr_2 in the conductive condition

E = power supply voltage

When the temperature coefficient of the timing resistor R_3 and the timing capacitor C is equal to zero, a

delay time in an exemplary circuit in practical use is expressed as follows:

Provided that $a = 0.5$, b=0.18, E=10 − 15V, Vd_1=0.5 − 0.7V, Vd_2=0.6 − 0.8V and an environmental temperature = −30°C − + 70°C, the delay time $T_{70(15)}$ means the shortest set time at +70°C and + 15V, and the delay Time $T_{-30(10)}$ means the longest set time at −30°C and + 10V. The ratio thereof will be $T_{-30(10)}/T_{70(15)}$ = 1.04. From the above expression it will be seen that the set time will hardly be affected by the variation of the power supply voltage and the environmental temperature. In the worst case when the power supply voltage varies from 10 to 15V, and the environmental temperature varies in all the domain between − 30°C through + 70°C, only 4% of difference will be produced. Therefore, without employing such expensive semiconductor elements as a Zener diode for compensating the voltage characteristic, a thermistor for compensating the temperature characteristic and a semiconductor varistor, a very stable set time in practical use will be obtained and a timer with high accuracy will be provided.

It is usual that the conventional silicon transistor has a base-emitter reverse withstand voltage (reverse breakdown voltage) of 5 − 7V. In the circuit of the above-mentioned embodiment of the present invention, in case the power supply voltage is 12V, R_1 and R_2 are so determined that the constant a=0.4, the first stage transistor Tr_1 does not enter the Zener domain and functions satisfactorily when the base of said transistor Tr_1 is reversely biased immediately after setting. But in case the constant a is selected to be a value of nearly 1, two times or more of delay times will be obtained with the same values of the timing resistor R_3 and timing capacitor C. Thus, in order to obtain a long delay time, in some cases it is more convenient to select the constant a to be a value of nearly 1, rather than to double the size of the timing capacitor C. Then, in order to select the constant a to be a value of nearly 1, a first stage transistor Tr_1 with a base-emitter withstand voltage higher than the power supply voltage should be employed. Otherwise, a diode D_2 with a withstand voltage higher than the power supply voltage should be connected in series with both the positive electrode of the timing capacitor C and the base of the first stage transistor Tr_1 as shown in FIG. **2**, thereby to operate in a preferable condition regardless of the value of the constant a.

Referring to FIG. **3**, a circuit diagram of another embodiment of the present invention will be explained. The base of a third transistor Tr_3 is connected with the collector of the first stage transistor Tr_1 shown in the circuit of FIG. **1**, and the collector of said transistor Tr_3 is connected with the +B power supply line and the emitter thereof is connected with the base of the second stage transistor Tr_2. In the circuit of FIG. **1**, in case the power supply voltage is 12V and the exciting current of the relay Y is 100 mA, the maximum value of the timing resistor R_3 allowed to be employed is at most 2 through 3 megohms, so that so long set time cannot be expected. On the other hand, in the circuit of FIG. **3**, the third transistor Tr_3 is additionarily employed and the D.C. current amplification factor of the second stage transistor Tr_2 will be increased equivalently, thereby raising the base resistance R_3 (timing resistance) of the first stage transistor Tr_1.

In the circuit diagram of another embodiment in FIG. **4**, a diode D_2 is connected between the first stage transistor Tr_1 and the timing capacitor C, thereby enabling to function satisfactorily regardless of the value of the constant a.

By adding the third transistor Tr_3 as shown in FIGS. **3** and **4**, in case the relay Y requiring the exciting current of 100 mA as mentioned above is used, the timing resistor R_3 of 100 megohm can be employed, thus enabling a timer of dozens of minutes of set time to be realized.

In the circuits of said FIGS. **3** and **4**, the collector of the third transistor Tr_3 is connected with the +B power supply line, but it may be connected with the collector of the second stage transistor Tr_2 as the Darlington connection. However, in this case there is caused such a defect that the collector-emitter saturation voltage of the second stage transistor Tr_2 rises to increase the loss of said transistor Tr_2. In the circuit of the present embodiment, as the current limiting resistor is not connected with the collector or the emitter of the third transistor Tr_3 (for the purpose of lowering the cost as much as possible), there remains necessity that the resistance of the collector resistor R_4 of the first stage transistor Tr_1 should be properly selected not to exceed the collector loss of the third transistor Tr_3.

In the present invention as mentioned above, the timing capacitor is charged up in the direction for cutting-off the transistor, then the voltage is applied thereto in the direction for discharging the thus charged charge to commence discharging and after a given time, said transistor will be made conductive to determine a set time. Owing to such a construction, the present invention enables the constituent elements to be reduced as much as possible, allows conventional semiconductors of reasonable price to be employed, and allows the timer to be mass-produced, thus enabling the cost to be lowered. Further according to the present invention, with a simple structure of the circuit, a set time can be determined to be several seconds through dozens of minutes and an excellent voltage characteristic and temperature characteristic can be obtained. Moreover, as the predetermined set time is not affected by the D.C. current amplification factor of the transistor, the operation of the relay and the open-circuit voltage, fluctuation in quality of the products can be reduced and the yield can be improved. The present invention further has some advantages that when it is not used for timer operation, the timer circuit and the load are interrupted from the power supply, so that the waste of electric power can be prevented and possible errorneous operation owing to noises can be well prevented.

While there have been described and illustrated several specific embodiments of the invention, it will be clear that variations in the details of the embodiments specifically illustrated and described may be made without departing from the true spirit and scope of the invention as defined in the appended claim.

What is claimed is:

1. An off delay timing circuit for use in an automobile, comprising:

first and second transistors of the same polarity and means connecting same in sequence for inverted operation with respect to each other;

load control means responsive to said second transistor for controlling energization of a load;

a voltage divider and a timing capacitor coupled hereto;

a setting switch connectible to a power source and including set contact means actuable to a set condition for charging said timing capacitor through said voltage divider and for energizing said load;

means connecting said timing capacitor to said first transistor for applying the resulting charge voltage on said capacitor to said first transistor as a reverse bias;

a timing resistor and means connecting same to said timing capacitor and responsive to switching of the setting switch from said set condition for discharging said timing capacitor gradually through the timing resistor to said power source to define a timing interval;

circuit means connected to said setting switch and load control means and connectible to said load and source for isolating and preventing current draw by the remainder of the timing circuit and said load from said source other than when said setting switch is in its set condition and during said timing interval;

said set contact means including first, second and third set contacts, said circuit means including leads connectible from the second and third set contacts to said source and load respectively for energizing said load from said source upon connection of the second and third set contacts, and means connecting said first set contact to said voltage divider and to the base of said second transistor for charging said timing capacitor from said source through said voltage divider and energizing said second transistor from said source when said setting switch is in its set condition, said setting switch further including means for interconnecting said first, second and third set contacts when said setting switch is in its set position.

2. The circuit of claim **1**, including conductor means connecting said third set contact in series with said load control means and second transistor for allowing current flow therethrough when the setting switch is in its set condition and also connecting said third set contact in series with said first transistor, said third set contact also being connected to said timing capacitor through said timing resistor, said load control means having a contact closable upon energization thereof for energizing said third set contact from the power source even when said setting switch is not in its set position.

3. An off delay timing circuit for use in an automobile, comprising:

first and second transistors of the same polarity and means connecting same in sequence for inverted operation with respect to each other;

load control means responsive to said second transistor for controlling energization of a load;

a voltage divider and a timing capacitor coupled thereto;

a setting switch connectible to a power source and including set contact means actuable to a set condition for charging said timing capacitor through said voltage divider and for energizing said load;

means connecting said timing capacitor to said first transistor for applying the resulting charge voltage on said capacitor to said first transistor as a reverse bias;

a timing resistor and means connecting same to said timing capacitor and responsive to switching of the setting switch from said set condition for discharging said timing capacitor gradually through the timing resistor to said power source to define a timing interval;

circuit means connected to said setting switch and load control means and connectible to said load and source for isolating and preventing current draw by the remainder of the timing circuit and said load from said source other than when said setting switch is in its set condition and during said timing interval;

the setting switch including means defining a set condition for applying energizing potential from said source through said voltage divider to charge said timing capacitor and to the base of the second transistor for turning same on and for independently providing operating potential from said source to the timing resistor, to the current carrying paths of the first and second transistors and to said load, said setting switch further including means defining a reset condition for shorting the base path through the second transistor to block conduction thereof and said setting switch further havng means defining a neutral condition for eliminating both the set and reset connections therethrough.

4. An off delay timing circuit for use in an automobile, comprising:

first and second transistors of the same polarity and means connecting same in sequence for inverted operation with respect to each other;

load control means responsive to said second transistor for controlling energization of a load;

a voltage divider and a timing capacitor coupled thereto;

a setting switch connectible to a power source and including set contact means actuable to a set condition for charging said timing capacitor through said voltage divider and for energizing said load;

means connecting said timing capacitor to said first transistor for applying the resulting charge voltage on said capacitor to said first transistor as a reverse bias;

a timing resistor and means connecting same to said timing capacitor and responsive to switching of the setting switch from said set condition for discharging said timing capacitor gradually through the timing resistor to said power source to define a timing interval;

circuit means connected to said setting switch and load control means and connectible to said load and source for isolating and preventing current draw by the remainder of the timing circuit and said load from said source other than when said setting switch is in its set condition and during said timing interval;

means responsive to the set condition of said setting switch for connecting said voltage divider across said power source, said timing capacitor being connected at one side to said voltage divider for charging therefrom, said timing capacitor being connected at the other side thereof to one end of said timing resistor and to the base of said first transistor, means connecting the free end of said timing resistor for energization by said power source during the set condition of said setting switch and dur-

ing said time interval, whereby current flow through said timing resistor biases said first transistor conductive during the set condition of the setting switch and the charged condition of said timing capacitor biases the base of the first transistor to nonconduction thereafter and to the end of the timing interval.

5. The circuit of claim **4**, including a diode interposed between said timing capacitor and the base of said first transistor for preventing reverse current flow through the base-emitter connection junction of said first transistor.

6. An off delay timing circuit for use in an automobile, comprising:

first and second transistors of the same polarity and means connecting same in sequence for inverted operation with respect to each other;

load control means responsive to said second transistor for controlling energization of a load;

a voltage divider and a timing capacitor coupled thereto;

a setting switch connectible to a power source and including set contact means actuable to a set condition for charging said timing capacitor through said voltage divider and for energizing said load;

means connecting said timing capacitor to said first transistor for applying the resulting charge voltage on said capacitor to said first transistor as a reverse bias;

a timing resistor and means connecting same to said timing capacitor and responsive to switching of the setting switch from said set condition for discharging said timing capacitor gradually through the timing resistor to said power source to define a timing interval;

circuit means connected to said setting switch and load control means and connectible to said load and source for isolating and preventing current draw by the remainder of the timing circuit and said load from said source other than when said setting switch is in its set condition and during said timing interval;

a third transistor and means coupling same in sequence between first and second transistors for enhancing the DC current amplification factor of the second transistor, said third transistor being direct coupled through its base-emitter circuit between said first and second transistors and having the collector thereof connectible to the power source, said timing resistor and timing capacitor being connected to the base of said first transistor, whereby provision of said third transistor allows raising of the value of said timing resistor and a consequent increase in the timed interval.

* * * * *