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(54) Title: NONVOLATILE MEMORY SYSTEM

(57) Abstract: A nonvolatile (NV) memory system includes a memory control module that encodes data to provide encoded logical data structures. The system also includes NV memory that includes X arrays that include physical data structures that differ in size from the encoded logical data structures. The memory control module writes/reads from the NV memory according to the encoded logical data structures. X is an integer greater than or equal to 1.

NONVOLATILE MEMORY SYSTEM

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Utility Application No. 12/025371, filed February 4, 2008, and U.S. Provisional Application No. 60/889078, filed on February 9, 2007. The disclosures of the above applications are incorporated herein by reference in its entirety.

FIELD

[0002] The present disclosure relates to memory systems and, more particularly, to systems and methods for storing data in nonvolatile (NV) memory.

BACKGROUND

[0003] The background description provided herein is for the purpose of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

[0004] Referring now to FIGs. 1, 2A and 2B, nonvolatile (NV) semiconductor memory 10 may include flash memory, static random access memory (SRAM), nitride read only memory (NROM), phase change memory, magnetic RAM, multi-state memory, etc. The NV semiconductor memory 10 may include one or more arrays 16 that may each be arranged on one or more memory chips. The arrays 16 may include data structures, such as blocks and pages. The arrays 16 may therefore be arranged as B blocks 18-1, 18-2, ..., and 18-B (collectively referred to as blocks 18).

[0005] In FIG. 2A, each block 18 includes P pages 20-1, 20-2, ..., and 20-P (collectively referred to as pages 20). In FIG. 2B, each page 20 may include a plurality of memory cells that are associated with a data portion 24 and may include other memory cells that are associated with an overhead data portion 26 such as error correcting code (ECC) data or other (O) overhead data.

[0006] Referring now to FIG. 2C, a memory drive may include one or more arrays 16-1, 16-2, ..., and 16-C (collectively referred to as arrays 16) and each include blocks 18. Usually, the control module addresses the memory drive according to a hardwired physical block size. Pages 20 in the blocks 18 may also have a hardwired physical page size and may therefore be referred to as physical pages. The number of memory cells in the data and overhead portions of the pages 20 may also be hardwired.

[0007] For example only, a NAND flash array may include 2048 blocks for a total of 2 Gigabytes (GB) of memory. Each block may include 128 kilobytes (KB) in 64 pages. Each page 20 may include 2112 bytes. Of the 2112 bytes, 2048 bytes may be associated with the data portion and 64 bytes may be associated with the overhead portion. Each memory cell may store a bit.

[0008] The memory control module erases pages 20 and blocks 18 according to predetermined erase blocks 29-1, 29-2, ..., and 29-R (collectively referred to as erase blocks 29). The memory control module generally requires data in an entire erase block to be erased simultaneously.

[0009] A host device may initiate a read operation and provide data files to the memory control module that are arranged in multiples of allocation units (AUs) of predefined size that fit in a physical block. AUs correspond to the smallest logical amount of memory space that can be allocated by the control module to store a file and may therefore be referred to as logical pages. Groupings of logical pages may be referred to as logical blocks.

[0010] When a write command is issued, data is sent in multiples of logical block size to the memory control module. The memory control module allocates the exact number of physical pages 20 to accommodate the logical pages. Even when ECC is used on logical page data, the number of parity bits are kept within the number of spare bits per overhead portion of a respective physical page. Therefore, one (ECC) coded logical page fits in an integer number of physical pages, and one coded logical block fits within an integer number of physical blocks.

SUMMARY

[0011] A nonvolatile (NV) memory system includes a memory control module that encodes data to provide encoded logical data structures. The system also includes NV memory that includes X arrays that include physical data structures that differ in size from the encoded logical data structures. The memory control module writes/reads from the NV memory according to the encoded logical data structures. X is an integer greater than or equal to 1.

[0012] In other features, the memory control module sends and receives the data in logical data structures. The logical data structures comprise at least one of logical pages and logical blocks. The physical data structures comprise at least one of physical pages and physical blocks in the NV memory. The memory control module includes an encoder module that selects one of N error correction code (ECC) rates where N>1. The encoder module performs encoding according to at least one of a Reed Solomon scheme, a Bose-Chaudhuri-Hocquenghem (BCH) scheme, a Low Density Parity Check (LDPC) scheme, a Gray code scheme, and a combination of two or more of the BCH scheme, the LDPC scheme, and the Gray code scheme.

[0013] In other features, the memory control module includes a decoder module that decodes the encoded logical data structures during a read operation from the NV memory. The memory control module writes to the X arrays in parallel when X>1. The memory control module writes a first portion of a first of the encoded logical data structures to a first of the X arrays while writing a second portion of the first of the encoded logical data structures to a second of the X arrays. The memory control module writes a first portion of a second of the encoded logical data structures to the second of the arrays while writing the first and second portions of the first of the encoded logical data structures.

[0014] In other features, the memory control module allocates buffers within the X arrays for each of the encoded logical data structures. The allocation is conducted so that portions of the encoded logical data structures that do not fit into the physical data structures are stored in the buffers. Each of the X arrays corresponds to one or more memory chips. The memory control module selectively determines an amount of data to erase in the NV memory

based on a size of the encoded logical data. The amount of data includes data within a predetermined number of cells within all of the X arrays.

[0015] In other features, the system includes a memory drive that includes the memory control module and the NV memory. The system further includes the host device that communicates with the memory drive according to the logical data structures. The NV memory includes at least one of flash memory, static random access memory (SRAM), nitride read only memory (NROM), phase change memory, magnetic RAM and multi-state memory. The physical data structures differ in size from the encoded logical data structures so that a size of the physical data structures and a size of the encoded logical data structures do not have an integer relationship.

[0016] In other features, a method for operating a nonvolatile (NV) memory system includes encoding data to provide encoded logical data structures. The method also includes writing/reading from NV memory according to the encoded logical data structures. The NV memory includes X arrays that include physical data structures that differ in size from the encoded logical data structures. X is an integer greater than or equal to 1.

[0017] In other features, the method includes sending and receiving the data external to the NV memory system in logical data structures. The logical data structures comprise at least one of logical pages and logical blocks. The physical data structures comprise at least one of physical pages and physical blocks in the NV memory. The method also includes selecting one of N error correction code (ECC) rates where N>1. The method also includes encoding the data according to at least one of a Reed Solomon scheme, a Bose-Chaudhuri-Hocquenghem (BCH) scheme, a Low Density Parity Check (LDPC) scheme, a Gray code scheme, and a combination of two or more of the BCH scheme, the LDPC scheme, and the Gray code scheme.

[0018] In other features, the method includes decoding the encoded logical data structures during a read operation from the NV memory. The method also includes writing to the X arrays in parallel when X>1. The method also includes writing a first portion of a first of the encoded logical data structures to a first of the X arrays while writing a second portion of the first of the encoded logical data structures to a second of the X arrays. The method also includes writing a first portion of a second of the encoded logical data structures to the second of the arrays while writing the first and second portions of the first of the encoded logical data structures.

[0019] In other features, the method includes allocating buffers within the X arrays for each of the encoded logical data structures. The allocation is conducted so that portions of the encoded logical data structures that do not fit into the physical data structures are stored in the buffers. Each of the X arrays corresponds to one or more memory chips. The method also includes determining an amount of data to erase in the NV memory based on a size of the encoded logical data. The amount of data includes data within a predetermined number of cells within all of the X arrays.

[0020] In other features, the NV memory includes at least one of flash memory, static random access memory (SRAM), nitride read only memory (NROM), phase change memory, magnetic RAM and multi-state memory. The physical data structures differ in size from the encoded logical data structures so that a size of the physical data structures and a size of the encoded logical data structures do not have an integer relationship.

[0021] In other features, a nonvolatile (NV) memory system includes memory control means for encoding data to provide encoded logical data structures. The system also includes NV means for storing data that includes X arrays that include physical data structures that differ in size from the encoded logical data structures. The memory control means writes/reads from the NV means according to the encoded logical data structures. X is an integer greater than or equal to 1.

[0022] In other features, the memory control means sends and receives the data in logical data structures. The logical data structures comprise at least one of logical pages and logical blocks. The physical data structures comprise at least one of physical pages and physical blocks in the NV means. The memory control means includes encoder means for selecting one of N error correction code (ECC) rates, where N>1. The encoder means performs encoding according to at least one of a Reed Solomon scheme, a Bose-

Chaudhuri-Hocquenghem (BCH) scheme, a Low Density Parity Check (LDPC) scheme, a Gray code scheme, and a combination of two or more of the BCH scheme, the LDPC scheme, and the Gray code scheme.

[0023] In other features, the memory control means includes decoder means for decoding the encoded logical data structures during a read operation from the NV means. The memory control means writes to the X arrays in parallel when X>1. The memory control means writes a first portion of a first of the encoded logical data structures to a first of the X arrays while writing a second portion of the first of the encoded logical data structures to a second of the X arrays. The memory control means writes a first portion of a second of the encoded logical data structures to the second of the arrays while writing the first and second portions of the first of the encoded logical data structures.

[0024] In other features, the memory control means allocates buffers within the X arrays for each of the encoded logical data structures so that portions of the encoded logical data structures that do not fit into the physical data structures are stored in the buffers. Each of the X arrays corresponds to one or more memory chips. The memory control means selectively determines an amount of data to erase in the NV means based on a size of the encoded logical data. The amount of data includes data within a predetermined number of cells within all of the X arrays.

[0025] In other features, the system includes memory drive means for storing data that includes the memory control means and the NV means. The system further includes the host device that communicates with the memory drive means according to the logical data structures. The NV means includes at least one of flash memory, static random access memory (SRAM), nitride read only memory (NROM), phase change memory, magnetic RAM and multi-state memory. The physical data structures differ in size from the encoded logical data structures so that a size of the physical data structures and a size of the encoded logical data structures do not have an integer relationship.

[0026] In still other features, the systems and methods described above are implemented by a computer program executed by one or more processors. The computer program can reside on a computer readable medium such as but not limited to memory, non-volatile data storage, and/or other suitable tangible storage mediums. The computer program operates a nonvolatile (NV) memory system and includes encoding data to provide encoded logical data structures. The computer program also includes writing/reading from NV memory according to the encoded logical data structures. The NV memory includes X arrays that include physical data structures that differ in size from the encoded logical data structures. X is an integer greater than or equal to 1.

[0027] In other features, the computer program includes sending and receiving the data external to the NV memory system in logical data structures. The logical data structures comprise at least one of logical pages and logical blocks. The physical data structures comprise at least one of physical pages and physical blocks in the NV memory. The computer program also includes selecting one of N error correction code (ECC) rates where N>1. The computer program also includes encoding the data according to at least one of a Reed Solomon scheme, a Bose-Chaudhuri-Hocquenghem (BCH) scheme, a Low Density Parity Check (LDPC) scheme, a Gray code scheme, and a combination of two or more of the BCH scheme, the LDPC scheme, and the Gray code scheme.

[0028] In other features, the computer program includes decoding the encoded logical data structures during a read operation from the NV memory. The computer program also includes writing to the X arrays in parallel when X>1. The computer program also includes writing a first portion of a first of the encoded logical data structures to a first of the X arrays while writing a second portion of the first of the encoded logical data structures to a second of the X arrays. The computer program also includes writing a first portion of a second of the encoded logical data structures to the second of the arrays while writing the first and second portions of the first of the encoded logical data structures.

[0029] In other features, the computer program includes allocating buffers within the X arrays for each of the encoded logical data structures so that portions of the encoded logical data structures that do not fit into the physical data structures are stored in the buffers. Each of the X arrays corresponds to one or more memory chips. The computer program also includes determining an amount of data to erase in the NV memory based on a size of the encoded logical data. The amount of data includes data within a predetermined number of cells within all of the X arrays.

[0030] In other features, the NV memory includes at least one of flash memory, static random access memory (SRAM), nitride read only memory (NROM), phase change memory, magnetic RAM and multi-state memory. The physical data structures differ in size from the encoded logical data structures so that a size of the physical data structures and a size of the encoded logical data structures do not have an integer relationship.

[0031] Further areas of applicability of the present disclosure will become apparent from the detailed description provided hereinafter. It should be understood that the detailed description and specific examples are intended for purposes of illustration only and are not intended to limit the scope of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] The present disclosure will become more fully understood from the detailed description and the accompanying drawings, wherein:

[0033] FIG. 1 is a functional block diagram of memory including blocks according to the prior art;

[0034] FIG. 2A illustrates pages within the blocks of memory according to the prior art;

[0035] FIG. 2B illustrates memory cells within the pages according to the prior art;

[0036] FIG. 2C illustrates memory arranged in erase blocks according to the prior art;

[0037] FIG. 3A is a functional block diagram of a memory system according to the present disclosure;

[0038] FIG. 3B is a functional block diagram of a write path module according to the present disclosure;

[0039] FIG. 3C is a functional block diagram of a read path module according to the present disclosure;

[0040] FIG. 3D is a functional block diagram of a write and read format modules according to the present disclosure;

[0041] FIG. 4 illustrates a simplified memory map according to the present disclosure;

[0042] FIG. 5 illustrates a simplified memory map according to the present disclosure;

[0043] FIG. 6 illustrates a simplified memory map according to the present disclosure;

[0044] FIG. 7 illustrates a method for operating a memory system according to the present disclosure;

[0045] FIG. 8A is a functional block diagram of a hard disk drive;

[0046] FIG. 8B is a functional block diagram of a DVD drive;

[0047] FIG. 8C is a functional block diagram of a high definition television;

[0048] FIG. 8D is a functional block diagram of a vehicle control system;

[0049] FIG. 8E is a functional block diagram of a cellular phone;

[0050] FIG. 8F is a functional block diagram of a set top box; and

[0051] FIG. 8G is a functional block diagram of a mobile device.

DETAILED DESCRIPTION

[0052] The following description is merely exemplary in nature and is in no way intended to limit the disclosure, its application, or uses. For purposes of clarity, the same reference numbers will be used in the drawings to identify similar elements. As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A or B or C), using a non-exclusive logical or. It should be understood that steps within a method may be executed in different order without altering the principles of the present disclosure.

[0053] As used herein, the term module refers to an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group) and memory that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable components that provide the described functionality.

[0054] Previously, a host device interfaced with a memory control module according to logical data structures, such as logical pages or blocks of logical pages, that were restricted to a predetermined size. The memory control module encoded the data, and either one coded logical page contained an integer number of physical pages within memory, or a physical page within memory contained an integer number of coded logical pages.

[0055] In other words, there previously was an integer relationship between the logical page and physical page, although the relationship was not necessarily 1:1. For example, a logical page could be 0.5 kilobytes (KB) while a physical page could be 2KB, or the logical page could be 4KB while the physical page could be 2KB. In either case, the logical page either completely fit in one physical page or was evenly distributed into several physical pages.

[0056] In the present disclosure, the memory control module may instead modify coded logical block (CLB) size and/or physical block size so that they are no longer integer multiples of each other. The CLBs may thus be spread among multiple arrays, which may be included on one or more memory chips. During a read operation, the memory control module may reformat data from the memory into groupings that conform to logical data structures of a host device interface. The host device may receive the data according to the logical data structures.

[0057] For example, a logical page can be 4.4KB while a hard-wired physical page is 2KB. In this case, the logical page may be unevenly distributed into, for example, 3 physical pages. The first two pages contain 2KB each, while the last physical page contains 0.4KB of the logical page. Also, the last physical page may contain a first portion of the next logical page.

[0058] Referring now to FIG. 3A, a memory system 66 for a nonvolatile (NV) semiconductor memory 68, such as multilevel flash memory, is illustrated. In FIG. 3A, a host device 70 communicates with a solid state NV memory drive 69 that includes a memory control module 72 and the NV memory 68. The memory control module 72 may communicate with the memory 68 via write and read path modules 73, 75 that erase, write to and read from erase blocks 80-1, 80-2, ..., and 80-A (collectively referred to as erase blocks 80).

[0059] The NV memory 68 may include one or more arrays 78-1, 78-2, ..., and 78-X (collectively referred to as array 78) of memory cells that may each correspond to one or more memory chips. The array 78 may be arranged according to physical memory blocks of predetermined size that include physical pages of predetermined size. The memory control module 72 may receive data in logical blocks and/or logical pages from the host device 70 and generate a physical format for the data that differs from the hard-wired physical format of the NV memory 68. The generated physical format is modified from the physical format and may therefore be referred to as a modified physical format. In other words, the memory control module 72 may write data according to coded logical block size and not physical block size.

[0060] The memory control module 72 may reformat physical blocks, physical pages and erase blocks 80 to, for example, increase error correction code (ECC) rates for the data. Different ECC rates may be used to maintain integrity of the data. ECC rates may be represented by fractional numbers and may indicate the portion of the total amount of data that is not part of the ECC. In other words, if the code rate is k/n, for every k bits of useful information, the coder generates n bits of data, of which n-k are redundant.

[0061] For example, a rate of 0.9 ECC may be used. If user data is 4KB per read/write operation, then the CLB size may be 4.4KB, which is 4.4*8/6=5.87 physical pages (if each cell contains 3 bits, and each physical page contains 2048 (2K) cells, then physical page size may be 6KB). Therefore, the CLB size may be larger than the physical block size, and CLB size may not be an integer multiple of the physical block size. Therefore, the memory control module 72 writes to the memory 68 based on the CLB size rather than the physical block size. As another example, if the ECC rate is 0.85, then CLB size may equal 4.7KB, which is 6.27 physical pages. The present disclosure may support multiple (for example, rate 0.9 and rate 0.85) ECC codes and select from the different ECC code rates for a particular field.

[0062] Referring now to FIG. 3B, the write path module 73 is illustrated. The write path module 73 may include an ECC encoder module 93 that encodes received data with an overhead portion. The ECC encoder module

93 may include a cyclic redundancy (CRC) module (not shown) that generates CRC bits based on user data. The ECC encoder module 93 may include other encoding modules, such as a Reed Solomon encoder module or a Bose-Chaudhuri-Hocquenghem (BCH)/Low Density Parity Check (LDPC) encoder module. The write path module 73 may also include a write format module 100 that generates the modified block and/or page format for the memory 68.

[0063] Referring now to FIG. 3C, a read path module 75 is illustrated. The read path module 75 includes a read format module 104 that reads data from the memory 68 based on the modified block and/or page format. The read path module 75 also includes an ECC decoder module 106 that decodes the read-back signals that were encoded by the ECC encoder module 93. The ECC decoder module may include, for example, a LDPC module, a Gray Code decoder module, a BCH decoder module, a Reed-Solomon decoder and/or a CRC decoder.

[0064] Referring now to FIG. 3D, the write and read format modules 100, 104 may employ column and row select modules (not shown) to select memory cells within the NV memory 68. The write format module 100 may also include a rate selection module 105 that selects a rate for the ECC encoder module 93. Alternatively, an external rate selection module may select the ECC rate. During a write operation, a logical block size module 108 of the write format module 100 receives ECC encoded logical blocks of data and determines a size of the CLBs.

[0065] A physical format module 110 allocates a portion of the memory 68 based on the size of the CLBs. The allocated portion may be referred to as a modified physical block of data and may include any number of memory cells, such as a particular cell, a row of cells, a column of cells, a block of cells, a page of cells, erase blocks, etc. The physical format module 110 may erase data in an erase block that may or may not correspond to a predetermined erase block 80 of the NV memory 68. At least a portion of the erase block 80 is allocated for the modified physical block. The physical format module 110 writes to cells within the modified physical block of the NV memory 68. The physical format module 110 may also include memory (not shown) that stores a memory map based on modified blocks of data.

[0066] The read format module 104 may include a read module 120 that reads back data from the NV memory 68 according to the modified physical block as provided by the physical format module 110. During a read operation, the read module 120 selects read target cells, which may include any number of memory cells, such as a particular cell, a row of cells, a column of cells, a block of cells, a page of cells, etc. Once the read target cells are selected, the read module 120 reads the read target cells. A logical block size module 122 may then reapportion the data (before or after decoding) according to the original logical blocks/pages as when the data was sent to the memory control module 72.

[0067] Referring now to FIG. 4, a modified memory map is shown for write/read operations. Arrays 78 are divided by erase blocks 80. The memory control module 72 writes CLBs 200-1, 200-2, ..., and 200-N (collectively referred to as CLBs 200) across the arrays 78 regardless of the original physical size of data structures in the arrays 78. For example, the first CLB 200-1 fills the memory cells in a physical page of array 78-1 and also fills memory cells within part of a physical page within array 78-2.

[0068] The memory control module 72 may write to some or all of the arrays 78 in parallel. For example, when the memory control module 72 writes three CLBs (CLB 1, CLB 2, CLB 3), after encoding, the memory control module 72 may send a first part 260 of CLB 1 to the first array 78-1, and simultaneously send a second part 262 of CLB 1 with a first part 264 of the CLB 2 to the second array 78-2, etc.

[0069] Conventional NV memory drives use a page/erase block structure to store data. For example, a physical page may contain 2KB of data plus an overhead area if each memory cell contains 1 bit of data. If each memory cell contains 3 bits of data, then the physical page size may be 6KB. An erase block contains an integer number of physical pages. Typical size for erase block may range from 128KB to 512KB. Data in the erase block may be erased simultaneously.

[0070] In the present disclosure, the memory control module 72 may define logical page size to be, for example, 4KB, so that write/read commands transfer a multiple of 4KB of data between the memory control module 72 and the host device 70. Meanwhile, the memory control module 72 may define a physical block size to be, for example, 4.4KB. The additional .4KB of the modified physical block may correspond to an additional .4KB of ECC added to the original 4KB.. In other words, logical page size (for example 4KB) may be an integer multiple of physical page size (for example 4KB) but differs from modified physical page size (for example 4.4KB). Likewise, if the memory control module 72 defines logical block size as 4KB, where logical block size is an integer multiple of physical block size (for example 4KB), modified physical block size may be set to, for example, 4.4KB, which is not an integer multiple of physical block size.

[0071] Referring now to FIGs. 5-6, simplified memory arrays 78 are provided to illustrate two exemplary methods for writing to the NV memory 68. The simplified memory arrays 78 include CLBs that are illustrated as integers (1-7). The first method, as in FIG. 5, includes spreading CLBs 200 across multiple arrays 78. Each of the CLBs 200 includes a portion 209-1, 209-2, ..., and 209-N that overlaps two or more physical blocks in two or more arrays 78. The second method of FIG. 6 includes setting each CLB 200 in a single array. For parallel writing according to the second method, the memory control module 72 may define a buffer 210-1, 210-2, ..., and 210-N in each array 78 to store a part of each of the CLBs 200 that exceeds (i.e. overflows) the physical blocks.

[0072] Referring now to FIG. 7 an exemplary method 300 for writing to and reading from memory is illustrated. Logic starts in step 302. In step 304, the memory control module 72 receives logical pages of data. In step 306, the memory control module 72 encodes the data. The encoding may be selectively based on a desired integrity for the data and/or may be predetermined. In step 308, if the CLBs match the physical blocks in memory, and control goes to step 312. In step 312, the memory control module 72 writes/reads from the memory and then decodes the data in step 314.

[0073] If in step 308 the CLBs differ from the physical blocks, the memory control module 72 modifies the physical blocks and/or pages in step 316. For example, if CLB size is 5.2KB and physical block or page size is 4KB, the memory control module 72 may request the memory drive to allocate enough space for the 5.2KB CLB size for each write operation. The allocated memory space may be referred to as modified physical blocks or pages that would then, for example, include 5.2KB. In step 320, the memory control module 72 writes/reads according to the modified physical blocks and/or pages.

[0074] The host device 70 may still transfer data using logical blocks/pages as the smallest unit, but the memory control module 72 may now accommodate high rate ECCs to the data before sending it to the memory drive. The present disclosure may also decrease write/read time by bypassing physical blocks and/or pages and by writing to multiple memory arrays simultaneously.

[0075] Referring now to FIGs. 8A-8G, various exemplary implementations incorporating the teachings of the present disclosure are shown.

[0076] Referring now to FIG. 8A, the teachings of the disclosure can be implemented in NV memory of a hard disk drive (HDD) 400. The HDD 400 includes a hard disk assembly (HDA) 401 and an HDD printed circuit board (PCB) 402. The HDA 401 may include a magnetic medium 403, such as one or more platters that store data, and a read/write device 404. The read/write device 404 may be arranged on an actuator arm 405 and may read and write data on the magnetic medium 403. Additionally, the HDA 401 includes a spindle motor 406 that rotates the magnetic medium 403 and a voice-coil motor (VCM) 407 that actuates the actuator arm 405. A preamplifier device 408 amplifies signals generated by the read/write device 404 during read operations and provides signals to the read/write device 404 during write operations.

[0077] The HDD PCB 402 includes a read/write channel module (hereinafter, "read channel") 409, a hard disk controller (HDC) module 410, a buffer 411, the NV memory 412, a processor 413, and a spindle/VCM driver module 414. The read channel 409 processes data received from and transmitted to the preamplifier device 408. The HDC module 410 controls components of the HDA 401 and communicates with an external device (not shown) via an I/O interface 415. The external device may include a computer, a multimedia device, a mobile computing device, etc. The I/O interface 415 may include wireline and/or wireless communication links.

[0078] The HDC module 410 may receive data from the HDA 401, the read channel 409, the buffer 411, NV memory 412, the processor 413, the spindle/VCM driver module 414, and/or the I/O interface 415. The processor 413 may process the data, including encoding, decoding, filtering, and/or formatting. The processed data may be output to the HDA 401, the read channel 409, the buffer 411, NV memory 412, the processor 413, the spindle/VCM driver module 414, and/or the I/O interface 415.

[0079] The HDC module 410 may use the buffer 411 and/or NV memory 412 to store data related to the control and operation of the HDD 400. The buffer 411 may include DRAM, SDRAM, etc. NV memory 412 may include any suitable type of semiconductor or solid-state memory, such as flash memory (including NAND and NOR flash memory), phase change memory, magnetic RAM, and multi-state memory, in which each memory cell has more than two states. The spindle/VCM driver module 414 controls the spindle motor 406 and the VCM 407. The HDD PCB 402 includes a power supply 416 that provides power to the components of the HDD 400.

[0080] Referring now to FIG. 8B, the teachings of the disclosure can be implemented in NV memory of a DVD drive 418 or of a CD drive (not shown). The DVD drive 418 includes a DVD PCB 419 and a DVD assembly (DVDA) 420. The DVD PCB 419 includes a DVD control module 421, a buffer 422, the NV memory 423, a processor 424, a spindle/FM (feed motor) driver module 425, an analog front-end module 426, a write strategy module 427, and a DSP module 428.

[0081] The DVD control module 421 controls components of the DVDA 420 and communicates with an external device (not shown) via an I/O interface 429. The external device may include a computer, a multimedia device, a mobile computing device, etc. The I/O interface 429 may include wireline and/or wireless communication links.

[0082] The DVD control module 421 may receive data from the buffer 422, NV memory 423, the processor 424, the spindle/FM driver module 425, the analog front-end module 426, the write strategy module 427, the DSP module 428, and/or the I/O interface 429. The processor 424 may process the data, including encoding, decoding, filtering, and/or formatting. The DSP module 428 performs signal processing, such as video and/or audio coding/decoding. The processed data may be output to the buffer 422, NV memory 423, the processor 424, the spindle/FM driver module 425, the analog front-end module 426, the write strategy module 427, the DSP module 428, and/or the I/O interface 429.

[0083] The DVD control module 421 may use the buffer 422 and/or NV memory 423 to store data related to the control and operation of the DVD drive 418. The buffer 422 may include DRAM, SDRAM, etc. NV memory 423 may include any suitable type of semiconductor or solid-state memory, such as flash memory (including NAND and NOR flash memory), phase change memory, magnetic RAM, and multi-state memory, in which each memory cell has more than two states. The DVD PCB 419 includes a power supply 430 that provides power to the components of the DVD drive 418.

[0084] The DVDA 420 may include a preamplifier device 431, a laser driver 432, and an optical device 433, which may be an optical read/write (ORW) device or an optical read-only (OR) device. A spindle motor 434 rotates an optical storage medium 435, and a feed motor 436 actuates the optical device 433 relative to the optical storage medium 435.

[0085] When reading data from the optical storage medium 435, the laser driver provides a read power to the optical device 433. The optical device 433 detects data from the optical storage medium 435, and transmits the data to the preamplifier device 431. The analog front-end module 426 receives data from the preamplifier device 431 and performs such functions as filtering and A/D conversion. To write to the optical storage medium 435, the write strategy module 427 transmits power level and timing data to the laser driver 432. The laser driver 432 controls the optical device 433 to write data to the optical storage medium 435.

[0086] Referring now to FIG. 8C, the teachings of the disclosure can be implemented in NV memory of a high definition television (HDTV) 437. The HDTV 437 includes an HDTV control module 438, a display 439, a power supply 440, the memory 441, a storage device 442, a network interface 443, and an external interface 445. If the network interface 443 includes a wireless local area network interface, an antenna (not shown) may be included.

[0087] The HDTV 437 can receive input signals from the network interface 443 and/or the external interface 445, which can send and receive data via cable, broadband Internet, and/or satellite. The HDTV control module 438 may process the input signals, including encoding, decoding, filtering, and/or formatting, and generate output signals. The output signals may be communicated to one or more of the display 439, memory 441, the storage device 442, the network interface 443, and the external interface 445.

[0088] Memory 441 may include random access memory (RAM) and/or NV memory. NV memory may include any suitable type of semiconductor or solid-state memory, such as flash memory (including NAND and NOR flash memory), phase change memory, magnetic RAM, and multi-state memory, in which each memory cell has more than two states. The storage device 442 may include an optical storage drive, such as a DVD drive, and/or a hard disk drive (HDD). The HDTV control module 438 communicates externally via the network interface 443 and/or the external interface 445. The power supply 440 provides power to the components of the HDTV 437.

[0089] Referring now to FIG. 8D, the teachings of the disclosure may be implemented in NV memory of a vehicle 446. The vehicle 446 may include a vehicle control system 447, a power supply 448, the memory 449, a storage device 450, and a network interface 452. If the network interface 452 includes a wireless local area network interface, an antenna (not shown) may be included. The vehicle control system 447 may be a powertrain control system, a body control system, an entertainment control system, an anti-lock braking system (ABS), a navigation system, a telematics system, a lane departure system, an adaptive cruise control system, etc.

[0090] The vehicle control system 447 may communicate with one or more sensors 454 and generate one or more output signals 456. The sensors 454 may include temperature sensors, acceleration sensors, pressure sensors, rotational sensors, airflow sensors, etc. The output signals 456 may control engine operating parameters, transmission operating parameters, suspension parameters, etc.

[0091] The power supply 448 provides power to the components of the vehicle 446. The vehicle control system 447 may store data in memory 449 and/or the storage device 450. Memory 449 may include random access memory (RAM) and/or NV memory. NV memory may include any suitable type of semiconductor or solid-state memory, such as flash memory (including NAND and NOR flash memory), phase change memory, magnetic RAM, and multi-state memory, in which each memory cell has more than two states. The storage device 450 may include an optical storage drive, such as a DVD drive, and/or a hard disk drive (HDD). The vehicle control system 447 may communicate externally using the network interface 452.

[0092] Referring now to FIG. 8E, the teachings of the disclosure can be implemented in NV memory of a cellular phone 458. The cellular phone 458 includes a phone control module 460, a power supply 462, the memory 464, a storage device 466, and a cellular network interface 467. The cellular phone 458 may include a network interface 468, a microphone 470, an audio output 472 such as a speaker and/or output jack, a display 474, and a user input device 476 such as a keypad and/or pointing device. If the network interface 468 includes a wireless local area network interface, an antenna (not shown) may be included.

[0093] The phone control module 460 may receive input signals from the cellular network interface 467, the network interface 468, the microphone 470, and/or the user input device 476. The phone control module 460 may process signals, including encoding, decoding, filtering, and/or formatting, and generate output signals. The output signals may be communicated to one or more of memory 464, the storage device 466, the cellular network interface 467, the network interface 468, and the audio output 472.

[0094] Memory 464 may include random access memory (RAM) and/or NV memory. NV memory may include any suitable type of semiconductor or solid-state memory, such as flash memory (including NAND and NOR flash memory), phase change memory, magnetic RAM, and multi-state memory, in which each memory cell has more than two states. The storage device 466 may include an optical storage drive, such as a DVD drive, and/or a hard disk drive (HDD). The power supply 462 provides power to the components of the cellular phone 458.

[0095] Referring now to FIG. 8F, the teachings of the disclosure can be implemented in NV memory of a set top box 478. The set top box 478 includes a set top control module 480, a display 481, a power supply 482, the memory 483, a storage device 484, and a network interface 485. If the network interface 485 includes a wireless local area network interface, an antenna (not shown) may be included.

[0096] The set top control module 480 may receive input signals from the network interface 485 and an external interface 487, which can send and receive data via cable, broadband Internet, and/or satellite. The set top control module 480 may process signals, including encoding, decoding, filtering, and/or formatting, and generate output signals. The output signals may include audio and/or video signals in standard and/or high definition formats. The output signals may be communicated to the network interface 485 and/or to the display 481. The display 481 may include a television, a projector, and/or a monitor.

[0097] The power supply 482 provides power to the components of the set top box 478. Memory 483 may include random access memory (RAM) and/or NV memory. NV memory may include any suitable type of semiconductor or solid-state memory, such as flash memory (including NAND and NOR flash memory), phase change memory, magnetic RAM, and multi-state memory, in which each memory cell has more than two states. The storage device 484 may include an optical storage drive, such as a DVD drive, and/or a hard disk drive (HDD).

[0098] Referring now to FIG. 8G, the teachings of the disclosure can be implemented in NV memory of a mobile device 489. The mobile device 489 may include a mobile device control module 490, a power supply 491, the memory 492, a storage device 493, a network interface 494, and an external interface 499. If the network interface 494 includes a wireless local area network interface, an antenna (not shown) may be included.

[0099] The mobile device control module 490 may receive input signals from the network interface 494 and/or the external interface 499. The external interface 499 may include USB, infrared, and/or Ethernet. The input signals may include compressed audio and/or video, and may be compliant with the MP3 format. Additionally, the mobile device control module 490 may receive input from a user input 496 such as a keypad, touchpad, or individual buttons. The mobile device control module 490 may process input signals, including encoding, decoding, filtering, and/or formatting, and generate output signals.

[0100] The mobile device control module 490 may output audio signals to an audio output 497 and video signals to a display 498. The audio output 497 may include a speaker and/or an output jack. The display 498 may present a graphical user interface, which may include menus, icons, etc. The power supply 491 provides power to the components of the mobile device 489. Memory 492 may include random access memory (RAM) and/or NV memory.

[0101] NV memory may include any suitable type of semiconductor or solid-state memory, such as flash memory (including NAND and NOR flash memory), phase change memory, magnetic RAM, and multi-state memory, in which each memory cell has more than two states. The storage device 493 may include an optical storage drive, such as a DVD drive, and/or a hard disk drive (HDD). The mobile device may include a personal digital assistant, a media player, a laptop computer, a gaming console, or other mobile computing device.

[0102] Those skilled in the art can now appreciate from the foregoing description that the broad teachings of the disclosure can be implemented in a variety of forms. Therefore, while this disclosure includes particular examples, the true scope of the disclosure should not be so limited since other modifications will become apparent to the skilled practitioner upon a study of the drawings, the specification, and the following claims.

CLAIMS

What is claimed is:

1. A nonvolatile (NV) memory system, comprising:

a memory control module that encodes data to provide encoded logical data structures; and

NV memory that comprises X arrays that include physical data structures that differ in size from said encoded logical data structures, wherein said memory control module writes/reads from said NV memory according to said encoded logical data structures, wherein X is an integer greater than or equal to 1.

2. The system of claim 1 wherein said memory control module sends and receives said data in logical data structures.

3. The system of claim 2 wherein said logical data structures comprise at least one of logical pages and logical blocks.

4. The system of claim 1 wherein said physical data structures comprise at least one of physical pages and physical blocks in said NV memory.

5. The system of claim 1 wherein said memory control module comprises an encoder module that selects one of N error correction code (ECC) rates, wherein N>1.

6. The system of claim 5 wherein said encoder module performs encoding according to at least one of a Reed Solomon scheme, a Bose-Chaudhuri-Hocquenghem (BCH) scheme, a Low Density Parity Check (LDPC) scheme, a Gray code scheme, and a combination of two or more of said BCH scheme, said LDPC scheme, and said Gray code scheme.

7. The system of claim 5 wherein said memory control module further comprises a decoder module that decodes said encoded logical data structures during a read operation from said NV memory.

8. The system of claim 1 wherein said memory control module writes to said X arrays in parallel when X>1.

9. The system of claim 8 wherein said memory control module writes a first portion of a first of said encoded logical data structures to a first of said X arrays while writing a second portion of said first of said encoded logical data structures to a second of said X arrays.

10. The system of claim 9 wherein said memory control module writes a first portion of a second of said encoded logical data structures to said second of said arrays while writing said first and second portions of said first of said encoded logical data structures.

11. The system of claim 8 wherein said memory control module allocates buffers within said X arrays for each of said encoded logical data structures so that portions of said encoded logical data structures that do not fit into said physical data structures are stored in said buffers.

12. The system of claim 8 wherein each of said X arrays corresponds to one or more memory chips.

13. The system of claim 1 wherein said memory control module selectively determines an amount of data to erase in said NV memory based on a size of said encoded logical data.

14. The system of claim 13 wherein said amount of data includes data within a predetermined number of cells within all of said X arrays.

15. The system of claim 2 further comprising a memory drive that comprises said memory control module and said NV memory.

16. The system of claim 15 further comprising said host device that communicates with said memory drive according to said logical data structures.

17. The system of claim 1 wherein said NV memory comprises at least one of flash memory, static random access memory (SRAM), nitride read only memory (NROM), phase change memory, magnetic RAM and multi-state memory.

18. The system of claim 1 wherein said physical data structures differ in size from said encoded logical data structures so that a size of said physical data structures and a size of said encoded logical data structures do not have an integer relationship.

19. A method for operating a nonvolatile (NV) memory system, comprising:

encoding data to provide encoded logical data structures; and

writing/reading from NV memory according to said encoded logical data structures, wherein said NV memory comprises X arrays that include physical data structures that differ in size from said encoded logical data structures, and wherein X is an integer greater than or equal to 1.

20. The method of claim 19 further comprising sending and receiving said data external to said NV memory system in logical data structures.

21. The method of claim 20 wherein said logical data structures comprise at least one of logical pages and logical blocks.

22. The method of claim 19 wherein said physical data structures comprise at least one of physical pages and physical blocks in said NV memory.

23. The method of claim 19 further comprising selecting one of N error correction code (ECC) rates, wherein N>1.

24. The method of claim 23 further comprising encoding said data according to at least one of a Reed Solomon scheme, a Bose-Chaudhuri-Hocquenghem (BCH) scheme, a Low Density Parity Check (LDPC) scheme, a Gray code scheme, and a combination of two or more of said BCH scheme, said LDPC scheme, and said Gray code scheme.

25. The method of claim 23 further comprising decoding said encoded logical data structures during a read operation from said NV memory.

26. The method of claim 19 further comprising writing to said X arrays in parallel when X>1.

27. The method of claim 26 further comprising writing a first portion of a first of said encoded logical data structures to a first of said X arrays while writing a second portion of said first of said encoded logical data structures to a second of said X arrays.

28. The method of claim 27 further comprising writing a first portion of a second of said encoded logical data structures to said second of said arrays while writing said first and second portions of said first of said encoded logical data structures.

29. The method of claim 26 further comprising allocating buffers within said X arrays for each of said encoded logical data structures so that portions of said encoded logical data structures that do not fit into said physical data structures are stored in said buffers.

30. The method of claim 26 wherein each of said X arrays corresponds to one or more memory chips.

31. The method of claim 19 further comprising determining an amount of data to erase in said NV memory based on a size of said encoded logical data.

32. The method of claim 31 wherein said amount of data includes data within a predetermined number of cells within all of said X arrays.

33. The method of claim 19 wherein said NV memory comprises at least one of flash memory, static random access memory (SRAM), nitride read only memory (NROM), phase change memory, magnetic RAM and multi-state memory.

34. The method of claim 19 wherein said physical data structures differ in size from said encoded logical data structures so that a size of said physical data structures and a size of said encoded logical data structures do not have an integer relationship.

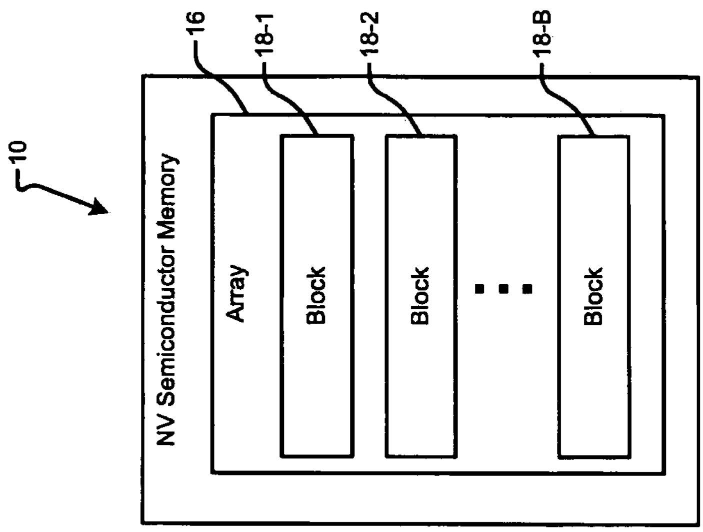

FIG. 1
(Prior Art)

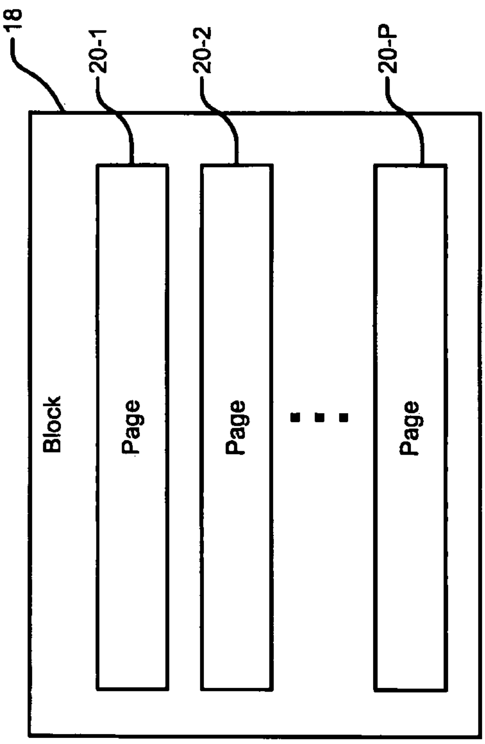

FIG. 2A
(Prior Art)

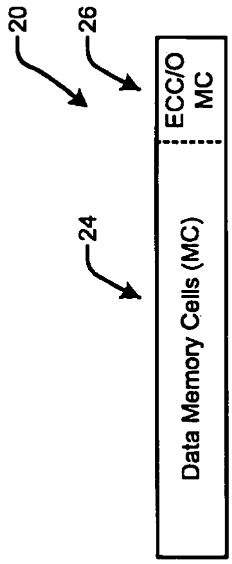

FIG. 2B
(Prior Art)

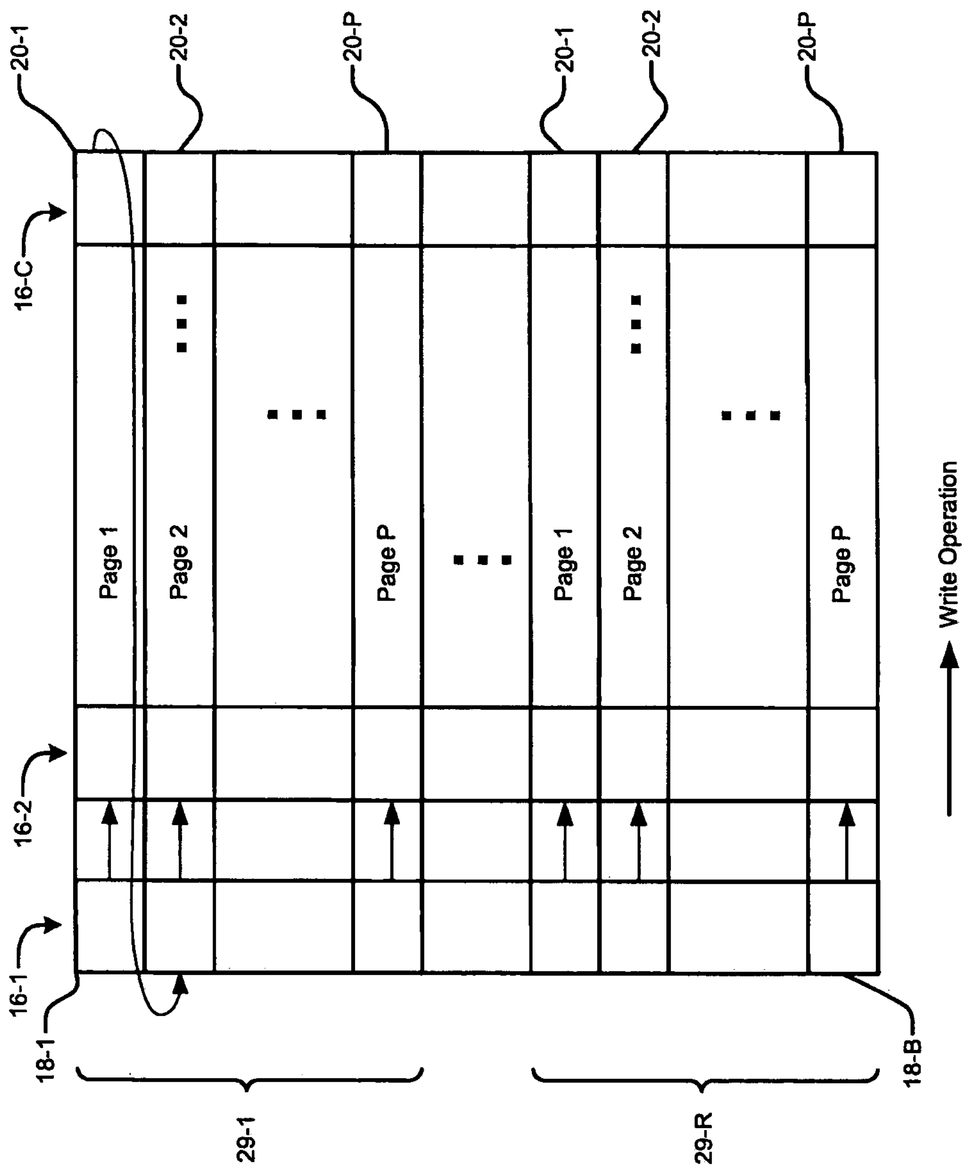

FIG. 2C
Prior Art

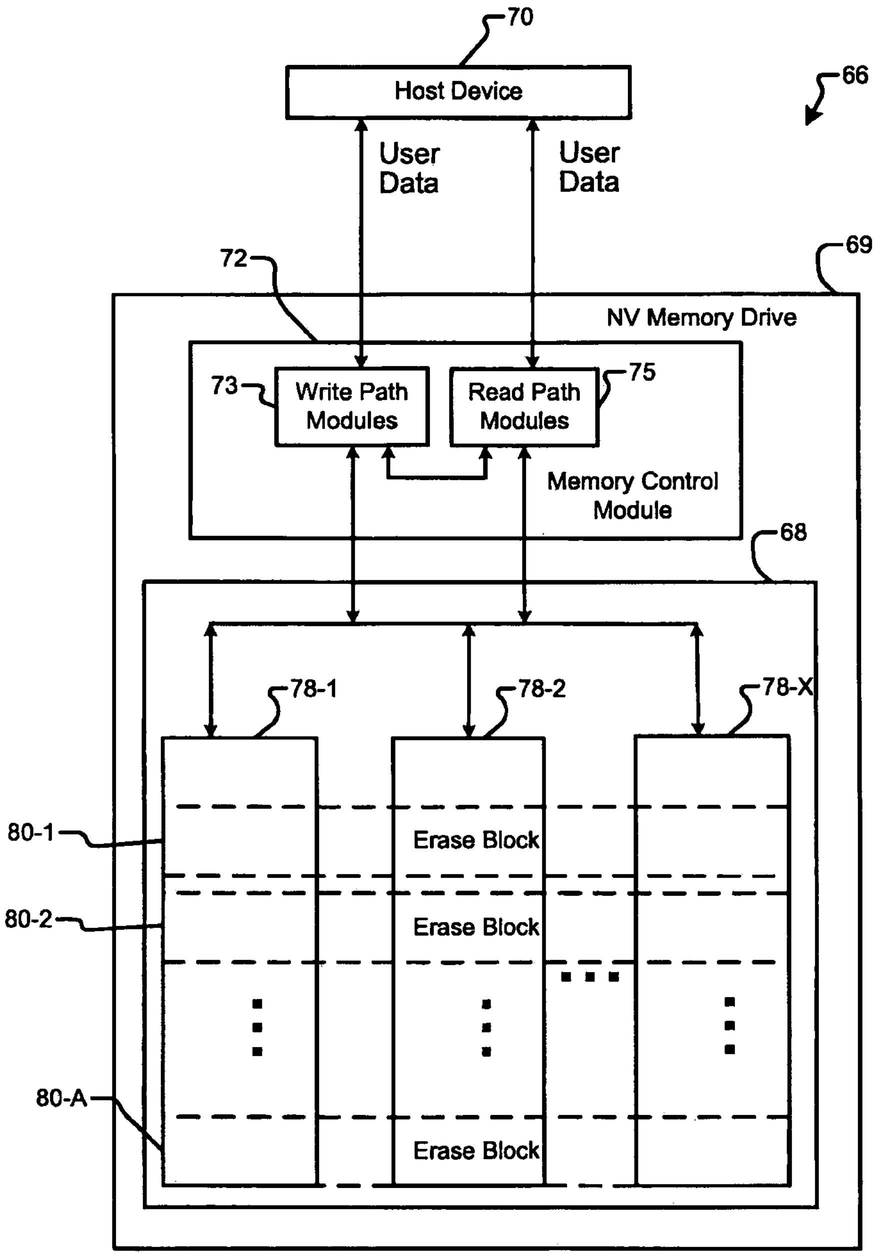
70
Host Device
66
User Data
User Data
72
69
NV Memory Drive
73
Write Path Modules
Read Path Modules
75
Memory Control Module
68
78-1
78-2
78-X
80-1
Erase Block
80-2
Erase Block
80-A
Erase Block

FIG. 3A

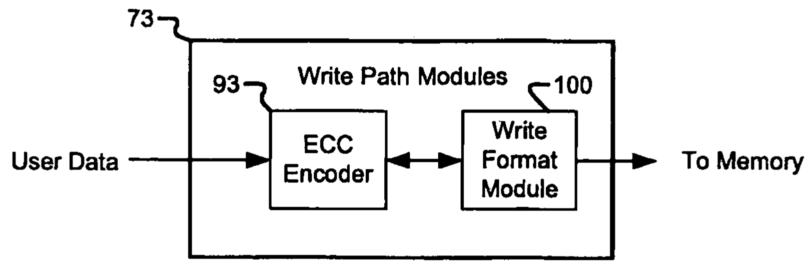
73
Write Path Modules
93
100
User Data
ECC Encoder
Write Format Module
To Memory

FIG. 3B

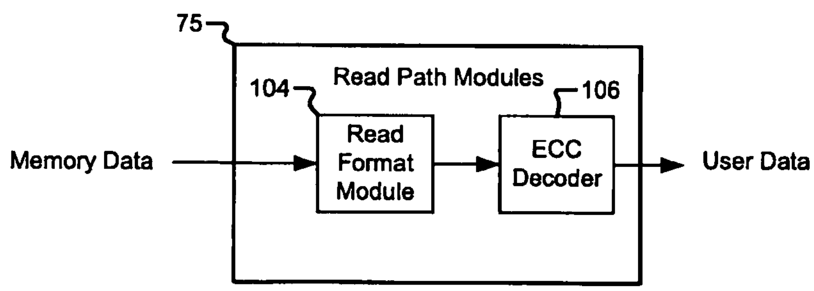
75
Read Path Modules
104
106
Memory Data
Read Format Module
ECC Decoder
User Data

FIG. 3C

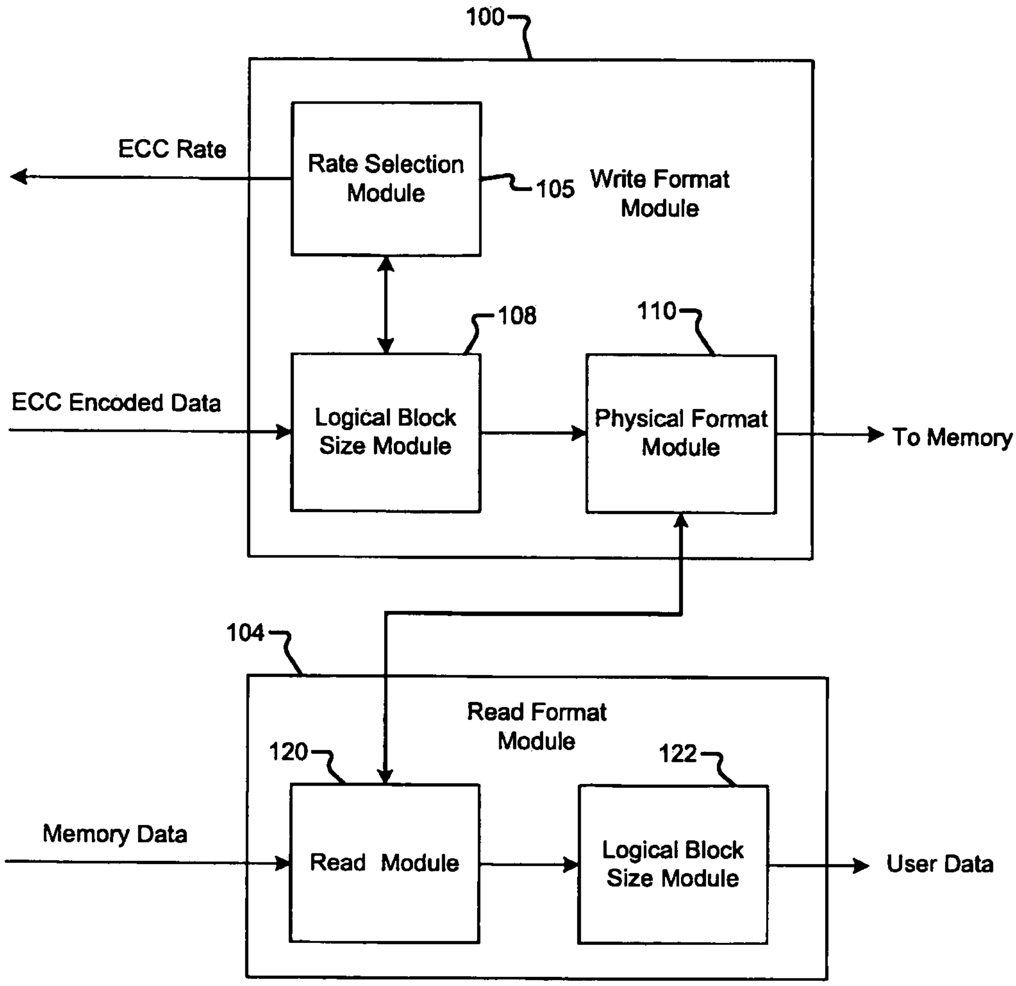
100
ECC Rate
Rate Selection Module
105
Write Format Module
108
110
ECC Encoded Data
Logical Block Size Module
Physical Format Module
To Memory
104
Read Format Module
120
122
Memory Data
Read Module
Logical Block Size Module
User Data

FIG. 3D

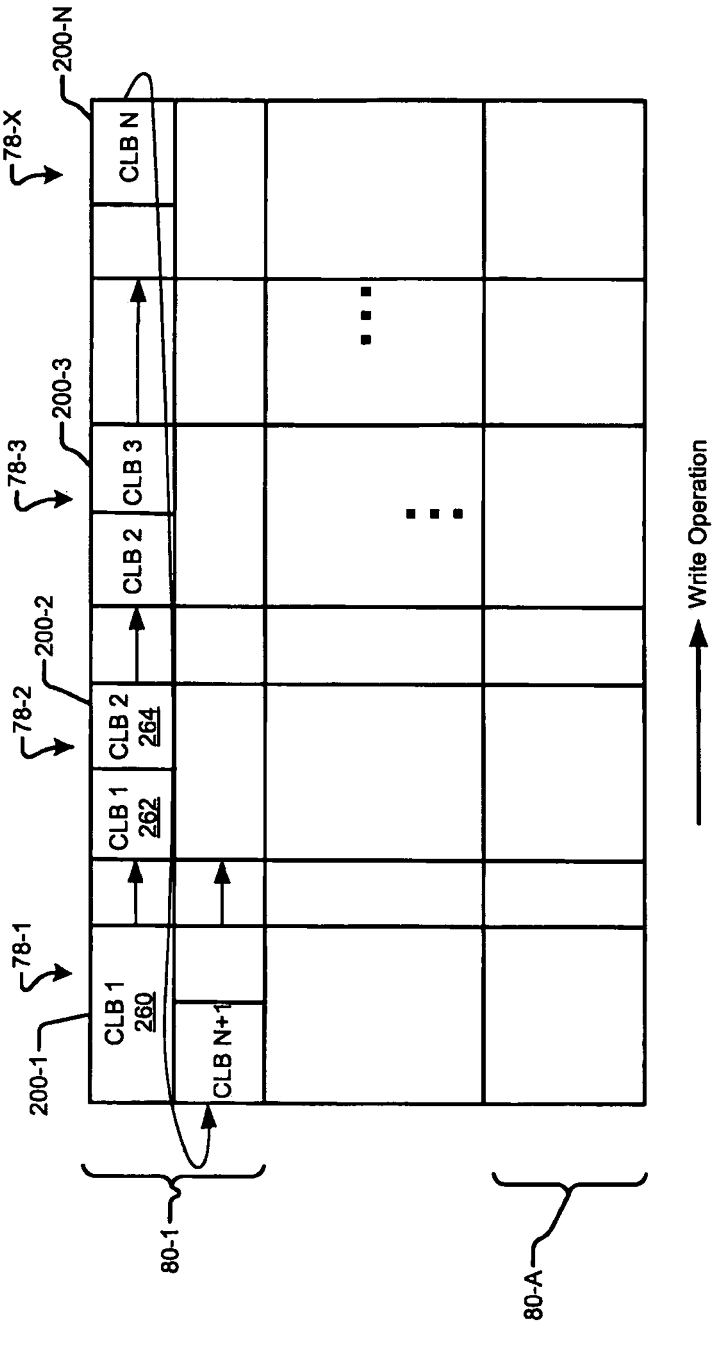
200-N
78-X
CLB N
200-3
78-3
CLB 3
CLB 2
200-2
78-2
CLB 2
264
CLB 1
262
78-1
CLB 1
260
200-1
CLB N+1
80-1
80-A
Write Operation

FIG. 4

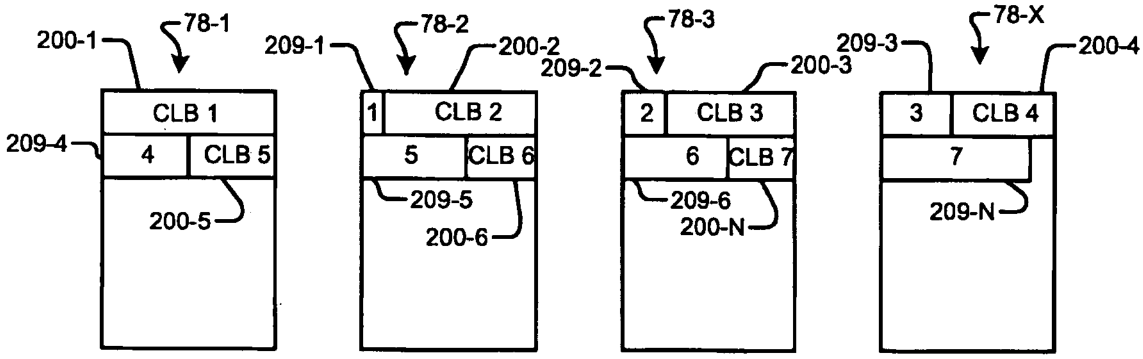
78-1
78-2
78-3
78-X
200-1
209-1
200-2
209-2
200-3
209-3
200-4
CLB 1
1
CLB 2
2
CLB 3
3
CLB 4
209-4
4
CLB 5
5
CLB 6
6
CLB 7
7
200-5
209-5
200-6
209-6
200-N
209-N

FIG. 5

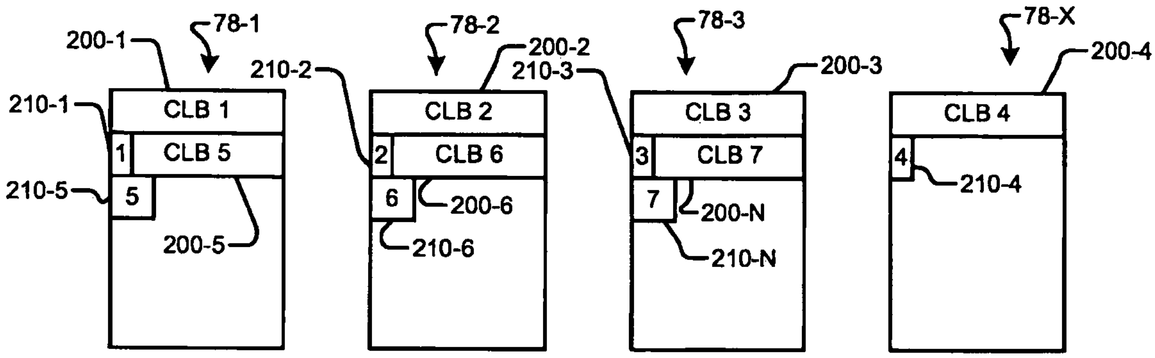
78-1
78-2
78-3
78-X
200-1
210-2
200-2
210-3
200-3
200-4
210-1
CLB 1
CLB 2
CLB 3
CLB 4
1
CLB 5
2
CLB 6
3
CLB 7
4
210-4
210-5
5
6
200-6
7
200-N
200-5
210-6
210-N

FIG. 6

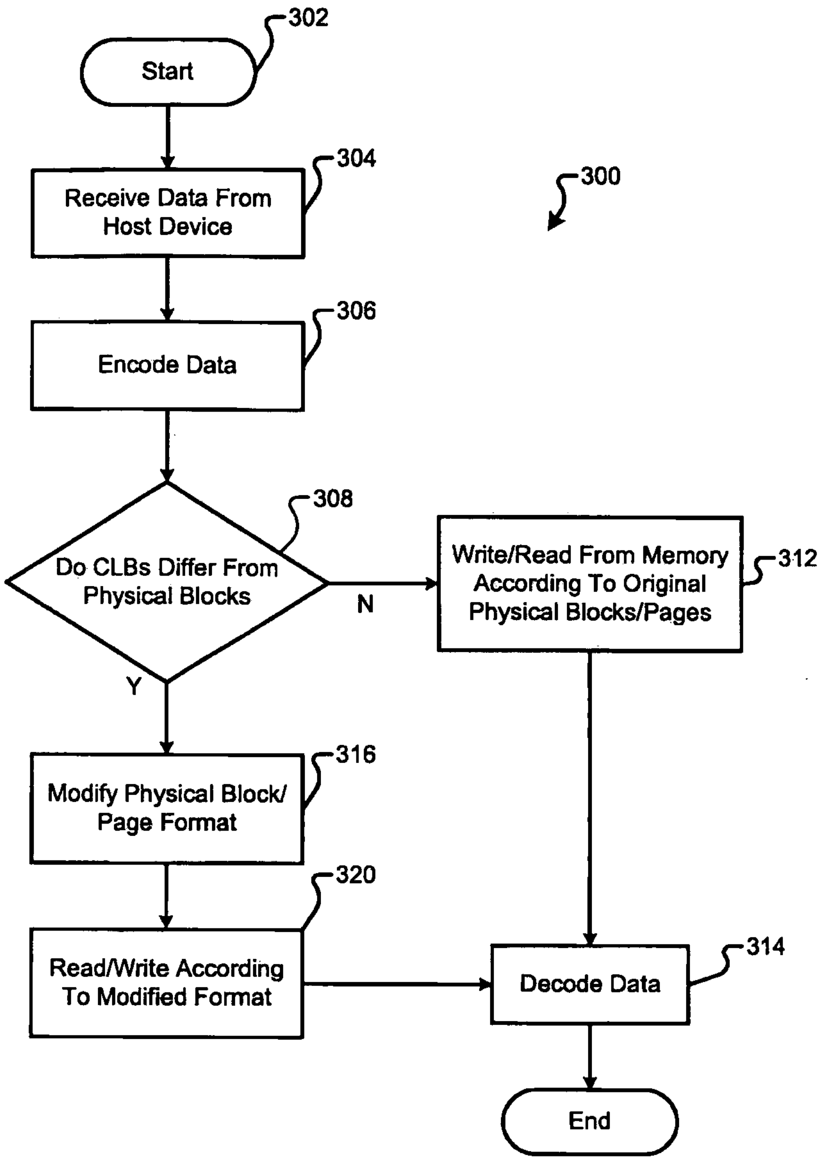
302
Start
304
Receive Data From Host Device
300
306
Encode Data
308
Do CLBs Differ From Physical Blocks
N
Y
Write/Read From Memory According To Original Physical Blocks/Pages
312
316
Modify Physical Block/ Page Format
320
Read/Write According To Modified Format
314
Decode Data
End

FIG. 7

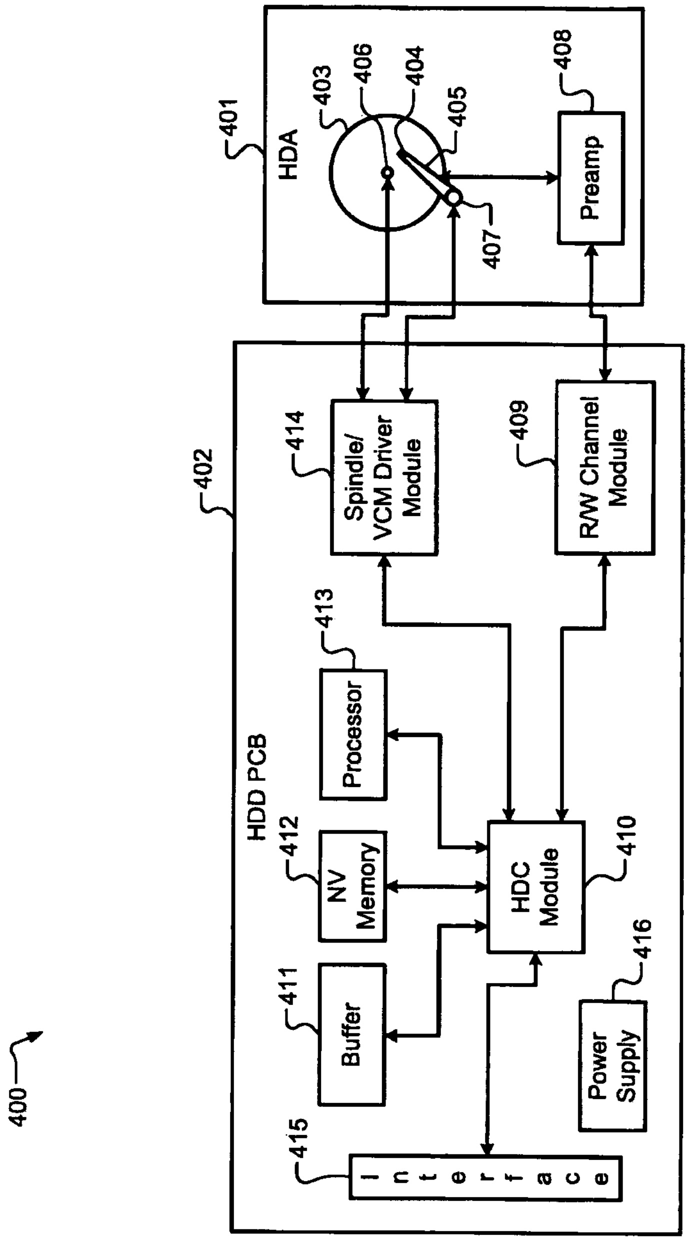
401
HDA
403
406
404
405
407
408
Preamp
402
HDD PCB
414
Spindle/ VCM Driver Module
409
R/W Channel Module
413
Processor
412
NV Memory
410
HDC Module
411
Buffer
416
Power Supply
415
Interface
400

FIG. 8A

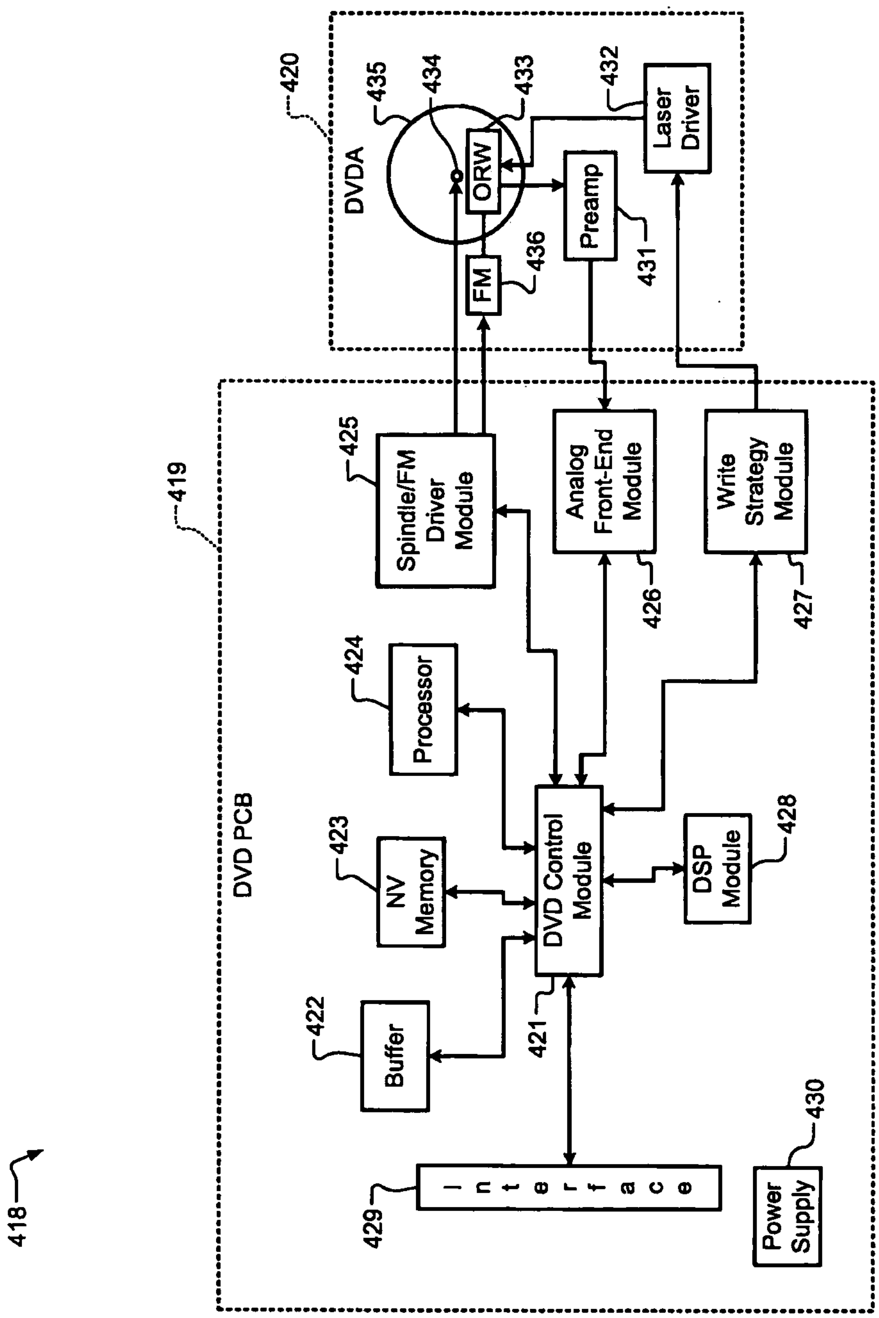
418
419
DVD PCB
420
DVDA
429
I n t e r f a c e
422
Buffer
423
NV Memory
424
Processor
425
Spindle/FM Driver Module
421
DVD Control Module
426
Analog Front-End Module
427
Write Strategy Module
428
DSP Module
430
Power Supply
431
Preamp
432
Laser Driver
433
ORW
434
435
436
FM

FIG. 8B

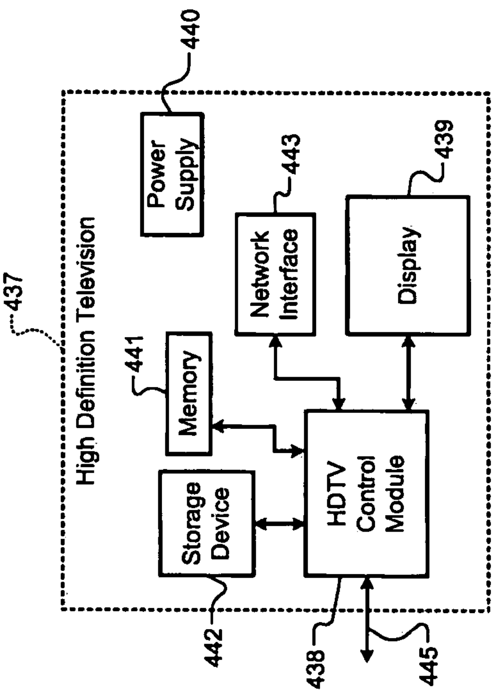
437
High Definition Television
Power Supply
440
Memory
441
Network Interface
443
Display
439
Storage Device
442
HDTV Control Module
438
445

FIG. 8C

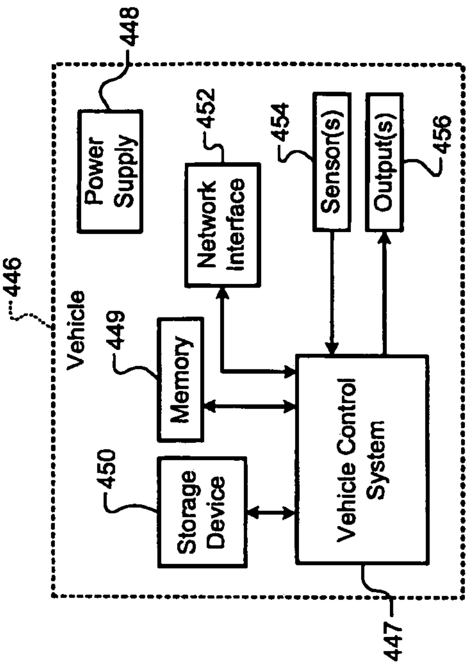
446
Vehicle
Power Supply
448
Memory
449
Network Interface
452
Sensor(s)
454
Output(s)
456
Storage Device
450
Vehicle Control System
447

FIG. 8D

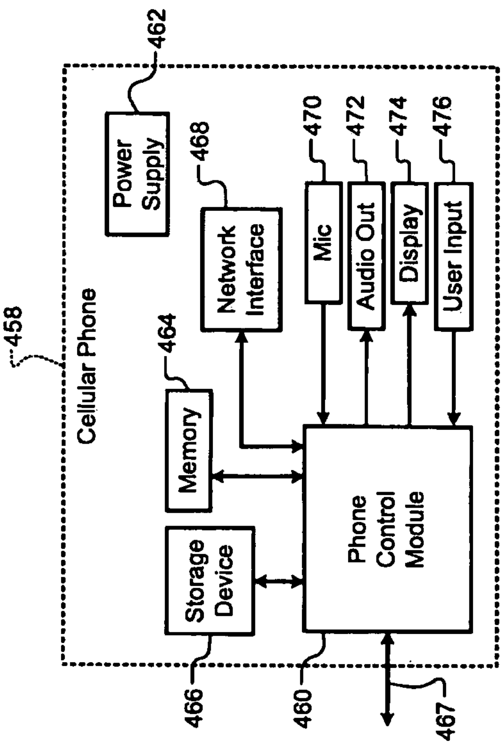
458
Cellular Phone
Power Supply
462
Network Interface
468
Memory
464
Storage Device
466
Phone Control Module
460
467
Mic
470
Audio Out
472
Display
474
User Input
476

FIG. 8E

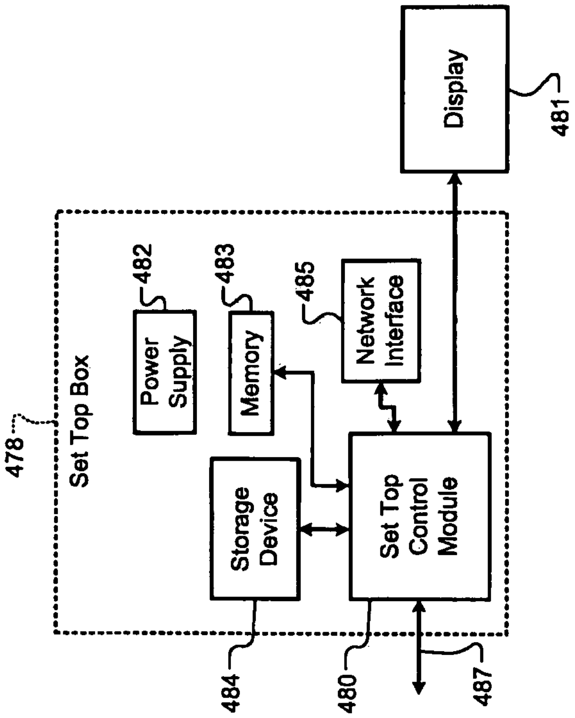
478
Set Top Box
Power Supply
482
Memory
483
Network Interface
485
Storage Device
484
Set Top Control Module
480
487
Display
481

FIG. 8F

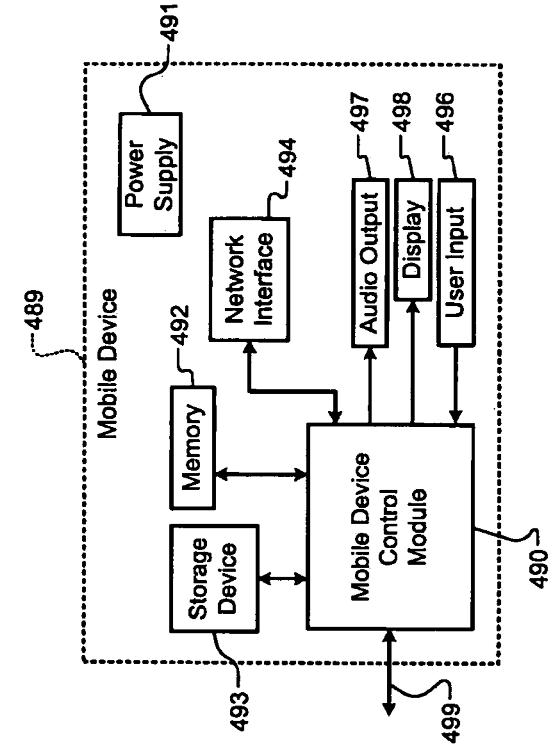
Mobile Device
489
Power Supply
491
Network Interface
494
Memory
492
Storage Device
493
Mobile Device Control Module
490
Audio Output
497
Display
498
User Input
496
499

FIG. 8G