



(51) International Patent Classification:

H01L 27/112 (2006.01) *H01L 23/525* (2006.01)
H01L 21/768 (2006.01)

(21) International Application Number:

PCT/US2017/025458

(22) International Filing Date:

31 March 2017 (31.03.2017)

(25) Filing Language:

English

(26) Publication Language:

English

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) Inventors: **THEN, Han Wui**; 4836 NW 162nd Terrace, Portland, Oregon 97229 (US). **PILLARISETTY, Ravi**; 925 NW Hoyt St, APT 226, Portland, Oregon 97209 (US). **DASGUPTA, Sansaptak**; 132 NE Greenridge Terrace, Hillsboro, Oregon 97124 (US). **RADOSAVLJEVIC, Marko**; 3684 NW Lorian, Portland, Oregon 97229 (US). **FISCHER, Paul B.**; 1558 NW 129th Place, Portland, Oregon 97229 (US).

(74) Agent: **ALI, Syed Nazeer**; Hanley, Flight & Zimmerman, LLC, 150 S. Wacker Drive, Suite 2200, Chicago, Illinois 60606 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG,

MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: SEMICONDUCTOR FUSE ELEMENTS AND METHODS OF PRODUCING THE SAME

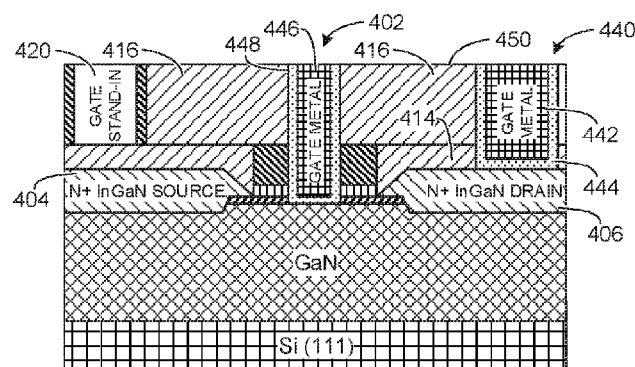


FIG. 4D

(57) Abstract: Semiconductor fuse elements and method of producing the same are disclosed. A disclosed example multilayered die includes a transistor comprising a source, a drain and a gate, a metal interconnect extending through an interlayer dielectric, and a dielectric layer disposed between the metal interconnect and the drain to define a programmable fuse element.



SEMICONDUCTOR FUSE ELEMENTS AND METHODS OF PRODUCING THE SAME

FIELD OF THE DISCLOSURE

[0001] This disclosure relates generally to semiconductor fabrication and, more particularly, semiconductor fuse elements and methods of producing the same.

BACKGROUND

[0002] Semiconductor devices such as microprocessors (e.g., processors) and/or integrated circuits have become smaller and more compact, while their die transistor counts have increased dramatically due to increasing computational needs (e.g., transistor counts in the billions). With this increased compactness, programmable logic circuits, such as fuse elements (e.g., semiconductor fuse elements), have been implemented onto the semiconductor devices. These fuse elements are used to program read-only memory (ROM) in integrated circuits such as radio frequency front-end modules (FEMs) or silicon on chip (SoC) designs.

[0003] Typical programmable fuse elements, which may be coupled to and/or be integrated in transistors, of semiconductor devices usually include a metal contact disposed between two different metals. In operation, a relatively high current is provided to select fuse elements of a semiconductor device, thereby resulting in thermally accelerated metal electro-migration in the select and/or designated fuse elements. As a result, respective contacts of the select fuse elements are prevented from carrying current, thereby effectively removing operational capabilities (e.g., current flow capabilities) of a portion of these fuse elements.

[0004] Known programmable fuse elements may require additional spacing, fabrication steps and/or materials beyond those needed for typical device fabrication (e.g., typical transistor and interconnect fabrication). Accordingly, implementation of these known fuse elements may necessitate

increased cost or manufacturing lead-times.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 is a cross-sectional view illustrating a known fuse element.

[0006] FIG. 2A illustrates an example wafer in which the examples disclosed herein may be implemented.

[0007] FIG. 2B illustrates an example die of the wafer of FIG. 2A.

[0008] FIG. 3 is a flowchart representative of an example method to produce dielectric fuse devices in accordance with the teachings of this disclosure.

[0009] FIGS. 4A-4D are detailed cross-sectional views along a line 4-4 of FIG. 2B depicting a device at various stages of fabrication to produce an example dielectric device in accordance with the teaching of this disclosure.

[0010] FIG. 5 is a flowchart representative of an alternative example method to produce an alternative example fuse device in accordance with the teachings of this disclosure.

[0011] FIGS. 6A and 6B are detailed cross-sectional views of an example fuse device produced using the example method of FIG. 5.

[0012] The figures are not to scale. Instead, to clarify multiple layers and regions, the thickness of the layers may be enlarged in the drawings. Wherever possible, the same reference numbers will be used throughout the drawing(s) and accompanying written description to refer to the same or like parts. As used in this patent, stating that any part (e.g., a layer, film, etc.) is in any way positioned on (e.g., positioned on, located on, disposed on, or formed on, etc.) another part, means that the referenced part is either in contact with the other part, or that the referenced part is above the other part with one or more intermediate part(s) located therebetween. Stating that any part is in contact with another part means that there is no intermediate part between the two parts.

DETAILED DESCRIPTION

[0013] Semiconductor fuse elements and methods of producing the same are disclosed. Known fuse elements integrated onto semiconductor devices and/or semiconductor dies usually require metal layers and/or structures having dissimilar materials. During programming of these known fuse elements, current passing through a contact disposed between two metal layers that are composed of different metals accelerates electron migration, thereby effectively rendering a respective fuse element inoperable for later operation. Often, numerous predetermined and/or selected fuse elements (e.g., a portion of the fuse elements defined) are provided with a relatively high current (e.g., a current greater than a threshold) to render them inoperable based on metal electro-migration. In particular, these known programmable fuse elements are often implemented in read-only memory (ROM) of fabricated semiconductor devices. Because of additional processing steps, material and/or space requirements beyond normal fabrication, implementation of these known fuse elements may necessitate increased costs as well as increased production times.

[0014] The examples disclosed herein enable cost-effective and reliable semiconductor fuse elements. In particular, some of the examples disclosed herein utilize a metal contact and a dielectric layer (e.g., silicon dioxide, silicon nitride, hafnium dioxide) that is disposed between the metal contact and a drain of a transistor (e.g., a gallium nitride n-type transistor) to define a fuse element. In such examples, a current above a threshold value may be applied to the contact to affect the dielectric layer (e.g., burn through the dielectric layer), thereby causing the metal contact to define an electrical short to the gate. As a result, the respective transistor is enabled.

[0015] Some of the examples disclosed herein utilize a multilayer fuse that is coupled to a drain of a transistor to define a re-programmable fuse element. This multilayer fuse may include a first metal layer, a reactive metal layer, an oxygen-rich layer and a second metal layer that is different from the first metal layer.

[0016] FIG. 1 is a cross-sectional view illustrating a known fuse element 100. The known fuse element 100 includes a multilayered structure 101, which includes a first metal layer 102, an interlayer dielectric 104, a second metal layer 106 that is composed of a different material from the first metal layer 102, and an interlayer dielectric 108, which may be etched off to expose the second metal layer 106 (e.g., for programming, etc.). According to the illustrated view of FIG. 1, a metal contact 110 disposed in the interlayer dielectric 104 extends between the first metal layer 102 and the second metal layer 106.

[0017] To program the fuse element 100, a voltage is applied between the first metal layer 102 and the second metal layer 106, thereby causing a current to flow across/through the metal contact 110. As a result, thermally accelerated metal electro-migration occurs between the first metal layer 102 and the second metal layer 106. Thereafter, the metal electro-migration prevents the contact 110 from being able to carry a significant amount of current (e.g., any current) flowing therethrough. In other words, because a significant amount of current is applied across the contact 110, the fuse element 100 no longer operates as a conductor during later operation because the contact 110 will not carry current. As a result, a transistor, of which the contact 110 is a part, may be prevented from functioning.

[0018] Currently, the first and second metal layers 102, 106 are different metals from those used in fabrication of semiconductor structures such as transistors and/or metal interconnects. Therefore, defining and/or fabricating the fuse element 100 may require additional processing time and/or costs.

[0019] FIG. 2A illustrates an example wafer 200 in which the examples disclosed herein may be implemented. The wafer 200 of the illustrated example consists of multiple semiconductor dies (e.g., system on a chip dies). These dies may be incorporated with semiconductor fuse elements disclosed herein during fabrication processes/steps. In this example, the individual semiconductor dies are functionally tested prior to being separated (e.g., cut) from the wafer 200. In particular, test patterns are provided to each

individual die and each individual die is monitored to have a designated response. In some examples, faulty dies discovered during this testing are discarded.

[0020] FIG. 2B illustrates an example die or system on a chip (e.g., a system on a chip die) 202 of the wafer 200 of FIG. 2A. In this example, the die 202 is cut from the wafer 200 and separated (e.g., cut and/or sliced) from the wafer 200 after being successfully tested with the aforementioned functionality test described above. The die 202 of the illustrated example may be used as an integrated circuit, a processor, a silicon on chip device and/or a radio frequency module, etc. The cross-section marked as 4-4 is described in greater detail below in connection with processing steps shown in FIGS. 4A-6B.

[0021] FIG. 3 is a flow chart representative of an example method 300 in accordance with the teachings of this disclosure. In particular, the example method 300 is used to define a dielectric fuse element in which a dielectric layer is used in conjunction with a metal interconnect that is electrically coupled to a drain of a transistor. The example method 300 of FIG. 3 begins as a wafer (e.g., the wafer 200) having a plurality of dies and/or silicon on chip devices is being fabricated. In particular, multiple layers are being placed (e.g., stacked, applied and/or deposited) to define individual multilayered dies. In this example, numerous applications of materials and/or coatings along with numerous etching and/or exposure processes are being used to produce and/or define these individual dies.

[0022] In this example, an interlayer dielectric is etched (e.g., selectively etched, etched using a mask layer, etc.) to expose a drain of a transistor disposed on a die (e.g., a substrate of a die) (block 302). In this example, the transistor is a gallium nitride n-type transistor. In some examples, multiple etching processes are used to expose the drain.

[0023] According to the illustrated example, a dielectric layer is provided on or coupled to the exposed drain on the die (block 304). In particular, the dielectric layer is deposited and/or layered onto the exposed drain of the transistor.

[0024] Next, a metal interconnect is coupled to the drain via the dielectric layer (block 306). In particular, the metal interconnect may be applied using a deposition and/or metallization process. In some examples, the dielectric layer is coupled to the drain along with metal interconnect (e.g., the both the metal interconnect and the dielectric layer are applied/provided simultaneously and/or during a same process, etc.).

[0025] FIGS. 4A-4D are detailed cross-sectional views along a line 4-4 of FIG. 2B depicting example steps to produce an example dielectric device in accordance with the teaching of this disclosure. Turning to FIG. 4A, a multilayered die structure 400 is shown. The multilayered die structure 400 of the illustrated example defines a transistor (e.g., an n-type gallium nitride transistor) and/or a transistor precursor that is undergoing fabrication to include functionality of a fused transistor element structure described below in connection with FIG. 4D and in accordance with the teachings of this disclosure.

[0026] According to the illustrated example, the multilayered die structure 400 includes a gate (e.g., a gate structure, a gate precursor, etc.) 402 that includes a gate dielectric 403 and a gate spacer 405, a source (e.g., an indium gallium nitride source) 404, a drain (e.g., an indium gallium nitride drain) 406, a substrate or body (e.g., a semiconductor substrate) 410 that is composed of gallium nitride in this example, and a silicon layer 412 disposed below the body 410. The example multilayered die structure 400 also includes a first interlayer dielectric 414 and a second interlayer dielectric 416 that is disposed above the first interlayer dielectric 414. The example second interlayer dielectric 416 includes contact precursors or structures 418.

[0027] In this example, gate stand-in material (e.g., a dummy material, a holder material, etc.) 420 is disposed in the second interlayer dielectric 416 proximate and/or above the source 404. Further, another stand-in material 424 is also disposed in the second interlayer dielectric proximate the gate 402. Similarly, stand-in material 426 is disposed in and/or above the second interlayer dielectric 416 proximate the drain 406.

[0028] Turning to FIG. 4B, a mask 430 has been provided above the second interlayer dielectric 416. In particular, the mask 430 is applied in a pattern (e.g., during a lithography process), thereby defining openings 432 in the mask 430. As a result, the stand-in material 420 corresponding to the source 406 is covered and/or protected by the masking 430. In other examples, the mask 430 is partially etched to define the openings 432.

[0029] To expose regions of the multilayered die structure 400 so that the gate 402 and the drain 406 can be electrically coupled to metal interconnects/contacts, the stand-in materials 424, 426 are etched away (e.g., a chemical etch process, a wet-etch process, a mechanical etching process, etc.) based on the aforementioned pattern of the masking 430. As a result, openings 434, 436 are defined at the respective contact structures 418. At this step, the first interlayer dielectric 414 is not yet etched. In this example, both of the stand-in materials 424, 426 are etched during the same etching process.

[0030] FIG. 4C depicts an additional etching process that has been used to define an opening 437 corresponding to the drain 406 and an opening 438 corresponding to the gate 402. In this example, a wet chemistry etch and/or a selective etch has been performed to increase respective depths of the openings 437, 438.

[0031] Now referring to FIG. 4D, an example fuse structure 440 is shown in accordance with the teachings of this disclosure. According to the illustrated example of FIG. 4D, the opening 437 (shown in FIG. 4C) has been provided with a metal contact 442 that is electrically coupled to the example drain 406. In this example, a dielectric layer 444 is disposed between the metal contact 442 and the drain 406, thereby defining a fuse element and/or fuse programming functionality. In particular, the metal contact as well as the dielectric layer 444 extend through the first interlayer dielectric 414. Further, the opening 438 (shown in FIG. 4C) of the gate 402 has been provided with a contact 446 that is at least partially surrounded and/or enclosed by a dielectric layer 448.

[0032] In this example, the metal contacts 442, 446 and the respective dielectric layers 444, 448 are defined, deposited and/or added during the same

process(es) to increase efficiency (e.g., time and/or cost efficiency) of the overall fabrication process. In some examples, the dielectric layers 444, 448 are applied/deposited prior to the metal contacts 442, 446 being defined and/or added/deposited (e.g., during a metallization and/or deposition process). In such examples, the metal contacts 442, 446 may be composed of the same materials. Likewise, both of the dielectric layers 444, 448 may be composed of the same materials. In such examples where either metal contacts or dielectric materials involve shared materials, the common materials may be applied during the same process, thereby increasing manufacturing/fabrication efficiency. In other examples, the metal contact 442 may have a different composition and/or processing from the metal contact 446. Additionally or alternatively, the dielectric layer 444 and the dielectric layer 448 may differ from one another in thickness and/or composition.

[0033] In this example, the dielectric layers 448, 444 are composed of silicon dioxide (SiO_2), which may range in thickness from approximately 2 to 10 nanometers (nm), for example. However, any appropriate material and/or dielectric layer stack may be used including materials with relative high dielectric constants (e.g., high kappa or K-values at a thickness of approximately 2 to 8 nm). In some examples, a silicon nitride (SiN) at a thickness between approximately 1 to 2 nm may be used. In some examples, hafnium dioxide (HfO_2) at a thickness of approximately 2 to 4 nm may be used.

[0034] To later define a contact structure that is to be electrically coupled to the source 404, a top surface 450 of the second interlayer dielectric 416 has been polished and/or etched to remove any appropriate masking or layers, thereby exposing the stand-in material 420. As a result, in this example, an additional etching process may be used to etch the stand-in material 420 so that a metal connect may be coupled (e.g., electrically and/or mechanically coupled) to the source 404.

[0035] In some examples, the metal contact 442 and the dielectric layer 444 are coupled to the source 404 instead. Additionally or alternatively, in some examples, the drain 406 is partially etched such that both the metal

contact 442 and the dielectric layer 444 at least partially extend into the drain 406 (e.g., into a portion of the drain 406 that is composed of indium gallium nitride).

[0036] To program the example fuse structure 440, a voltage above a threshold is applied to the metal contact 442, thereby causing breakdown of the dielectric layer 444 and, in turn, causing an electrical short between the metal contact 442 and the drain 406. In other words, the metal contact 442 is shorted to the drain 406, thereby causing an electrical coupling to be formed between the metal contact 442 and the drain 406. In this example, the applied current renders an associated transistor of the fuse structure 440 to be enabled instead of disabling the transistor, as described above in connection with the known fuse element 100 of FIG. 1.

[0037] FIG. 5 is a flowchart representative of an alternative example method 500 to produce an alternative example fuse device (shown below in connection with FIGS. 6A and 6B) in accordance with the teachings of this disclosure. In this example, a multilayered fuse structure is to be produced in conjunction with and/or as part of a transistor. In this example, the multilayered fuse device is reprogrammable (e.g., not permanently programmed by being rendered inoperable) based on a layered composition and/or layer stack-up in conjunction with reversing voltage polarities.

[0038] According to the illustrated example, an interlayer dielectric is etched to expose a drain of a transistor (block 502). In particular, the interlayer dielectric may be chemical etched, mechanically etched, and/or selectively etched. In some examples, at least portion of the drain is also etched.

[0039] Next, in some examples, a metal interconnect/contact is provided to the drain (block 504). In particular, the metal interconnect of the illustrated example is both electrically and mechanically coupled to the gate of the transistor.

[0040] A multilayered fuse (e.g., a fuse stack, a layered fuse) and/or a portion of the multilayered fuse (e.g., the metal interconnect/contact forms part of the multilayered fuse) is then coupled to the metal interconnect (block 506). For example, the multilayered fuse is coupled to the metal interconnect

in situ and/or pre-assembled/pre-stacked. In other examples, layers of the multilayer fuse are deposited in part(s) and/or individual layers. In some examples, the multilayered fuse is coupled to the drain of the transistor. Example structures/layering of the multilayered fuse are described in detail below in connection with FIGS. 6A and 6B. Finally, the process ends.

[0041] FIGS. 6A and 6B are detailed cross-sectional views of an example multilayered fuse device 600 produced using the example method 500 of FIG. 5. According to the illustrated example of FIG. 6A, the example fuse device 600 includes a fuse structure (e.g., a multilayer fuse, a layered fuse stack-up, layering leading up to and including the drain 406) 602, which is described below in detail in connection with FIG. 6B, an interlayer dielectric 604, a layered portion (e.g., a portion that is added to define fuse functionality) 608, and a metal contact (e.g., a trench contact metal) 610.

[0042] In this example, the metal contact 610 electrically bridges both the layered portion 608 as well as the drain 406 together. Further, the layered fuse portion is positioned within an etched region of the interlayer dielectric 604. In contrast to the fuse structure 440 of FIG. 4C, a dielectric layer is not disposed between the metal contact 610 and the drain 406. However, in some other examples, there may be a dielectric layer disposed between the metal contact 610 and the drain 406. Additionally or alternatively, the layered portion 608 may directly contact and/or be coupled to the drain 406.

[0043] Turning to FIG. 6B, the fuse structure 602 is shown in detail. According to the illustrated example, the layered portion 608 includes an upper metal layer 620, a reactive metal layer 622 that is below the upper metal layer 620, and an oxygen-rich layer 624 that is below the reactive metal layer 622. In this example, the metal contact 610 and the drain 406 are shown below the oxygen-rich layer 624 of the layered portion 608.

[0044] In this example, the reactive metal layer 622, which is implemented as hafnium in this example, is approximately 2-8 nm (e.g., 7 nm) thick. However, tantalum or zirconium may be used instead at a similar thickness, for example.

[0045] Further, the oxygen-rich layer 624, which is implemented as hafnium di-oxide in this example, is approximately 2-8 nm thick (e.g., 3 nm thick). In other examples, tantalum pentoxide (Ta_2O_5) or zirconium dioxide (ZrO_2) at a similar thickness, for example.

[0046] In this example, the upper metal layer 620 is composed of titanium nitride while the metal contact 610 is composed of tungsten. In this example, the drain 406 is composed of indium gallium nitride. However, any appropriate combination of dissimilar metals may be used.

[0047] In this example, the fuse structure 602 is reprogrammable between operative and in-operative states by reversing a polarity of voltage applied across the fuse structure 602. In particular, different polarities of applied voltage cause particle migration(s) between layers that render an operable state of the fuse structure 602.

[0048] The example materials and thicknesses used are only examples, and appropriate thickness and/or material composition(s) may be used, as appropriate, for the application. Further, the layer composition and/or stacking may be varied.

[0049] Example 1 includes a multilayered die comprising a transistor including a source, a drain, and a gate, and a metal interconnect extending through an interlayer dielectric, and a dielectric layer disposed between the metal interconnect and the drain to define a programmable fuse element.

[0050] Example 2 includes the subject matter of Example 1, and further includes a semiconductor substrate below the source and the drain.

[0051] Example 3 includes the subject matter of Example 2, where the semiconductor substrate includes gallium nitride.

[0052] Example 4 includes the subject matter of any one of Examples 3 or 4, and further includes.

[0053] Example 5 includes the subject matter of any one of Examples 1 to 4, where a contact of the gate and the metal interconnect comprise the same material.

[0054] Example 6 includes the subject matter of any one of Examples 1 to 5, and further includes a layered fuse structure above the metal interconnect.

[0055] Example 7 includes the subject matter of any one of Examples 1 to 6, where the transistor is an n-type gallium nitride transistor.

[0056] Example 8 includes the subject matter of any one of Examples 1 to 7, where the dielectric layer includes silicon dioxide.

[0057] Example 9 includes a method including etching an interlayer dielectric to expose a drain of a transistor on a die, and providing a dielectric layer to be disposed between the drain and a metal interconnect to define a programmable fuse element.

[0058] Example 10 includes the subject matter of Example 9, and further includes providing a semiconductor substrate below the drain, the semiconductor substrate including gallium nitride.

[0059] Example 11 includes the subject matter of Example 10, where the metal interconnect is a first metal interconnect, and further including providing the first metal interconnect during a same process step as providing a second metal interconnect to a gate of the transistor.

[0060] Example 12 includes the subject matter of Example 11, where the second metal interconnect is provided with the dielectric layer.

[0061] Example 13 includes the subject matter of any one of Examples 9 to 12, where the dielectric layer includes silicon dioxide.

[0062] Example 14 includes the subject matter of any one of Examples 9 to 13, where the transistor is an n-type gallium nitride transistor.

[0063] Example 15 includes a multilayered die comprising a transistor including a source, a drain, and a gate, and a multilayered fuse electrically coupled to the drain, where the multilayered fuse defines a programmable fuse element. The multilayered fuse includes a first metal layer, a second metal layer including a different material from the first metal layer, a reactive metal layer disposed between the first and second metal layers, and an oxygen-rich layer proximate the reactive metal layer.

[0064] Example 16 includes the subject matter of Example 15, where the reactive metal layer includes hafnium.

[0065] Example 17 includes the subject matter of Example 15, where the oxygen-rich layer includes hafnium di-oxide.

[0066] Example 18 includes the subject matter of Example 15, where the reactive metal layer includes zirconium.

[0067] Example 19 includes the subject matter of Example 18, where the oxygen-rich layer includes zirconium dioxide.

[0068] Example 20 includes the subject matter of Example 15, where the reactive metal layer includes tantalum.

[0069] Example 21 includes the subject matter of Example 20, where the oxygen-rich layer includes tantalum pentoxide.

[0070] Example 22 includes the subject matter of any one of Examples 15 to 21, where the first metal layer includes titanium nitride.

[0071] Example 23 includes the subject matter of any one of Examples 15 to 22, where the second metal layer includes tungsten.

[0072] Example 24 includes the subject matter of any one of Examples 15 to 23, where the reactive metal layer is approximately 2 to 8 nanometers thick.

[0073] Example 25 includes a method comprising etching a first interlayer dielectric to expose a drain of a transistor on a die, and coupling a multilayered fuse to the drain. The multilayered fuse includes a first metal layer, a second metal layer including a different material from the first metal layer, a reactive metal layer disposed between the first and second metal layers, and an oxygen-rich layer proximate the reactive metal layer.

[0074] Example 26 includes the subject matter of Example 25, where coupling the multilayered fuse to the drain includes assembling the multilayered fuse to a metal interconnect that is coupled to the drain.

[0075] Example 27 includes the subject matter of Example 25, where coupling the multilayered fuse to the drain includes depositing layers of the multilayered fuse separately.

[0076] Example 28 includes the subject matter of any one of Examples 25-27, where the reactive metal layer includes hafnium.

[0077] Example 29 includes the subject matter of Example 28, where the oxygen-rich layer includes hafnium di-oxide.

[0078] Example 30 includes the subject matter of any one of Examples 25-27, where the reactive metal layer includes zirconium.

[0079] Example 31 includes the subject matter of Example 30, where the oxygen-rich layer includes zirconium dioxide.

[0080] Example 32 includes the subject matter of any one of Examples 25-27, where the reactive metal layer includes tantalum.

[0081] Example 33 includes the subject matter of Example 32, where the oxygen-rich layer includes tantalum pentoxide.

[0082] Example 34 includes the subject matter of any one of Examples 25-33, where the first metal layer includes titanium nitride.

[0083] Example 35 includes the subject matter of any one of Examples 25-34, where the second metal layer includes tungsten.

[0084] Example 35 includes the subject matter of any one of Examples 25-34, where the second metal layer includes tungsten.

[0085] Example 36 includes the subject matter of any one of Examples 25-35, where the reactive metal layer is approximately 2 to 8 nanometers thick.

[0086] From the foregoing, it will be appreciated that the above disclosed methods, apparatus and articles of manufacture allow space-saving, reliable and cost-effective programmable elements for semiconductor devices. As a result, the examples disclosed herein enable overall reduced costs and sizes of their respective device packaging and/or structures (e.g., overall packaging of the semiconductor die and/or silicon on chip structures).

[0087] Although certain example methods, apparatus and articles of manufacture have been disclosed herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of manufacture fairly falling within the scope of the claims of this patent. While the examples disclosed herein generally show a single memory

bit or fuse element, the examples disclosed herein may be applied to an array of fuse elements to achieve larger memory blocks (e.g., kilobits, megabits, gigabits, etc.). Further, these fuse arrays may be fabricated as an integrated component that forms part of any appropriate logic processor chip, communications processor chip, RF front-end chip, etc.

What Is Claimed Is:

1. A multilayered die comprising:
a transistor including a source, a drain, and a gate;
a metal interconnect extending through an interlayer dielectric;
and
a dielectric layer disposed between the metal interconnect and the drain to define a programmable fuse element.
2. The multilayered die as defined in claim 1, further including a semiconductor substrate below the source and the drain.
3. The multilayered die as defined in claim 2, wherein the semiconductor substrate includes gallium nitride.
4. The multilayered die as defined in any one of claims 2 or 3, further including a silicon layer below the semiconductor substrate.
5. The multilayered die as defined in any one of claims 1-4, wherein a contact of the gate and the metal interconnect comprise the same material.
6. The multilayered die as defined in any one of claims 1-5, further including a layered fuse structure above the metal interconnect.
7. The multilayered die as defined in any one of claims 1-6, wherein the transistor is an n-type gallium nitride transistor.
8. The multilayered die as defined in any one of claims 1-7, wherein the dielectric layer includes silicon dioxide.
9. A method comprising:
etching an interlayer dielectric to expose a drain of a transistor on a die; and
providing a dielectric layer to be disposed between the drain and a metal interconnect to define a programmable fuse element.
10. The method as defined in claim 9, further including providing a semiconductor substrate below the drain, the semiconductor substrate including gallium nitride.

11. The method as defined in claim 10, wherein the metal interconnect is a first metal interconnect, and further including providing the first metal interconnect during a same process step as providing a second metal interconnect to a gate of the transistor.

12. The method as defined in claim 11, wherein the second metal interconnect is provided with the dielectric layer.

13. The method as defined in any one of claims 9-12, wherein the dielectric layer includes silicon dioxide.

14. The method as defined in any one of claims 9-13, wherein the transistor is an n-type gallium nitride transistor.

15. A multilayered die comprising:

a transistor including a source, a drain, and a gate; and

a multilayered fuse electrically coupled to the drain, the multilayered fuse defining a programmable fuse element, wherein the multilayered fuse includes:

a first metal layer,

a second metal layer including a different material from the first metal layer,

a reactive metal layer disposed between the first and second metal layers, and

an oxygen-rich layer proximate the reactive metal layer.

16. The multilayered die as defined in claim 15, wherein the reactive metal layer includes hafnium.

17. The multilayered die as defined in 16, wherein the oxygen-rich layer includes hafnium di-oxide.

18. The multilayered die as defined in claim 15, wherein the reactive metal layer includes zirconium.

19. The multilayered die as defined in 18, wherein the oxygen-rich layer includes zirconium dioxide.

20. The multilayered die as defined in claim 15, wherein the reactive metal layer includes tantalum.

21. The multilayered die as defined in claim 20, wherein the oxygen-rich layer includes tantalum pentoxide.

22. The multilayered die as defined in any one of claims 15-21, wherein the first metal layer includes titanium nitride.

23. The multilayered die as defined in any one of claims 15-22, wherein the second metal layer includes tungsten.

24. The multilayered die as defined in any one of claims 15-23, wherein the reactive metal layer is approximately 2 to 8 nanometers thick.

25. A method comprising:
etching a first interlayer dielectric to expose a drain of a transistor on a die; and
coupling a multilayered fuse to the drain, wherein the multilayered fuse includes:

- a first metal layer,
- a second metal layer including a different material from the first metal layer,
- a reactive metal layer disposed between the first and second metal layers, and
- an oxygen-rich layer proximate the reactive metal layer.

26. The method as defined in claim 25, wherein coupling the multilayered fuse to the drain includes assembling the multilayered fuse to a metal interconnect that is coupled to the drain.

27. The method as defined in claim 25, wherein coupling the multilayered fuse to the drain includes depositing layers of the multilayered fuse separately.

28. The method as defined in any one of claims 25-27, wherein the reactive metal layer includes hafnium.

29. The method as defined in claim 28, wherein the oxygen-rich layer includes hafnium di-oxide.

30. The method as defined in any one of claims 25-27, wherein the reactive metal layer includes zirconium.

31. The method as defined in 30, wherein the oxygen-rich layer includes zirconium dioxide.

32. The method as defined in any one of claims 25-27, wherein the reactive metal layer includes tantalum.

33. The method as defined in 32, wherein the oxygen-rich layer includes tantalum pentoxide.

34. The method as defined in any one of claims 25-33, wherein the first metal layer includes titanium nitride.

35. The method as defined in any one of claims 25-34, wherein the second metal layer includes tungsten.

36. The method as defined in any one of claims 25-35, wherein the reactive metal layer is approximately 2 to 8 nanometers thick.

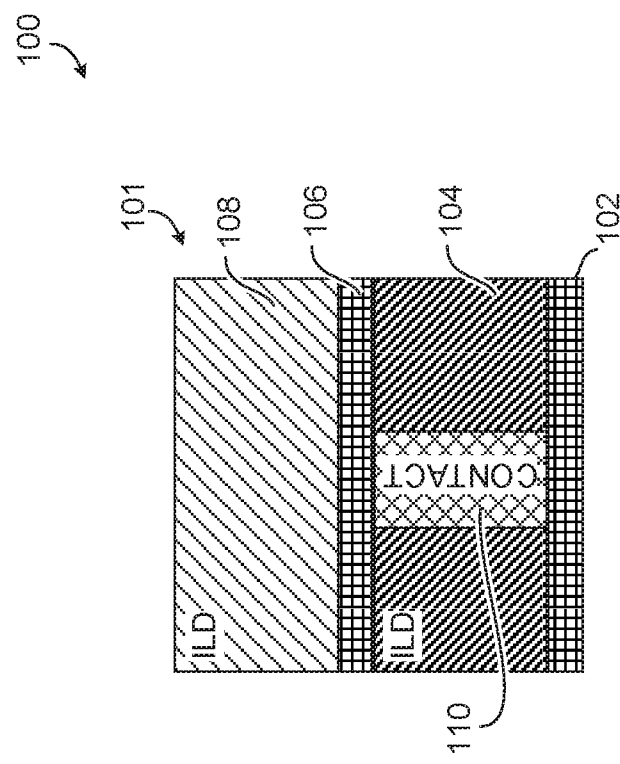
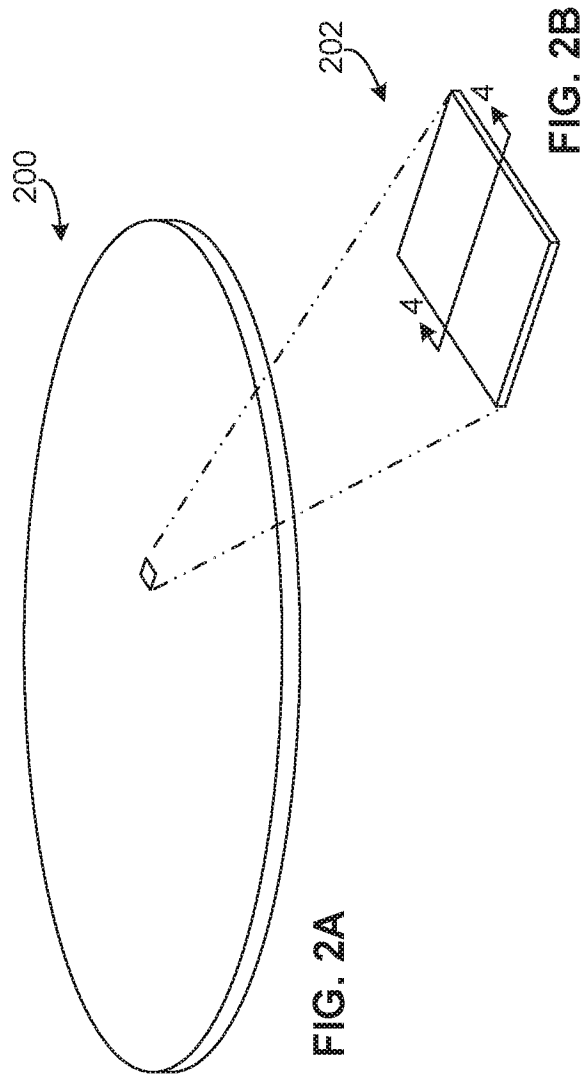
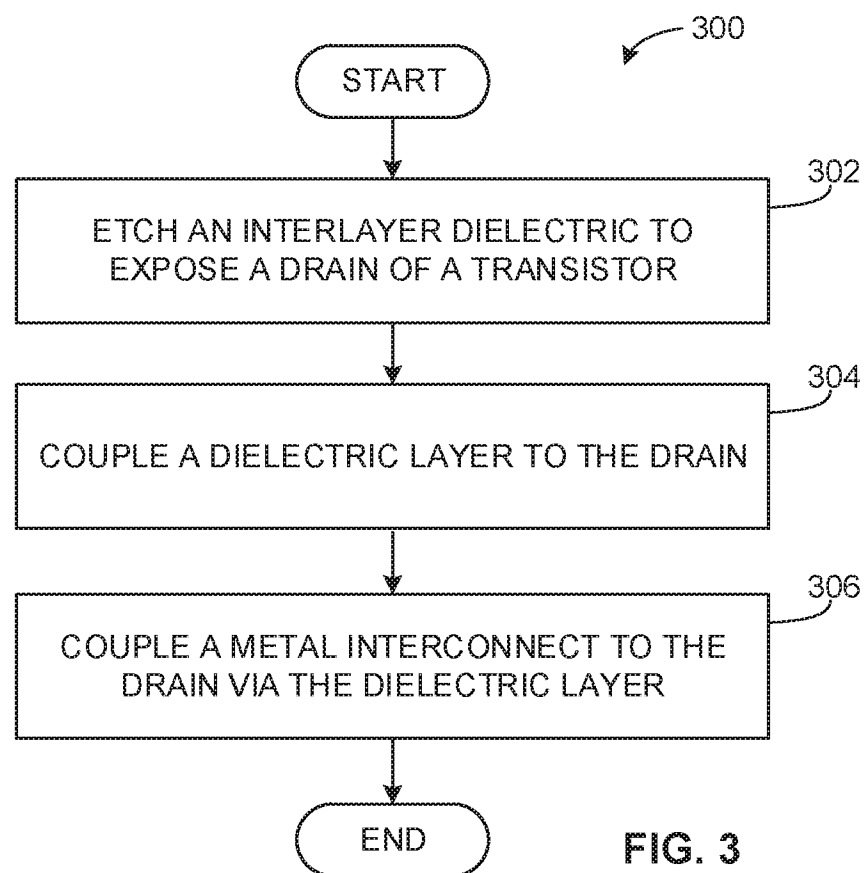
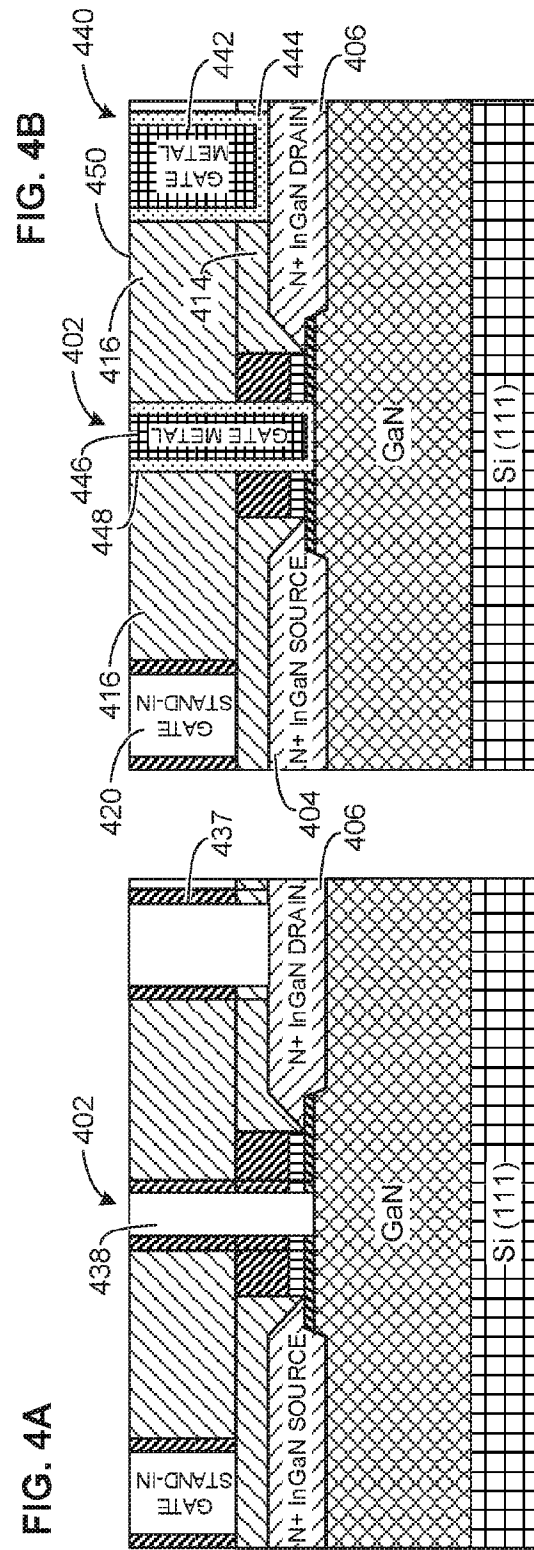
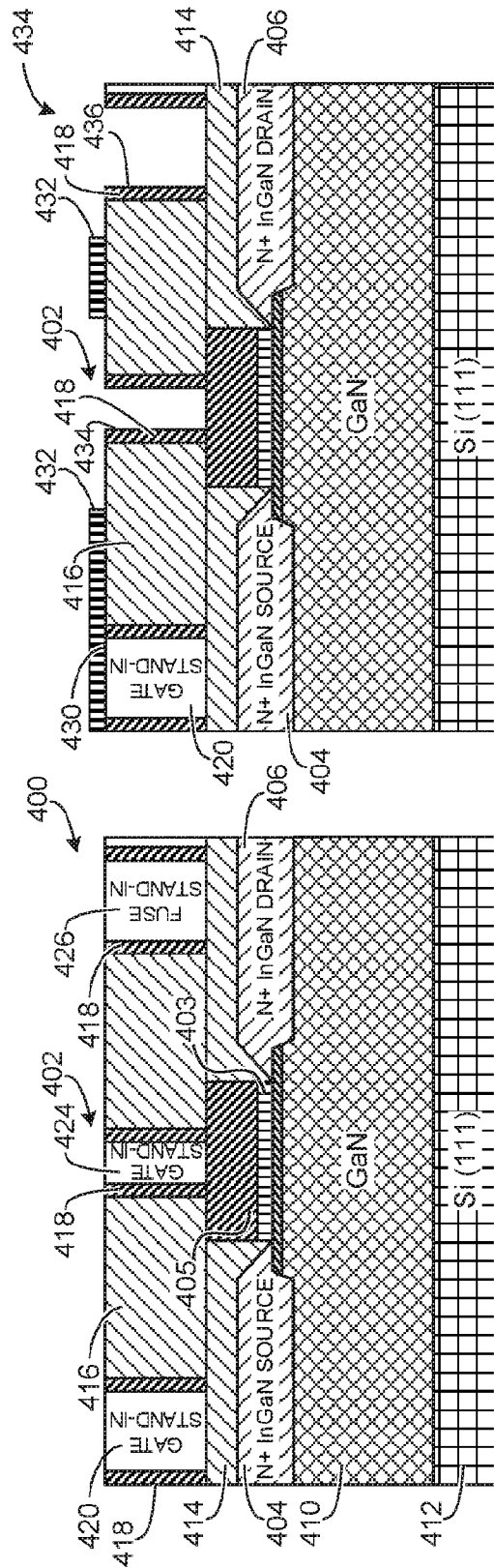
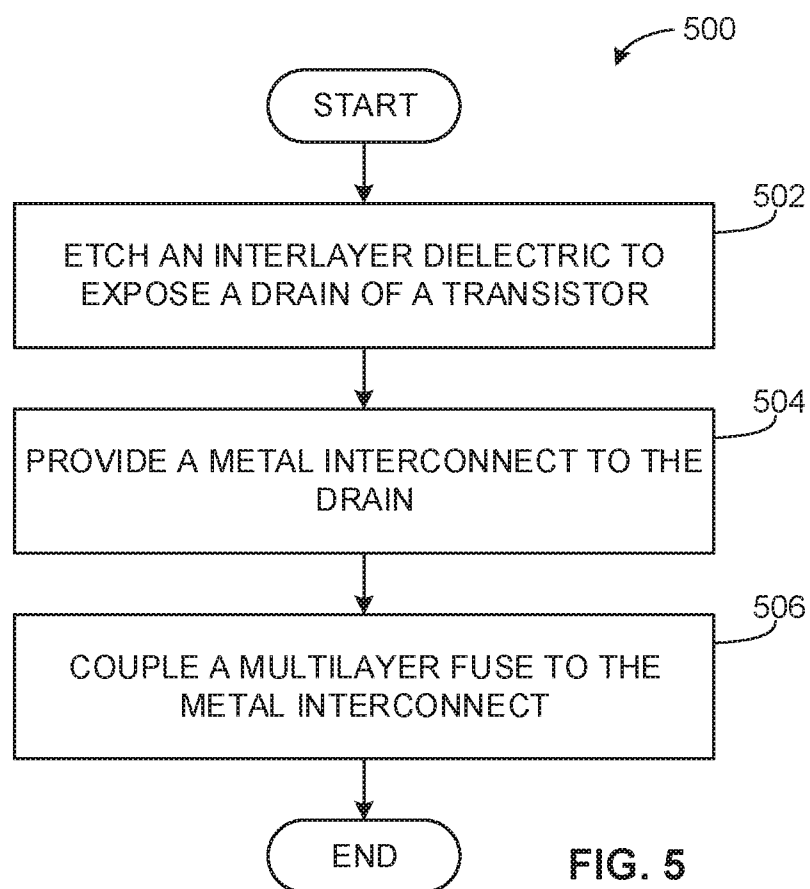


FIG. 1
(PRIOR ART)



**FIG. 3**





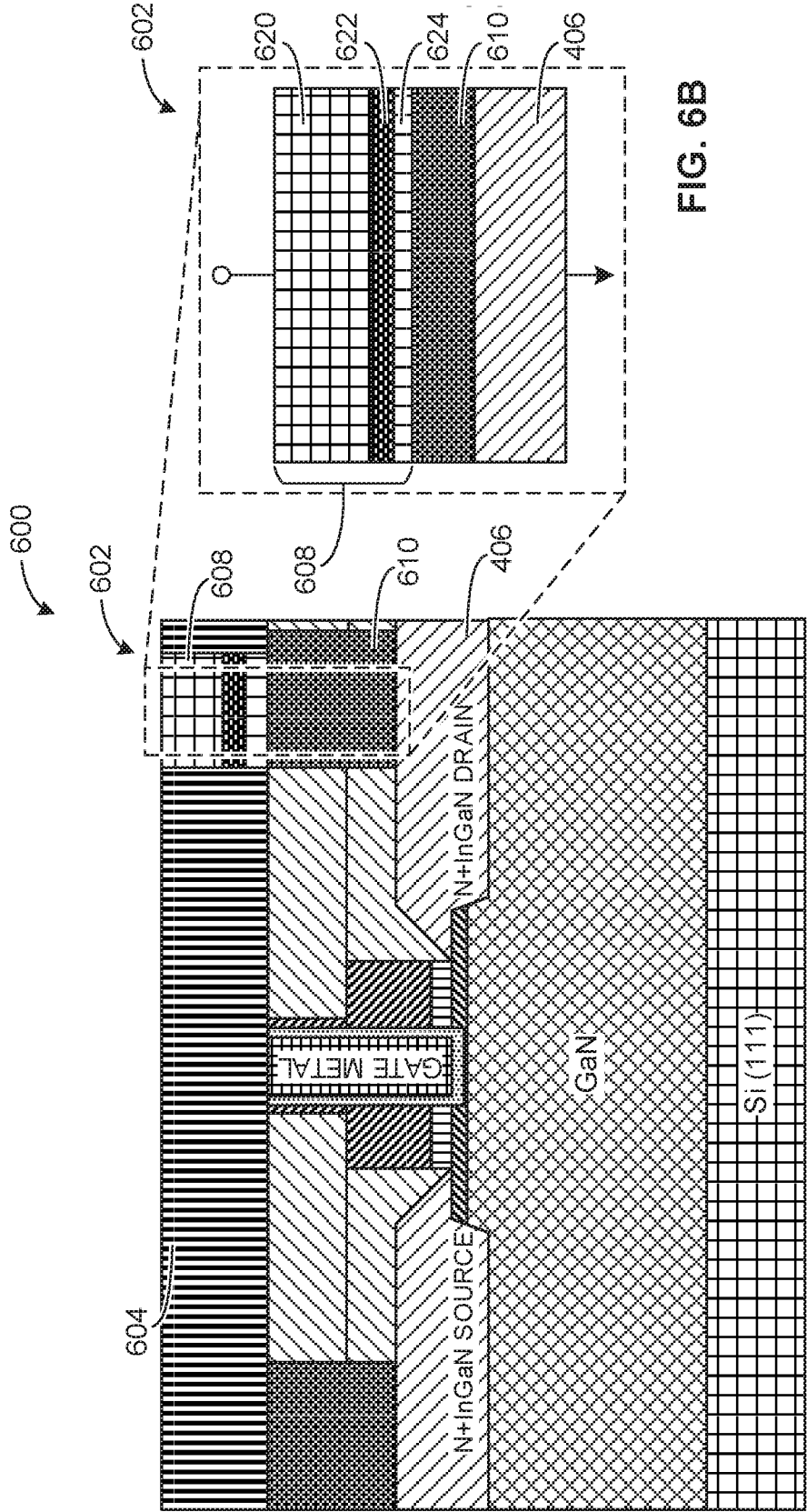


FIG. 6A

FIG. 6B

A. CLASSIFICATION OF SUBJECT MATTER**H01L 27/112(2006.01)i, H01L 21/768(2006.01)i, H01L 23/525(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/112; H01L 27/06; H01L 21/302; H01L 27/13; H01L 21/20; H01L 29/772; H01L 21/338; H01L 21/02; H01L 29/06; H01L 21/768; H01L 23/525

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: fuse, transistor, metal, interconnect, dielectric, layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012-0273798 A1 (ALPTEKIN et al.) 01 November 2012 See paragraphs [0028]–[0052], claim 12 and figures 1L–1Q.	1–36
A	US 2013-0126979 A1 (CHERN et al.) 23 May 2013 See paragraphs [0016]–[0035] and figure 2M.	1–36
A	US 2015-0001638 A1 (INFINEON TECHNOLOGIES AG) 01 January 2015 See claims 1–8 and figures 4a–7.	1–36
A	US 6372652 B1 (VERMA et al.) 16 April 2002 See claims 1–7 and figures 6–8.	1–36
A	US 8450163 B2 (BEYER et al.) 28 May 2013 See claims 1–5 and figures 1a–1l.	1–36



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 December 2017 (27.12.2017)

Date of mailing of the international search report

27 December 2017 (27.12.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

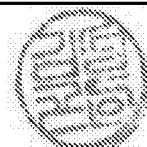
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

KIM, Sung Gon

Telephone No. +82-42-481-8746



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/025458

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0273798 A1	01/11/2012	US 2013-0119483 A1 US 8415250 B2 US 8643122 B2	16/05/2013 09/04/2013 04/02/2014
US 2013-0126979 A1	23/05/2013	CN 103137553 A US 2017-062335 A1 US 9524934 B2	05/06/2013 02/03/2017 20/12/2016
US 2015-0001638 A1	01/01/2015	US 2010-0193867 A1 US 8865592 B2 US 9437593 B2	05/08/2010 21/10/2014 06/09/2016
US 6372652 B1	16/04/2002	EP 1122785 A1 SG 90735 A1	08/08/2001 20/08/2002
US 8450163 B2	28/05/2013	DE 102010028465 A1 DE 102010028465 B4 US 2011-0266633 A1	03/11/2011 19/09/2013 03/11/2011