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(71) **Applicants** *(for all designated States except US):* **MAGIC TECHNOLOGIES, INC.** [US/US]; 463 South Milpitas Blvd., Milpitas, CA 95035 (US). **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; IP Law Department, 1101 Kitchawan Road, Route 134, T.J. Watson Research Center, P.O. Box 218, Yorktown Heights, NY 10598 (US).

(72) **Inventors; and**

(75) **Inventors/ Applicants** *(for US only):* **YANG, Hsu, Kai** [US/US]; 2980 Amoroso Court, Pleasanton, CA 94566 (US). **NAKAMURA, Yutaka** [JP/JP]; Storch 201, Kashiwaya-cho 18, Shijodori-Aburackoji-nishiiru, Shimogyo-ku, Syoto-shi, Kyoto-fu, 600-8498 (JP). **DEBROSSE, John** [US/US]; 212 Buckingham Drive, Colchester, VT 05446 (US).

(74) **Agent: ACKERMAN, Stephen, B.;** Saile Ackerman LLC, 28 Davis Avenue, Poughkeepsie, NY 12603 (US).

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[Continued on next page]

(54) Title: SHARED BIT LINE SMT MRAM ARRAY WITH SHUNTING TRANSISTORS BETWEEN THE BIT LINES

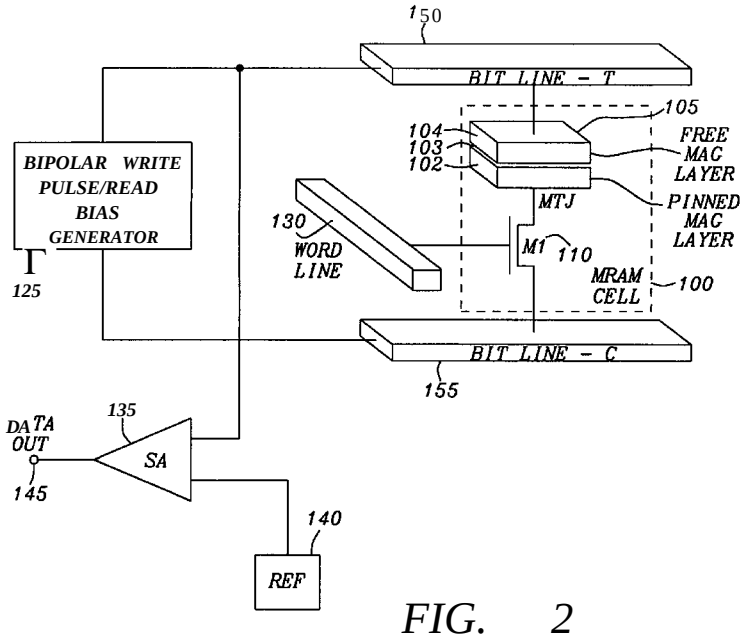

FIG. 2

(57) Abstract: An array of rows and columns of SMT MRAM cells has each of the columns associated with one of its adjacent columns. Each of the SMT MRAM cells of the column is connected to a true data bit line and each of the SMT MRAM cells of the associated pair of columns is connected to a shared complement data bit line. A shunting switch device is connected between each of the true data bit lines and the shared complement data bit line for selectively connecting one of the true data bit lines to the shared complement data bit line to effectively reduce the resistance of the complement data bit line and to eliminate program disturb effects in adjacent non-selected columns of the SMT MRAM cells.

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Shared Bit Line SMT MRAM Array with Shunting Transistors Between the Bit Lines

Background of the Invention

Field of the Invention

[0001] This invention relates generally to memory cells and array structures for memory cells. More particularly, this invention relates to magnetic random access memory (MRAM) cells and array structures for spin moment transfer (SMT) MRAM cells.

Description of Related Art

[0002] The term spin moment transfer MRAM refers to a magnetic tunnel junction (MTJ) random access memory (RAM). In this context, the term "spin" refers to the angular momentum of electrons passing through an MTJ that will alter the magnetic moment of a free layer of an MTJ device. Electrons possess both electric charge and angular momentum (or spin). it is known in the art that a current of spin-polarized electrons can change the magnetic orientation of a free ferromagnetic layer of an MTJ via an exchange of spin angular momentum.

[0003] "A Novel Nonvolatile Memory with Spin-torque Transfer Magnetization Switching: Spin-Ram", Hosomi, et al., IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest. Dec. 2005, pp.: 459- 462, provides a nonvolatile memory utilizing spin-torque transfer magnetization switching (STS), abbreviated Spin-RAM. The Spin-RAM is programmed by magnetization reversal through an interaction of a spin momentum-torque-transferred current and a magnetic moment of memory layers in magnetic tunnel junctions (MTJs), and therefore an external magnetic field is unnecessary as that for a conventional MRAM.

[0004] A spin-torque MTJ element has two ferromagnetic layers and a spacer layer between the ferromagnetic layers. One ferromagnetic layer is a pinned magnetic layer and the other ferromagnetic layer is a free magnetic layer. The spacer layer is a tunnel barrier layer. When a spin polarized electron flows through

the ferromagnetic layers, the spin direction rotates according to the directions of magnetic moment. The rotation of spin direction of the electrons in the ferromagnetic layers is the origin of a spin-torque to the magnetic moment. If the given torque is large enough, magnetization of ferromagnetic layer and thus the magnetic moment is reversed. The magnetization of the ferromagnetic layers transforms from parallel to anti-parallel alignment. This changes the MTJ element from a low resistance state to a high resistance state thus changing the logic state of the MTJ element from a first logic state (0) to a second logic state (1). A voltage source provides the programming voltage that generates the programming current that is reversed appropriately change the programming state of the MTJ element. Reading an SMT MRAM cell involves applying a voltage across the SMT MRAM cell and detecting the resistance (or current) difference.

[0005] As illustrated in Fig. 1, a spin moment transfer (SMT) MRAM cell 100 consists of an MTJ element 105 and a Metal Oxide Semiconductor (MOS) gating transistor 110. The MTJ element 105 is composed of a pinned ferromagnetic layer 102 and a free ferromagnetic layer 104, arid a tunnel barrier layer 103. The drain of the gating transistor 110 is connected through a nonmagnetic layer to the pinned ferromagnetic layer 102. The free ferromagnetic layer 104 is connected to a bit line 115 and the source of the gating transistor 110 is connected the source line 120. The bit line 115 and source select line 120 are connected to the bipolar write pulse/read bias generator 125. The bipolar write pulse/read bias generator 125 provides the necessary programming current to the MTJ element 105 through the bit line 115 and the source select line 120. The direction being determined by logic state being programmed to the MTJ element 105.

[0006] The gate of the gating transistor 110 is connected to a word line 130. The word line 130 transfers a word line select voltage to the gate of the gating transistor 110 to activate the gating transistor 110 for reading or writing the logic state of the MTJ element 105. A sense amplifier 135 has one input terminal connected to the bit line and a second input terminal connected to a voltage reference circuit. When the word line 130 has the word line select voltage activated to turn on the gating transistor 110, the bipolar write pulse/read bias generator 125 generates a bias current that passes through MTJ element 105. A voltage is

developed across the MTJ element **105** that is sensed by the sense amplifier **135** and compared with the reference voltage generator to determine the logic state written to the MTJ element **105.** This logic state is transferred to the output terminal of the sense amplifier **135** as to the data output signal **145.**

[0007] Arrays of spin moment transfer (SMT) MRAM cell **100** are arranged in rows and columns. Each row of the spin-transfer based magneto tunnel junction memory devices may have their source line **120** commonly connected to a source line selection circuit or tied to a ground reference point. In other arrangements of an array of SMT MRAM cells **100,** as shown in U. S. Patent Application 200/60018057 (Huai), the SMT MRAM cells **100** are organized into an array having two bit lines. The two bit lines are structures such that the current flowing perpendicularly through the MTJ **105** is controlled by the difference of the bias voltages of the two bit lines for each spin moment transfer (SMT) MRAM cell **100.** Two reading/writing column selection circuits are provided to control the voltages on the bit lines.

Summary of the Invention

[0008] An object of this invention is to provide an array of SMT MRAM cells with paired columns of the SMT MRAM cells having shared bit lines with means for lowering the resistance of the shared bit lines.

[0009] Another object of this invention is inhibiting program disturbance of a non-selected column of a pair of columns of the SMT MRAM cells.

[0010] To accomplish at least one of these objects, an array of SMT MRAM cells is arranged in rows and columns. An array of SMT MRAM cells is arranged in rows and columns. Each of the columns of SMT MRAM cells is associated with one of its adjacent columns of SMT MRAM cells. Each column is connected to a true data bit line and each associated pair of columns of SMT MRAM cells is connected to a shared complement data bit line. A shunting switch device is connected between each of the true data bit lines and the shared complement data bit line for selectively connecting one of the true data bit lines to the shared complement data bit line to effectively reduce the resistance of the complement data bit line and to

eliminate program disturb effects in adjacent non-selected columns of the SMT MRAM cells. An activation terminal of each of the shunting switch device is connected to a column address decoder such that the shunting switch device is activated to connect the true data bit line associated with the non-selected column in parallel with the complement data bit line. The shared complement data bit line may be wider than the true data bit line to further lower the resistance of the shared complement data bit line. In some embodiments the shared complement data bit line may be twice the dimension of the true data bit line.

[001 1] In other embodiments, a bit line structure for connecting columns of SMT MRAM cells within an array of SMT MRAM cells has a true data bit line connected to an MTJ device of each SMT MRAM cell of each column of the SMT MRAM cells. A complement data bit line is connected to a source of a gating transistor of each SMT MRAM cell of the each column of the SMT MRAM cells. The bit line structure has a shunting switch transistor connected between the true data bit line and the complement data bit line of the associated pairs of columns of the SMT MRAM cells. The shunting switch transistors have an activation terminal that, when activated, connects the true data bit line of an unselected column of the SMT MRAM cells in parallel with the shared complement data bit line to effectively reduce program disturb effects in the unselected column of SMT MRAM cells. The shared complement data bit line may be wider than the true data bit liine to further lower the resistance of the shared complement data bit line. The shared complement data bit line may be twice the dimension of the true data bit line.

[0012] In other embodiments, a method for reducing resistance of a shared bit line and reducing program disturb effects of unselected columns of SMT MRAM cells in an array of SMT MRAM cells begins by providing an array of SMT MRAM cells where columns of the SMT MRAM cells are mutually connected to a shared complement data bit line through the source of a gating transistor of each of the SMT MRAM cells of the pair of columns of SMT MRAM cells. The shared complement data bit line may be wider than the true data bit line to further lower the resistance of the shared complement data bit line. In some embodiments the shared complement data bit line may be twice the dimension of the true data bit line.

[001 3] Each of the SMT MRAM cells of each column of the SMT MRAM cells is connected to a true data bit line through an MTJ device within the SMT MRAM cells. A source of a gating transistor of the pair of adjacent columns of SMT MRAM cells is connected to a complement data bit line. A shunting switch transistor is connected between the true data bit line and the complement data bit line of the associated pairs of columns of the SMT MRAM cells. During a program operation, an address is decoded to select a row and columns of the array of SMT MRAM cells. An activation terminal of each of the shunting switch transistor of each unselected column of the array of SMT MRAM cells is initiated to turn on the shunting switch transistors to connect the true data bit line of the unselected column of the SMT MRAM cells in parallel with the shared complement data bit line to effectively reduce program disturb effects in the unselected column of SMT MRAM cells. The programming drive current is then activated to program the selected SMT MRAM cells of the selected rows and columns.

[0014] Further, in other embodiments, an array of SMT MRAM cells is arranged in rows and columns. Each of the columns of SMT MRAM cells is associated with one of its adjacent columns of SMT MRAM cells. Each column is connected to a true data bit line and to a complement data bit line.

[0015] A shunting switch device is connected between the true data bit line and the complement data bit line of the connected columns of SMT MRAM cells for selectively connecting one of the true data bit lines to the complement data bit line to effectively reduce the resistance of the complement data bit line and to eliminate program disturb effects in adjacent non-selected columns of the SMT MRAM cells. The complement data bit lines are connected such that they are shared during a program operation to further reduce the resistance of the complement data bit lines. An activation terminal of each of the shunting switch devices is connected to a column address decoder such that the shunting switch device is activated to connect the true data bit line associated with the non-selected column in parallel with the complement data bit line.

[0016] Still further, in other embodiments, an array of SMT MRAM cells is arranged in rows and columns. Each of the columns of SMT MRAM cells is

associated with one of its adjacent columns of SMT MRAM cells. Each column is connected to a true data bit line and to a complement data bit line. At least one true data bit line shunting switch device is connected between the true data bit line and the complement data bit line of the connected columns of SMT MRAM cells for selectively connecting one of the true data bit lines to the complement data bit line. The complement data bit lines of the associated adjacent columns have at least one complement data bit line shunting switch device connected between the adjacent complement data bit lines such that they are shared during a program operation to further reduce the resistance of the complement data bit lines. An activation terminal of each of the shunting switch devices is connected to a column address decoder such that the shunting switch device is activated to connect the two complement data bit lines and the true data bit line associated with the non-selected column in parallel to effectively reduce the resistance of the complement data bit line and to eliminate program disturb effects in adjacent non-selected columns of the SMT MRAM cells.

Brief Description of the Drawings

[0017] Fig. 1 is a functional diagram of a SMT MRAM memory cell and its peripheral circuitry of the prior art.

[0018] Fig. 2 is a functional diagram of a SMT MRAM memory cell and its peripheral circuitry.

[0019] Fig. 3 is a schematic diagram of an embodiment of an array of SMT MRAM memory cells.

[0020] Fig. 4 is block diagram of an embodiment of an SMT MRAM memory device.

[0021] Fig. 5 is a flow diagram for a method to effectively reduce program disturb effects in the unselected column of SMT MRAM cells.

[0022] Fig. 6 is a schematic diagram of another embodiment of an array of SMT MRAM memory cells having shunting switch transistors.

[0023] Fig. 7 is a schematic diagram of still another embodiment of an array of SMT MRAM memory cells having shunting switch transistors.

Detailed Description of the Invention

[0024] The embodiments of SMT MRAM cell arrays have columns of SMT MRAM memory cells with pairs of bit lines, for the sake of convention, have one of the bit line referred to as a true data bit line and the other bit line referred to as the complement data bit line. In the prior art, as described in Huai, Fig. 9, each column of cells has a pair of bit lines. Such architecture has too many bit lines and the bit line connecting to the source sides of gating transistor **110** of Fig. 2 is highly resistive. High bit line resistance puts constraint on how many cells that may be grouped in a basic array with decoders and drivers. In embodiments of this invention, adjacent pairs of columns are connected to share a bit the complement data bit lines. The complement data bit lines are effectively merged to form the complement data bit lines. Therefore, in some embodiments, the complement data bit lines are formed to be much wider and therefore less resistive. This permits a larger and more efficient array in terms of area. However, in the shared complement data bit line structure, the adjacent SMT MRAM memory cell of an SMT MRAM memory cell being programmed will be disturbed during programming. To effectively reduce program disturb effects in the unselected column of SMT MRAM cells, shunting switch transistors are added between each of the true data bit lines and the shared complement data bit lines.

[0025] Referring to Fig. 2, the structure of the SMT MRAM memory cell is essentially identical to that of Fig. 1, except the source of the gating transistor **110** of the SMT MRAM memory cell **100** is connected to the shared complement data bit line **155.** In the embodiments, the complement data bit line **155** is structured to be in parallel with the true data bit line **150.** The true data bit line **150** is connected to the free ferromagnetic layer **104** of the MTJ element **105.** The true data bit line **150** and the complement data bit line **155** are connected to THE bipolar write pulse/read bias

generator **125.** The complement data bit line **155** is shared with an identical SMT MRAM memory cell **100** in an adjacent column of SMT MRAM memory cells **100.**

[0026] The complement data bit line **155** that is connected to the source of the gating transistor **110,** is the first metal layer line in the physical construction of the SMT MRAM memory cell **100.** The true data bit line **150** is the last, or the top most metal line in the physical cell stack. The first metal bit line of the complement data bit line **155** has to share the space with vias connecting the drain side of the gating transistor **110** to the bottom plate **102** of MTJ element **105** thus forcing the first metal bit line of the complement data bit line **155** usually to be thinner. The first metal bit line of the complement data bit line **155** being narrower and thinner are therefore much more resistive than the top true data bit line **150.** By sharing two adjacent complement data bit lines **155,** the width of shared line is effectively wider by three times - two lines plus the spacing between the two adjacent complement data bit lines **155.** The disadvantage of doing so is that the SMT MRAM memory cell **100** adjacent to the cell being programmed will see a disturb condition because they share the same selected word line **130.** The shunting transistor (or transistors if we put more than one between the bit lines true and complement) will help to reduce this disturb condition. The further reduction in resistance of the two adjacent complement data bit lines **155** comes from the neighboring true bit line **150** is also in parallel with the complement bit line **155.** But this requires more than one shunting transistor between the true and complement bit lines.

[0027] Fig. 3 illustrates an embodiment of an array **200** of the SMT MRAM memory cells **100.** The SMT MRAM memory cells **100** are arranged into rows and columns to form the array **200.** The MTJ element of each SMT MRAM memory cells **100** is connected to one of the true data bit lines **250a, 259b, ..., 250n.**

[0028] Adjacent columns of SMT MRAM memory cells **100** are associated with each other. A shunting switch transistor **205a, ..., 205n** and **206a, ..., 206n** connects each true data bit line **250a, 250b, ..., 250n-1 , 250n** to its associated shared complement data bit line **255a, ..., 255n.** A first source/drain of each of the shunting switch transistor **205a, ..., 205n** and **206a, ..., 206n** is connected to the true data bit line **250a, 250b, ... 250n-1, 250n.** The second source/drain of each of

the shunting switch transistor **205a, ..., 205n** and **206a, ..., 206n** is connected to one shared complement data bit line **255a, ..., 255n.** The gate of each of the shunting switch transistors **205a, ..., 205n** is connected to the in-phase column address select bit **Ay 210** and the gate of each of the shunting switch transistor **206a, ..., 206n** is connected to the out-of-phase column address select bit $\overline{\text{Ay}}$ **212.** The in-phase column address select bit **Ay** and the out-of-phase column address select bit $\overline{\text{Ay}}$ **212** originate from a column or bit line decoder selector that decodes an address to select the columns of the array **200** for programming, reading, and erasing.

[0029] Each of the true data bit lines **250a, 250b, ..., 250n-1, 250n** is connected to a first source/drain of a true data bit line switch transistor **215a, 215b, ..., 215n-1, 215n.** The second source/drain of each of the true data bit line switch transistors **215a, 215b, ..., 215n-1, 215n** is connected to a true program data voltage distribution line **247.** Each shared complement data bit line **255a, ..., 255n** is connected to a first source/drain of each of the complement data bit line switch transistors **220a, ..., 220n.** The second source/drain of each of the complement data bit line switch transistors **220a, ..., 220n** is connected to a complement data program voltage distribution line **245.** The gates of the true data bit line switch transistors **215a, 215b, ..., 215n-1, 215n** are connected to the bit line decode select circuit **227.** The decode select circuit **225** receives an address, decodes the address and activates the appropriate gate of the true data bit line switch transistors **215a, 215b, ..., 215n-1, 215n** to activate the selected column or columns for programming, erasing, and reading the selected SMT MRAM memory cells **100.**

[0030] Each of the complement data bit lines **255a, 255b, ..., 255n-1, 255n** is connected to a first source/drain of a complement data bit line switch transistor **220a, 220b, ..., 220n-1, 220n.** The second source/drain of each of the complement data bit line switch transistors **220a, 220b, ..., 220n-1, 220n** is connected to a program voltage distribution line **245.** Each shared complement data bit line **255a, ..., 255n** is connected to a first source/drain of each of the complement data bit line switch transistors **220a, ..., 220n.** The second source/drain of each of the complement data bit line switch transistors **220a, ..., 220n** is connected to a program voltage distribution line **245.** The gates of the complement data bit line switch transistors

220a, 220b, ..., 220n-1 , 220n are connected to the bit line decode select circuit **225.** As above, the decode select circuit **225** receives an address, decodes the address and activates the appropriate gate of the complement data bit line switch transistors **220a, 220b, ..., 220n-1, 220n** to activate the selected column or columns for programming, erasing, and reading the selected SMT MRAM memory cells **100.**

[0031] During programming of selected SMT MRAM memory cells **100,** the shunting switch transistors **205a, ..., 205n** are activated to effectively place unselected true data bit line **250a, 250b, ..., 250n-1, 250n** in parallel with the shared complement data bit line **255a, ..., 255n** for each paired columns of the SMT MRAM memory cells **100.** By placing the true data bit line **250a, 250b, ..., 250n-1 , 250n** in parallel with the shared complement data bit line **255a, ..., 255n,** the resistance of the shared complement data bit line **255a, ..., 255n** is effectively decreased and prevents disturb program currents from passing through the unselected SMT MRAM cells **100.**

[0032] Fig. **4** is block diagram of an embodiment of an SMT MRAM memory device showing a shared bit line structure with shunting switch transistors between the true data bit lines and the shared complement data bit lines. The SMT MRAM memory device has an array of SMT MRAM memory cells **100** that is formed of multiple sub-arrays **200** of SMT MRAM memory cells **100.** The SMT MRAM memory cells **100** are formed in rows and columns with the structure as described in Fig. 2. With each row of the SMT MRAM memory cells **100** are connected to one of the word lines **315a, ... 315m, 316a, ..., 316m.** Each column of the SMT MRAM memory cells **100** is connected to one of the true data bit lines **320a, 320b, ..., 320n-1, 320n, 321a, 321b, ..., 321 n-1, 321 n,** and **322a, 322b, ..., 322n-1 , 322n.** Adjacent columns are paired and connected to one of the shared complement data bit line **325a, ... 325m, 326a, ..., 326m,** and **327a, ... 327m.** The true data bit lines **320a, 320b, ..., 320n-1, 320n, 321a, 321b, ..., 321n-1 , 321n,** and **322a, 322b, ..., 322n-1, 322n** are connected to their associated shared complement data bit line **325a, ..., 325m, 326a, ..., 326m,** and **327a, ..., 327m** through their respective shunting switch transistors **205** and **206** to selectively connected the true data bit lines **320a, 320b, ... 320n-1 , 320n, 321a, 321b, ... 321n-1, 321n,** and **322a, 322b, ..., 322n-1, 322n** of the unselected column of SMT MRAM memory cells **100** to the associated shared

complement data bit line **325a, ..., 325m, 326a, ..., 326m,** and **327a, ..., 327m** as described above.

[0033] The true data bit lines **320a, 320b, ..., 320n-1 , 320n, 321 a , 321 b, ..., 321 n-1, 321 n ,** and **322a, 322b, ..., 322n-1 , 322n** are connected to the bit line decode selector circuit **305a.** The shared complement data bit line **325a, ..., 325m, 326a, ..., 326m,** and **327a, ..., 327m** are connected to the bit line decode selector circuit **305b** The bit line decode selector circuits **305a** and **305b** are connected to the bit line decode circuit **355** The bit line decode circuit receives the external address lines **365** and the external control lines **360** and decodes the decoded address **370** and transmits the decoded address **370** to the bit line decode selector circuits **305a** and **305b** to select the desired columns of selected sub-arrays **200** of the SMT MRAM memory cells **100.**

[0034] The write/read generator **335** receives the clock timing signal **345** and the data input signal **350** and conditions and amplifies the data input signal **350** to form the true program data Dw **375** and the complement data program **376.** The true program data D_W **375** and the complement data program $\overline{D_W}$ **376** are transferred respectively through the bit line decode selector circuits **305a** and **305b** to the appropriate true data bit lines **320a, 320b, ..., 320n-1, 320 n , 321a, 321b, ..., 321 n-1 , 321n,** and **322a, 322b, ..., 322n-1, 322n** and the shared complement data bit lines **325a, ..., 325m, 326a, ..., 326m,** and **327a, ..., 327m.**

[0035] During a programming operation, the shunting switch transistors **205** and **206** of the unselected columns are activated to shunt the true data bit lines **320a, 320b, ..., 320n-1, 320n, 321a, 321b, ..., 321 n-1, 321 n ,** and **322a, 322b, ..., 322n-1, 322n** of the unselected columns to shared complement data bit lines **325a, ..., 325m, 326a, ... 326m,** and **327a, ..., 327m** to prevent disturb program currents from passing through the unselected SMT MRAM cells **100** and to further decrease the effective resistance of the complement data bit lines **325a, ..., 325m, 326a, ..., 326m,** and **327a, ..., 327m.**

[0036] During a read operation, a read current is passed from the bit line decode selector **305a** through the selected true data bit lines **320a, 320b, ..., 320n-**

1, 320n, 321a, 321b, ..., 321 n-1 , 321 n, and **322a, 322b, ..., 322n-1, 322n** to the MTJ of the SMT MRAM memory cells **100** to the shared complement data bit line **325a, ..., 325m, 326a, ..., 326m,** and **327a, ..., 327m** to the bit line decode selector **305b.** The sense amplifiers are connected to the through the bit line decode selector **305a** to sense the voltage developed across the MTJ of the selected SMT MRAM memory cells **100** to detect the data stored in the selected SMT MRAM **100.** The data driver **385** receives the captured data conditions and amplifies the data to generate the output data **390** that is transferred to external circuitry.

[0037] Refer now to Fig. 5 for a discussion of an embodiment of a method to reduce the resistance of a complement data bit line during a programming operation and to effectively reduce program disturb effects in unselected columns of SMT MRAM memory cells. A provided array of SMT MRAM memory cells is structured and operates as described in Fig. 3 where columns of the SMT MRAM cells are mutually connected to a shared complement data bit line through the source of a gating transistor of each of the SMT MRAM cells of the pair of columns of SMT MRAM cells. Each of the SMT MRAM cells of each column of the SMT MRAM cells is connected to a true data bit line. Each of the true data bit lines is connected to an MTJ device within the SMT MRAM cells. A source of a gating transistor of the pair of adjacent columns of SMT MRAM cells is connected to a complement data bit line. A shunting switch transistor is connected between the true data bit line and the complement data bit line of the associated pairs of columns of the SMT MRAM cells. During a program operation, an address is decoded (Box **400)** to select a row (Box **405)** and columns (Box **410)** of the array of SMT MRAM cells. A gating terminal of each of the shunting switch transistor of each unselected column of the array of SMT MRAM cells is activated (Box **415)** to turn on the shunting switch transistors to connect the true data bit line of the unselected columns of the SMT MRAM cells in parallel with the shared complement data bit line to effectively reduce program disturb effects in the unselected column of SMT MRAM cells. The programming drive current is then activated (Box **420)** to program the selected SMT MRAM cells of the selected rows and columns.

[0038] Fig. 6 illustrates an alternate embodiment of an array **200** of the SMT MRAM memory cells **100.** The SMT MRAM memory cells **100** are arranged into

rows and columns to form the array **200** as described above in Fig. 3. The MTJ element of each SMT MRAM memory cells **100** is connected to one of the true data bit lines **250a, 259b, ..., 250n** and to one of the complement data bit line **500a, ..., 500n** and **501a, ..., 501 n.**

[0039] Adjacent columns of SMT MRAM memory cells **100** are associated with each other. A shunting switch transistor **505a, ... 505n** and **506a, ..., 506n** connects each true data bit line **250a, 250b, ..., 250n-1 , 250n** to its associated complement data bit line **500a, ..., 500n** and **501a, ..., 501 n.** A first source/drain of each of the shunting switch transistors **505a, ..., 505n** and **506a, ..., 506n** is connected to the true data bit line **250a, 250b, ..., 250n-1 , 250n.** The second source/drain of each of the shunting switch transistors **505a, ..., 505n** and **506a, ..., 506n** is connected to one associated complement data bit line **500a, ..., 500n** and **501a, ..., 501 n.** The gate of each of the shunting switch transistors **505a, ..., 505n** is connected to the in-phase column address select bit **Ay 210** and the gate of each of the shunting switch transistor **506a, ..., 506n** is connected to the out-of-phase column address select bit $\overline{\text{Ay}}$ **212.** The in-phase column address select bit **Ay** and the out-of-phase column address select bit $\overline{\text{Ay}}$ **212** originate from a column or bit line decoder selector that decodes an address to select the columns of the array **200** for programming, reading, and erasing.

[0040] Each of the true data bit lines **250a, 250b, ..., 250n-1, 250n** is connected to a first source/drain of a true data bit line switch transistor **215a, 215b, ..., 215n-1, 215n.** The second source/drain of each of the true data bit line switch transistors **215a, 215b, ..., 215n-1, 215n** is connected to a true program data voltage distribution line **247.** Each shared complement data bit line **500a, ..., 500n** and **501a, ..., 501n** is connected to a first source/drain of each of the complement data bit line switch transistors **220a, ..., 215n.** The second source/drain of each of the complement data bit line switch transistors **220a, ... 215n** is connected to a complement data program voltage distribution line **245.** The gates of the true data bit line switch transistors **215a, 215b, ..., 215n-1 , 215n** are connected to the bit line decode select circuit **225.** The decode select circuit **225** receives an address, decodes the address and activates the appropriate gate of the true data bit line

switch transistors **215a, 215b, ..., 215n-1, 215n** to activate the selected column or columns for programming, erasing, and reading the selected SMT MRAM memory cells **100.**

[0041] Each of the complement data bit lines **500a, ..., 500n** is connected to a first source/drain of a complement data bit line switch transistor **520a, ..., 520n** and each of the complement data bit lines **501a, ... 501n** is connected to the first source/drain of a complement data bit line switch transistors **521a, ..., 521n.** The second source/drain of each of the complement data bit line switch transistors **520a, ..., 520n** and **521a, ..., 521n** is connected to a program voltage distribution line **245.** The gates of the complement data bit line switch transistors **520a, ..., 520n** and **521a, ..., 521n** are connected to the bit line decode select circuit **225.** As above, the decode select circuit **225** receives an address, decodes the address and activates the appropriate gate of the complement data bit line switch transistors **520a, ..., 520n** and **521a, ..., 521n** to activate the selected column or columns for programming, erasing, and reading the selected SMT MRAM memory cells **100.**

[0042] During programming of selected SMT MRAM memory cells **100,** the shunting switch transistors **505a, ..., 505n** and **506a, ..., 506n** are selectively activated to effectively place unselected true data bit lines **250a, 250b, ..., 250n-1, 250n** in parallel with their associated complement data bit line **500a, ..., 500n** and **501a, ..., 501n** for each of the columns of the SMT MRAM memory cells **100.** By placing the true data bit line **250a, 250b, ..., 250n-1, 250n** in parallel with the complement data bit line **500a, ..., 500n** and **501a, ..., 501n,** the resistance of the complement data bit line **500a, ..., 500n** and **501a, ..., 501n** is effectively decreased and prevents disturb program currents from passing through the unselected SMT MRAM cells **100.** Further during programming. the complement data bit line switch transistors **520a, ..., 520n** and **521a, ..., 521n** of the unselected columns are activated to effectively place the complement data bit line **500a, ..., 500n** and **501a, ..., 501n** of the selected column in parallel with the complement data bit line **500a, ..., 500n** and **501a, ..., 501n** of the associated adjacent unselected column of the SMT MRAM memory cells **100.** The placing the complement data bit lines **500a, ..., 500n** and **501a, ..., 501n** of the associated adjacent selected and unselected bit lines in parallel effectively reduces the resistance of the complement data bit line

500a, ..., 500n and **501a, ..., 501n** of the selected columns of SMT MRAM memory cells **100** and any magnetic field resulting in a program disturb of the unselected SMT MRAM memory cells **100** is mitigated.

[0043] The bit line decode selector circuit **225** must be structured to activate the complement data bit line switch transistors **520a, ..., 520n** and **521a, ..., 521 n** appropriately for the unselected complement data bit line **500a, ..., 500n** and **501a, ..., 501n** to connected selected and unselected complement data bit line **500a, ..., 500n** and **501a, ..., 501 n** in parallel. The bit line decode selector circuit **225** must further deactivate the true data bit line switch transistors **215a, 215b, ..., 215n-1, 215n** for the unselected true data bit lines **250a, 250b, ..., 250n-1 , 250n** to prevent the true program data voltage distribution line **247** from being applied to the unselected true data bit lines **250a, 250b, ..., 250n-1, 250n** and thus to the selected and unselected complement data bit lines **500a, ..., 500n** and **501a, ..., 501 n.**

[0044] Fig. 7 illustrates a generalized embodiment of an array **200** of the SMT MRAM memory cells **100.** The SMT MRAM memory cells **100** are arranged into rows and columns to form the array **200** as described above in Figs. 3 and 6. The MTJ element of each SMT MRAM memory cells **100** is connected to one of the true data bit lines **250a, 259b, ..., 250n** and to one of the complement data bit line **500a, ..., 500n** and **501a, ..., 501 n.**

[0045] Adjacent columns of SMT MRAM memory cells **100** are associated with each other. A shunting switch transistor **600a, ..., 600n, 601a, ..., 601n, 605a, ..., 605n** and **606a, ..., 606n** connects each true data bit line **250a, 250b, ..., 250n-1, 250n** to its associated complement data bit line **500a, ..., 500n** and **501a, ..., 501 n.** A first source/drain of each of the shunting switch transistors **600a, ..., 600n, 601a, ..., 601 n, 605a, ..., 605n** and **606a, ..., 606n** is connected to one of the true data bit lines **250a, 250b, ..., 250n-1, 250n.** The second source/drain of each of the shunting switch transistors **600a, ..., 600n, 601a, ..., 601 n, 605a, ..., 605n** and **606a, ..., 606n** is connected to one associated complement data bit line **500a, ..., 500n** and **501a, ..., 501 n.** The gate of each of the shunting switch transistors **600a, ..., 600n,** and **605a, ..., 605n** is connected to the in-phase column address select bit **Ay 620a** and **620b** and the gate of each of the shunting switch transistor **601a, ...,**

601n and **606a, ... 606n** is connected to the out-of-phase column address select bit $\overline{\text{Ay}}$ **621a** and **621b.** The in-phase column address select bit **Ay 620a** and **620b** and the out-of-phase column address select bit $\overline{\text{Ay}}$ **621a** and **621b** originate from a column or bit line decoder selector that decodes an address to select the columns of the array **200** for programming, reading, and erasing. In the generalized embodiment there may be an number of the shunting switch transistors **600a, ..., 600n, 601a, ..., 601n, 605a, ..., 605n** and **606a, ..., 606n** placed in parallel between the true data bit lines **250a, 250b, ..., 250n-1, 250n** and their associated complement data bit lines **500a, ..., 500n** and **501a, ..., 501n** with two of the shunting switch transistors **600a, ..., 600n, 601a, ..., 601n, 605a, ..., 605n** and **606a, ..., 606n** connected between each of the true data bit line **250a, 250b, ..., 250n-1, 250n** and their associated complement data bit line **500a, ..., 500n** and **501a, ..., 501n.**

[0046] Each of the complement data bit lines **500a, ... 500n** and **501a, ..., 501n** of the associated columns of SMT MRAM's **100** has a pair of complement bit line shunting transistors **615a, ..., 615n** and **616a, ..., 616n.** Again as described above, in the generalized embodiment, the number of complement bit line shunting transistors **615a, ..., 615n** and **616a, ..., 616n** may be any number to assist in reducing the resistance of the complement data bit line **500a, ..., 500n** and **501a, ..., 501n,** with the two of this illustration being exemplary. A first source/drain of the complement bit line shunting transistors **615a, ..., 615n** and **616a, ..., 616n** is connected to a first of the complement data bit lines **500a, ..., 500n** and **501a, ..., 501n** and a second source/drain of the complement data bit line **500a, ..., 500n** and **501a, ..., 501n** being connected to a second of the associated complement data bit lines **500a, ..., 500n** and **501a, ..., 501n.** The gates of the complement bit line shunting transistors **615a, ..., 615n** and **616a, ..., 616n** are connected to a program command signal to activate the connection of the associated complement data bit line **500a, ..., 500n** and **501a, ..., 501n** through the complement bit line shunting transistors **615a, ..., 615n** and **616a, ..., 616n** during a program operation and to disconnect the complement bit line shunting transistors **615a, ..., 615n** and **616a, ..., 616n** during read and erase operations.

[0047] As shown in Fig. 6, each of the true data bit lines **250a, 250b, ..., 250n-1, 250n** is connected to a first source/drain of a true data bit line switch transistor **215a, 215b, ..., 215n-1, 215n.** The second source/drain of each of the true data bit line switch transistors **215a, 215b, ..., 215n-1, 215n** is connected to a true program data voltage distribution line **247.** Each shared complement data bit line **500a, ..., 500n** and **501a, ..., 501n** is connected to a first source/drain of each of the complement data bit line switch transistors **220a, ..., 215n.** The second source/drain of each of the complement data bit line switch transistors **220a, ..., 215n** is connected to a complement data program voltage distribution line **245.** The gates of the true data bit line switch transistors **215a, 215b, ..., 215n-1, 215n** are connected to the bit line decode select circuit **225.** The decode select circuit **225** receives an address, decodes the address and activates the appropriate gate of the true data bit line switch transistors **215a, 215b, ..., 215n-1, 215n** to activate the selected column or columns for programming, erasing, and reading the selected SMT MRAM memory cells **100.**

[0048] Further, as shown in Fig. 6, each of the complement data bit lines **500a, ..., 500n** is connected to a first source/drain of a complement data bit line switch transistor **520a, ..., 520n** and each of the complement data bit lines **501a, ... 501n** is connected to the first source/drain of a complement data bit line switch transistors **521a, ..., 521n.** The second source/drain of each of the complement data bit line switch transistors **520a, ..., 520n** and **521a, ..., 521n** is connected to a program voltage distribution line **245.** The gates of the complement data bit line switch transistors **220a, 220b, ..., 220n-1, 220n** are connected to the bit line decode select circuit **225.** As above, the decode select circuit **225** receives an address, decodes the address and activates the appropriate gate of the complement data bit line switch transistors **2 520a, ..., 520n** and **521a, ..., 521n** to activate the selected column or columns for programming, erasing, and reading the selected SMT MRAM memory cells **100.**

[0049] During programming of selected SMT MRAM memory cells **100,** the in-phase column address select bit **Ay 620a** and **620b** and the out-of-phase column address select bit $\overline{\mathbf{Ay}}$ **621a** and **621b** are selectively activated to turn on the

selected shunting switch transistors **600a, ..., 600n, 601a, ..., 601n, 605a, ..., 605n** and **606a, ..., 606n** to effectively place unselected true data bit lines **250a, 250b, ..., 250n-1, 250n** in parallel with their associated complement data bit line **500a, ..., 500n** and **501a, ..., 501n** for each of the columns of the SMT MRAM memory cells **100.** The Program command signals **625a** and **625b** are activated to turn on the selected complement bit line shunting transistors **615a, ... 615n** and **616a, ..., 616n** place the complement data bit lines **500a, ..., 500n** and **501a, ..., 501n** of the associated column pairs of the SMT MRAM memory cells **100** in parallel to further reduce the resistance of the complement data bit line **500a, ..., 500n** and **501a, ..., 501n.**

[0050] By placing the true data bit line **250a, 250b, ..., 250n-1, 250n** in parallel with the complement data bit line **500a, ..., 500n** and **501a, ..., 501n,** the resistance of the complement data bit line **500a, ..., 500n** and **501a, ..., 501n** is effectively decreased and any magnetic field resulting in a program disturb of the unselected SMT MRAM memory cells **100** is mitigated.

[0051] The bit line decode selector circuit **225** must deactivate the true data bit line switch transistors **215a, 215b, ..., 215n-1, 215n** for the unselected true data bit lines **250a, 250b, ..., 250n-1, 250n** to prevent the true program data voltage distribution line **247** from being applied to the unselected true data bit lines **250a, 250b, ..., 250n-1, 250n** and thus to the selected and unselected complement data bit lines **500a, ..., 500n** and **501a, ..., 501n.**

[0052] The placing of the shunting switch transistors **600a, ..., 600n, 601a, ..., 601n, 605a, ... 605n** and **606a, ..., 606n** and the complement bit line shunting transistors **615a, ..., 615n** and **616a, ..., 616n** in the various locations through out the array **200** of SMT MRAM memory cells **100** of Figs. 3, 4, 6, and 7 as stated above decreases the resistance of the complement data bit lines **500a, ..., 500n** and **501a, ... 501n,** therefore a larger and more efficient array in terms of area is now formed.

[0053] While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled

in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

[0054] The invention claimed is:

1. An array of SMT MRAM cells comprising:

paired columns of the SMT MRAM cells;

a plurality of first type bit lines, wherein each of the first type bit lines are connected to a terminal of an MTJ device of each of the SMT MRAM cells on one column of the SMT MRAM cells;

a plurality of second type bit lines, wherein each of the second type bit lines is connected to a source terminal of a gating device of each of the SMT MRAM cells on one column; and

means for connecting the first type bit lines with the second type bit lines of the same column to inhibit program disturbance of an unselected column of the pair of columns of the SMT MRAM cells.

2. The array of SMT MRAM cells of claim 1 wherein each of the second type bit lines is connected to of the adjacent columns of SMT MRAM cells.

3. The array of SMT MRAM cells of claim 2 wherein the second type bit lines are constructed to have a width that is sufficiently wide to reduce a resistance of the second type bit line such that the array of SMT MRAM cells is larger and is more efficiently in terms of area.

4. The array of SMT MRAM cells of claim 3 wherein the width of the second type bit line is twice the width of the first type bit line.

5. The array of SMT MRAM cells of claim 1 wherein each of the columns of the SMT MRAM cells are connected to one adjacent second type bit lines of the plurality of the second type bit lines.

6. The array of SMT MRAM cells of claim 5 further comprising means for connecting the two adjacent second type bit lines in parallel to merge the two adjacent second type bit lines to appear much wider and therefore less resistive to permit a larger and more area efficient array of SMT MRAM cells.

7. The array of SMT MRAM cells of claim 1 wherein the first type bit line is a true data bit line and the second type bit line is a complement data bit line.

8. An SMT MRAM device comprising:

SMT MRAM memory cells arranged in an array of rows and columns such that each of the columns of SMT MRAM cells is associated with one of its adjacent columns of SMT MRAM cells.

a plurality of true data bit lines where each of the true data bit lines is connected to one adjacent column;

a plurality of complement data bit lines, wherein each of the plurality of complement data bit lines are connected with each SMT MRAM cell of a pair of columns of the SMT MRAM cells such that each of the plurality of complement data bit lines is shared with the pair of columns of the SMT MRAM cells; and

a plurality of shunting switch devices, wherein each of the shunting switch devices is connected between one of the true data bit lines and the shared complement data bit line for selectively connecting one of the true data bit lines to the shared complement data bit line to effectively reduce the resistance of the complement data bit line and to eliminate program disturb effects in adjacent non-selected columns of the SMT MRAM cells.

9. The SMT MRAM device of claim 8 further comprising a column address decoder in communication with an activation terminal of each of the shunting switch devices such that the shunting switch device is activated to connect the true data bit line associated with the non-selected column in parallel with the complement data bit line.

10. The SMT MRAM device of claim 8 wherein the shared complement data bit line is wider than the true data bit line to further lower the resistance of the shared complement data bit line.

11. The SMT MRAM device of claim 10 wherein the shared complement data bit line is twice the dimension of the true data bit line.

12. A bit line structure for connecting columns of SMT MRAM cells within an array of SMT MRAM cells arranged in rows and columns comprising

a true data bit line connected to an MTJ device of each SMT MRAM cell of a column of the SMT MRAM cells

a complement data bit line connected to a source of a gating transistor of each SMT MRAM cell of a pair of associated columns of the SMT MRAM cells.

at least one shunting switch transistor connected between the true data bit line and the complement data bit line of the associated pair of columns of the SMT MRAM cells such that the at least one shunting switch transistor has an activation terminal that, when activated, connects the true data bit line of an unselected column of the SMT MRAM cells in parallel with the shared complement data bit line to effectively reduce program disturb effects in the unselected column of SMT MRAM cells.

13. The bit line structure of claim 12 wherein the shared complement data bit line is wider than the true data bit line to further lower the resistance of the shared complement data bit line.

14. The bit line structure of claim 13 wherein the shared complement data bit line may be twice the dimension of the true data bit line.

15. A method for reducing resistance of a shared complement bit line and reducing program disturb effects of unselected columns of SMT MRAM cells in a programming operation in an array of SMT MRAM cells comprising;

providing an array of rows and columns of SMT MRAM cells wherein pairs of columns of the SMT MRAM cells are each mutually connected to one shared complement data bit line through the

source of a gating transistor of each of the SMT MRAM cells of the pair of columns of SMT MRAM cells and each of the SMT MRAM cells of each column of the SMT MRAM cells is connected to one true data bit line, and a shunting switch transistor is connected between the true data bit line and the complement data bit line of the associated pairs of columns of the SMT MRAM cells;

decoding an address to select one row and at least one column of the array of SMT MRAM cells;

initiating an activation terminal of each of the shunting switch transistor of each unselected column of the array of SMT MRAM cells to turn on the shunting switch transistors to connect the true data bit line of the unselected column of the SMT MRAM cells in parallel with the shared complement data bit line to effectively reduce program disturb effects in the unselected column of SMT MRAM cells.

activating a programming drive current to program the selected SMT MRAM cells of the selected rows and columns.

16. The method of claim 15 wherein each of the true data bit lines is connected to an MTJ device within the SMT MRAM cells and a source of a gating transistor of the pair of adjacent columns of SMT MRAM cells is connected to a complement data bit line.

17. The method of claim 15 wherein each of the columns of SMT MRAM cells is associated with one of its adjacent columns of SMT MRAM cells. Each column is connected to a true data bit line and to a complement data bit line.

18. An SMT MRAM memory device comprising:

array of rows and columns of SMT MRAM cells wherein Each of the columns of SMT MRAM cells is associated with one of its adjacent columns of SMT MRAM cells;

a plurality of true data bit lines, wherein each of the true data bit lines is connected to each of the SMT MRAM cells of one of the columns of SMT MRAM cells;

a plurality of complement data bit lines, wherein each complement data bit line is associated with one of the true data bit lines and connected each of the SMT MRAM cells connected to its associated true data bit line;

a plurality of true data bit line shunting switch devices, wherein at least one true data bit line shunting switch devices is connected between the true data bit line and the complement data bit line of the connected columns of SMT MRAM cells for selectively connecting one of the true data bit lines to its associated complement data bit line of a non-selected column in parallel to effectively to eliminate program disturb effects in adjacent non-selected columns of the SMT MRAM cells.

19. The SMT MRAM memory device of claim 18 further comprising a plurality of complement data bit line shunting switch devices connected between two complement data bit lines of adjacent columns of SMT MRAM cells to selectively connect the two complement data bit lines of the adjacent columns together in parallel to merge the two adjacent complement data bit lines to appear as single much wider complement data bit line that is less resistive to permit a larger and more area efficient array of SMT MRAM cells.

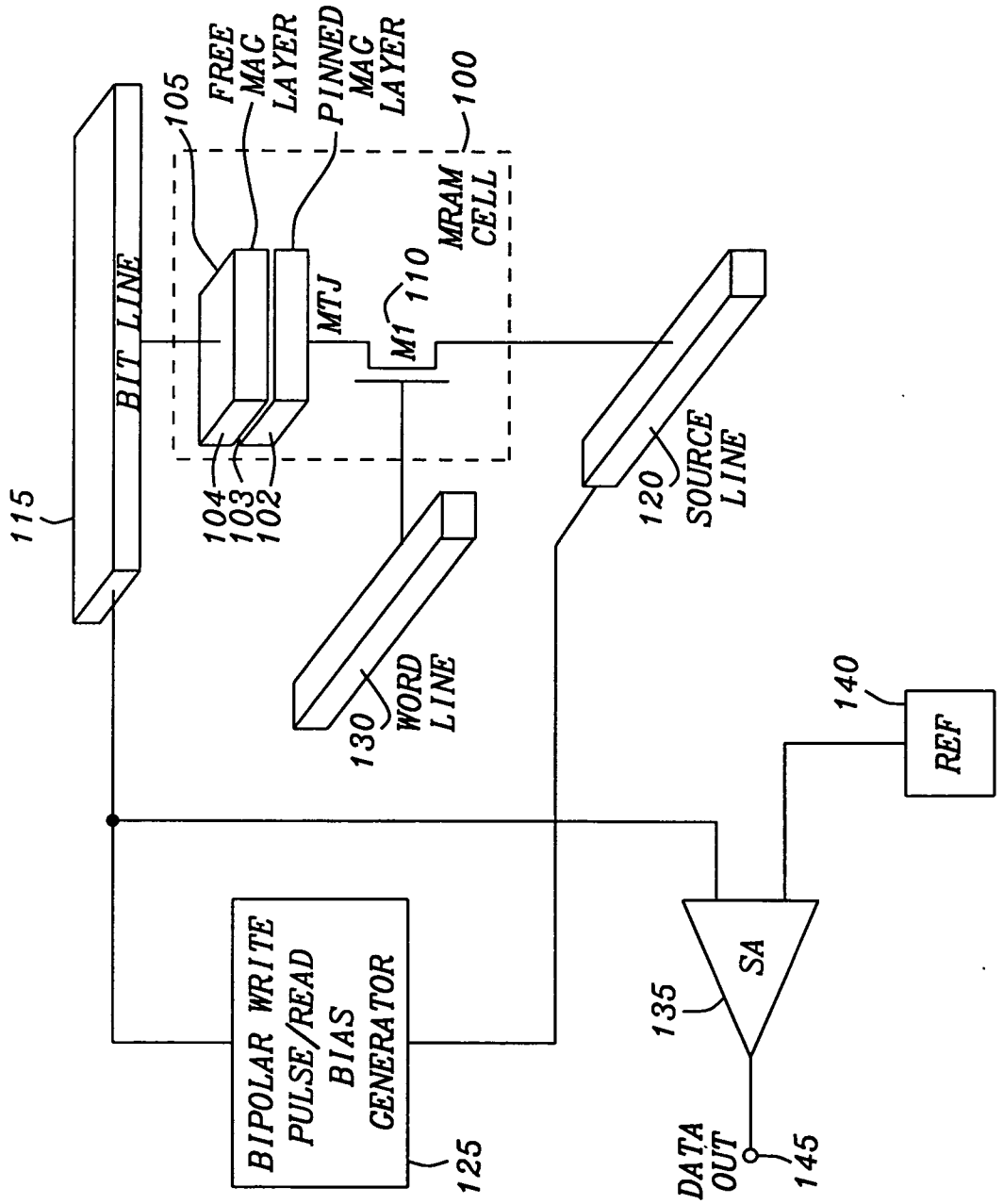
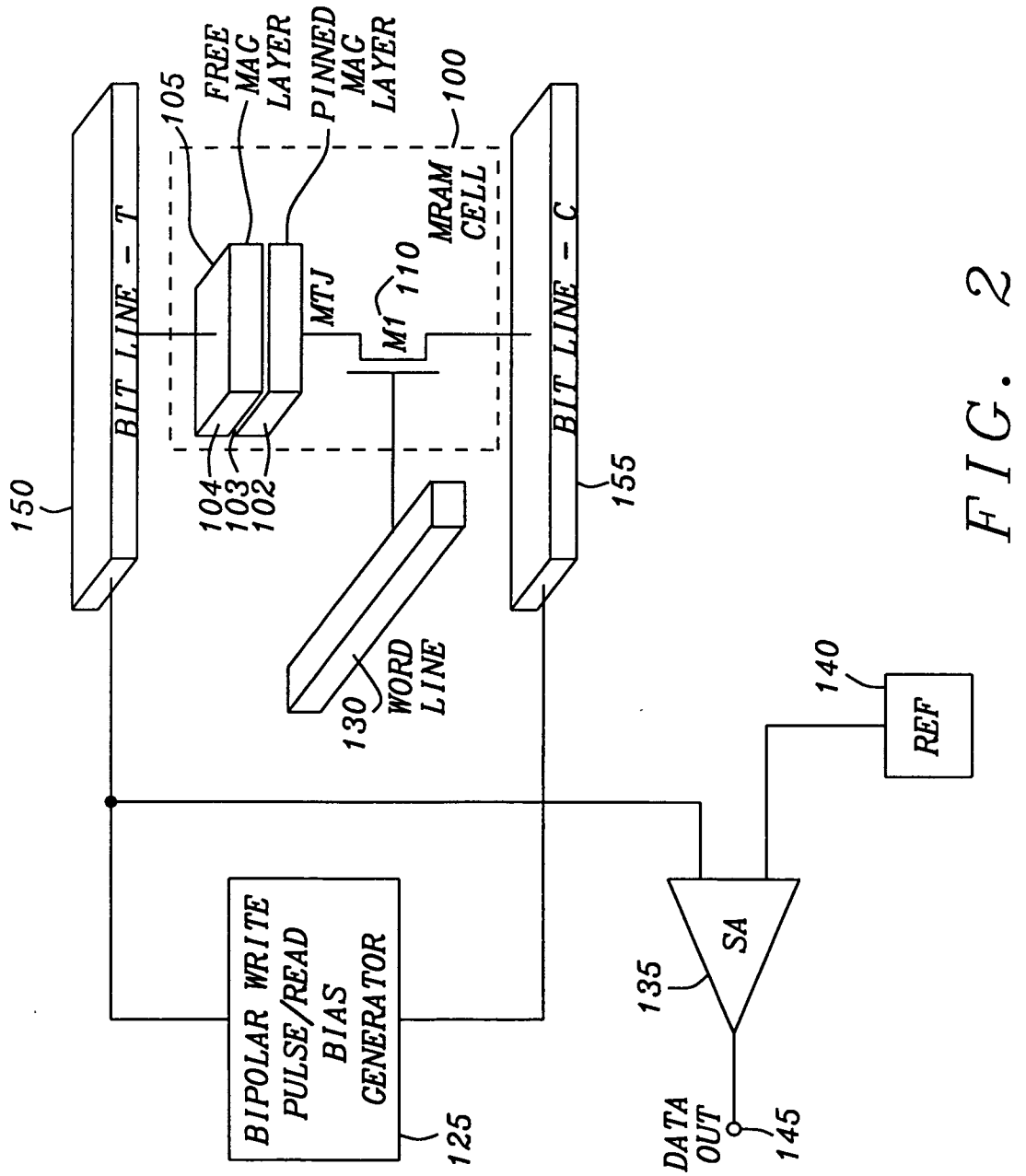


FIG. 1 – Prior Art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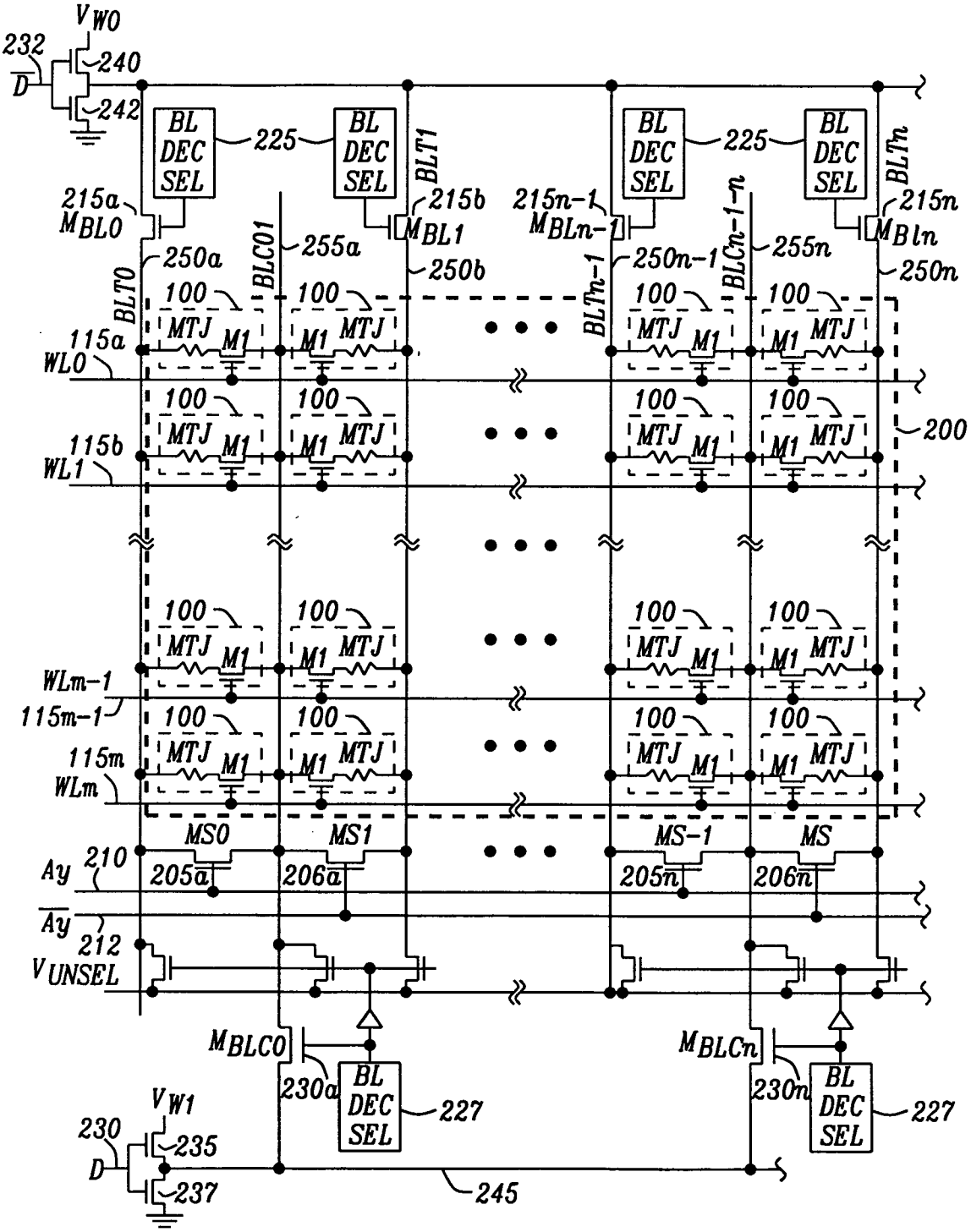
100
MRAM CELL
BIT LINE - T
BIT LINE - C
MTJ
M1
110
150
155
104
103
102
WORD LINE
130
140
REF
BIPOLAR WRITE PULSE/READ BIAS GENERATOR
125
SA
135
DATA OUT
145

FIG. 2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MBLn-1
215n
MBln
250a
BLT0
BLC01
255a
250b
BLTn-1
250n-1
BLCn-1-n
255n
250n
100
MTJ
M1
115a
WL0
115b
WL1
200
WLm-1
115m-1
115m
WLm
MS0
MS1
MS-1
MS
Ay
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205a
206a
205n
206n
Ay
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230n
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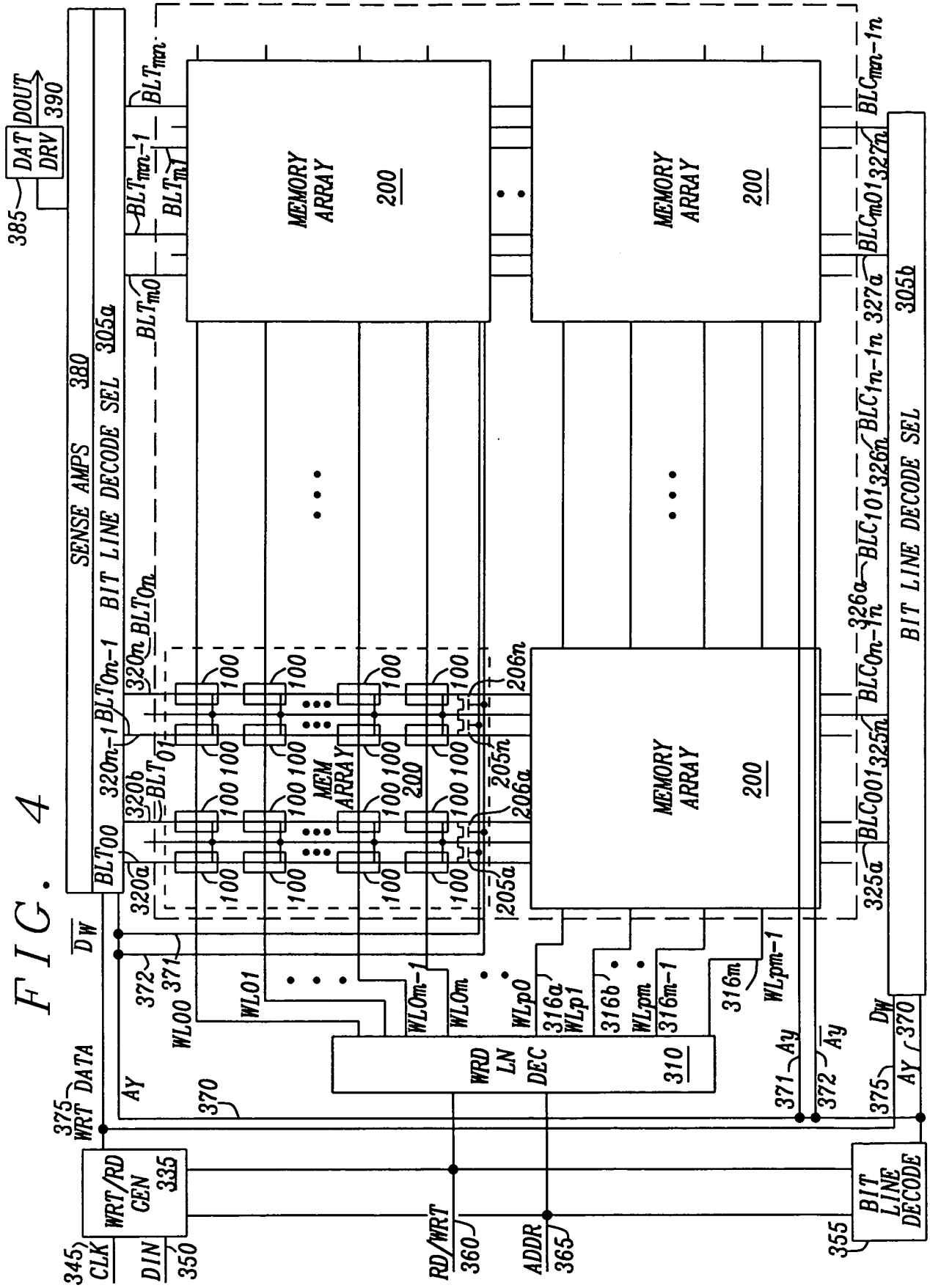
VW1
230
235
237
245

FIG. 3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MEM ARRAY
SENSE AMPS
380
BIT LINE DECODE SEL
305a
305b
DAT
DOUT
DRV
390
385
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375
WRT/RD GEN
335
CLK
345
DIN
350
RD/WRT
360
ADDR
365
BIT LINE DECODE
355
WRD LN DEC
310
WL00
WL01
WLm-1
WLm
WLp0
WLp1
WLpm
WLpm-1
316a
316b
316m-1
316m
370
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372
Ay
Dw
100
205a
205n
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320b
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320m
325a
325m
326a
326m
327a
327m

FIG. 4

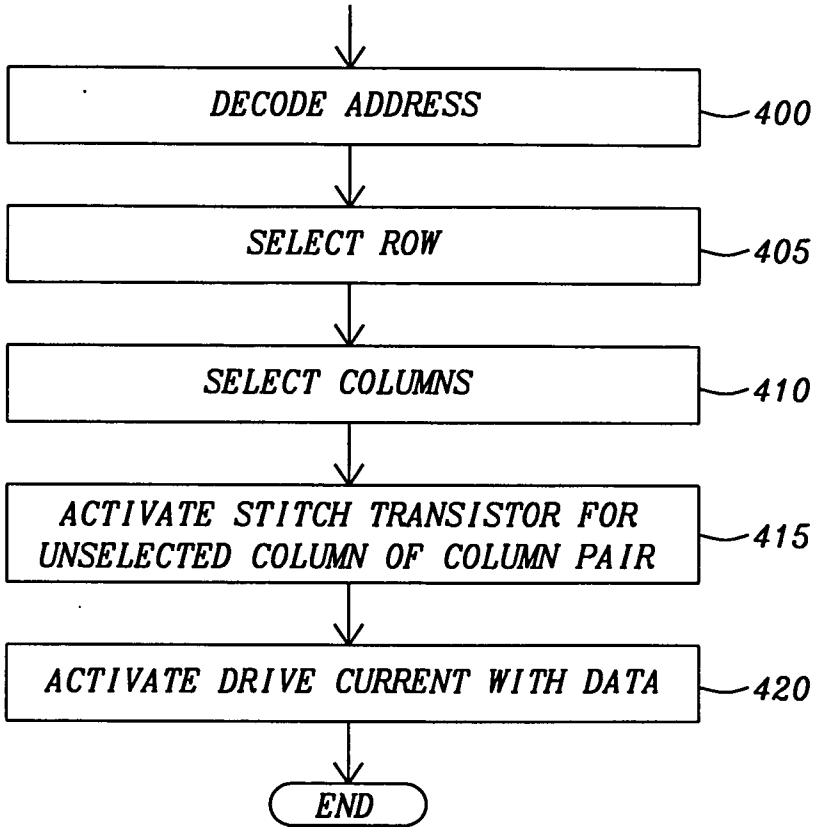
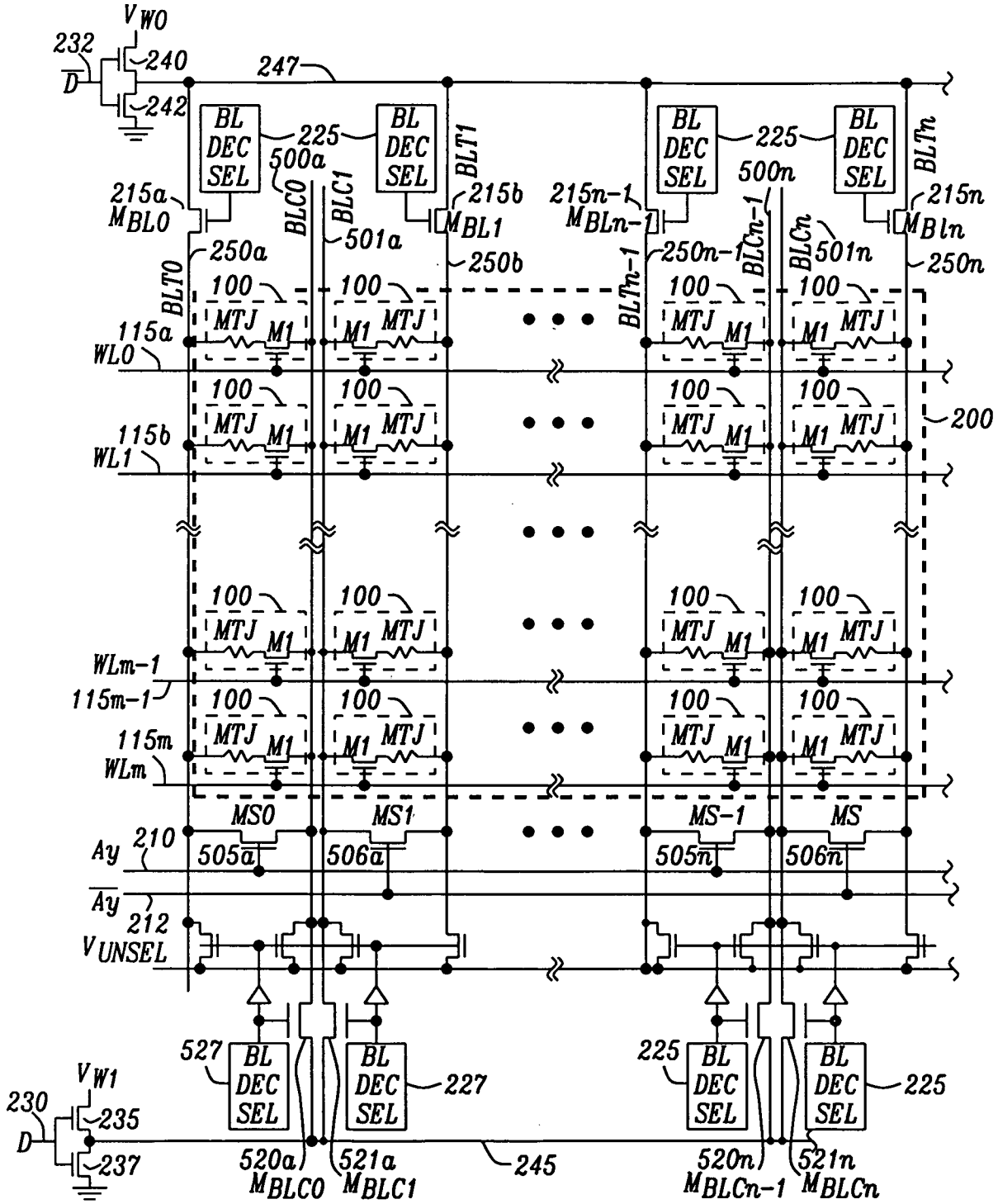

DECODE ADDRESS
400
SELECT ROW
405
SELECT COLUMNS
410
ACTIVATE STITCH TRANSISTOR FOR UNSELECTED COLUMN OF COLUMN PAIR
415
ACTIVATE DRIVE CURRENT WITH DATA
420
END

FIG. 5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D
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M1
115a
WL0
115b
WL1
200
WLm-1
115m-1
115m
WLm
MS0
MS1
210
Ay
505a
506a
212
VUNSEL
527
227
VW1
230
235
237
520a
MBLC0
521a
MBLC1
245
215n-1
MBLn-1
500n
BLCn-1
BLCn
BLTn-1
BLTn
215n
MBln
501n
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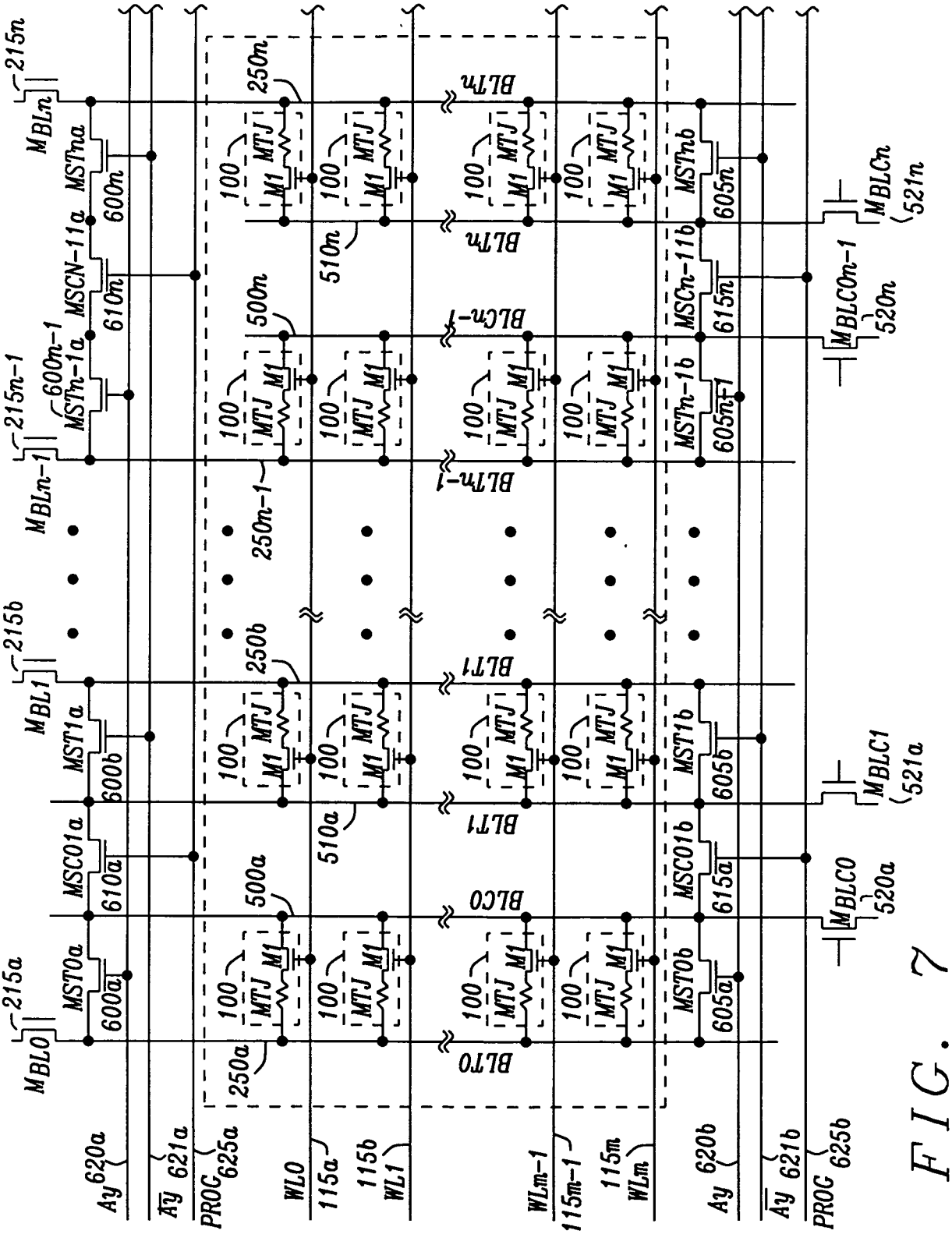
250n
MS-1
MS
505n
506n
520n
MBLCn-1
521n
MBLCn

FIG. 6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MBLCn
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MST1a
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MSTna
MST0b
MST1b
MSCn-11b
MSTn-1b
MSTnb
MSC01a
MSC01b
MTJ
M1
BLT0
BLT1
BLTn-1
BLTn
BLC0
BLCn-1
Ay
Ay
PROC
PROC
WL0
WL1
WLm-1
WLm

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 11/01157

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G11C 5/08 (2011.01)
USPC - 365/66
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - G11C 5/08 (2011.01)
USPC - 365/66

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 711/104; 365/1 ; 365/171 ; 365/232

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Databases: USPTO PubWEST(PGPB,USPT,EPAB,JPAB); Google Scholar
Search terms: shunt, resistance, line, width, disturbance, switch, pair, column, decoder, spin, memory, bit, share, gate, read, write, adjacent

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	**US 2009/0014703 A1 (INABA) 15 January 2009 (15.01.2009); fig 1-5, 9-10, 12-13, 16; para [0019]-[0027], [0035]-[0123]**	**1-19**
Y	**US 2006/0023490 A1 (BOEVE) 02 February 2006 (02.02.2006); fig 4-5, 11; para [0046]-[0051], [0070], [0072]-[0075]**	**1-19**
Y	**US 2010/0091557 A1 (HIDAKA) 15 April 2010 (15.04.2010); fig 2, 19; para [0041]-[0064], [0207]-[0245]**	**8-19**
A	**US 2008/0043514 A1 (UEDA) 21 February 2008 (21.02.2008); para [0038]-[0085]**	**1-19**

☐ Further documents are listed in the continuation of Box C.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 October **2011 (25.10.2011)**	15 NOV 2011
Name and mailing address of the ISA/US **Mail Stop PCT, Attn: ISA/US, Commissioner for Patents** **P.O. Box 1450, Alexandria, Virginia 22313-1450** Facsimile No. 571-273-3201	Authorized officer: **Lee W. Young** **PCT Helpdesk: 571-272-4300** **PCT OSP: 571-272-7774**