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(54) **Title**: CIRCUIT ARRANGEMENT AND MANUFACTURING METHOD THEREOF

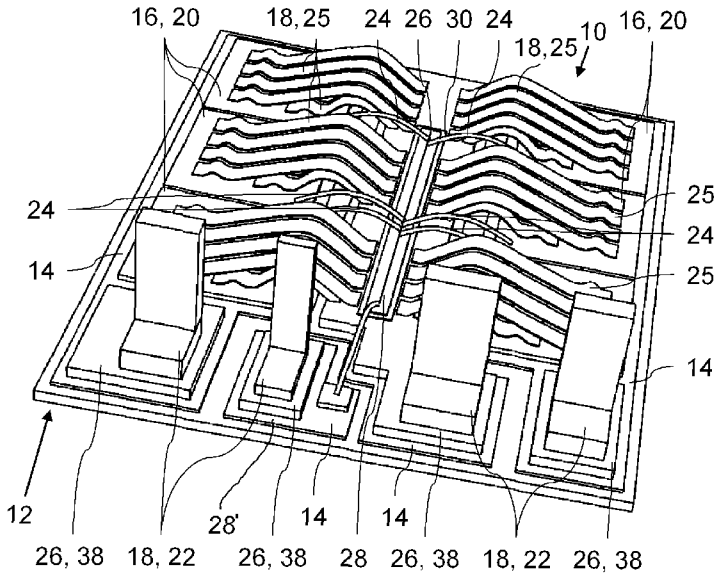

FIG. 1

(57) **Abstract**: The invention relates to a circuit arrangement (10) in which a power functional device (16) and a conductor element (18) are mounted, the arrangement (10) comprising a substrate (12), a wiring layer (14) provided on the substrate (12) and electrically connected to the functional device (16) and to the conductor element (18) and an intermediate electric contact device, which is mounted on the wiring layer (14) to provide on the side opposite to the wiring layer a contact region for contacting the conductor element (18). According to the invention the conductor element (18) is contacting the intermediate electric contact device in the contact region which is opposite to an area, in which the electric contact device is fixed to the wiring layer. The invention further relates to a corresponding manufacturing method of a circuit arrangement.

WO 2011/036307 A1

Description

Circuit arrangement and manufacturing method thereof

Technical Field

[0001] The invention relates to a circuit arrangement in which a power functional device, preferably a power semiconductor such as a transistor or diode, and a conductor element are mounted, the arrangement comprising a substrate, a wiring layer provided on the substrate and electrically connected to the power functional device and to the conductor element, and an intermediate electric contact device, which is mounted on an according part of the wiring layer to provide a corresponding contact region for contacting the functional device and/or the conductor element.

Background Art

[0002] Document EP 1 711 040 B1 depicts a circuit device in which a functional device and an externally leading conductor are mounted, the circuit device comprising a substrate, a wiring layer provided on the substrate and electrically connected to the functional device and to the externally leading conductor, and an additional coating metal layer formed on a part of the wiring layer to provide a corresponding contact region for contacting the functional device. The wiring layer and the additional coating metal layer constitute a metallisation of the substrate. Unfortunately the low temperature bonding proposed in this document needs a silver plating which will hinder the use of ultra sonic welding for the terminals.

[0003] The metallisation constituted by the wiring layer and the coating metal layer on the part of the wiring layer contributes with relatively high resistivity contribution (about 30 μΩ) to the overall arrangement resistance. One possible solution is using a substrate metallisation that is in general thicker for decreasing the resistivity. A problem when increasing the metallisation thickness is that the layout tolerances increase at the same time. Therefore the layout would have to be changed with loss of cross sectional area again.

[0004] Another drawback of a generally thicker substrate metallisation is that the mechanic stress at the metallisation edges of the wiring layer will increase where crack growth in the especially ceramic substrate is initiated (the polyimide might prevent it).

[0005] From EP 1 830 406 A1 a power module is known. In this known power module a power semiconductor is mounted on top of a heat spreader. According to the figures of EP 1 830 406 A1 the heat spreader is aligned with the element on which it is mounted.

[0006] From DE 43 00 516 A1 another power module is known. In this known power module a contact plate is arranged on top of a diode in order to ease the connection to a massive copper element.

[0007] From "Low-inductance module construction for high speed, high-current IGBT module suitable for electric vehicle application" by T. Tsunoda et al. (Power Semiconductor devices and ICS, 1993, ISPSD '93., Proceedings of the 5th International Symposium on Monterey, CA, USA 18-20 May 1993, New York, NY, USA IEEE, US, 18 May 1993) a multi-layered DBC substrate is known. By the proposed construction the collector and emitter terminals are arranged closely to each other in order to compensate for the magnetic field generated by the current flow in individual terminals.

Summary of invention

[0008] It is the object of the invention to provide a circuit arrangement, which overcomes the aforementioned disadvantages.

[0009] This object is achieved by the present invention as defined in claim 1. The intermediate electric contact device is fixed to the according part of the wiring layer only in finite sub-areas of the entire outer side (or interface) of the wiring layer. According to the claim1, the intermediate contact device has a first side on which the intermediate contact device is fixed to the wiring layer. Opposite to the part of the wiring layer, in which the intermediate contact device is fixed to the wiring layer, the intermediate contact device has a contact region, in which the conductor element is contacting the intermediate contact device. By this arrangement, the wiring

layer as well as the substrate can be protected from damages during attaching of the conductor element.

[0010] A further advantage is, that when fixing the intermediate contact device on top of a track of the wiring layer being thinner than the intermediate contact device, the stress at the metallisation edge at the wiring layer is not increased a lot because a fixation area of the fixation is smaller than the metallisation area below. There is a margin between the intermediate contact device and the metallisation edge.

[0011] According to a preferred embodiment of the invention, the intermediate contact device is fixed to the wiring layer by soldering and/or low-temperature bonding (LTB).

[0012] According to another preferred embodiment of the invention, the conductor element is an externally leading conductor.

[0013] According to yet another preferred embodiment of the invention, the power functional device is a power transistor, especially an insulated gate bipolar transistor, or a (power) diode. The insulated gate bipolar transistor or IGBT is a three-terminal power semiconductor device, noted for high efficiency and fast switching. In the active state of the IGBT a voltage or potential difference between the emitter as well as a corresponding emitter track and the gate as well as the corresponding gate track of the IGBT is a low voltage. Furthermore selectively thickening the emitter tracks is less critical for reliability because the emitter track does not see that high temperatures than the collector tracks.

[0014] According to one preferred embodiment of the invention, the at least partial electrically conductible contact device is a metal foil or metal plate. The metal plate can be standard insulated metal technology (IMS). The bonding of the plate can be done in the process step as the bonding of the power functional device (die-bonding). The metal foil or metal plate preferably is thicker than 100 µm, more preferably thicker than 200 µm.

[0015] According to another preferred embodiment of the invention, the at least partial electrically conductible contact device is a circuit board for selectively contacting other elements and/or devices of the circuit arrangement.

[0016] According to yet another preferred embodiment of the invention, the intermediate contact device and at least one bonding element for electrically contacting the power functional device with the wiring layer are integrally formed. The intermediate contact device being integrally formed with the bonding element saves costs and simplifies the mounting of the arrangement.

[0017] The present invention further relates to a method of manufacturing a circuit arrangement in which at least one functional device and at least one conductor element is mounted, wherein the arrangement comprises a substrate and a wiring layer provided on the substrate, the method comprising the steps of:

- mounting and electrically contacting an intermediate contact device on an the wiring layer to provide contact region on one side of the intermediate contact device, which is opposite to the wiring layer (14); and
- directly electrically connecting the conductor element to the intermediate contact device in the contact region.

[0018] According to a preferred embodiment of the invention, the intermediate contact device is fixed to the wiring layer by soldering and/or low-temperature bonding (LTB).

[0019] According to another preferred embodiment of the invention, the wiring device is an externally leading conductor or terminal of the arrangement.

[0020] According to yet another preferred embodiment of the invention, the power functional device is a power transistor, especially an insulated gate bipolar transistor, or diode.

[0021] According to one preferred embodiment of the invention, the at least partial electrically conductible contact device is a metal foil or metal plate. The metal plate can be standard IMS technology. The bonding of the plate can be done in the process step as the bonding of the power functional device (die-bonding). The metal foil or metal plate preferably is thicker than 100 µm, more preferably thicker than 200 µm.

[0022] According to another preferred embodiment of the invention, the at least partial electrically conductible contact device is a circuit board.

[0023] According to yet another preferred embodiment of the invention, the intermediate contact device and at least one bonding element for electrically contacting the power functional device with the wiring layer are integrally formed. The intermediate contact device being integrally formed with the bonding element saves costs and simplifies the mounting of the arrangement.

Brief description of drawings

[0024] These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

[0025] In the drawings:

[0026] Fig. 1 depicts a circuit arrangement according to a first embodiment of the invention;

[0027] Fig. 2 shows the circuit arrangement of Fig. 1 in a sectional view;

[0028] Fig. 3 shows a circuit arrangement according to a second embodiment of the invention in a sectional view;

[0029] Fig. 4 shows a circuit arrangement according to a third embodiment of the invention in a sectional view; and

[0030] Fig. 5 depicts a circuit arrangement according to a fourth embodiment of the invention.

Description of embodiments

[0031] Fig. 1 and 2 show a power circuit arrangement 10 comprising a substrate 12 being a ceramic substrate and a structured wiring layer 14 provided on the substrate 12. The wiring layer 14 has at least a first track and a second track, which is insulated from the fist track. In the current embodiment, the first track is formed by a collector track 36 and the second track is formed by an emitter track 30. In other embodiments, the wiring layer could have more than two tracks. In the current embodiment, the wiring layer 14 has a third track being a gate track. The structured wiring layer 14 especially is preferably made of copper. Preferably the wiring layer 14 has a thickness of 200 µm to 400 µm. In the circuit arrangement 10 of the present

embodiment six power functional devices 16 (not shown in detail) and a plurality of conductor elements 18 are mounted on the power circuit arrangement 10. The power functional devices 16 are power semiconductor devices such as power transistors 20, especially power IGBTs (IGBT: Insulated Gate Bipolar Transistor), and diodes. The conductor elements 18 preferably are externally leading conductors 22 for externally connecting the power functional device 16 outside the circuit arrangement 10 and/or bonding elements, in particular bonding wires 25. The externally leading conductors 22 preferably are L-shaped power terminals of the circuit arrangement. These power terminals are e.g. made of so called “moly plates”, i.e. a metal-free compound composed of molybdenum disulfide and graphite preferably with a synthetic non-melting carrier.

[0032] As shown in Fig. 1, the power circuit arrangement 10 has four externally leading conductors 22. Between each of the externally leading conductor 22 and the respective area of the wiring layer 14 just below the externally leading conductor 22 an intermediate contact device 26 is arranged. The intermediate contact device 26 has a first side and a second side which is at least approximately parallel to the first side. The first side of the intermediate contact device 26 is electrical conductively fixed to the wiring layer 14. On the second side, the intermediate contact device 26 provides a contact region for contacting at least one conductor element 18, for example the externally leading conductor 22. The conductor element 18 is electrical conductively fixed on the intermediate contact device 26. Further, the contact region is opposite of the area on the first side in which the intermediate contact device is electrical conductively fixed to the wiring layer 14.

[0033] The intermediate contact devices 26 between the conductor elements 18, e.g. the externally leading conductors (terminals) 22, and the wiring layer 14 protect the ceramic substrate 12 when bonding the externally leading conductors 22 by ultrasonic welding (also laser and resistive welding). For that purpose the intermediate contact devices 26 must also be bonded on top of the parts of the structured wiring layer 14 being the collector tracks

36, emitter track 30 and/or the gate track 28' just below the feet of the externally leading conductors 22 (terminal feet). It should be understood, that the intermediate contact device 26 is only needed if connecting the conductor element 18 directly to the wiring layer 14 could damage the ceramic substrate 12 and/or the wiring layer 14. Thus in other preferred embodiments not shown in the figure only one or several of the conductor elements 18, in particular one or several of the externally leading conductors 22 are connected to the respective track of the wiring layer by an intermediate contact device 26.

[0034] Preferably, the intermediate contact device is a metal foil or metal plate. Hence, the intermediate contact device 26 is self-contained. The bonding of the metal foil or metal plate can be done in the process step as the bonding of the power functional device (die-bonding). The metal foil or metal plate preferably is thicker than 100 µm, more preferably thicker than 200 µm.

[0035] In general, the power functional devices 16 are electrically connected to the externally leading conductors 22 via their connector areas (not shown), bonding elements being bonding wires 25 and the intermediate contact devices 26 as well as tracks 36 established by the wiring layer 14 and intermediate contact devices 26.

[0036] In the embodiment shown in Fig. 1 and 2 an upper or emitter contact of each of the power functional devices 16 is electrically contacted by bonding wires 25 leading to a metal foil 34 arranged on the emitter track 30 of the wiring layer 14. The metal foil 34 is a possible embodiment of the intermediate contact device 26 according to the present invention. A lower or collector contact of each of the power functional devices 16 is in electrical contact to one of the collector tracks 36 of the wiring layer 14. Further, on each collector track 36 a metal plate 38 is arranged, which is a further embodiment of the intermediate contact device 26. As described above, the metal plate 38 on the collector tracks 36 is for protecting the ceramic substrate 12. The metal foil 34 on the emitter track 30 is not only for protecting the ceramic substrate 12 but also for lowering the resistivity as discussed below.

[0037] The intermediate contact devices 26 are preferably arranged in direct electrical contact to the conductor elements 18 (especially the externally leading conductors 22) and/or to the wiring layer, which is preferably formed by the at least first and second track, in particular the collector track 36 and the emitter track 30 for the IGBT transistors 20.

[0038] An additional electrical resistance film 32 is located between the gate track 28 formed by an additional wiring strip and the emitter track 30 formed by the respective part of the structured wiring layer 14 and the intermediate contact device 26 being a metal foil 34. The metal foil 34 is electrical conductively fixed on the respective part of the structured wiring layer 14. Preferably, the gate track 28 and the intermediate contact device on which the gate track 28 is provided, is formed by a partial electrically conductible metal foil or metal plate by insulated metal technology (IMS).

[0039] Each of the two collector tracks shown in Figs. 1 to 5 directly contacts three IGBTs and/or diodes by their collector connector areas.

[0040] According to the invention, the intermediate electric contact devices 26 are mounted on a respective part of the wiring layer 14 to provide a corresponding contact region for contacting the power functional device 16. Further, an intermediate electric contact device 26 is mounted on one part of the wiring layer 14 that forms the emitter track 30.

[0041] As shown in more detail in Fig. 2, in the circuit arrangement 10 preferably a metallic plate or thick metallic foil 34 is bonded on the part of the wiring layer 14 building the emitter track 30. The plate or foil 34 provides on top the additional metallisation or wiring strip being the gate track 28 for the IGBTs. The plate or foil can be standard IMS technology ("DENKA HITT PLATE"). The bonding of the plate or foil 34 can be done in the process step as the bonding of the power functional devices 16 (being a die-bonding). The bonding method preferably is soldering or low-temperature bonding (LTB). Thus, the joint between the wiring layer 14 and the intermediate contact device 26 is a soldering joint or a joint made by low-temperature bonding. The plate on top of the part of the wiring layer 14 lowers the resistance of the overall emitter path. For a standard IGBT module (e. g. "HiPak2") the reduction could be more than 10 μΩ. For a

1700 V / 3600 A arrangement or module this reduces the voltage drop by more than 36 mV (around 1.5% of the on-stat voltage).

[0042] The gained thickness of the emitter track 30 allows making the emitter track 30 narrower. The narrower emitter track 30 allows to reduce the overall area of the substrate 12 or to form a larger area of the collector tracks 36. A corresponding arrangement is shown in Fig. 3.

[0043] Fig. 3 is essentially in accordance with Fig. 2, wherein the width of the emitter track 30 is narrower than in the embodiment of the circuit arrangement 10 shown in Fig. 2. The larger area of the collector track 36 increases the heat spreading. Having a larger distance between the surface of the substrate 12 and the heating power functional device 16 will also improve the case temperature cycling capability because there is less temperature difference ΔT and thus less stress at the surface of the substrate solder.

[0044] Because of the narrower emitter track 30 larger collector tracks 36 can be used with a substrate 12 of the same size. Fig. 4 shows an according circuit arrangement with larger collector tracks. The active area of the collector tracks can be increased by more than 10%.

[0045] Fig. 5 is essentially in accordance with Figs. 1 to 4, wherein a plurality of bonding metal sheets 38 electrically connecting the emitter track 30 to the corresponding emitter connector areas of the power functional devices 16 and the intermediate contact device 26 connecting the emitter track 30 with the corresponding (emitter) conductor element 18 being an externally leading conductor 22 are integrally formed as a intermediate contact device 26 fixed to the emitter connector area of the power functional devices 16 and to the corresponding (emitter) conductor element 18. This intermediate contact device 26 shown in Fig. 5 is directly contacting the emitter of the power functional device 16 and/or the corresponding conductor element 18.

[0046] In the die-attach process intermediate contact devices 26, especially metal plates 38 can be bonded that provide several functions:

- Lowering the electric resistance,
- Protection of the ceramics when welding the power terminals (e. g.

strong moly plates),

- Carrying the gate circuit on top.

[0047] The corresponding manufacturing method comprises the steps of:

- fixing the intermediate contact device, e.g. the metal foil 34 or plate 38, on an according part of the wiring layer 14 only in finite sub-areas of the entire outer side of the wiring layer to provide a corresponding contact region for the conductor element 18; and
- directly or indirectly electrically connecting the functional device(s) and the conductor 22 to the metal foil 34 or plate 38.

[0048] The corresponding resistance of the collector tracks drops from 8.2 μΩ to 6.8 μΩ, the resistance of the emitter track drops from 24.2 μΩ to 6.8 μΩ, the total reduction is about 18,8 μΩ.

[0049] In further embodiments, not shown in the figures, only one or several of the intermediate contact devices shown in Fig. 1 to 5 are arranged on the wiring layer 14. It is also possible that at least one conductor element 18 is directly connected to the wiring layer 14.

[0050] While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive; the invention is not limited to the disclosed embodiments.

[0051] Other variations to be disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure, and the appended claims. In the claims, the word “comprising” does not exclude other elements or steps, and the indefinite article “a” or “an” does not exclude a plurality. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage. Any reference signs in the claims should not be construed as limiting scope.

Reference signs list

[0052]

10	circuit arrangement
12	substrate
14	wiring layer
16	functional device
18	conductor element
20	power transistor
22	externally leading conductor
24	bonding wire
25	bonding metal sheet
26	intermediate contact device
28	gate track
30	emitter track
32	resistance film
34	metal foil
36	collector track
38	metal plate

Claims

1. A circuit arrangement (10) comprising:
   - a substrate (12);
   - a wiring layer (14) provided on the substrate (12) and electrically connected to a power functional device (16) and to a conductor element (18); and
   - an intermediate contact device, which is mounted on the wiring layer (14) to provide on the side opposite to the wiring layer a contact region for contacting the conductor element (18); wherein the intermediate contact device (26) has at least a first side and a second side, the second side is at least approximately parallel to the first side, wherein the intermediate contact device (26) is fixed to the wiring layer (14) on the first side, characterized in that the conductor element (18) is contacting the intermediate contact device (26) on the second side in the contact region which is opposite to an area on the first side in which the intermediate contact device (26) is electrical conductively fixed to the wiring layer (14).
2. The circuit arrangement according to claim 1, wherein the intermediate contact device (26) is fixed to the wiring layer by a soldering joint and/or by a joint made by low-temperature bonding.
3. The circuit arrangement according to claim 1 or 2, wherein the intermediate electric contact device (26) is fixed to an according part of the wiring layer (14) in finite sub areas of the entire outer side of the wiring layer.
4. The circuit arrangement according to one of claims 1 to 3, wherein the conductor element (18) is an externally leading conductor (22) or a bonding element leading from the intermediate contact device to the power functional device (16).
5. The circuit arrangement according to one of claims 1 to 4, wherein the power functional device (16) is a power semiconductor device, such as a power transistor (20), especially an insulated gate bipolar transistor, or a diode.
6. The circuit arrangement according to one of claims 1 to 5, wherein the intermediate contact device is at least partial electrically conductible, and wherein the intermediate contact device (26) is preferably a metal foil, a metal sheet or a metal plate.

7. The circuit arrangement according to one of claims 1 to 5, wherein the at least partial electrically conductible intermediate contact device (26) is a circuit board.
8. The circuit arrangement according to one of the claims 1 to 7, wherein the intermediate contact device is thicker than 100 µm, more preferably thicker than 200 µm.
9. The circuit arrangement according to one of the claims 1 to 8, wherein the intermediate contact device (26) and a bonding element for electrically contacting the power functional device (16) with the wiring layer (14) are integrally formed.
10. The circuit arrangement according to one of the claims 1 to 9, wherein the intermediate contact device (26) is completely in direct electrical and mechanical contact to the wiring layer (14).
11. The circuit arrangement according to one of the claims 1 to 10, wherein the intermediate contact device (26) is self-contained.
12. A method of manufacturing a circuit arrangement, in particular according to one of the claim 1 to 11, in which at least one power functional device (16) and at least one conductor element (18) is mounted, wherein the arrangement comprises a substrate (12) and a wiring layer (14) provided on the substrate, the method comprising the steps of:
    - mounting and electrically contacting an intermediate contact device (26) on the wiring layer to provide a contact region on one side of the intermediate contact device, which is opposite to the wiring layer (14); and
    - directly electrically connecting the conductor element (18) to the intermediate contact device in the contact region.
13. The method according to claim 12, wherein the mounting of the intermediate contact element to a part of the wiring layer is a fixing of the intermediate contact element to the part only in finite sub-areas of the entire outer side of the wiring layer.
14. The method according to claim 12 or 13, wherein the intermediate contact device (26) is fixed to the wiring layer by soldering and/or low-temperature bonding.

15. The method according to one of the claims 12 tor 14, wherein the conductor element is an externally leading conductor.
16. The method according to one of claims 12to 15, wherein the power functional device is a power semiconductor, such as a power transistor, especially an insulated gate bipolar transistor, or a diode.
17. The method according to one of claims 12to 16, wherein the intermediate contact device is at least partial electrically conductible, and wherein the intermediate contact device (26) is preferably a metal foil, a metal sheet or a metal plate.
18. The method according to one of claims 12 to 17, wherein the intermediate contact device is at least partial electrically conductible, and wherein the intermediate contact device (26) is a circuit board.
19. The method according to one of claims 12 to 18, wherein the intermediate contact device and a bonding element for electrically contacting the power functional device with the wiring layer are integrally formed.

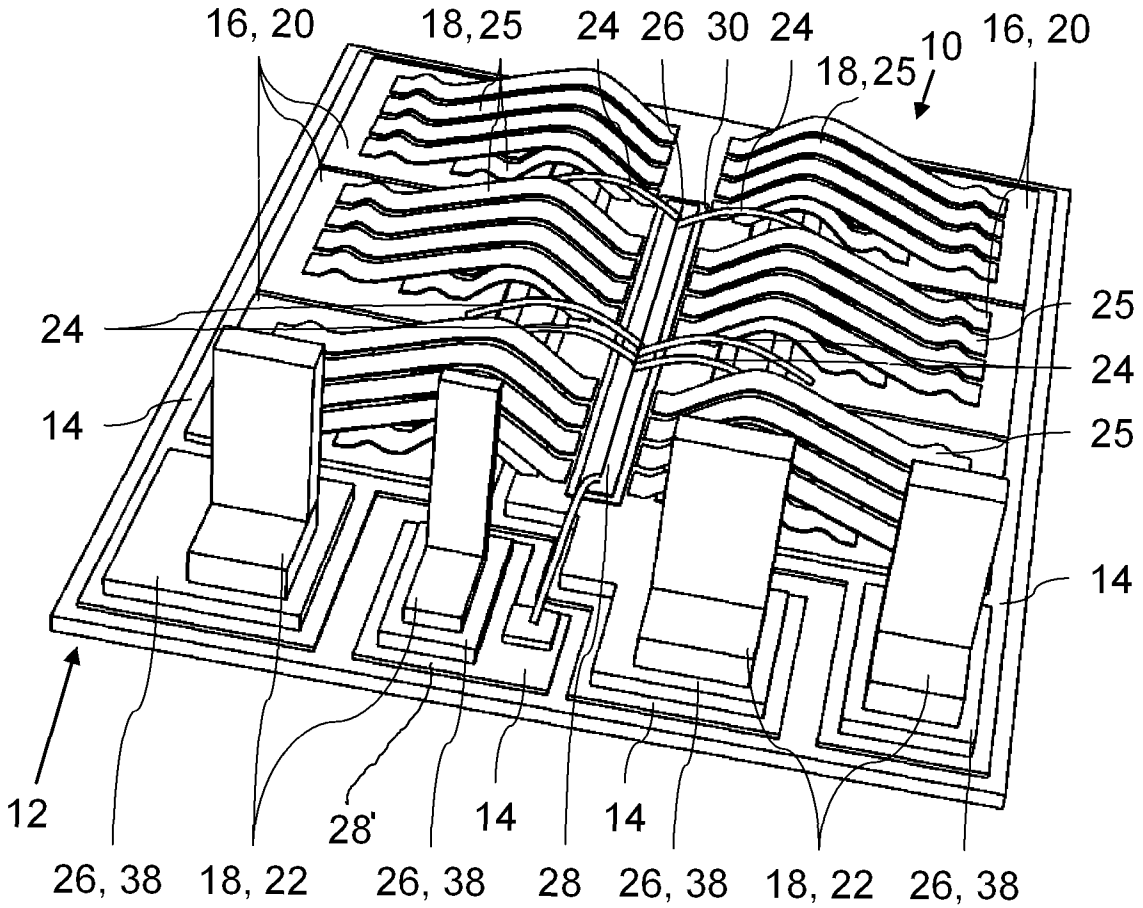
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FIG. 1

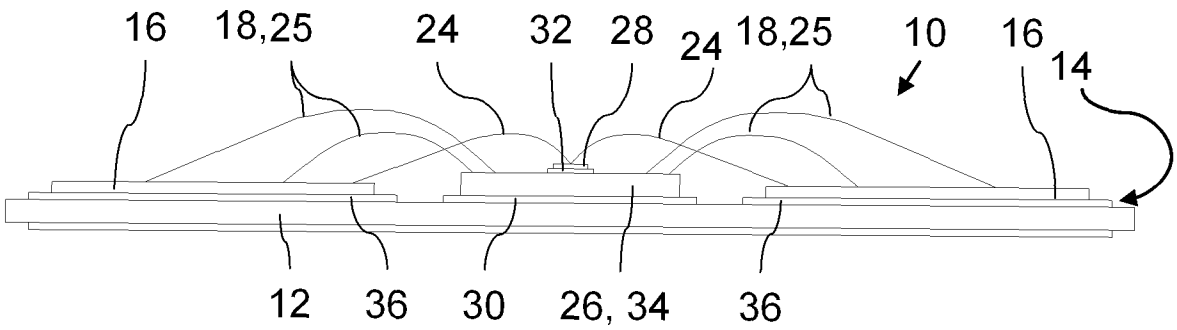
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Fig. 2

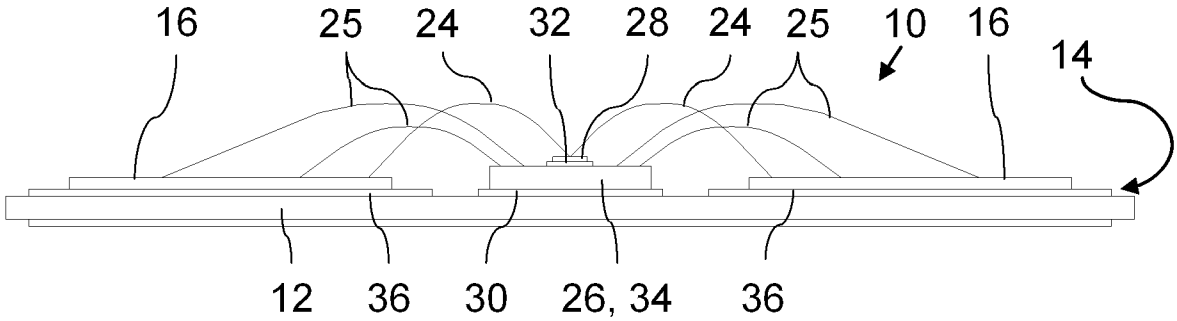

Fig. 3

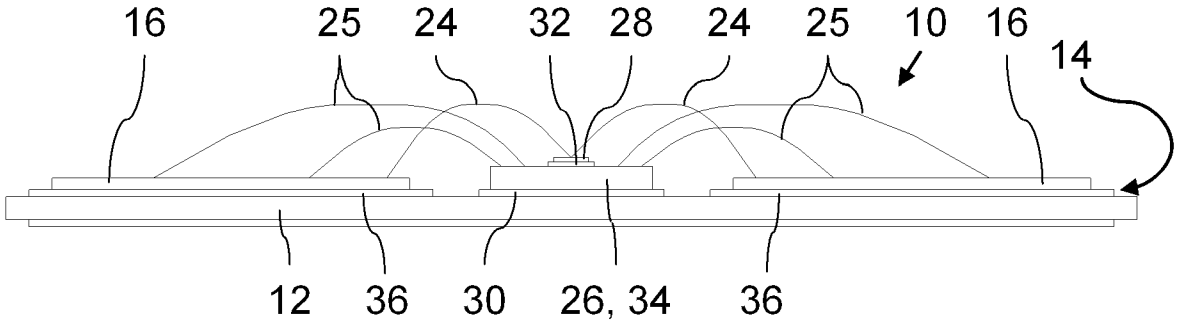

Fig. 4

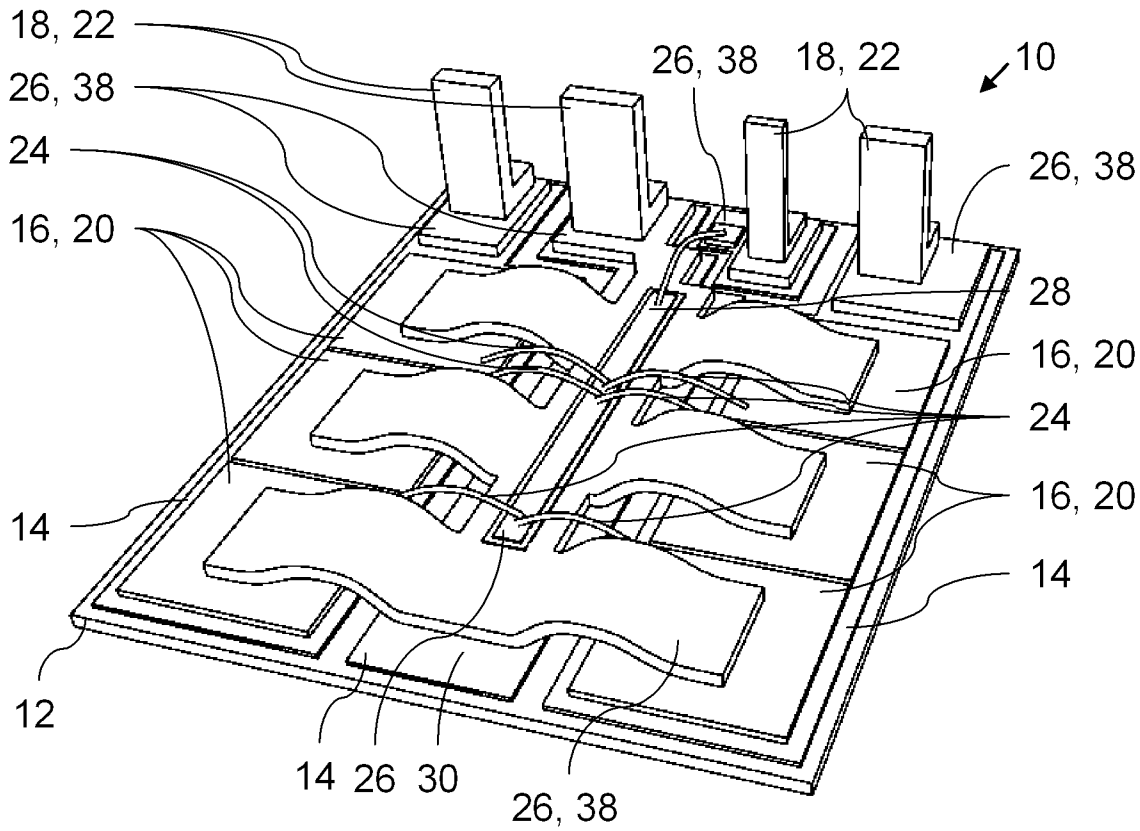

Fig. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/064377

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L25/07 H01L23/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L H05K H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/127503 A1 (GOBL CHRISTIAN [DE] ET AL GOEBL CHRISTIAN [DE] ET AL) 16 June 2005 (2005-06-16) paragraphs [0027] - [0032], [0034]; figure 1	1,2,4-6, 10-12, 14-17
X	EP 0 277 606 A2 (IBM [US]) 10 August 1988 (1988-08-10) column 7, line 7 - line 15 column 8, line 26 - line 39; figure 2 column 6, line 7 - line 12 column 5, line 40 - column 6, line 6 column 5, line 19 - line 31	1,3,5, 7-13, 16-19

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
11 November 2010	19/11/2010

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2005127503 A1	16-06-2005	BR PI0405288 A	19-07-2005
		DE 10355925 A1	30-06-2005
		EP 1548829 A2	29-06-2005
		JP 2005167241 A	23-06-2005
		KR 20050052341 A	02-06-2005
EP 0277606 A2	10-08-1988	DE 3888552 D1	28-04-1994
		DE 3888552 T2	27-10-1994
		JP 1891930 C	07-12-1994
		JP 6018247 B	09-03-1994
		JP 63196051 A	15-08-1988
		US 4766670 A	30-08-1988