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(54) **MECHANISM FOR PROVIDING OVER-VOLTAGE PROTECTION DURING POWER UP OF DC-DC CONVERTER**

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(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 925 days.

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(51) **Int. Cl.**  
**H03K 17/16** (2006.01)

(52) **U.S. Cl.** ..... **327/381**; 327/380; 361/90; 361/91.1; 361/91.2

(58) **Field of Classification Search** ..... 327/110, 327/180, 372; 361/91.1; 323/224, 282, 283, 323/284

See application file for complete search history.

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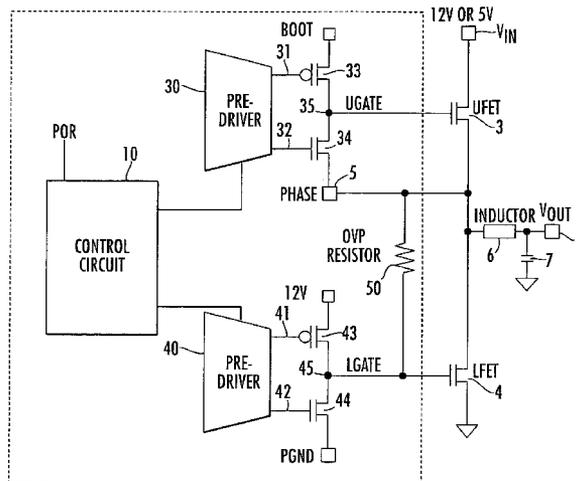
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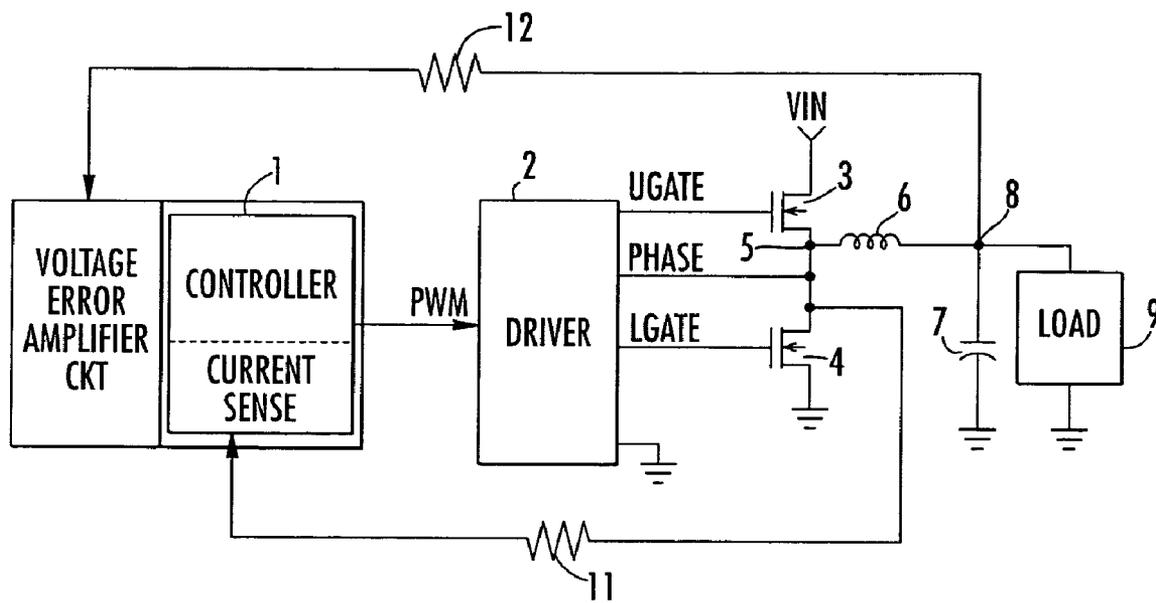
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(57) **ABSTRACT**

An over-voltage protection circuit prevents an anomaly, such as a short circuit in the upper-switched electronic device of a DC-DC power supply, from propagating to downstream circuitry. The over-voltage protection circuit, which includes an overvoltage sense resistor coupled between an output of the upper or high side FET and the gate of the lower FET, is operative to sense a short circuit fault condition in the circuit path through the upper FET during initial power up of the system. In response to this condition, the lower NFET device is turned on so as to provide an immediate by-pass of the overvoltage condition to ground, and thereby prevent excessive voltage from being applied by the output terminal to downstream powered circuitry.

**8 Claims, 4 Drawing Sheets**





**FIG. 1**  
**(PRIOR ART)**

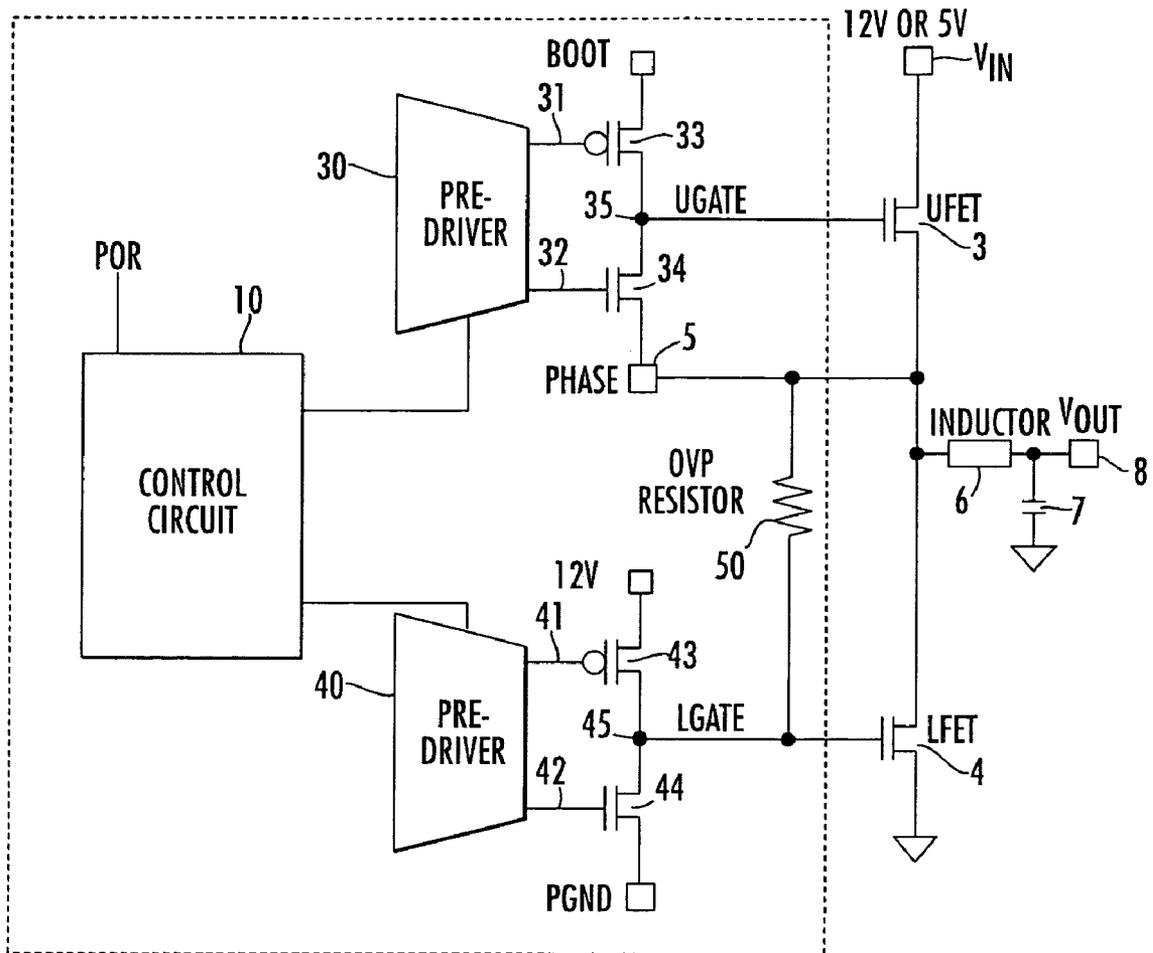


FIG. 2

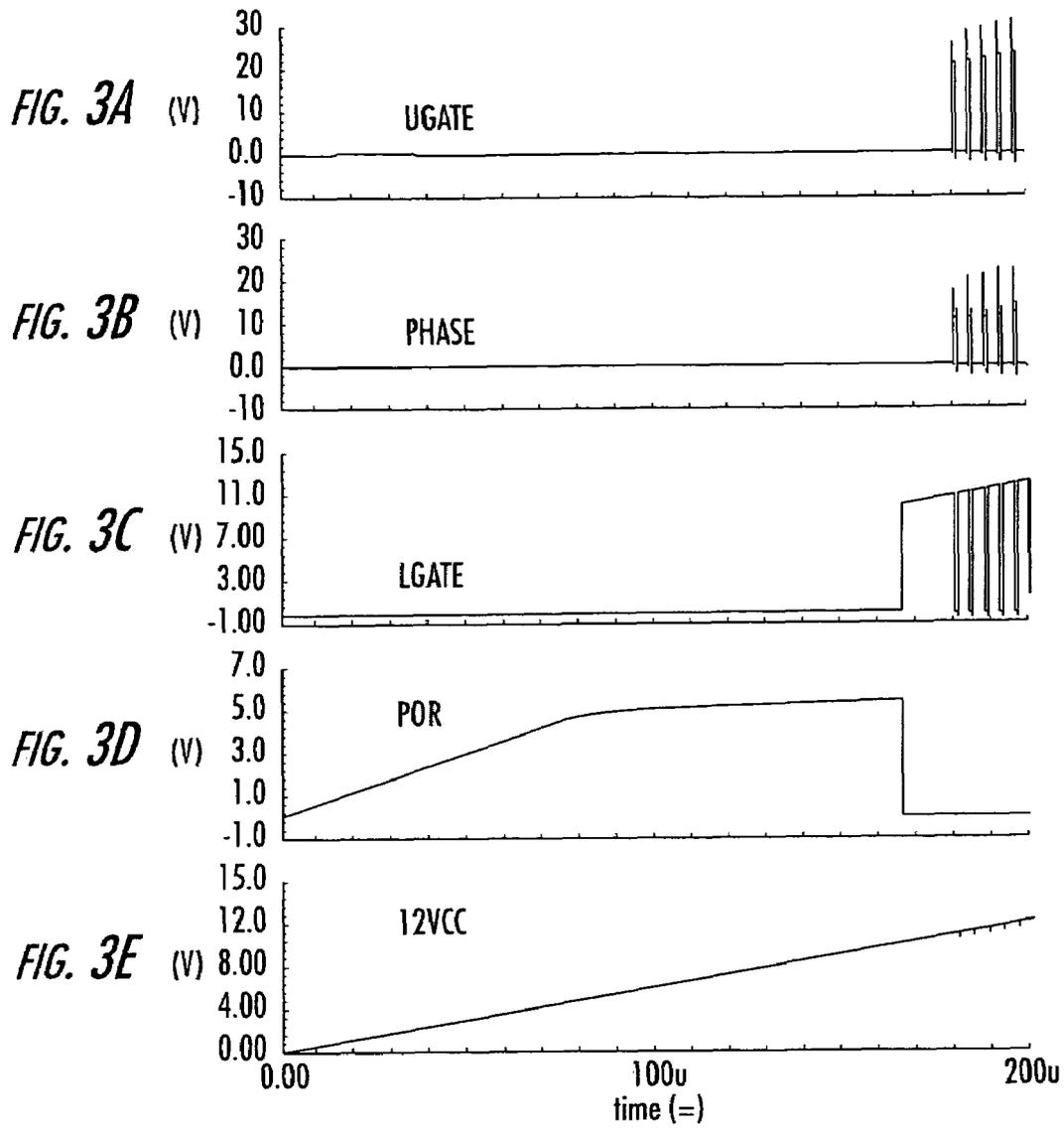


FIG. 4A

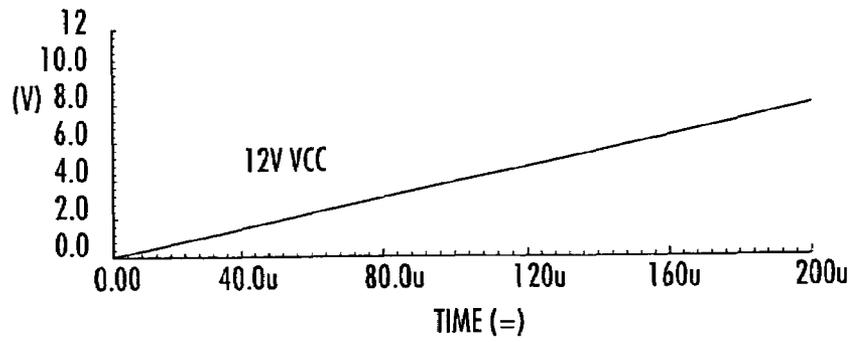


FIG. 4B

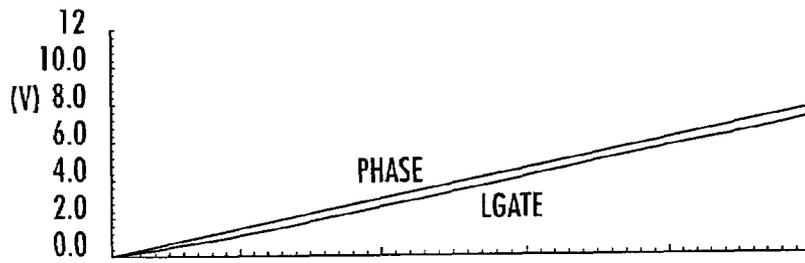


FIG. 4C

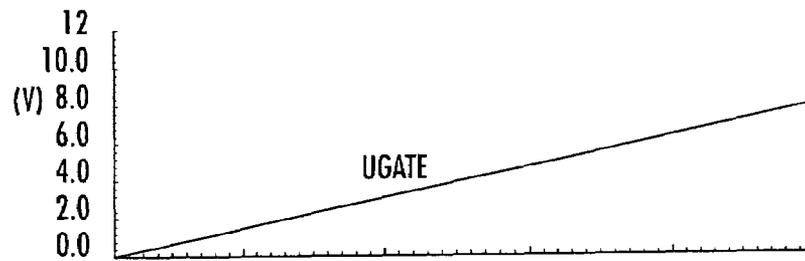
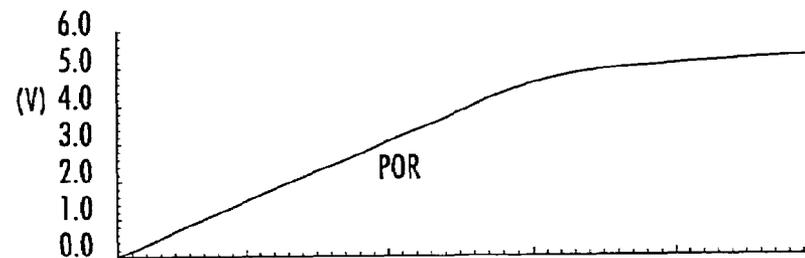


FIG. 4D



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## MECHANISM FOR PROVIDING OVER-VOLTAGE PROTECTION DURING POWER UP OF DC-DC CONVERTER

### CROSS-REFERENCE TO RELATED APPLICATION

The present application is a continuation application of U.S. patent application Ser. No. 10/685,314, filed on Oct. 14, 2003, by Noel B. DeQuina et al., entitled "Mechanism For Providing Over-Voltage Protection During Power Up of DC-DC Converter", now U.S. Pat. No. 6,873,191, issued Mar. 29, 2005, and claims the benefit of co-pending U.S. application Ser. No. 60/437,179, filed Dec. 31, 2002, by Noel B. DeQuina et al., entitled: "Mechanism for Providing Over-Voltage Protection During Power Up of DC-DC Converter," assigned to the assignee of the present application and the disclosure of which is incorporated herein.

### FIELD OF THE INVENTION

The present invention relates in general to DC power supply systems and components therefor, and is particularly directed to a new and improved over-voltage protection apparatus that is configured to sense the onset of an over-voltage condition associated with a shorted upper FET of a DC-DC converter and, in response thereto, to effect a controlled by-pass of the over-voltage condition and shut-down of the power supply, so as to protect electronic circuitry powered thereby.

### BACKGROUND OF THE INVENTION

Electrical power for an integrated circuit (IC), such as but not limited to a microprocessor chip of a personal computer, is typically supplied by one or more direct current (battery) power sources, such as a buck-mode, pulse width modulation (PWM) based, DC-DC converter of the type diagrammatically shown in FIG. 1. As shown therein, a PWM control circuit 1 supplies a synchronous PWM signal to a switching circuit driver 2, that controls the turn-on and turn-off of a pair of electronic power switching devices, to which a powered load 9 is coupled. In the illustrated DC-DC converter, the electronic power switching devices comprise an upper (or high side) power NMOSFET (or NFET) device 3, and a lower (or low side) power NFET device 4, having their drain-source current flow paths connected in series between a pair of power supply rails (e.g., VIN and ground (GND)).

The upper NFET device UFET 3 is turned on and off by an upper gate-switching signal UGATE applied to its gate from driver 2, while the lower NFET device LFET 4 is turned on and off by a lower gate-switching signal LGATE supplied from driver 2. A common or phase node 5 between the two NFETs is coupled through an inductor 6 to a load reservoir capacitor 7 that is coupled to a reference voltage terminal (GND). The connection 8 between inductor 6 and capacitor 7 serves as an output node from which a desired (regulated) DC output voltage Vout is applied to a LOAD 9 (coupled to GND).

The output node connection 8 is also fed back via a feedback resistor 12 to error amplifier circuitry within the PWM controller 1. The error amplifier circuitry is used to regulate the converter's DC output voltage relative to a reference voltage supply. In addition, the common node 5 between the controllably switched NFETs is coupled via a current sense resistor 11 to current-sensing circuitry within the controller 1, in response to which the controller adjusts duty ratio of the

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PWM signal, as necessary, to maintain the converter's DC output within a prescribed set of parameters.

In the course of supplying power from the power supply to its powered components, it is of critical importance that an anomaly in the power supply path, such as a short circuit in the upper switched NFET (which may be due to a bad component or inadvertent shorting of its drain and during manufacture), not propagate to downstream circuitry, especially a microprocessor chip.

### SUMMARY OF THE INVENTION

The present invention successfully addresses this potential problem by means of an over-voltage protection circuit that is incorporated into the FET switching circuitry. This over-voltage protection circuit is operative to sense a short circuit fault condition in the circuit path through the upper or high side FET during initial power up of the system and, in response thereto, to turn on the lower NFET device. This results in an immediate by-pass of the overvoltage condition to ground, and thereby prevents excessive voltage from being applied by the output terminal to downstream powered circuitry.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 diagrammatically illustrates a conventional buck-mode, pulse width modulation (PWM) based, DC-DC converter;

FIG. 2 diagrammatically illustrates an embodiment of the over-voltage protection scheme of the present invention;

FIGS. 3A-3E are timing diagrams associated with the normal power-up operation of a DC-DC converter incorporating the over-voltage protection scheme of FIG. 2; and

FIGS. 4A-4D are timing diagrams associated with a short across the source-drain path of the upper FET of a DC-DC converter incorporating the over-voltage protection scheme of FIG. 2.

### DETAILED DESCRIPTION

Attention is now directed to FIG. 2, wherein an embodiment of the over-voltage protection scheme according to the present invention is diagrammatically illustrated as comprising an overvoltage protection (OVP) control circuit 10, to which a power on reset (POR) signal is supplied, and which is incorporated as an augmentation to the driver circuitry 2 of the circuitry of FIG. 1, described above. Control circuit 10 is operative to perform the functionality of the control circuit 1 of FIG. 1 and incorporates combinational logic and flip-flops that implement the overvoltage protection control functionality described below. The protection circuit of FIG. 2 further includes respective upper and lower pre-driver circuits 30 and 40, which are operative to supply gate drive signals to the upper NFET 3 and lower NFET 4. In addition, an overvoltage protection resistor 50 is coupled between the phase node 5 and the LGATE input to the lower NFET 4.

The upper pre-driver circuit 30 is coupled to receive an upper drive control signal from the OVP controller circuit 10, and has first and second output control lines 31 and 32 coupled to the gates of an upper PFET switch 33 and an upper NFET switch 34, respectively. PFET switch 33 and NFET switch 34 have their source-drain paths coupled in series between a bootstrap supply node BOOT and the PHASE node 5. The common connection 35 of PFET 33 and NFET 34 is coupled as an upper gate drive UGATE to upper NFET 3.

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The lower pre-driver circuit **40** is coupled to receive a lower drive control signal from the OVP controller circuit **10**, and has first and second output control lines **41** and **42** respectively coupled to the gates of a lower PFET switch **43** and a lower NFET switch **44**. PFET switch **43** and NFET switch **44** have their source-drain paths coupled in series between a 12V supply node and a power ground (PGND) node. The common connection **45** of PFET **43** and NFET **44** is coupled as a lower gate drive LGATE to lower NFET **4**.

FIGS. 3A-3E are timing diagrams of normal power-up operation, where there is no short across the upper FET **3**. In particular, FIG. 3A shows the upper gate UGATE voltage being asserted by the upper predriver circuitry to the gate of upper UFET **3** at a value on the order of zero volts. FIG. 3B shows the phase voltage at phase node **5** also at zero volts. Similarly, FIG. 3C shows the lower gate LGATE voltage being asserted by the lower pre-driver to the gate of LFET **4** at a value on the order of zero volts. FIG. 3D shows the power on reset input voltage ramping up, to track the power supply voltage ramp applied at the voltage input terminal shown in FIG. 3E. Eventually, as shown in FIG. 3D, the operational power level reaches a voltage on the order of 5 VDC. Subsequently, switchmode operation begins, as shown in the right hand portion of the Figures, so that the output node is at its regulated voltage.

The case where a short occurs across the source-drain path of the upper NFET **3** during power-up is shown in FIGS. 4A-4D. In particular, FIG. 4A shows the voltage at input node Vin ramping up from zero toward 12 volts. With a short across the source and drain of upper NFET **3**, this will cause the voltage at the PHASE node **5** to also begin ramping toward the twelve-volt supply rail. As the phase voltage increases, the OVP resistor **50** couples this voltage to the LGATE input of lower NFET **4**, as shown in FIG. 4B. In response to this voltage exceeding the threshold voltage of the lower NFET **4**, NFET **4** turns on, creating a current path from the power supply input at Vin through the source-drain paths of both UFET **3** and LFET **4** to power ground.

When this happens, the voltage error amplifier in the power supply's control circuitry will detect a short to ground at the supply output, and take action to shut down the operation of the converter to prevent potential damage to powered components. In addition, during this shorted condition, the controller **1** is operative to cause the predriver circuits **30** and **40** to turn off the upper and lower FET pairs **33**, **34** and **43**, **44**. This ensures that the gate drive to LFET **4** tracks only through the OVP resistor **50** to the shorted state of UFET **3**. FIG. 4C shows the UGATE ramp, while FIG. 4D shows the power on reset (POR) voltage ramping up to five volts.

As will be appreciated from the foregoing description, the present invention is operative to prevent an anomaly, such as a short circuit in the upper-switched electronic device of a DC-DC power supply, from propagating to downstream circuitry, by means of an over-voltage protection circuit that is incorporated into the FET switching circuitry. This over-voltage protection circuit is operative to sense a short circuit fault condition in the circuit path through the upper or high side FET during initial power up of the system and, in response thereto, to turn on the lower NFET device. This results in an immediate by-pass of the overvoltage condition to ground, and thereby prevents excessive voltage from being applied by the output terminal to downstream powered circuitry.

While we have shown and described an embodiment in accordance with the present invention, it is to be understood that the same is not limited thereto but is susceptible to numerous changes and modifications as known to a person skilled in

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the art. We therefore do not wish to be limited to the details shown and described herein, but intend to cover all such changes and modifications as are obvious to one of ordinary skill in the art.

What is claimed is:

**1.** An over-voltage protection apparatus for generating a regulated DC output voltage at an output node which is arranged to be coupled to a device powered thereby comprising:

a DC-DC converter which is operative to generate a regulated output voltage derived from a supply voltage, said DC-DC converter having a pulse width modulation (PWM) generator which generates a PWM switching signal that switchably controls operation of a switching circuit containing first and second electronic power switching devices coupled between a power supply terminal to which said power supply voltage is coupled and a reference voltage terminal to which a reference voltage is coupled, said first and second electronic power switching devices having a common node there between coupled through an inductance to said output node; and  
 a by-pass circuit, having an input connected to said common node and an output connected to a control input of said second electronic power switching device, and being operative, in response to detecting a voltage at said common node indicative of an effective short circuit through said first switching device between said power supply terminal and said common node, to turn on said second electronic power switching device, so as to provide a by-pass current flow path from said common node to said reference voltage terminal, and thereby prevent an over-voltage from being applied to said output node and said powered device.

**2.** The apparatus according to claim **1**, wherein said by-pass circuit comprises a sense resistor connected to said common node and to said control input of said second electronic power switching device.

**3.** The apparatus according to claim **2**, wherein said switching circuit further includes an upper predriver switching circuit comprised of third and fourth electronic power switching devices respectively coupled between a first voltage supply terminal and said common node, and having a common connection there between coupled to the control electrode of said first electronic power switching device.

**4.** The apparatus according to claim **3**, wherein said switching circuit further includes a lower predriver switching circuit comprised of fifth and sixth electronic power switching devices respectively coupled between a second voltage supply terminal and a further reference node, and having a common connection there between coupled to the control electrode of said second electronic power switching device.

**5.** A method for controlling the operation of a DC-DC converter, which is operative to generate a regulated DC output voltage derived from a supply voltage, said DC-DC converter having a pulse width modulation (PWM) generator which generates a PWM switching signal that switchably controls operation of a switching circuit containing first and second electronic power switching devices coupled between a power supply terminal to which said power supply voltage is coupled and a reference voltage terminal to which a reference voltage is coupled, said first and second electronic power switching devices having a common node there between coupled through an inductance to said output node, said method comprising the steps of:

(a) monitoring, at said common node, the voltage at said common node for the occurrence of a voltage indicative

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of an effective short circuit from said power supply terminal through said first switching device to said common node; and

(b) in response to detecting, at said common node, said voltage indicative of said occurrence of an effective short circuit through said first switching device, providing a by-pass through said second switching device to said reference voltage terminal, and shutdown of the power supply, so as to protect electronic circuitry powered thereby from said over-voltage.

6. The method according to claim 5, wherein step (b) comprises connecting an over-voltage sense resistor to said common node and to a control input of said second electronic power switching device and, in response to said overvoltage sense resistor sensing, at said common node, said voltage indicative of said occurrence of an effective short circuit through said first switching device, turning on said second electronic power switching device, so as to provide a by-pass current flow path between said common node and said refer-

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ence voltage supply terminal, thereby preventing an over-voltage from being applied to said output node and said powered device.

7. The method according to claim 6, wherein said switching circuit further includes an upper predriver switching circuit comprised of third and fourth electronic power switching devices respectively coupled between a first voltage supply terminal and said common node, and having a common connection there between coupled to the control electrode of said first electronic power switching device.

8. The method according to claim 7, wherein said switching circuit further includes a lower predriver switching circuit comprised of fifth and sixth electronic power switching devices respectively coupled between a second voltage supply terminal and a further reference node, and having a common connection there between coupled to the control electrode of said second electronic power switching device.

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