



- (51) International Patent Classification: G02B 6/42 (2006.01)
- (21) International Application Number: PCT/EP2018/050188
- (22) International Filing Date: 04 January 2018 (04.01.2018)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data: 62/443,576 06 January 2017 (06.01.2017) US
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- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH,

(54) Title: COPACKAGING OF ASIC AND SILICON PHOTONICS

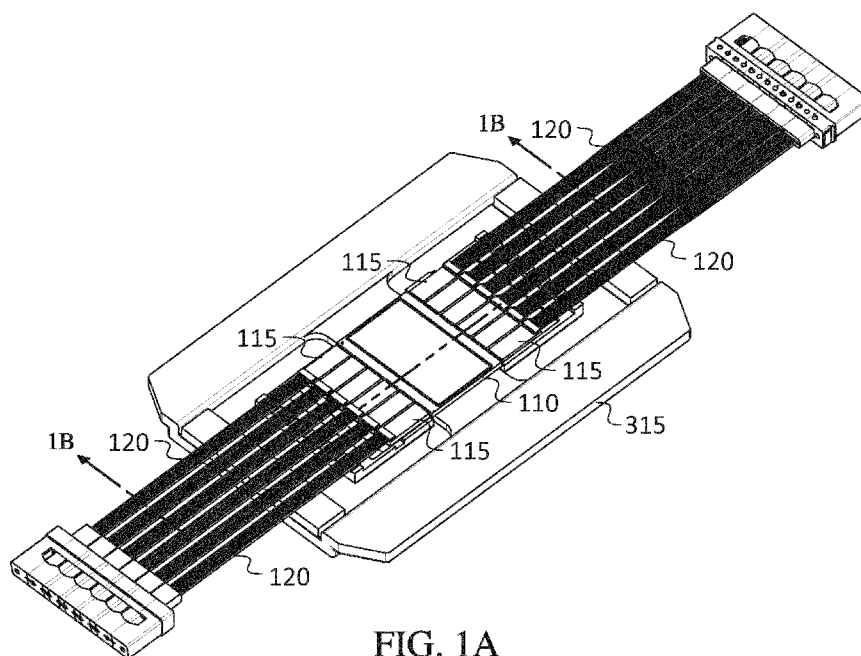


FIG. 1A

(57) Abstract: A system and method for packing optical and electronic components. A module includes an electronic integrated circuit (110) and a plurality of photonic integrated circuits (115), connected to the electronic integrated circuit (110) by wire bonds or by wire bonds and other conductors. A metal cover (315) of the module is in thermal contact with the electronic integrated circuit (110) and facilitates extraction of heat from the electronic integrated circuit (110). Arrays of optical fibers (120) are connected to the photonic integrated circuits (115).



GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,
EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

COPACKAGING OF ASIC AND SILICON PHOTONICS

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] The present application claims priority to and the benefit of U.S. Provisional Application No. 62/443,576, filed January 6, 2017, entitled "COPACKAGING OF ASIC AND SILICON PHOTONICS", the entire content of which is incorporated herein by reference.

FIELD

[0002] One or more aspects of embodiments according to the present invention relate to data processing, and more particularly to a module for performing data processing.

BACKGROUND

[0003] Various design considerations may apply in the design of a module including an electronic integrated circuit (IC) and having optical data ports. Such a module may have a plurality of optical inputs (e.g., optical fibers) for receiving optical data, and a plurality of optical outputs (e.g., optical fibers) for transmitting optical data. Photonic integrated circuits may be used to convert the received optical data to electrical data, the electrical data may be processed by an electronic integrated circuit to form output electrical data, and the output electrical data may be converted to optical data by additional photonic integrated circuits. In the design of the module, it may be advantageous for example (i) to keep power conductors short, to reduce voltage drops (e.g., if the electronic integrated circuit operates at 0.9V), (ii) to provide a path for heat to escape from the electronic integrated circuit, and (iii) to provide a benign temperature range for the photonic integrated circuits.

[0004] Thus, there is a need for a module providing such advantages.

SUMMARY

[0005] Aspects of embodiments of the present disclosure are directed toward a system and method of packaging for electronic and optical components.

[0006] According to an embodiment of the present invention there is provided a module, including: a substrate including a plurality of conductive traces and a first plurality of contacts, each contact being electrically connected to a corresponding conductive trace of the plurality of conductive traces; an electronic integrated circuit having a top surface and a bottom surface, and including: a second plurality of contacts on a first portion of a bottom surface of the electronic integrated circuit; a third plurality of contacts on a second portion of the bottom surface of the electronic integrated circuit; and a fourth plurality of contacts on a third portion of the bottom surface of the electronic integrated circuit, each of the contacts of the second plurality of contacts being vertically aligned with and connected to a corresponding contact of the first plurality of contacts, wherein: the second portion of the bottom surface overhangs a first edge of the substrate, and the third portion of the bottom surface overhangs a second edge of the substrate.

[0007] In one embodiment, each contact of the first plurality of contacts is secured to a contact of the second plurality of contacts with solder; each of the third plurality of contacts is a wire bond pad; and each of the fourth plurality of contacts is a wire bond pad.

[0008] In one embodiment, each of the third plurality of contacts is a wire bond pad, and the module further includes: a first plurality of photonic integrated circuit assemblies, each of the first plurality of photonic integrated circuit assemblies having a wire bond pad adjacent to a contact of the third plurality of contacts; and a plurality of wire bonds, each of the wire bonds connecting a wire bond pad of a photonic integrated circuit assembly of the first plurality of photonic integrated circuit assemblies to a contact of the third plurality of contacts.

[0009] In one embodiment, the module includes: a second plurality of photonic integrated circuit assemblies, each of the second plurality of photonic integrated circuit assemblies having a wire bond pad adjacent to a contact of the fourth plurality of contacts; and a plurality of wire bonds, each of the wire bonds connecting a wire bond pad of a photonic integrated circuit assembly of the second plurality of photonic integrated circuit assemblies to a contact of the fourth plurality of contacts.

[0010] In one embodiment, the module includes: a plurality of photonic integrated circuit assemblies, each of the plurality of photonic integrated circuit assemblies having a wire bond pad adjacent to a contact of the third plurality of contacts, wherein a photonic integrated circuit

assembly of the plurality of photonic integrated circuit assemblies includes: a photonic integrated circuit; and a mode converter adjacent to the photonic integrated circuit and configured to convert between an optical mode of the photonic integrated circuit and an optical mode of an optical fiber, wherein the wire bond pad of the photonic integrated circuit assembly is on the photonic integrated circuit.

[0011] In one embodiment, the substrate is an organic substrate.

[0012] In one embodiment, the substrate has the shape of an H.

[0013] In one embodiment, a contact of the first plurality of contacts is secured to a contact of the second plurality of contacts with a connection selected from the group consisting of a copper pillar and a thermocompression stud bump.

[0014] In one embodiment, the module includes: a plurality of photonic integrated circuit assemblies, each of the plurality of photonic integrated circuit assemblies having a wire bond pad adjacent to a contact of the third plurality of contacts, wherein a photonic integrated circuit assembly of the plurality of photonic integrated circuit assemblies includes: a V-groove block having a V-groove securing an optical fiber; and a photonic integrated circuit including the wire bond pad, wherein the photonic integrated circuit has an optical aperture aligned with the optical fiber, and includes a mode converter configured to convert between an optical mode of the photonic integrated circuit and an optical mode of the optical fiber.

[0015] In one embodiment, the module includes: a plurality of photonic integrated circuits, each of the plurality of photonic integrated circuits having a wire bond pad adjacent to a contact of the third plurality of contacts, wherein a photonic integrated circuit of the plurality of photonic integrated circuits has a V-groove securing an optical fiber.

[0016] In one embodiment, the module includes an upper cover, and having a thermal path, with a thermal resistance of less than $0.1^{\circ}\text{C}/\text{W}$, between the bottom surface of the electronic integrated circuit and an exterior surface of the upper cover.

[0017] In one embodiment, the upper cover includes, on an interior surface of the upper cover, a pedestal, the pedestal being part of the thermal path.

[0018] In one embodiment, the module includes a plurality of photonic integrated circuit assemblies, each of the plurality of photonic integrated circuit assemblies being secured to the upper cover.

[0019] In one embodiment, the photonic integrated circuit assemblies are secured to a carrier, and the carrier is secured to the upper cover.

[0020] In one embodiment, the carrier has a thermal resistance, between any one of the photonic integrated circuit assemblies and the exterior surface of the upper cover, of at least 10°C/W.

[0021] In one embodiment, each of the third plurality of contacts is a wire bond pad; the substrate has an otherwise convex shape with one or more cutouts; a first cutout of the one or more cutouts is over the second portion of the bottom surface of the electronic integrated circuit; and the first cutout is configured to allow the formation of wire bonds to the third plurality of contacts when the electronic integrated circuit is secured to the substrate.

[0022] In one embodiment, the contacts of the first plurality of contacts are on a first surface of the substrate; the substrate further includes a fifth plurality of contacts, on a second surface of the substrate, opposite the first surface of the substrate; and the contacts of the fifth plurality of contacts form a land grid array.

[0023] In one embodiment, the module includes: a plurality of photonic integrated circuit assemblies, each of the plurality of photonic integrated circuit assemblies having a wire bond pad adjacent to a contact of the third plurality of contacts; a first heater, in thermal contact with a first photonic integrated circuit of a photonic integrated circuit assembly of the plurality of photonic integrated circuit assemblies; and a temperature sensor, in thermal contact with the first photonic integrated circuit.

[0024] In one embodiment, the module includes: a plurality of photonic integrated circuit assemblies, each of the plurality of photonic integrated circuit assemblies having a wire bond pad adjacent to a contact of the third plurality of contacts; a first heater, integral with a first photonic integrated circuit of a photonic integrated circuit assembly of the plurality of photonic integrated circuit assemblies; and a temperature sensor, integral with the first photonic integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] These and other features and advantages of the present invention will be appreciated and understood with reference to the specification, claims, and appended drawings wherein:

[0026] FIG. 1A is a perspective view of a portion of a module, according to an embodiment of the present invention;

[0027] FIG. 1B is a cross-sectional view of a module, according to an embodiment of the present invention;

[0028] FIG. 2A is a perspective view of a portion of a module, according to an embodiment of the present invention;

[0029] FIG. 2B is a cross-sectional view of a module, according to an embodiment of the present invention;

[0030] FIG. 3A is a perspective view of a portion of a module, according to an embodiment of the present invention;

[0031] FIG. 3B is a cross-sectional view of a module, according to an embodiment of the present invention;

[0032] FIG. 4 is a perspective view of a portion of a module, according to an embodiment of the present invention;

[0033] FIG. 5 is a perspective view of a portion of a module, according to an embodiment of the present invention;

[0034] FIG. 6 is a cross-sectional view of a portion of a module, according to an embodiment of the present invention;

[0035] FIG. 7A is a perspective view of a module, according to an embodiment of the present invention;

[0036] FIG. 7B is a perspective view of a module, according to an embodiment of the present invention;

[0037] FIG. 8 is a perspective view of a portion of a module, according to an embodiment of the present invention;

[0038] FIG. 9A is a perspective view of a substrate, according to an embodiment of the present invention;

- [0039] FIG. 9B is a perspective view of an electronic integrated circuit, according to an embodiment of the present invention;
- [0040] FIG. 9C is an enlarged perspective view of a portion of an electronic integrated circuit, according to an embodiment of the present invention;
- [0041] FIG. 9D is a perspective view of an electronic integrated circuit on a substrate, according to an embodiment of the present invention;
- [0042] FIG. 10A is a perspective view of a cover, according to an embodiment of the present invention;
- [0043] FIG. 10B is a perspective view of a cover, according to an embodiment of the present invention;
- [0044] FIG. 10C is a perspective view of a portion of a module, according to an embodiment of the present invention;
- [0045] FIG. 11A is a perspective view of a portion of a module, according to an embodiment of the present invention;
- [0046] FIG. 11B is an enlarged perspective view of a portion of a module, according to an embodiment of the present invention;
- [0047] FIG. 12A is a perspective view of a portion of a photonic integrated circuit subassembly, according to an embodiment of the present invention;
- [0048] FIG. 12B is a perspective view of a photonic integrated circuit, according to an embodiment of the present invention;
- [0049] FIG. 12C is a perspective view of a reinforcing block, according to an embodiment of the present invention;
- [0050] FIG. 12D is a perspective view of a photonic integrated circuit subassembly, according to an embodiment of the present invention;
- [0051] FIG. 13A is a perspective view of a photonic integrated circuit subassembly, according to an embodiment of the present invention;
- [0052] FIG. 13B is a perspective view of a subcarrier, according to an embodiment of the present invention;

[0053] FIG. 13C is a perspective view of a subcarrier with a plurality of photonic integrated circuit subassemblies, according to an embodiment of the present invention;

[0054] FIG. 14A is a perspective view of a strain relief, according to an embodiment of the present invention;

[0055] FIG. 14B is a perspective view of a portion of a module, according to an embodiment of the present invention;

[0056] FIG. 15A is a perspective view of a portion of a module, according to an embodiment of the present invention;

[0057] FIG. 15B is an enlarged perspective view of a portion of a module, according to an embodiment of the present invention;

[0058] FIG. 16A is a perspective view of a strain relief, according to an embodiment of the present invention;

[0059] FIG. 16B is a perspective view of a cover, according to an embodiment of the present invention;

[0060] FIG. 16C is a perspective view of a portion of a module, according to an embodiment of the present invention;

[0061] FIG. 16D is a perspective view of a module, according to an embodiment of the present invention;

[0062] FIG. 17 is a perspective view of a module, according to an embodiment of the present invention;

[0063] FIG. 18 is a cutaway perspective view of a portion of a module, according to an embodiment of the present invention;

[0064] FIG. 19 is an enlarged perspective view of a portion of a module, according to an embodiment of the present invention;

[0065] FIG. 20A is a perspective view of a module, according to an embodiment of the present invention;

[0066] FIG. 20B is a perspective view of a portion of a module, according to an embodiment of the present invention;

[0067] FIG. 21A is a perspective view of a module, according to an embodiment of the present invention;

[0068] FIG. 21B is a perspective view of a portion of a module, according to an embodiment of the present invention;

[0069] FIG. 22A is a perspective view of a portion of a module, according to an embodiment of the present invention;

[0070] FIG. 22B is a perspective view of a module, according to an embodiment of the present invention;

[0071] FIG. 22C is a perspective view of a module, according to an embodiment of the present invention;

[0072] FIG. 22D is a perspective view of an electronic integrated circuit on a substrate, according to an embodiment of the present invention; and

[0073] FIG. 23 is an enlarged perspective view of a portion of a module, according to an embodiment of the present invention.

[0074] FIGs. 1A, 2A, 3A, 4, 5, and 7-23 are to drawn to scale, for a plurality of respective embodiments.

DETAILED DESCRIPTION

[0075] The detailed description set forth below in connection with the appended drawings is intended as a description of exemplary embodiments of a module including an electronic integrated circuit and having optical data ports provided in accordance with the present invention and is not intended to represent the only forms in which the present invention may be constructed or utilized. The description sets forth the features of the present invention in connection with the illustrated embodiments. It is to be understood, however, that the same or equivalent functions and structures may be accomplished by different embodiments that are also intended to be encompassed within the spirit and scope of the invention. As denoted elsewhere herein, like element numbers are intended to indicate like elements or features.

[0076] FIG. 1A shows an opto-electronic module including an electronic integrated circuit 110 (which may be an application specific integrated circuit (ASIC), and which may be a

complementary metal oxide (CMOS) ASIC), and a plurality of photonic integrated circuits (PICs) 115. The photonic integrated circuits 115 are arranged along two opposite edges of the electronic integrated circuit 110, which is substantially rectangular (e.g., it may be rectangular, or it may have the shape of a rectangle with a truncated corner). An array of fibers 120 (i.e., optical fibers) is connected to each of the photonic integrated circuits 115. The fibers 120 may carry high speed digital data (at data rates of more than 1 gigabit/second (Gb/s) per fiber, e.g., at a rate of 25 Gb/s per fiber, net of overhead such as error correcting coding). The photonic integrated circuits 115 may operate as transceivers, converting optically transported digital data to electrical digital data at similar data rates or the same data rates, or vice versa. Accordingly the electronic integrated circuit 110 may have one or more arrays of high-speed electrical connections (e.g., an array of such connections along each of the two opposite edges of the electronic integrated circuit 110 along which the photonic integrated circuits 115 are arranged). The electronic integrated circuit 110 may further have power connections and low-speed input/output (I/O) connections that may be employed, for example, to provide power to the electronic integrated circuit 110 and to set control registers in the electronic integrated circuit 110, respectively. The electronic integrated circuit 110 may be a bare die, i.e., it may not be separately encapsulated in a package (e.g., a plastic package).

[0077] FIG. 1B shows an enlarged view of a central portion of a cross section taken along the cutting plane 1B-1B shown in FIG. 1A. The embodiment of FIG. 1A is not identical to that of FIG. 1B, but it shows the orientation of the cutting plane used to form FIG. 1B, with respect to the electronic integrated circuit 110, the plurality of photonic integrated circuits 115, and the arrays of fibers 120. Referring to FIG. 1B, in one embodiment the electronic integrated circuit 110 has through silicon vias (TSVs) 117. Power connections and low-speed input/output connections are routed through the TSVs 117, and through a main substrate 125 (which may be a ceramic substrate) to a land grid array (LGA) on the lower surface of the main substrate 125. The main substrate 125 may have an array of solder pads arranged on a relatively fine grid e.g. 150 um to form the contact to the integrated circuit 110. From the solder pad array, the connections may be further routed through the substrate 125 to a land grid array on a relatively coarse pitch of, e.g., 800 microns. An electrical interposer 130 may be used to connect to a host printed circuit board (PCB) 150 (not shown in FIG. 1A). The electrical interposer 130 may be a contact array with compliant contacts

capable of forming an electrical contact with features such as those of the land grid array, while absorbing mechanical tolerances inherent in this type of assembly and not requiring that the opto-electronic module be exposed to high temperatures (as soldering the module directly to the PCB 150 would). The host printed circuit board 150 may be fabricated using a lower-cost process not capable of forming fine pitch features. A heat sink 155 may be employed to remove heat from the electronic integrated circuit 110, through a compliant thermal pad 157 between the heat sink 155 and the integrated circuit 110.

[0078] The photonic integrated circuits 115 are connected to the electronic integrated circuit 110 by wire bonds 160, which are bonded to wire bond pads on the photonic integrated circuits 115 and on the face of the electronic integrated circuit 110. As used herein, the “face” or “bottom surface” of the electronic integrated circuit 110 (which, in the view of FIG. 1B, faces up) is a surface having a plurality of contacts (e.g., wire bond pads) for forming connections to photonic integrated circuits 115. Each fiber of each array of fibers 120 may be connected to a respective photonic integrated circuit 115 through a beam expander 140, which may be, for example, a tapered waveguide of an array of tapered waveguides on a silicon chip. The same silicon chip may include an array of V-grooves, each configured to receive and align a fiber to the wide end of a respective tapered waveguide. The fibers may be held in place in the array of V-grooves by a block referred to herein as a glass lid 145. The glass lid 145 may be composed of glass; in other embodiments a similar lid composed of a suitable polymer is used instead, to similar effect. The beam expander 140 is configured to transform light propagating with a first, generally smaller, transverse mode to light propagating with a second, generally larger, transverse mode. Although it is referred to herein as a beam “expander”, the beam expander 140 may equally well be employed, for light travelling in the opposite direction through it, to transform light propagating with the second, generally larger, transverse mode to light propagating with the first, generally smaller, transverse mode. The beam expander 140 may also be referred to as a “mode converter”. In some embodiments (such as the embodiment illustrated, for example, in FIG. 1A) the V-grooves and beam expanders 140 are integrated into the photonic integrated circuits 115.

[0079] FIG. 2A shows, like FIG. 1A, an opto-electronic module including an electronic integrated circuit 110, and a plurality of photonic integrated circuits 115, each connected to an

array of fibers 120. FIG. 2B shows an enlarged view of a central portion of a cross section taken along the cutting plane 2B-2B shown in FIG. 2A. The embodiment of FIG. 2A is not identical to that of FIG. 2B, but it shows the orientation of the cutting plane used to form FIG. 2B, with respect to the electronic integrated circuit 110, the plurality of photonic integrated circuits 115, and the arrays of fibers 120. In some embodiments (e.g., when the electronic integrated circuit 110 does not have through silicon vias 117), contacts for power and low-speed input/output connections to the electronic integrated circuit 110 may be on the face, or bottom surface, of the electronic integrated circuit 110. In the embodiment of FIG. 2B, a power distribution substrate 205 is connected to the face of the electronic integrated circuit (e.g., by a ball grid array (BGA)), to provide power connections and low-speed input/output (I/O) connections without using TSVs. A heat sink 155 is employed to remove heat from the electronic integrated circuit 110, through the balls of the ball grid array, through the power distribution substrate 205, and through the compliant thermal pad 157. Because the cutting plane used to generate the cross-sectional view of FIG. 2B does not pass through certain elements such as the photonic integrated circuits 115 and the fibers 120, these elements are not visible in FIG. 2B. These elements may be secured in place, and connected together and to the electronic integrated circuit 110, in a manner similar to that shown in FIGs. 1A and 1B.

[0080] FIG. 3A shows, like FIG. 1A, an opto-electronic module including an electronic integrated circuit 110, and a plurality of photonic integrated circuits 115, each connected to an array of fibers 120. FIG. 3B shows an enlarged view of a central portion of a cross section taken along the cutting plane 3B-3B shown in FIG. 3A. The embodiment of FIG. 3A is not identical to that of FIG. 3B, but it shows the orientation of the cutting plane used to form FIG. 1B, with respect to the electronic integrated circuit 110, the plurality of photonic integrated circuits 115, and the arrays of fibers 120.

[0081] In one embodiment, the main substrate 125 has a first plurality of contacts on an upper surface adjacent to a bottom surface of the electronic integrated circuit 110. The main substrate 125 includes a plurality of conductive traces 305 (e.g., printed circuit board traces) and vias 118 and is configured to provide power connections and low-speed input/output (I/O) connections to the electronic integrated circuit through a second plurality of contacts, on the bottom surface of the

electronic integrated circuit (labeled “CMOS chip”), each of which is aligned with, and connected to (e.g., soldered to), a corresponding contact of the first plurality of contacts. In FIG. 3B, the solder contacts are shown schematically as solder balls in the shape they may have before a reflow operation. Wire bonds 160 connect the electronic integrated circuit 110 to photonic integrated circuits 115. A metal cover 315 with a heat sink 155 may be in thermal contact, through a thermal pad 157 (which, as illustrated in FIG. 3B, is too thin to be visible as a separate element), with a surface of the electronic integrated circuit 110. Supports 116 may be used to secure the beam expanders 140 (through the glass lids 145) to the metal cover 315. The opto-electronic module may have a heat transfer surface, e.g., a surface through which heat may be removed from the opto-electronic module (e.g., the upper surface of the metal cover 315, in the view of FIG. 3B). The opto-electronic module may have a high thermal conductivity thermal path from the electronic integrated circuit 110 to the heat transfer surface, so that heat may be extracted from the electronic integrated circuit 110 through the heat transfer surface. In such an embodiment, a separate heat sink 155 may be secured to the heat transfer surface to remove heat from the opto-electronic module (as shown in FIG. 3B), or heat may be removed from the heat transfer surface in some other manner (e.g., using a heat pipe). In some embodiments, the opto-electronic module includes a plurality of heat transfer surfaces.

[0082] Referring to FIG. 4, in an embodiment (such as the embodiment of FIG. 3B) in which the electronic integrated circuit 110 faces the main substrate 125, cutouts 410 may be provided in the substrate to allow wire bonds to be formed after the electronic integrated circuit is soldered to the substrate. The substrate may be an organic substrate (e.g., a reinforced organic polymer, such as fiberglass reinforced epoxy). The main substrate 125 has a shape that has the two oblong cutouts 410 and six circular cutouts 415 and is otherwise convex (being a rectangle with truncated corners).

[0083] Referring to FIG. 5, in some embodiments, the main substrate 125 is in the shape of an “H”, providing access for forming wire bonds 160, and also providing access for installing the photonic integrated circuits 115 after the substrate and electronic integrated circuit 110 have been assembled with the metal cover. This shape makes it unnecessary for the main substrate 125 to have a step in thickness, which in the embodiment of FIG. 3B provides space for beam expanders 140. An H shape may be formed by forming two rectangular cutouts 510 (FIG. 9A) in an otherwise

convex rectangular shape (or, in the case of the embodiment of FIG. 5, a shape that further has two semicircular cutouts 525). One or more land grid arrays 515 of contacts on the bottom surface of the substrate may be used to form connections to a host printed circuit board; in other embodiments a pin grid array may be used instead. A plurality of decoupling capacitors 520 (e.g., surface mount power supply decoupling capacitors for the electronic integrated circuit 110) may be arranged on the bottom surface of the main substrate 125. Heaters 505 may be used to control the temperature of the photonic integrated circuits 115, as discussed in further detail below.

[0084] Referring to FIG. 6, in some embodiments, the temperature of a photonic integrated circuit 115 may be controlled using one or more flex sensors 605 on one side of the photonic integrated circuit (labelled “Si”), and one or more flex heaters 610 on the other side. A layer of insulating material 615 (e.g., FR4) may be provided between the sandwich (the sandwich including the flex sensor 605, the photonic integrated circuit 115, and the flex heater 610) and the heat sink 155, so that the heater may be capable of maintaining a temperature difference between the heat sink and the photonic integrated circuit 115. The sandwich may be potted in an encapsulation material 620. Such a system may be used when the photonic integrated circuit is sufficiently temperature sensitive that coarser temperature control (e.g., controlling the temperature of the heat sink using a fan) is not sufficient. In some embodiments, temperature control may be provided using instead one or more temperature sensors and one or more heaters that are integral with the photonic integrated circuit (e.g., the temperature sensor and heater are silicon devices fabricated directly on or in the photonic integrated circuit, and form a part of the photonic integrated circuit). In other embodiments, the temperature sensor may be a discrete component mounted on the flex circuit.

[0085] Referring to FIGs. 7A and 7B, in one embodiment, the metal cover 315, or “metal lid” is secured to one surface (e.g., the upper surface) of the main substrate 125 (FIG. 7A), and a “bottom cover” 705 is secured to the opposite (bottom) surface of the substrate (FIG. 7B).

[0086] Referring to FIG. 8 (showing the module with the bottom cover removed), a plurality of photonic integrated circuits 115 are mounted in a carrier (or “subcarrier”) 805 (illustrated in further detail in FIG. 13B), on each side of the electronic integrated circuit 110. The photonic integrated circuits 115 on one side of the electronic integrated circuit 110 may include input photonic

integrated circuits 115 (e.g., photonic integrated circuits configured to convert optical data to electrical data) and the photonic integrated circuits 115 on the other side (e.g., the opposite side) of the electronic integrated circuit 110 may include output photonic integrated circuits 115 (e.g., photonic integrated circuits configured to convert electrical data to optical data). In other embodiments, the plurality of photonic integrated circuits 115 on one side (or on both sides) of the electronic integrated circuit 110 may include both input photonic integrated circuits 115 and output photonic integrated circuits 115, or some of the photonic integrated circuits 115 may be configured to perform both input and output functions. The fibers are secured to the subcarriers, for further strain relief, at fiber anchoring points 810, at which the fibers cross, and are bonded (e.g., with epoxy) to rails 1310 (FIG. 13B) on the respective subcarriers 805.

[0087] FIG. 9A shows the main substrate 125. FIG. 9B is a perspective face-up view of the electronic integrated circuit 110, and FIG. 9C is an enlarged perspective view of a portion, identified by a dashed rectangle labeled “9C”, of FIG. 9B. FIG. 9C shows both flip chip solder bumps 905 (through which the electronic integrated circuit 110 may be connected and secured to the main substrate 125) and wire bond pads 910 (through which the electronic integrated circuit 110 may be connected to the photonic integrated circuits 115). For simplicity, only two rows of solder bumps 905 are shown, other embodiments may have a full or partial 2D array of bumps. During assembly, the electronic integrated circuit may be soldered to the substrate, e.g., using a reflow process. In some embodiments, the electronic integrated circuit 110 is connected to the substrate by another method (e.g., using copper pillars, thermocompression stud bumps, a land grid array or a pin grid array instead of solder bumps). If the method employed to connect the electronic integrated circuit 110 to the main substrate 125 does not include soldering the electronic integrated circuit 110 to the main substrate 125, the electronic integrated circuit 110 may be clamped to the main substrate 125 by the metal cover 315. FIG. 9D shows the subassembly formed by securing the electronic integrated circuit 110 to the main substrate 125. The portions of the bottom surface of the electronic integrated circuit 110 that have the wire bond pads 910 (e.g., areas of the bottom surface along two opposite edges of the electronic integrated circuit 110) may overhang the main substrate 125 (e.g., may overhang two corresponding edges of the main substrate 125) as shown, so that the wire bond pads may be exposed, when viewed from below.

[0088] FIGs. 10A – 10C show the metal cover (or “copper cover”, or “copper lid”, or “upper cover”) in one embodiment. Referring to FIG. 10B, the metal cover 315 may have two walls 1010 and two flanges 1015, and a pedestal 1020 on its bottom surface for making thermal contact with the upper surface of the electronic integrated circuit 110. The pedestal may extend all the way across the metal cover 315, between the two walls 1010 as shown, or it may be smaller (e.g., it may have a rectangular shape of a size similar to that of the top surface of the electronic integrated circuit 110). In some embodiments the pedestal is absent. A thermal interface material (TIM) (e.g., forming a thermal pad 157 as illustrated in FIG. 1B) may be used between the surface of the pedestal (or the bottom surface of the metal cover, if the pedestal is absent) and the upper surface of the electronic integrated circuit. In some embodiments the thermal resistance from the electronic integrated circuit die to the outer surface of the metal cover may be $0.1^{\circ}\text{C}/\text{W}$, or between $0.1^{\circ}\text{C}/\text{W}$ and $0.01^{\circ}\text{C}/\text{W}$, or less than $0.01^{\circ}\text{C}/\text{W}$. As illustrated in FIG. 10C, the two flanges 1015 may be close to the upper surface of the main substrate 125 when the metal cover is installed on the electronic integrated circuit. Gaps between the substrate and respective flanges may be filled with a suitable bonding agent (e.g., epoxy), to secure the metal cover to the substrate.

[0089] FIG. 11A is a bottom view of the subassembly including the electronic integrated circuit, the substrate, and the metal cover, showing the overhang mentioned above, and mounting areas for photonics assemblies 1320 (FIG. 13C; described in further detail below). FIG. 11B is an enlarged perspective view of a portion, identified by a dashed rectangle labeled “11B”, of FIG. 11A.

[0090] In some embodiments, as mentioned above, silicon chips including beam expanders 140 and V-grooves for aligning the fibers may be used with the photonic integrated circuits 115 (instead of integrating these features into the photonic integrated circuits 115 as illustrated, for example, in FIGs. 1A, 2A, 3A, and 8). Referring to FIGs. 12A-D, in other embodiments the V-grooves and the beam expanders 140 may be fabricated in separate parts, referred to as V-groove blocks 1210. Each V-groove block 1210 may be assembled with an array of fibers 120, a glass lid 145, a photonic integrated circuit 115 (FIG. 12B) and a reinforcing block 1215 (FIG. 12C) to form a subassembly 1220, shown in FIG. 12D, and referred to herein as a “PIC subassembly” 1220. The assembly procedure for fabricating a PIC subassembly may include actively aligning the set of

fibers (e.g., the set of five fibers) to corresponding optical apertures (e.g., optical input and/or output apertures) of the photonic integrated circuit, and securing together the fibers, the V-groove block 1210, the glass lid 145, and the reinforcing block 1215, e.g., with epoxy. Each PIC subassembly 1220 may be a testable subassembly and may be tested before being incorporated into a module.

[0091] Referring to FIG. 13A, in another embodiment a PIC subassembly 1220 includes an array of fibers 120, a photonic integrated circuit 115, and a glass lid 145. Such a PIC subassembly 1220 may perform similar functions to those of the PIC subassembly 1220 illustrated in FIG. 12D. The photonic integrated circuit 115 of FIG. 13A may include an integral V-groove array and an integral array of beam expanders 140, as well as other optical and/or electrical functions. For example, the photonic integrated circuit 115 of FIG. 13A may convert optical signals to electrical signals (e.g., using photodetectors) or it may convert electrical signals to optical signals (e.g., by receiving unmodulated light on a plurality of input fibers, and modulating the light with the electrical signals, using an array of modulators, to generate modulated light transmitted on a plurality of output fibers).

[0092] A subcarrier (or “carrier” or “sub carrier”) 805 (FIG. 13B) may be used to secure together a plurality of PIC subassemblies 1220 (e.g., six PIC subassemblies 1220), forming assemblies referred to herein as “photonics assemblies” 1320 (FIG. 13C). The subcarrier 805 may be composed of a material having a suitably low coefficient of thermal expansion and suitable thermal conductivity, e.g., copper tungsten, or a plastic or other polymer. The carrier material may have a thermal conductivity of, e.g., 160 W/m/K, for an embodiment without heaters. If heaters are included, the thermal conductivity may be reduced, e.g., to 0.25 W/m/K, to improve the heating efficiency. Materials with intermediate values of thermal conductivity may be selected to provide the optimum combination of heating efficiency and thermal time constant. The PIC subassemblies 1220 may be secured to the subcarrier 805 with a suitable bonding agent (e.g., epoxy).

[0093] Referring to FIGs. 14A and 14B, an upper strain relief 1410 (FIG. 14A) may be bonded into each of two locations in the metal cover 315 to form the subassembly shown in FIG. 14B, which includes the main substrate 125, the electronic integrated circuit 110, the metal cover 315, and two upper strain reliefs 1410 as shown. In some embodiments the surface of each upper strain

relief 1410 that abuts against the fibers 120 is flat as shown; in other embodiments it may have a shallow channel for each array of fibers 120 to constrain the array of fibers 120 laterally. A suitable bonding agent, e.g., a silicone elastomer, may be used. Two photonics assemblies 1320 may then be bonded (e.g., using a suitable epoxy) to respective mounting areas, on the bottom surface of the metal cover 315, and the photonic integrated circuits 115 may be wire bonded to the electronic integrated circuit 110 to form the subassembly illustrated in FIG. 15A. FIG. 15B is an enlarged perspective view of a portion, identified by a dashed rectangle labeled "15B", of FIG. 15A. FIG. 15B shows the set of wire bonds 160 connecting one of the photonic integrated circuits 115 to the electronic integrated circuit 110, and it shows the access (for forming the wire bonds 160) that the cutout 510 in the main substrate 125 provides to the region in which the wire bonds 160 are formed.

[0094] FIG. 16A shows a lower strain relief 1610. Like the upper strain reliefs 1410, the surface of the lower strain relief 1610 that abuts against the fibers 120 is flat as shown; in other embodiments it may have a shallow channel for each array of fibers 120. FIG. 16B shows a top perspective view of the bottom cover 705. The top surface of the bottom cover 705 may have a pocket 1620 to provide clearance for the decoupling capacitors 520, or other components such as a flex circuit to provide electrical power to the heaters and sensors.

[0095] FIG. 16C shows a subassembly that results from the installation of a lower strain relief 1610 in each of two places; each of these may be bonded to a corresponding upper strain relief, and to the fibers, with a suitable bonding agent, e.g., a silicone elastomer. FIG. 16D shows a completed assembly, after installation of the bottom cover 705, which may be bonded to the two lower strain reliefs, also with a suitable bonding agent, e.g., a silicone elastomer. The installation and bonding of the lower strain reliefs 1610 and of the bottom cover 705 may be performed in one step, using the same bonding agent. The bottom cover 705 may include bosses configured to fit into the cutouts in the substrate to facilitate alignment during this assembly step. FIG. 17 shows a bottom view of the complete module, with the bottom cover illustrated as being transparent, allowing certain interior features of the module to be visible.

[0096] FIG. 18 shows a cutaway perspective view of a complete module including an electronic integrated circuit 110 and having optical data ports, with a cutting plane offset from the

center of the module. FIG. 19 shows an embodiment in which the electronic integrated circuit 110 is flip-chip mounted on the main substrate 125 (e.g., using copper pillars), and traces 1910 on the main substrate 125 form connections between high-speed electrical contacts of the electronic integrated circuit 110 and corresponding wire bond pads on the main substrate 125. Two pockets are formed in (e.g., milled into) the main substrate 125 for the photonics assemblies 1320, which are then bonded into the pockets. Wire bonds 160 are used to connect the wire bond pads on the photonic integrated circuits 115 to the traces 1910 on the main substrate 125.

[0097] In another embodiment, illustrated in FIGs. 20A and 20B, a rectangular main substrate 125 is secured (e.g., soldered) to the electronic integrated circuit 110 and bonded to the metal cover 315. Wire bonds 160 are formed between the wire bond pads on the photonic integrated circuits 115 and the wire bond pads on the electronic integrated circuit 110. A cover (e.g., a two-piece reinforced plastic cover 2020, as shown in FIG. 20A) may then be bonded to the metal cover, along with upper and lower strain reliefs, to seal the module. FIG. 21 A shows an embodiment in which each of the main substrate 125 and the bottom cover 705 has the shape of an H, and FIG. 21B shows an interior view of such an embodiment.

[0098] In another embodiment, illustrated in FIG. 22A, (in a manner similar to that of the embodiment of FIG. 19) the electronic integrated circuit is flip-chip mounted on the main substrate 125 (e.g., using copper pillars), and traces on the main substrate 125 form connections between high-speed contacts of the electronic integrated circuit 110 and corresponding wire bond pads on the main substrate 125. The main substrate 125 and the photonics assemblies are bonded to the upper surface of a (e.g., molded liquid crystal polymer plastic) bottom cover 2210. Wire bonds 160 are used to connect the wire bond pads on the photonic integrated circuits to the traces on the main substrate 125. In some embodiments the bottom cover 2210 is molded to include the features of subcarriers 805 (e.g., pockets for photonic integrated circuits 115, and anchor points) so that the photonic integrated circuits 115 are bonded directly to the bottom cover and separate subcarriers are not used. Flex circuits 2215 may be employed to carry drive current from the main substrate 125 to the heaters 505. Once otherwise assembled, the subassembly of FIG. 22A may be covered with a flat metal lid 2220 to form the assembly of FIG. 22B. FIG. 22C shows a bottom view of such an embodiment, and FIG. 22D shows a subassembly, including an electronic integrated circuit

110 secured and connected to a main substrate 125, which may be fabricated as part of the fabrication process of such an embodiment.

[0099] FIG. 23 is an enlarged view of a portion of FIG. 16C. As mentioned above, in this embodiment, each of the photonic integrated circuits 115 includes V-grooves, and a separate V-groove block and a reinforcing block are not used. Instead the fiber ends are placed in the V-grooves of the photonic integrated circuit 115, clamped and bonded in place with, e.g., a glass lid 145 (or with a polymer lid) and epoxy. In such an embodiment, the fibers may be placed and bonded into the V-grooves either before or after connections are made to the photonic integrated circuit.

[00100] As used herein, a “photonic chip” is any part consisting of a substrate having an upper surface, and layers, features, and/or devices, including at least one optical waveguide, fabricated in the upper layers of the substrate. Spatially relative terms, such as “beneath”, “below”, “lower”, “under”, “above”, “upper” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that such spatially relative terms are intended to encompass different orientations of the device in use or in operation, in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as “below” or “beneath” or “under” other elements or features would then be oriented “above” the other elements or features. Thus, the example terms “below” and “under” can encompass both an orientation of above and below. The device may be otherwise oriented (e.g., rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein should be interpreted accordingly. In addition, it will also be understood that when a layer is referred to as being “between” two layers, it can be the only layer between the two layers, or one or more intervening layers may also be present.

[00101] Although exemplary embodiments of a module including an electronic integrated circuit and having optical data ports have been specifically described and illustrated herein, many modifications and variations will be apparent to those skilled in the art. Accordingly, it is to be understood that a module including an electronic integrated circuit and having optical data ports

constructed according to principles of this invention may be embodied other than as specifically described herein. The invention is also defined in the following claims, and equivalents thereof.

WHAT IS CLAIMED IS:

1. A module, comprising:

a substrate comprising a plurality of conductive traces and a first plurality of contacts, each contact being electrically connected to a corresponding conductive trace of the plurality of conductive traces;

an electronic integrated circuit having a top surface and a bottom surface, and comprising:

a second plurality of contacts on a first portion of a bottom surface of the electronic integrated circuit;

a third plurality of contacts on a second portion of the bottom surface of the electronic integrated circuit; and

a fourth plurality of contacts on a third portion of the bottom surface of the electronic integrated circuit,

each of the contacts of the second plurality of contacts being vertically aligned with and connected to a corresponding contact of the first plurality of contacts,

wherein:

the second portion of the bottom surface overhangs a first edge of the substrate, and

the third portion of the bottom surface overhangs a second edge of the substrate.

2. The module of claim 1, wherein:

each contact of the first plurality of contacts is secured to a contact of the second plurality of contacts with solder;

each of the third plurality of contacts is a wire bond pad; and

each of the fourth plurality of contacts is a wire bond pad.

3. The module of claim 1, wherein each of the third plurality of contacts is a wire bond pad, and the module further comprises:

a first plurality of photonic integrated circuit assemblies, each of the first plurality of photonic integrated circuit assemblies having a wire bond pad adjacent to a contact of the third plurality of contacts; and

a plurality of wire bonds, each of the wire bonds connecting a wire bond pad of a photonic integrated circuit assembly of the first plurality of photonic integrated circuit assemblies to a contact of the third plurality of contacts.

4. The module of claim 3, further comprising:

a second plurality of photonic integrated circuit assemblies, each of the second plurality of photonic integrated circuit assemblies having a wire bond pad adjacent to a contact of the fourth plurality of contacts; and

a plurality of wire bonds, each of the wire bonds connecting a wire bond pad of a photonic integrated circuit assembly of the second plurality of photonic integrated circuit assemblies to a contact of the fourth plurality of contacts.

5. The module of claim 1, further comprising:

a plurality of photonic integrated circuit assemblies, each of the plurality of photonic integrated circuit assemblies having a wire bond pad adjacent to a contact of the third plurality of contacts,

wherein a photonic integrated circuit assembly of the plurality of photonic integrated circuit assemblies comprises:

a photonic integrated circuit; and

a mode converter adjacent to the photonic integrated circuit and configured to convert between an optical mode of the photonic integrated circuit and an optical mode of an optical fiber,

wherein the wire bond pad of the photonic integrated circuit assembly is on the photonic integrated circuit.

6. The module of claim 1, wherein the substrate is an organic substrate.

7. The module of claim 1, wherein the substrate has the shape of an H.

8. The module of claim 1, wherein a contact of the first plurality of contacts is secured to a contact of the second plurality of contacts with a connection selected from the group consisting of a copper pillar and a thermocompression stud bump.

9. The module of claim 1, further comprising:
a plurality of photonic integrated circuit assemblies, each of the plurality of photonic integrated circuit assemblies having a wire bond pad adjacent to a contact of the third plurality of contacts,
wherein a photonic integrated circuit assembly of the plurality of photonic integrated circuit assemblies comprises:
a V-groove block having a V-groove securing an optical fiber; and
a photonic integrated circuit comprising the wire bond pad,
wherein the photonic integrated circuit has an optical aperture aligned with the optical fiber, and comprises a mode converter configured to convert between an optical mode of the photonic integrated circuit and an optical mode of the optical fiber.

10. The module of claim 1, further comprising:
a plurality of photonic integrated circuits, each of the plurality of photonic integrated circuits having a wire bond pad adjacent to a contact of the third plurality of contacts,
wherein a photonic integrated circuit of the plurality of photonic integrated circuits has a V-groove securing an optical fiber.

11. The module of claim 1, further comprising an upper cover, and having a thermal path, with a thermal resistance of less than $0.1^{\circ}\text{C}/\text{W}$, between the bottom surface of the electronic integrated circuit and an exterior surface of the upper cover.

12. The module of claim 11, wherein the upper cover comprises, on an interior surface of the upper cover, a pedestal, the pedestal being part of the thermal path.

13. The module of claim 11, further comprising a plurality of photonic integrated circuit assemblies, each of the plurality of photonic integrated circuit assemblies being secured to the upper cover.

14. The module of claim 13, wherein the photonic integrated circuit assemblies are secured to a carrier, and the carrier is secured to the upper cover.

15. The module of claim 14, wherein the carrier has a thermal resistance, between any one of the photonic integrated circuit assemblies and the exterior surface of the upper cover, of at least 10°C/W.

16. The module of claim 1, wherein:
each of the third plurality of contacts is a wire bond pad;
the substrate has an otherwise convex shape with one or more cutouts;
a first cutout of the one or more cutouts is over the second portion of the bottom surface of the electronic integrated circuit; and
the first cutout is configured to allow the formation of wire bonds to the third plurality of contacts when the electronic integrated circuit is secured to the substrate.

17. The module of claim 1, wherein:
the contacts of the first plurality of contacts are on a first surface of the substrate;
the substrate further comprises a fifth plurality of contacts, on a second surface of the substrate, opposite the first surface of the substrate; and
the contacts of the fifth plurality of contacts form a land grid array.

18. The module of claim 1, further comprising:
a plurality of photonic integrated circuit assemblies, each of the plurality of photonic integrated circuit assemblies having a wire bond pad adjacent to a contact of the third plurality of contacts;

a first heater, in thermal contact with a first photonic integrated circuit of a photonic integrated circuit assembly of the plurality of photonic integrated circuit assemblies; and
a temperature sensor, in thermal contact with the first photonic integrated circuit.

19. The module of claim 1, further comprising:

a plurality of photonic integrated circuit assemblies, each of the plurality of photonic integrated circuit assemblies having a wire bond pad adjacent to a contact of the third plurality of contacts;

a first heater, integral with a first photonic integrated circuit of a photonic integrated circuit assembly of the plurality of photonic integrated circuit assemblies; and
a temperature sensor, integral with the first photonic integrated circuit.

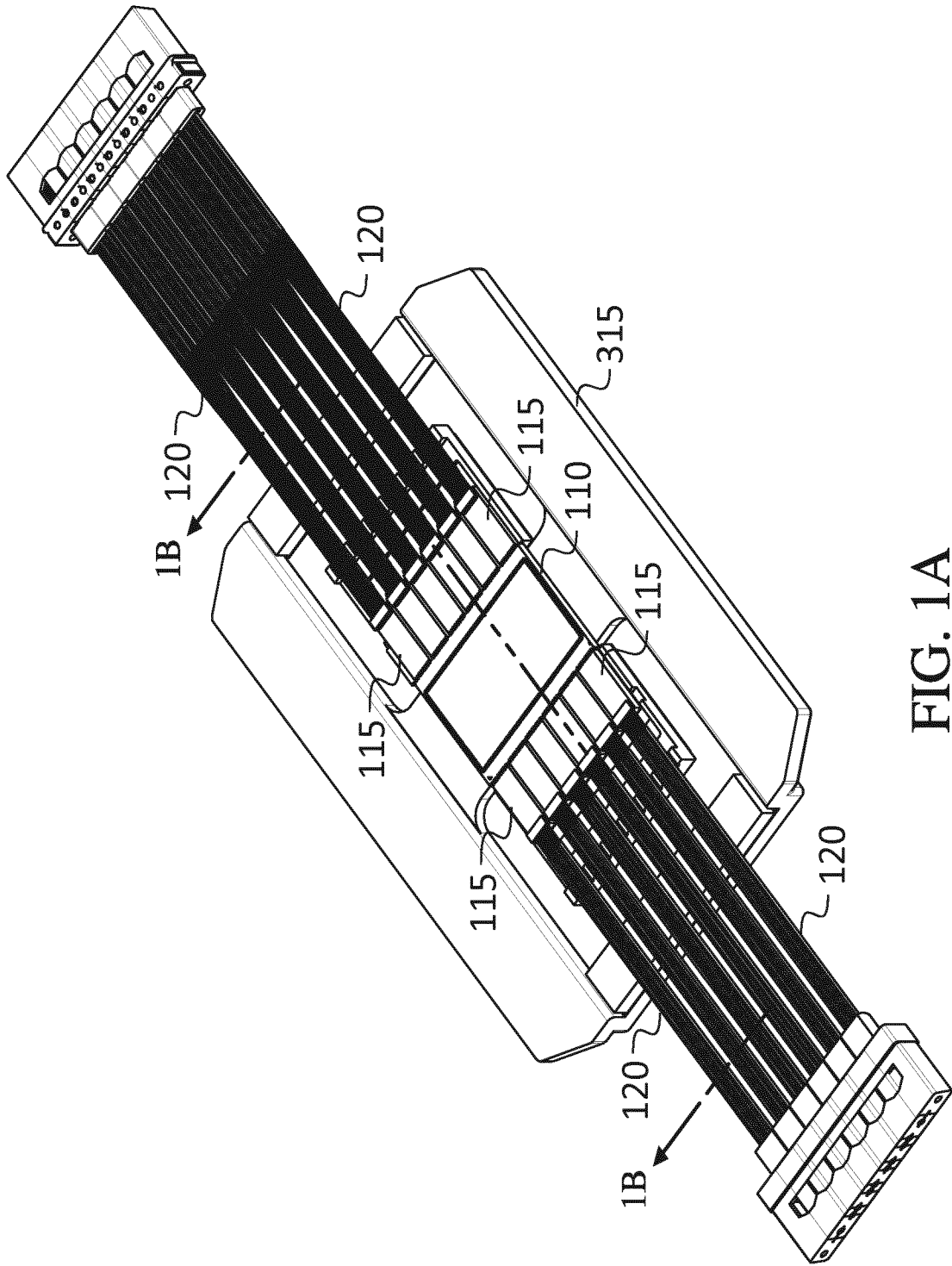


FIG. 1A

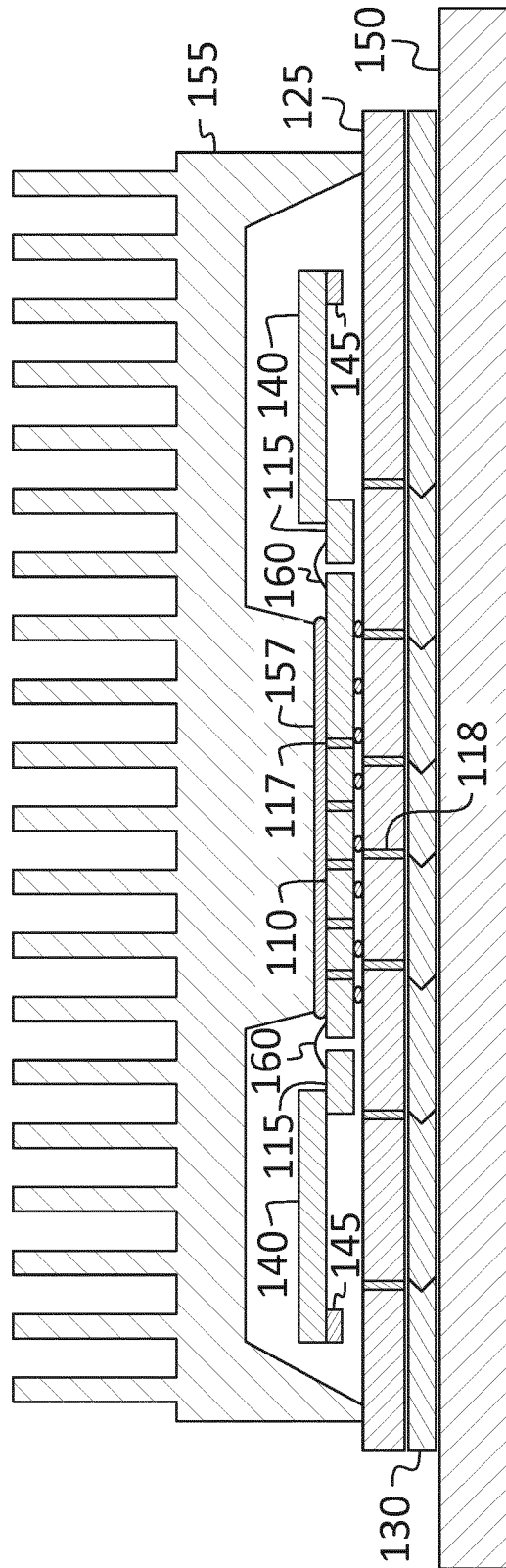


FIG. 1B

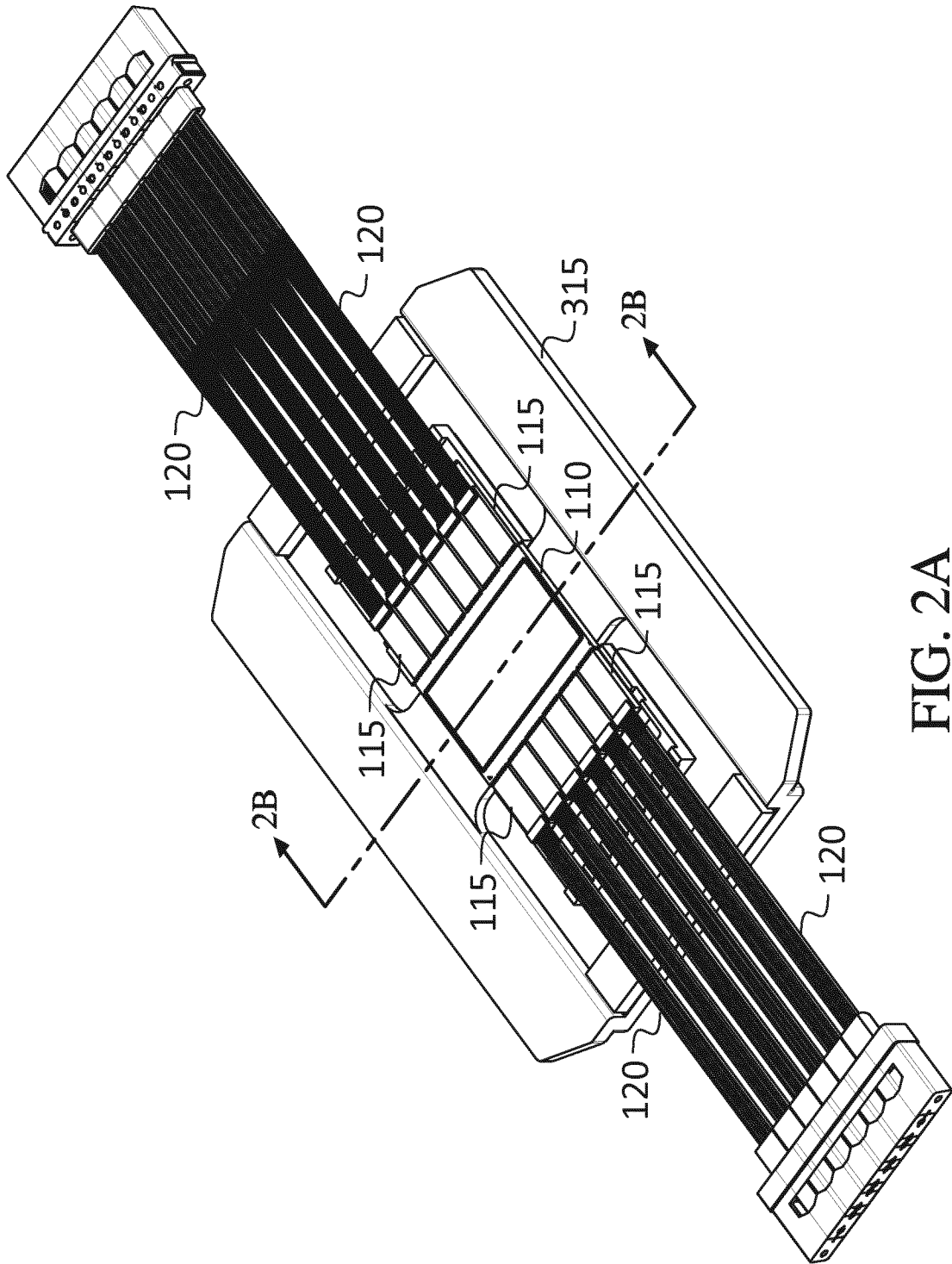


FIG. 2A

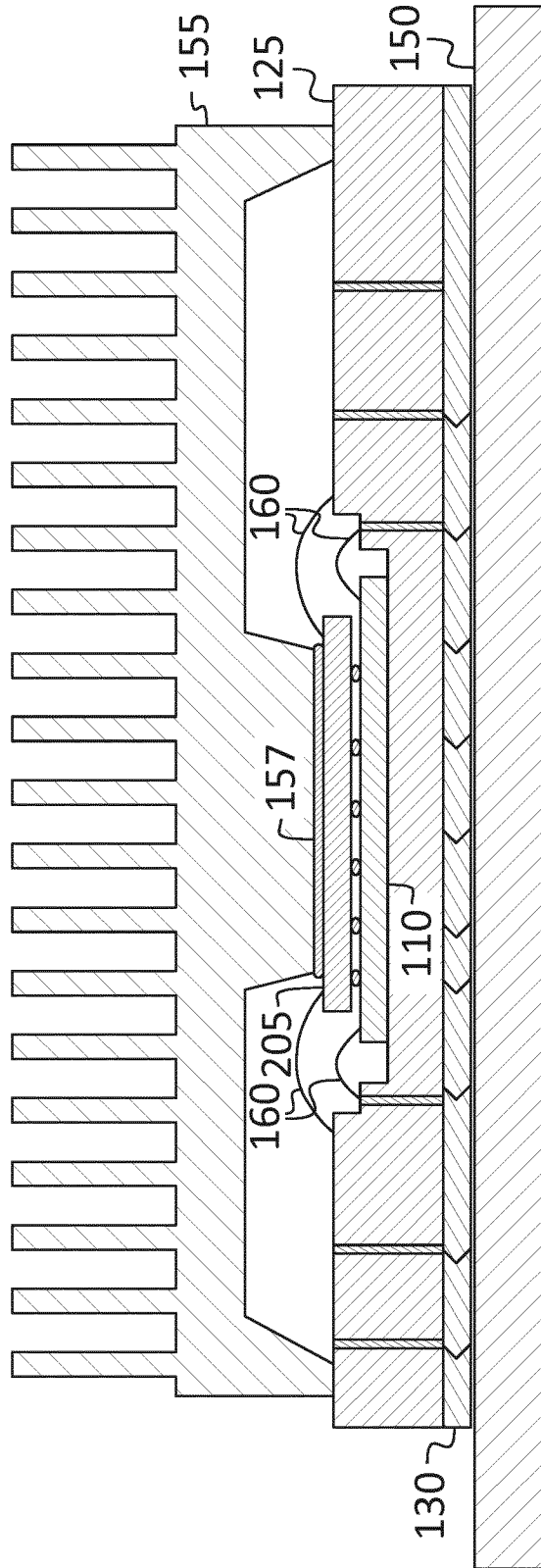


FIG. 2B

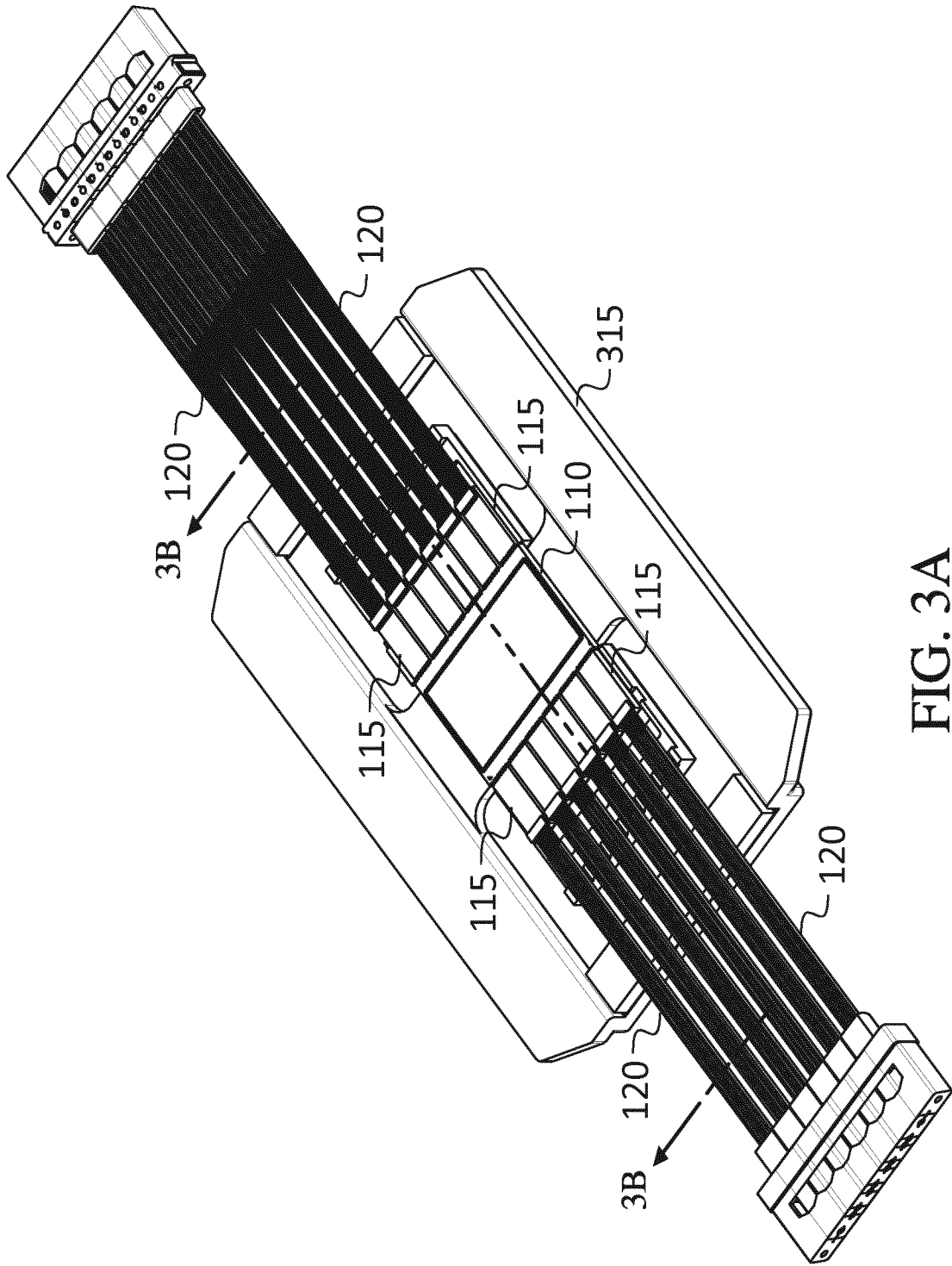


FIG. 3A

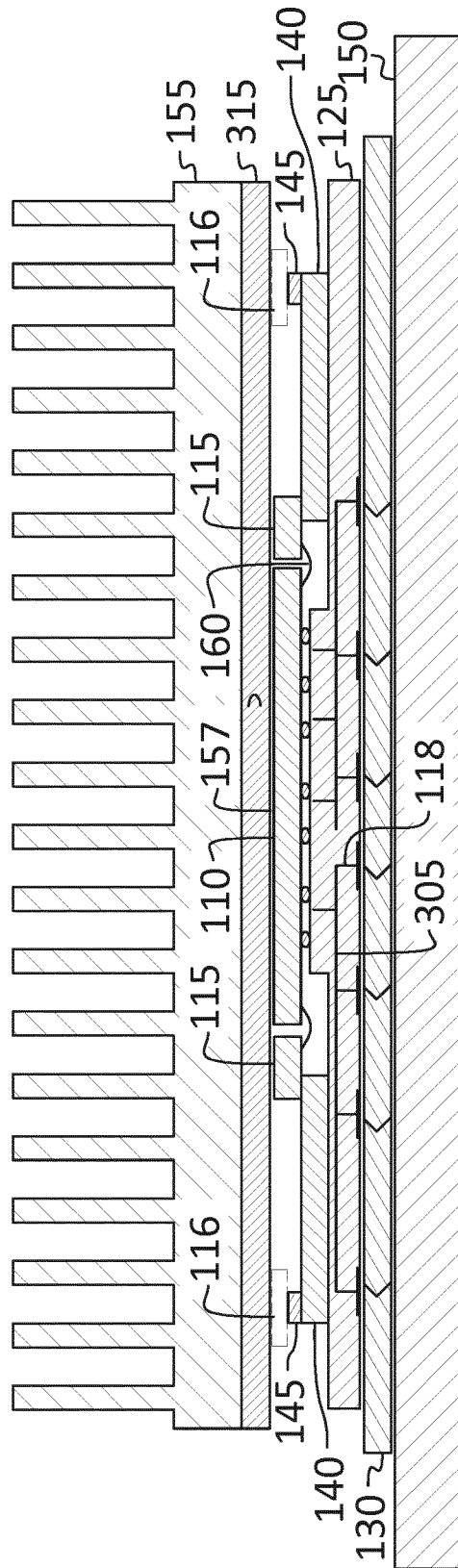
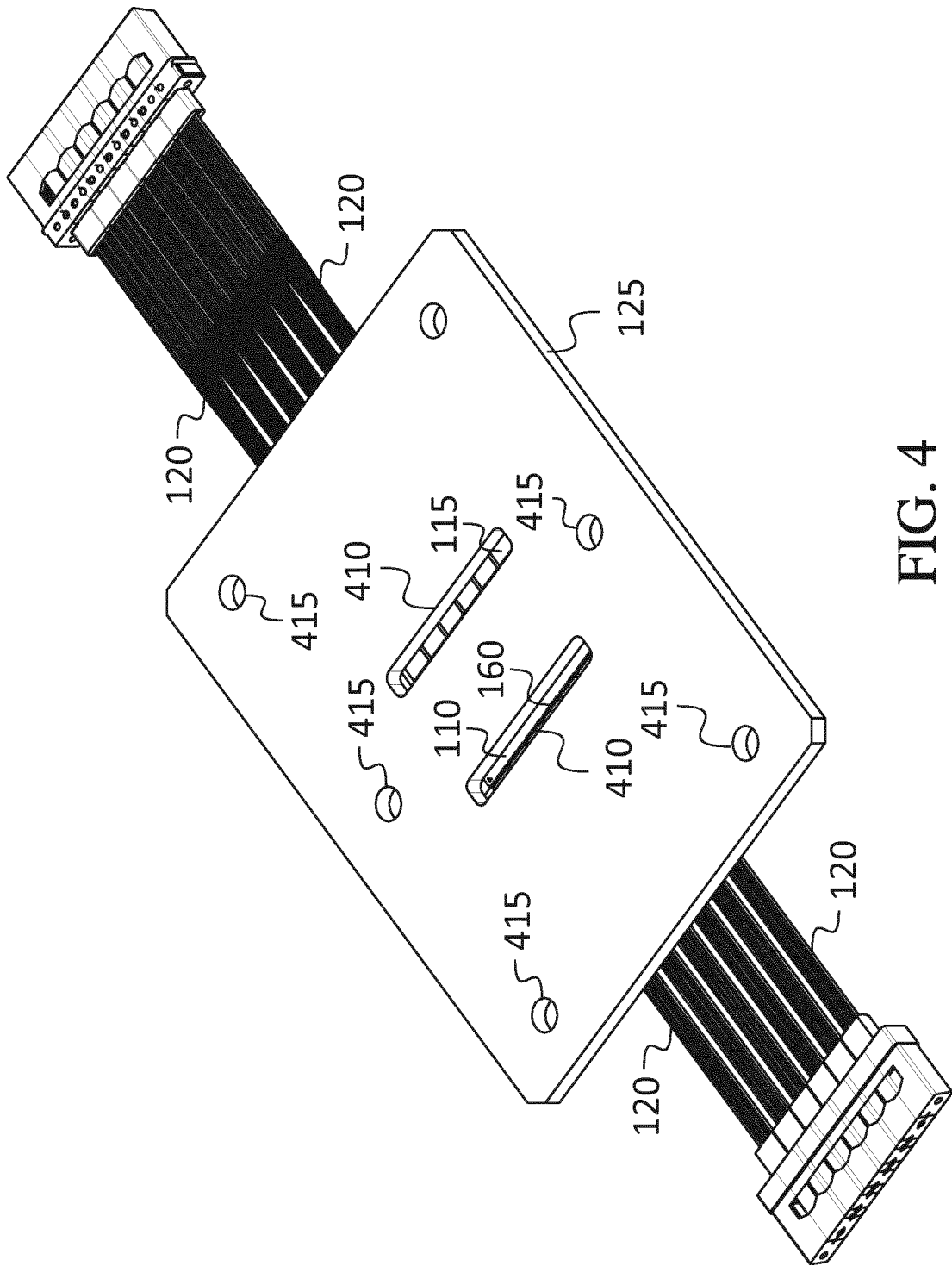
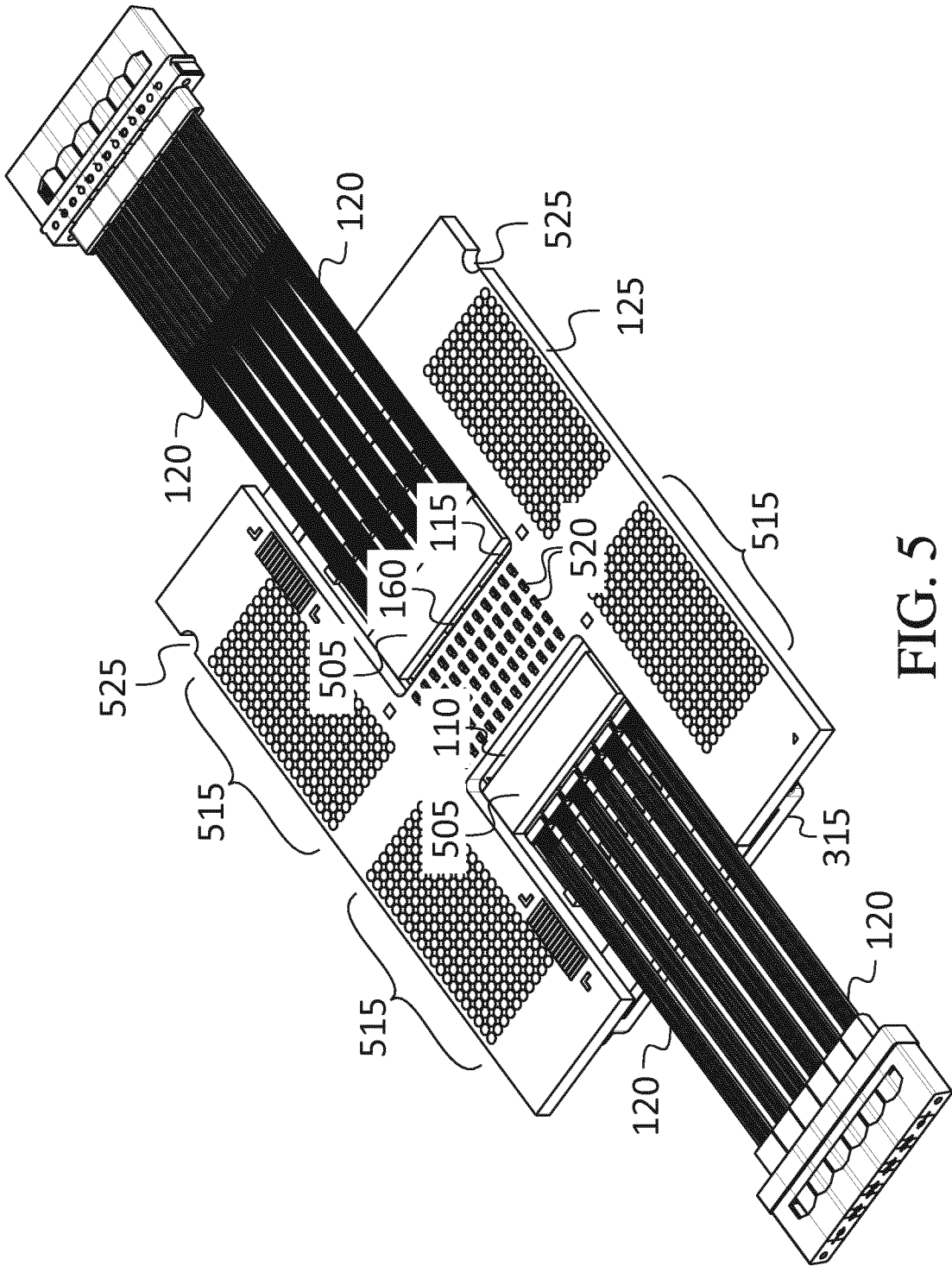


FIG. 3B





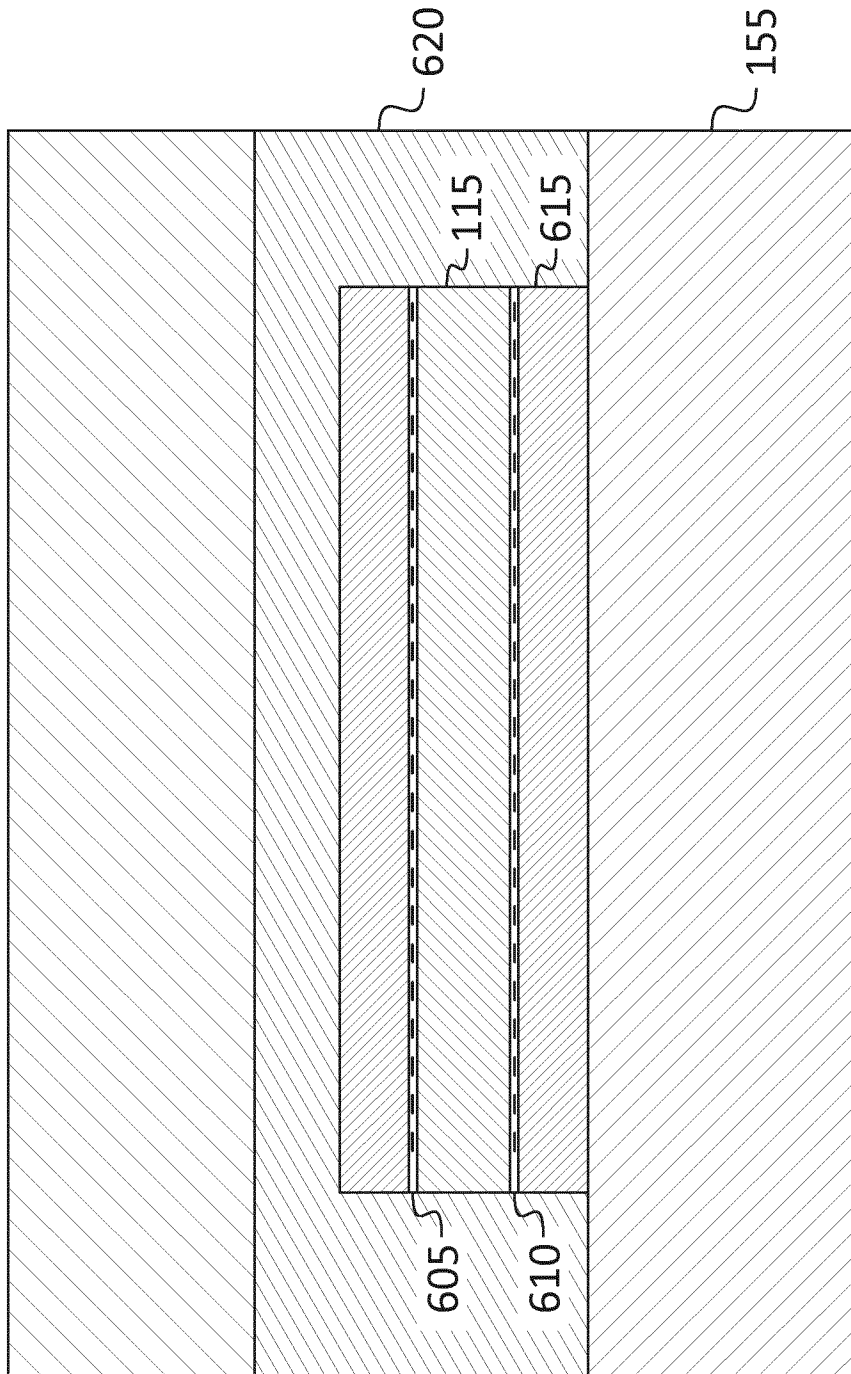


FIG. 6

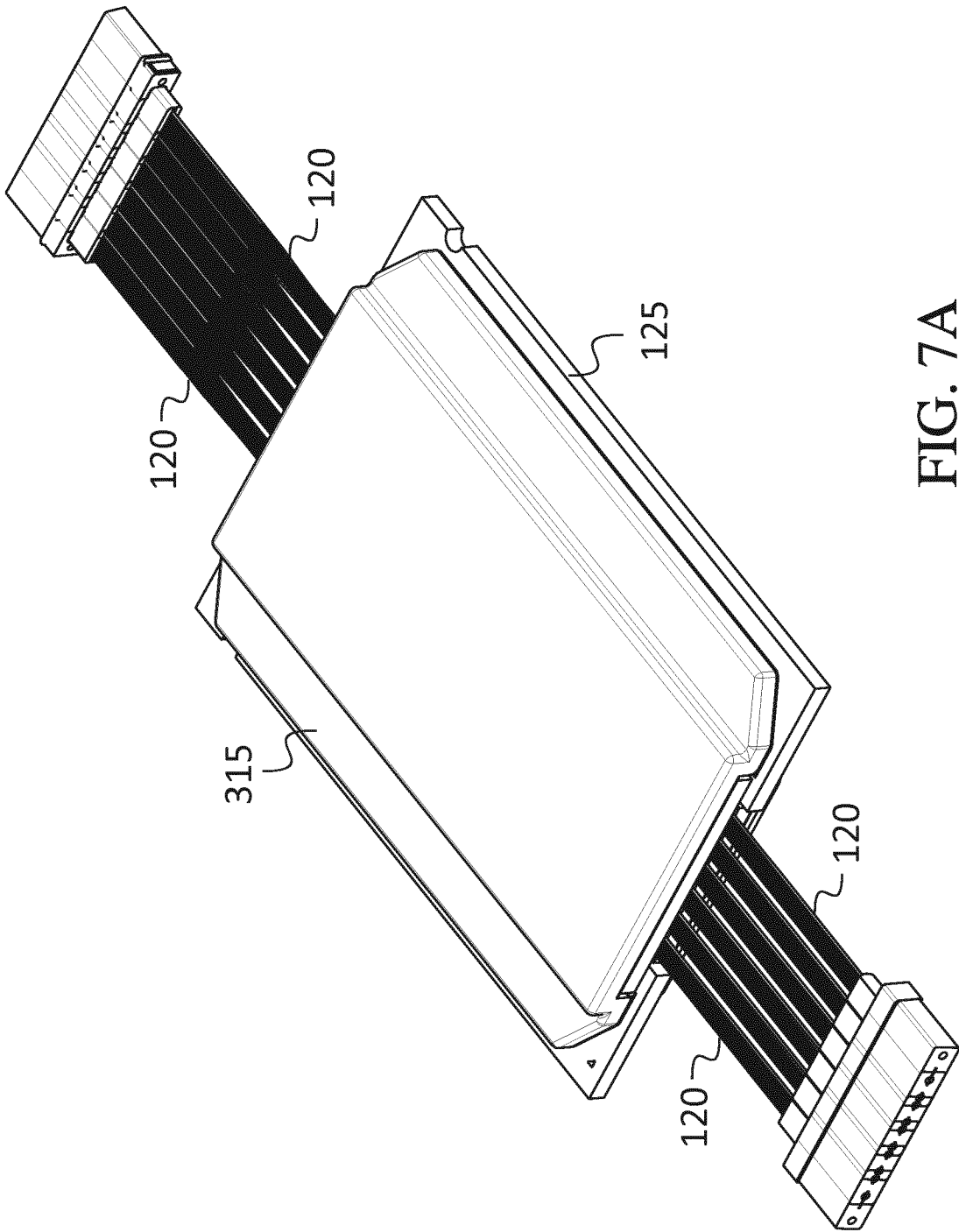


FIG. 7A

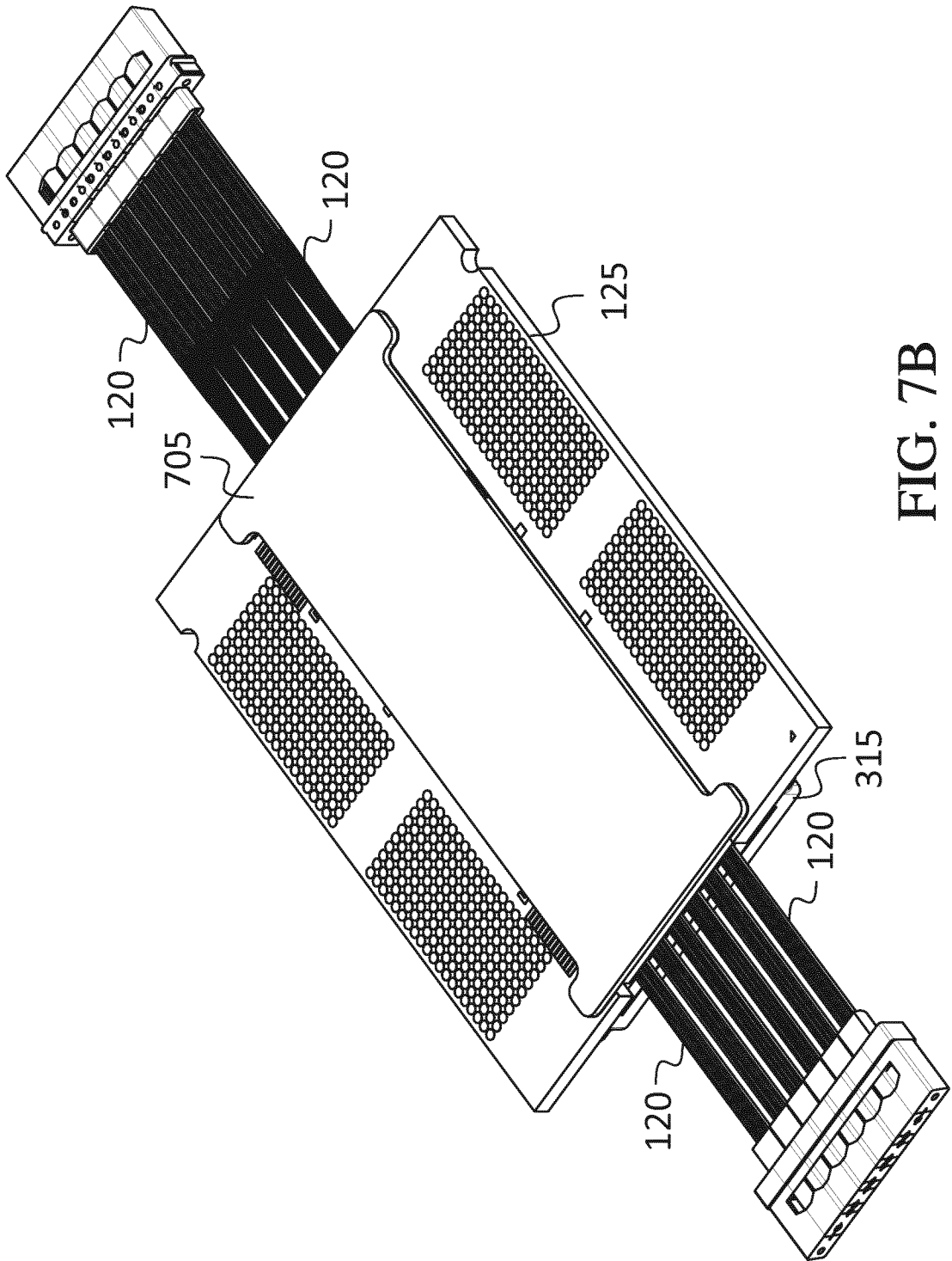


FIG. 7B

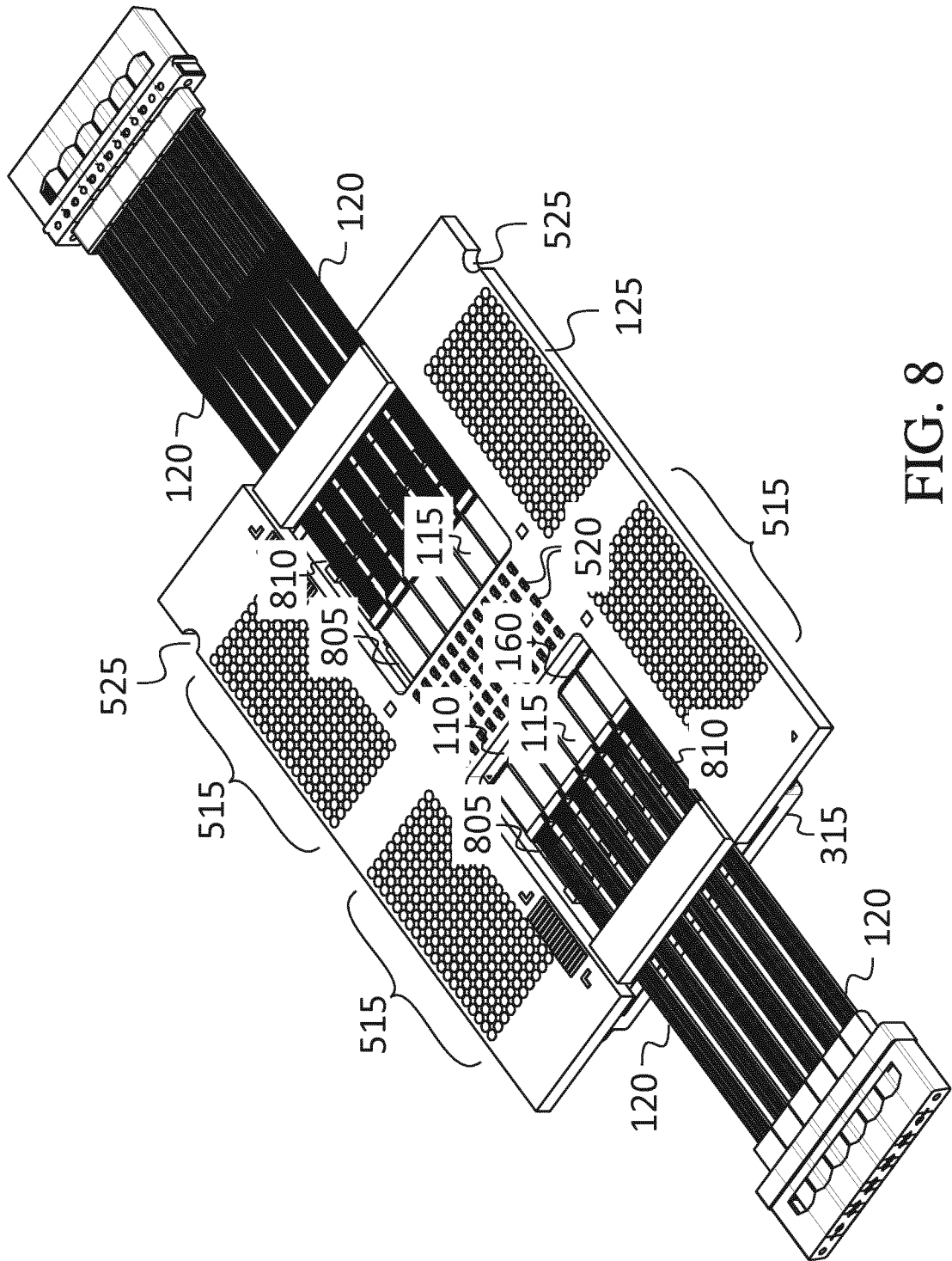


FIG. 8

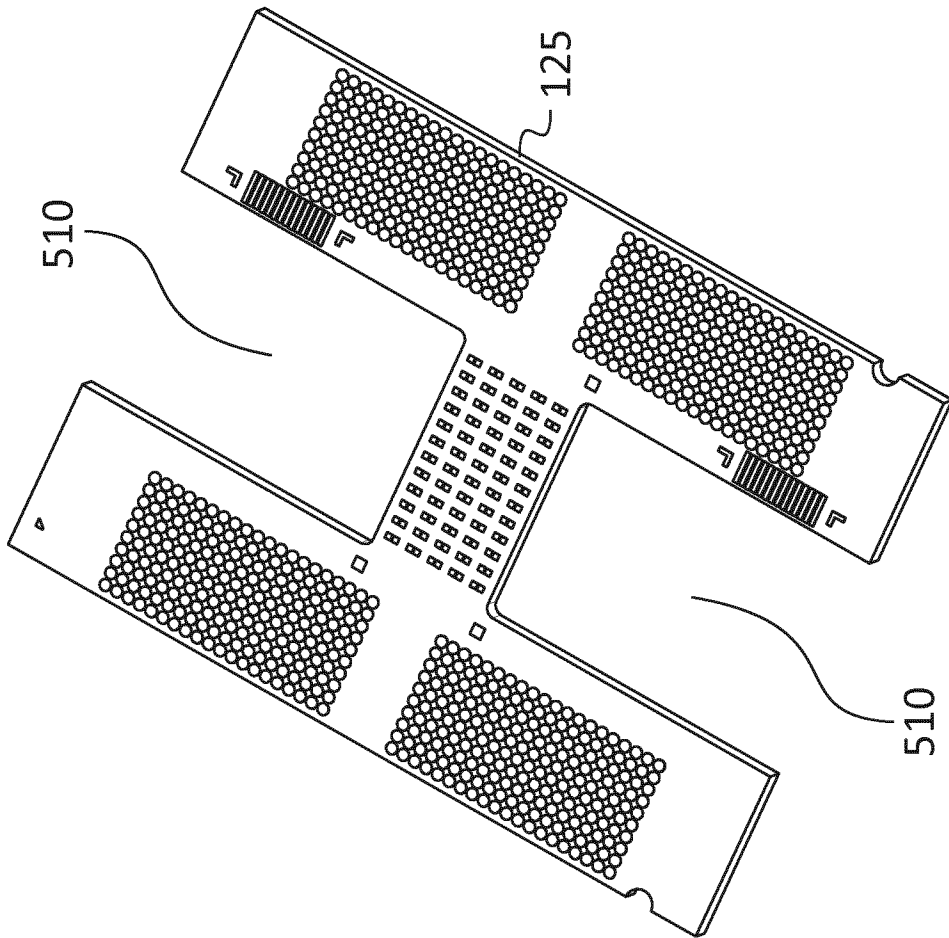


FIG. 9A

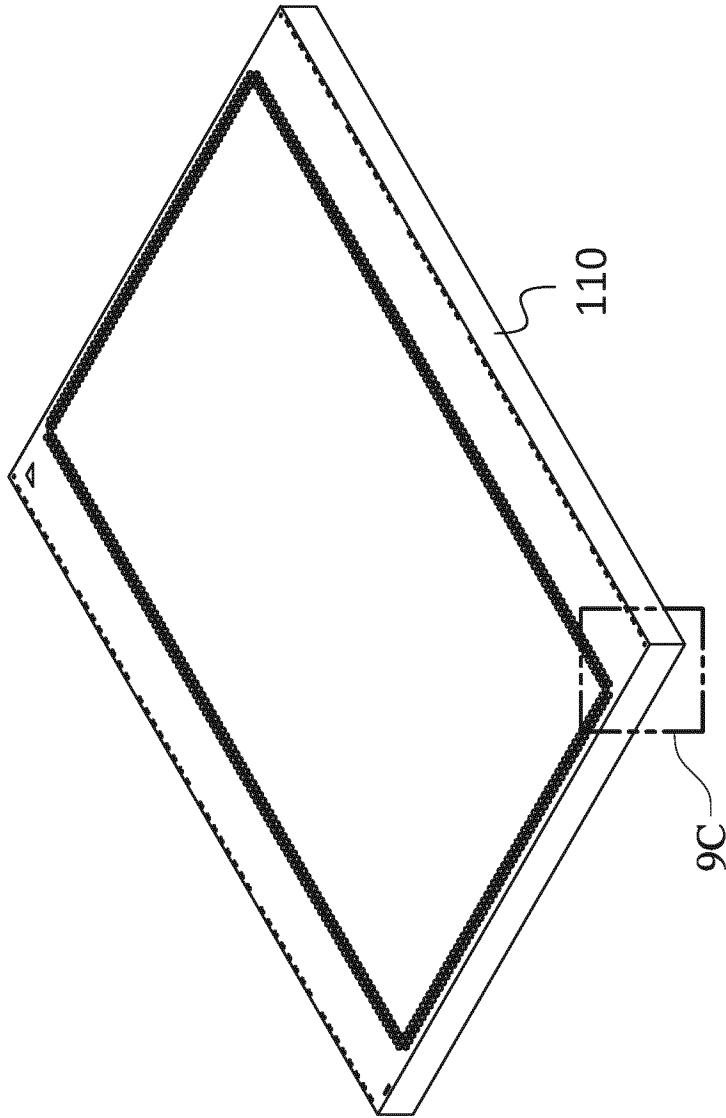


FIG. 9B

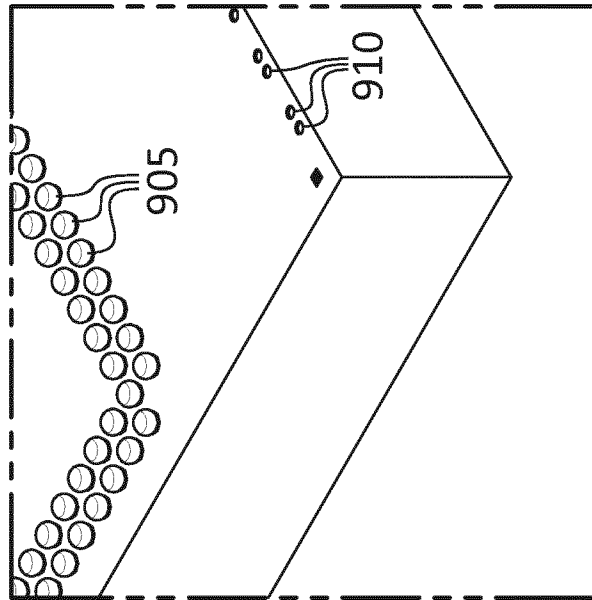


FIG. 9C

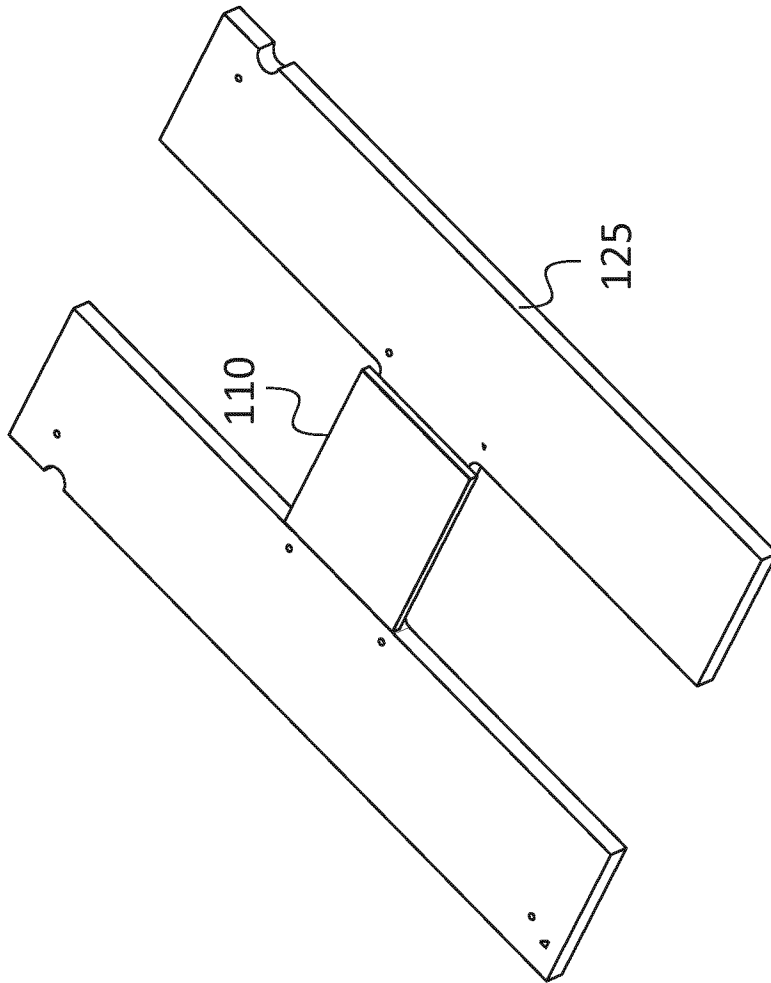


FIG. 9D

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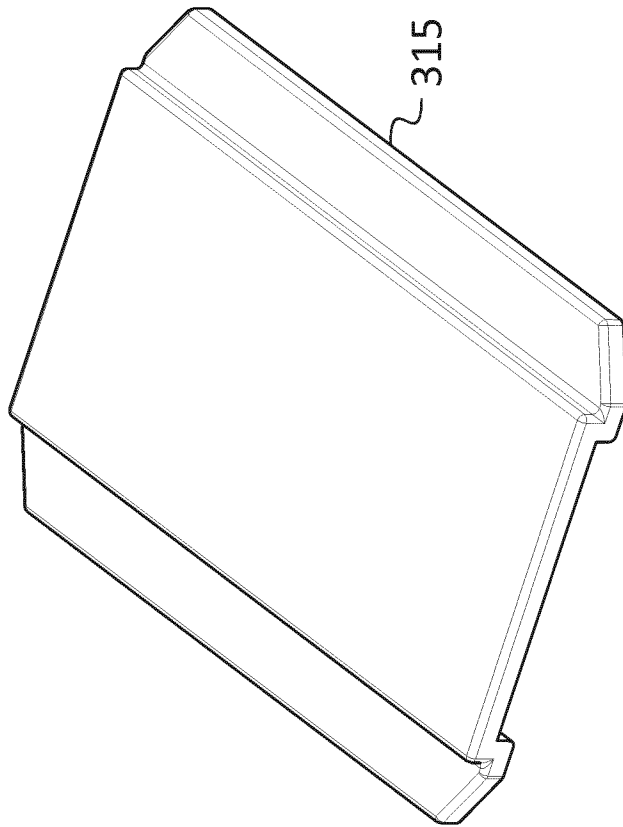


FIG. 10A

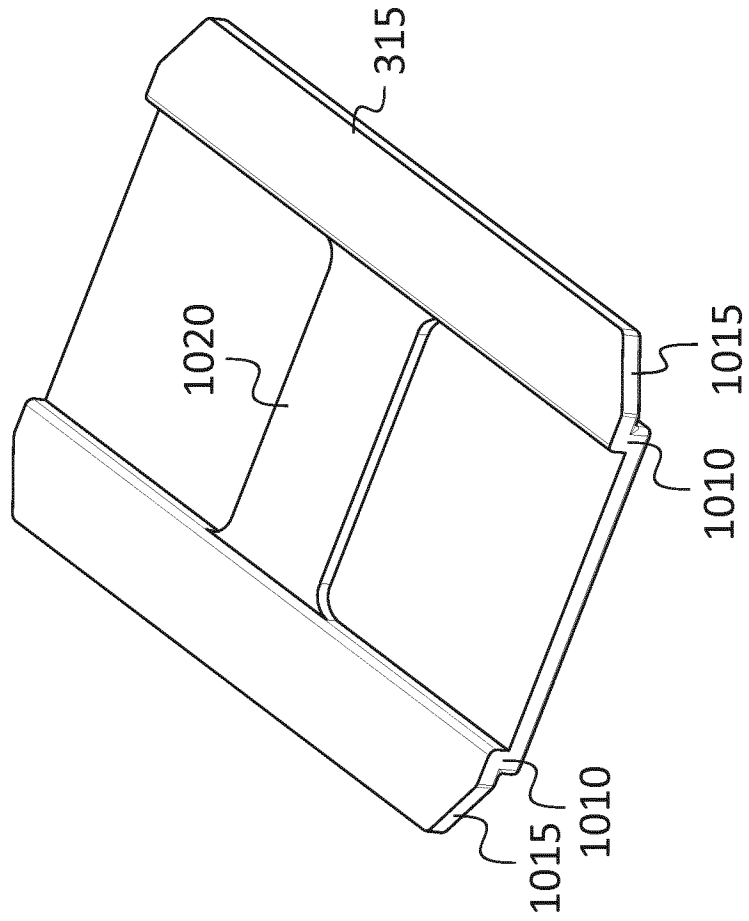


FIG. 10B

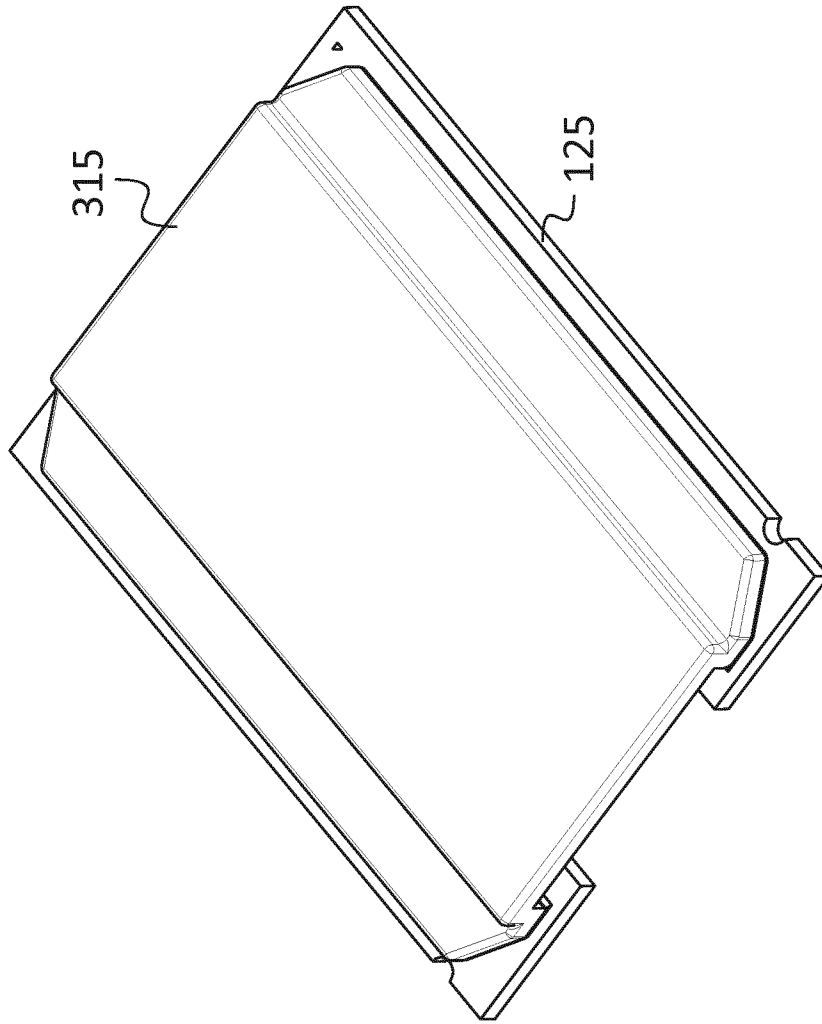


FIG. 10C

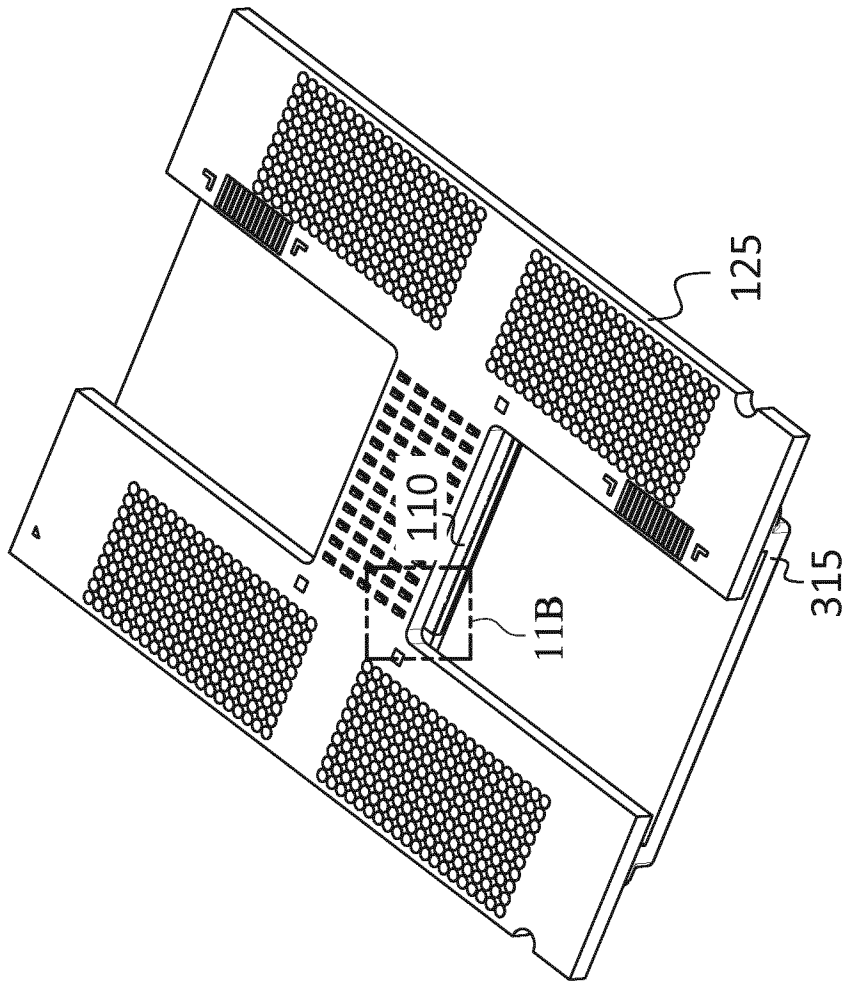


FIG. 11A

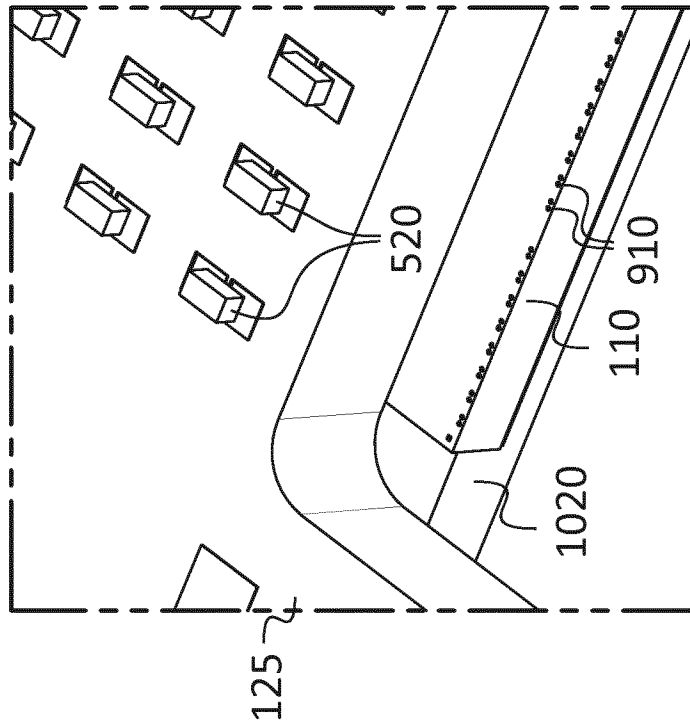


FIG. 11B

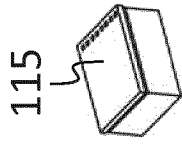


FIG. 12B

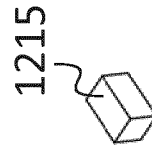


FIG. 12C

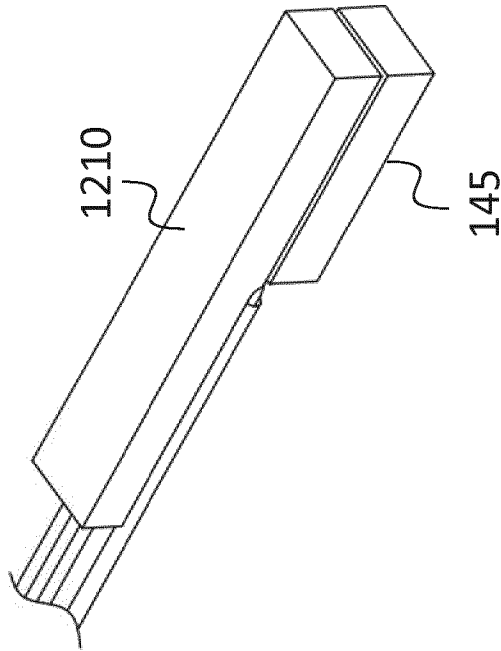


FIG. 12A

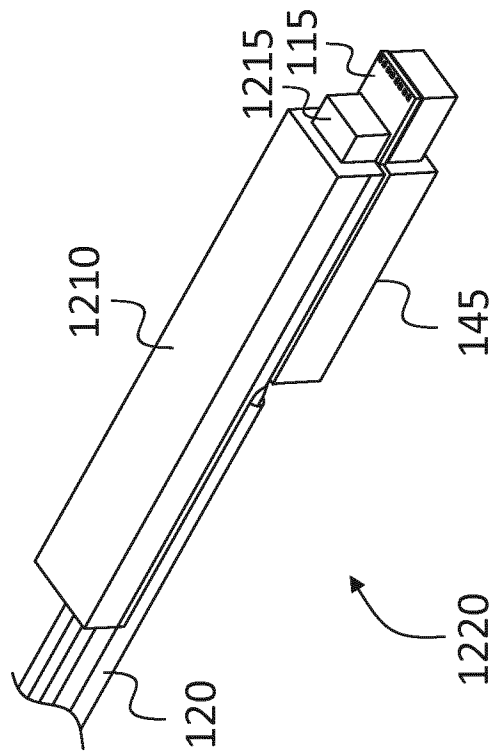


FIG. 12D

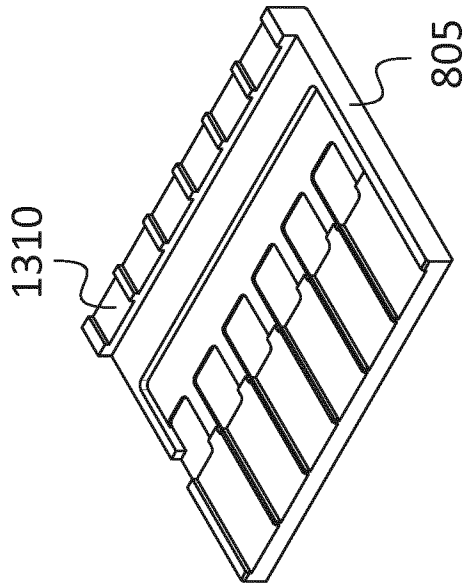


FIG. 13B

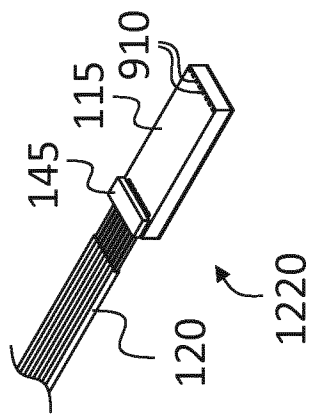


FIG. 13A

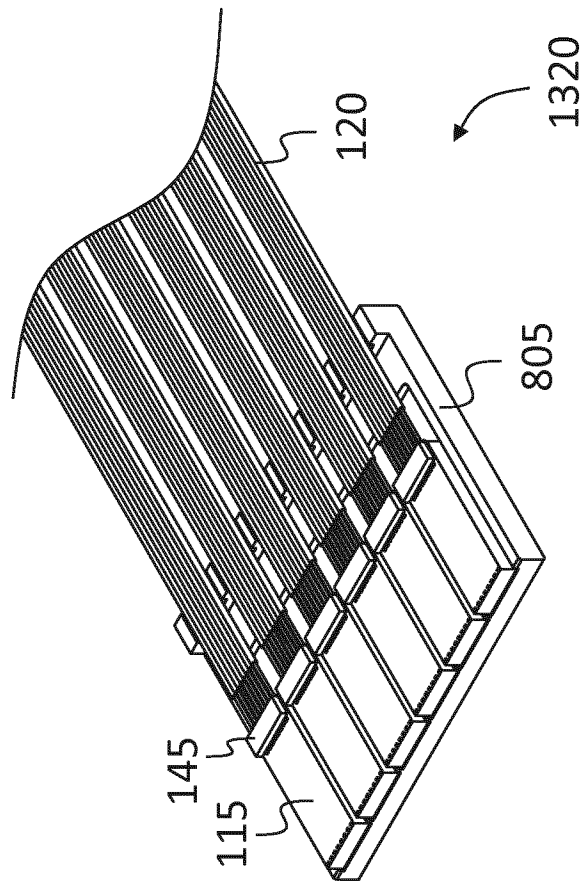


FIG. 13C

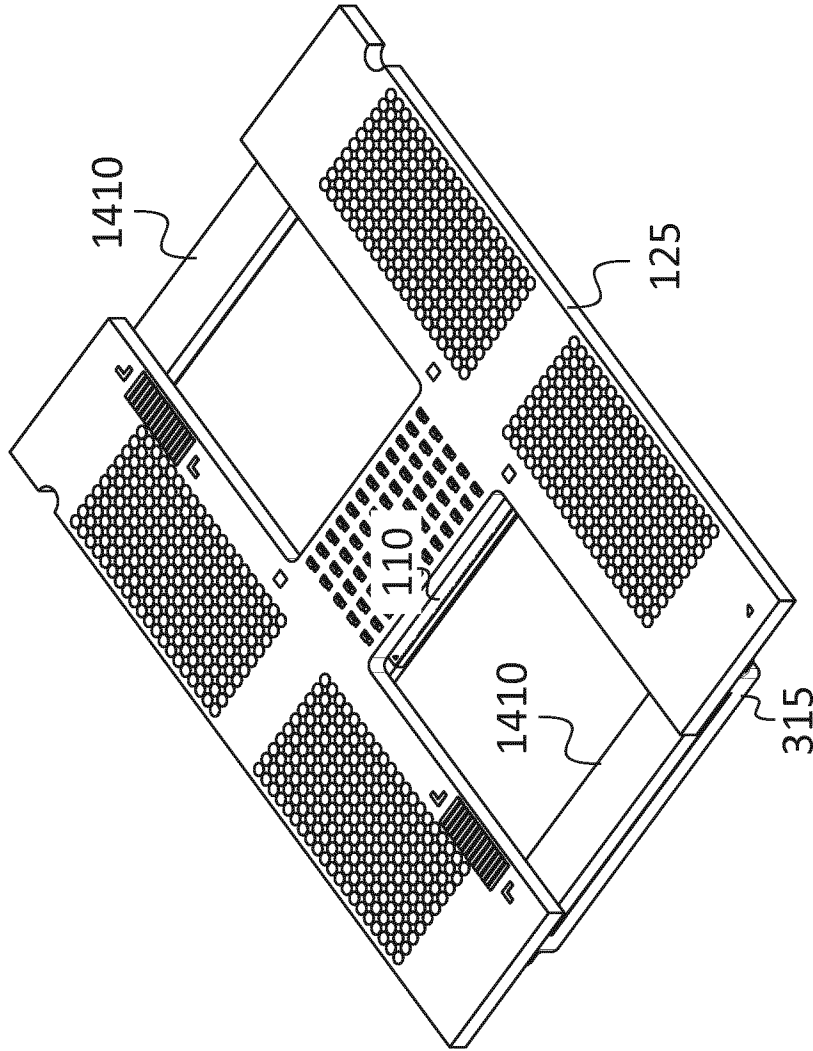
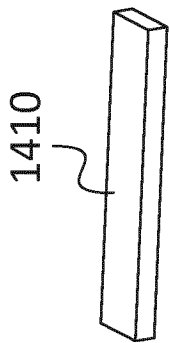


FIG. 14B

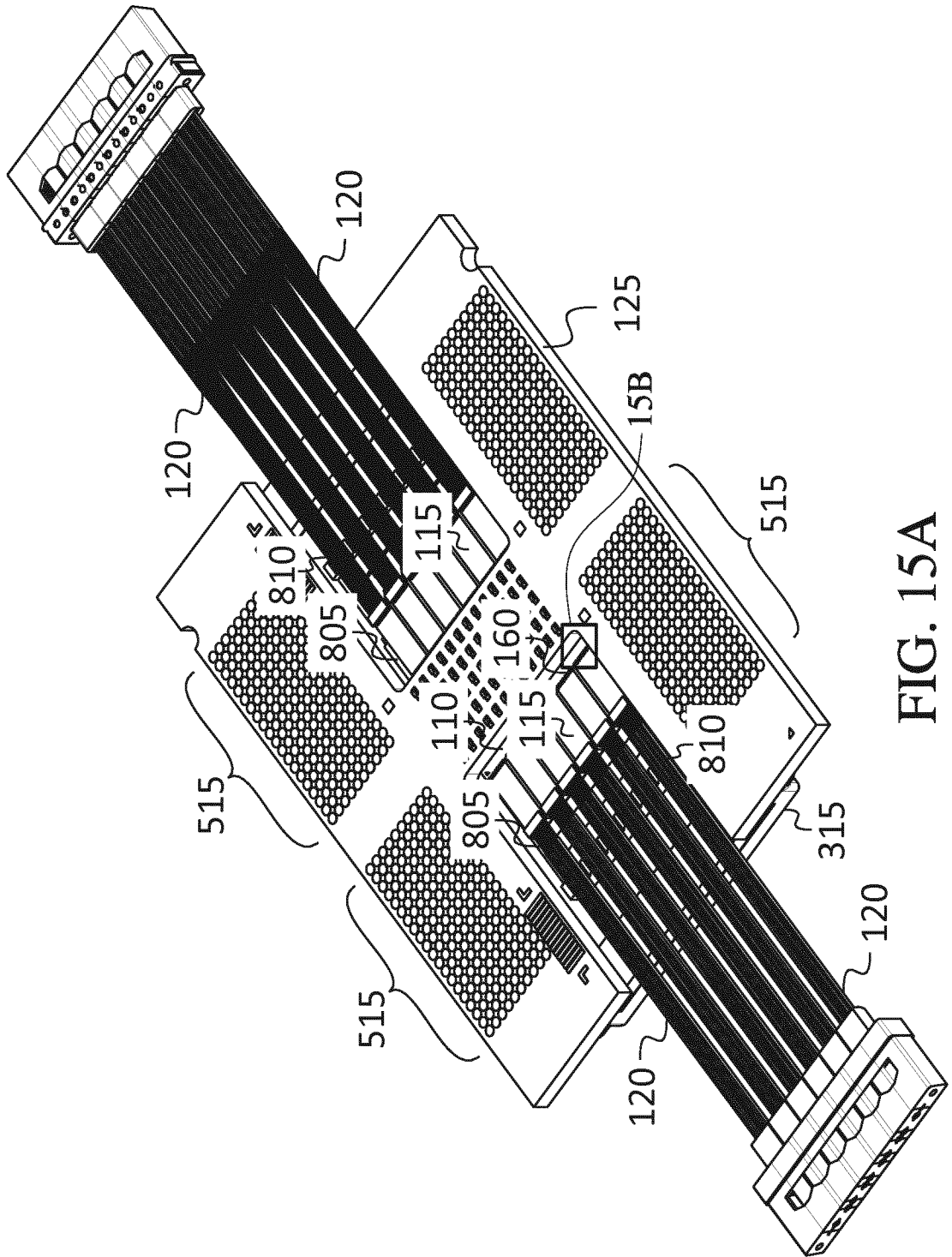


FIG. 15A

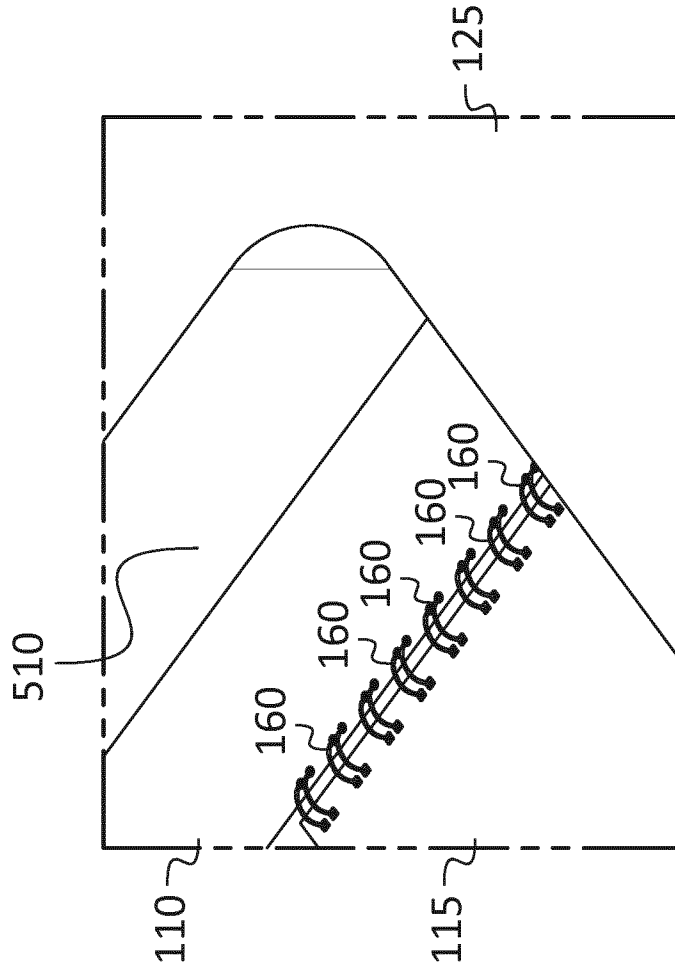


FIG. 15B

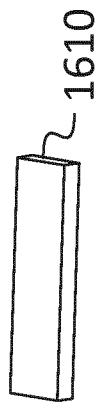


FIG. 16A

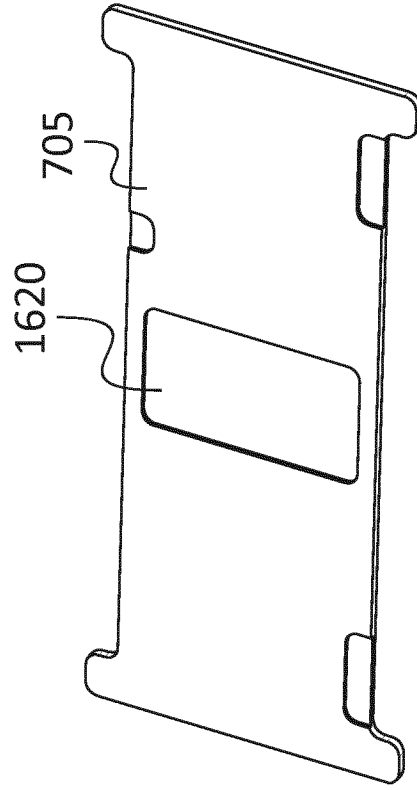


FIG. 16B

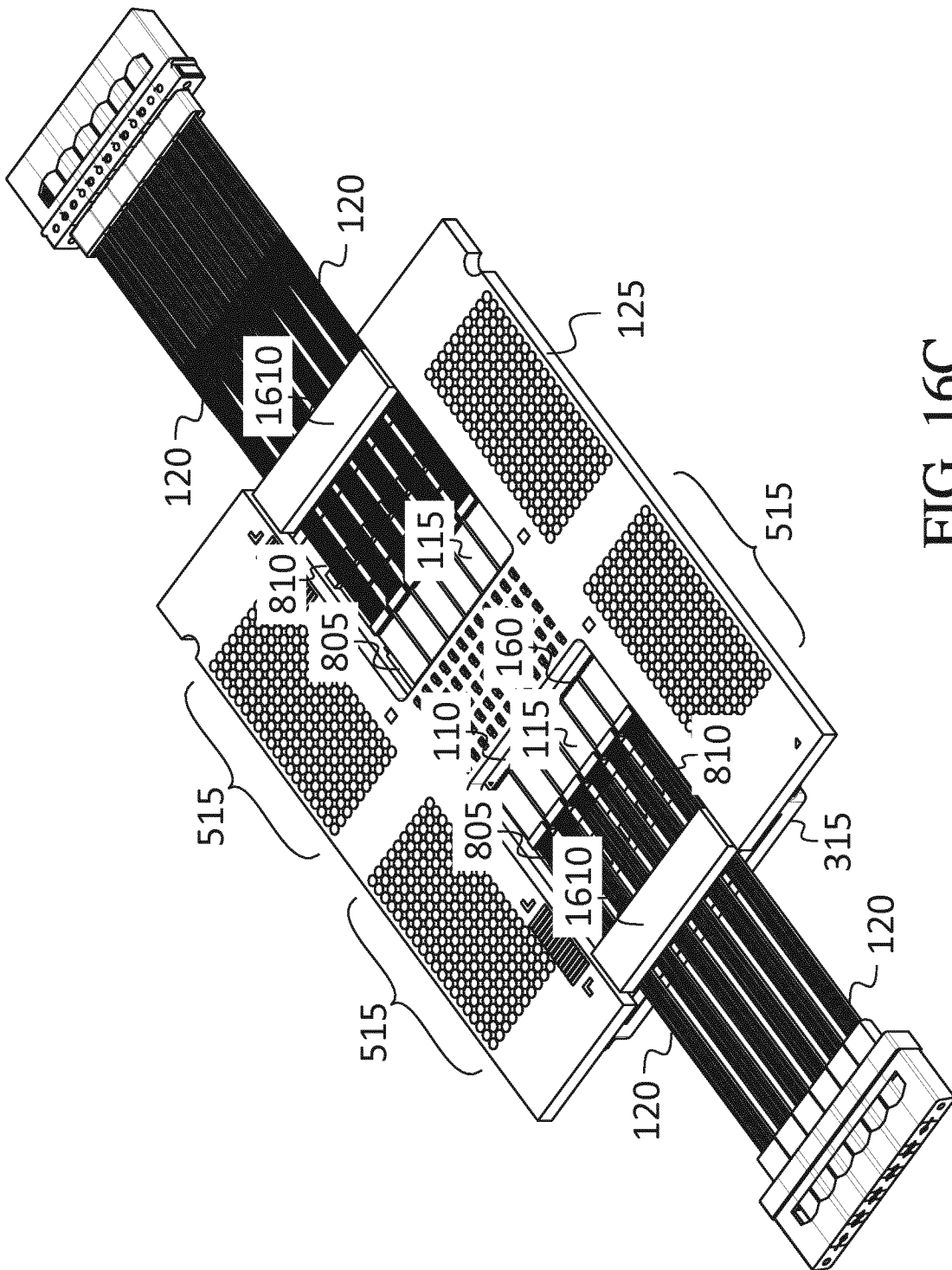


FIG. 16C

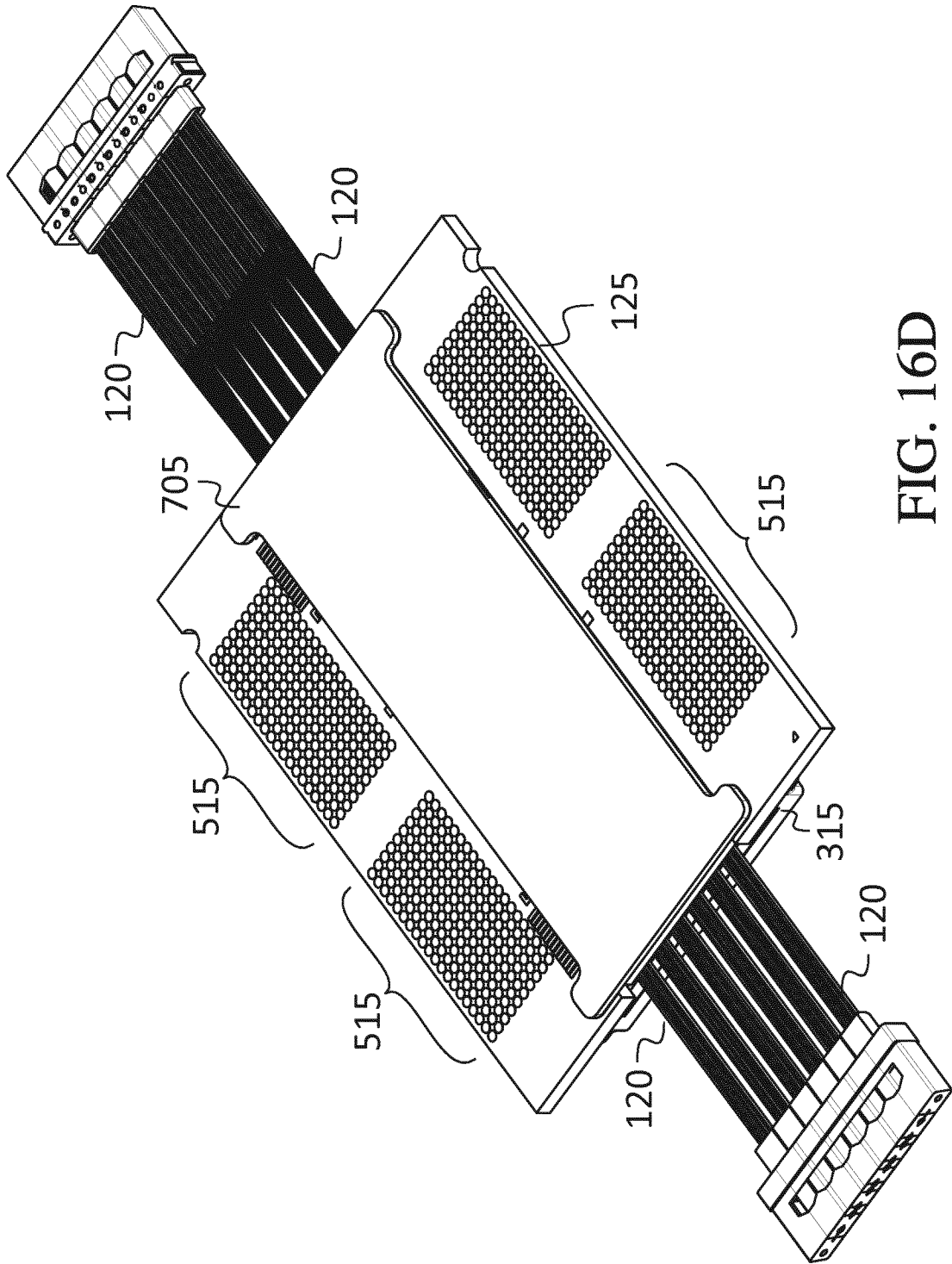


FIG. 16D

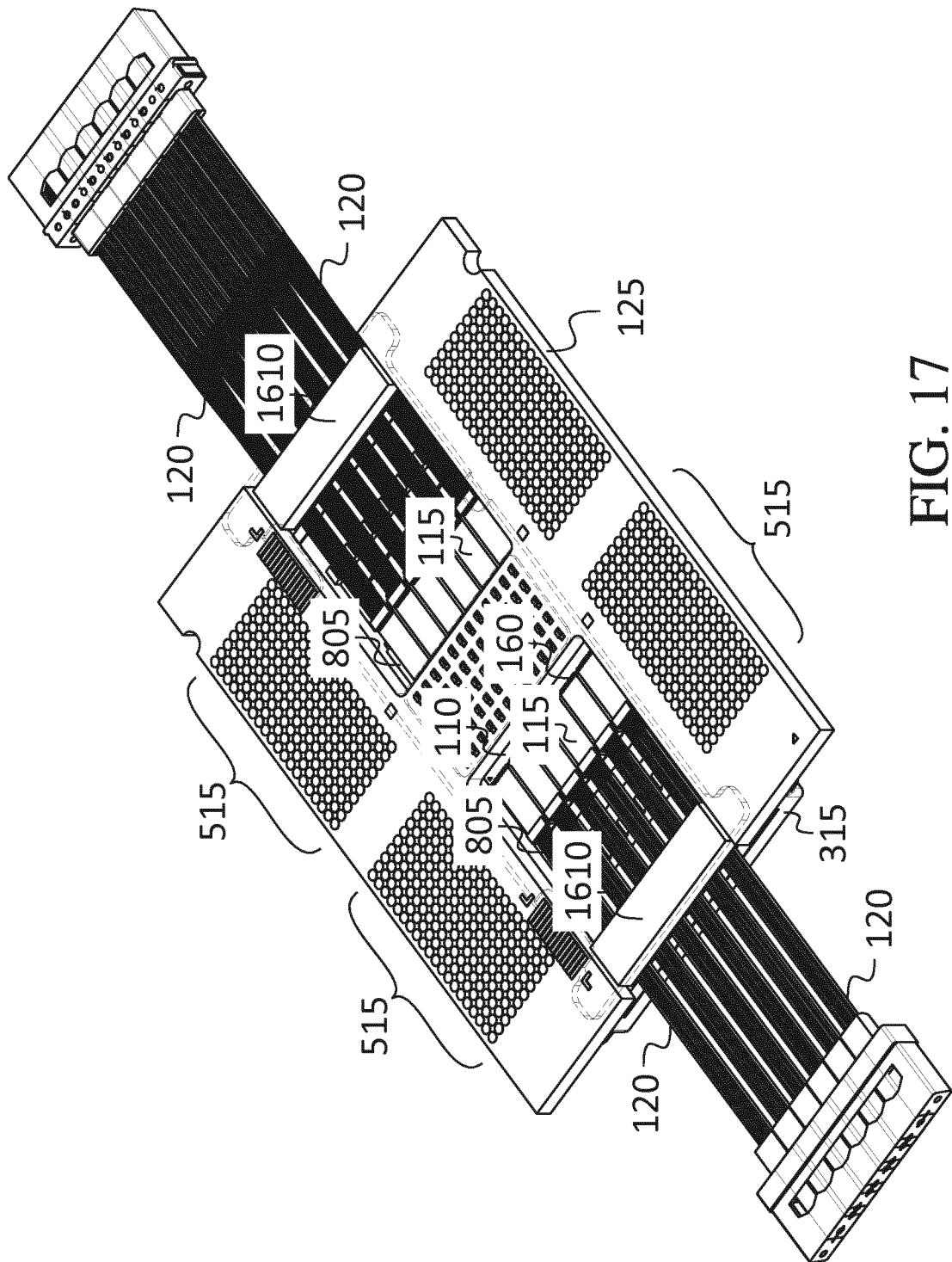


FIG. 17

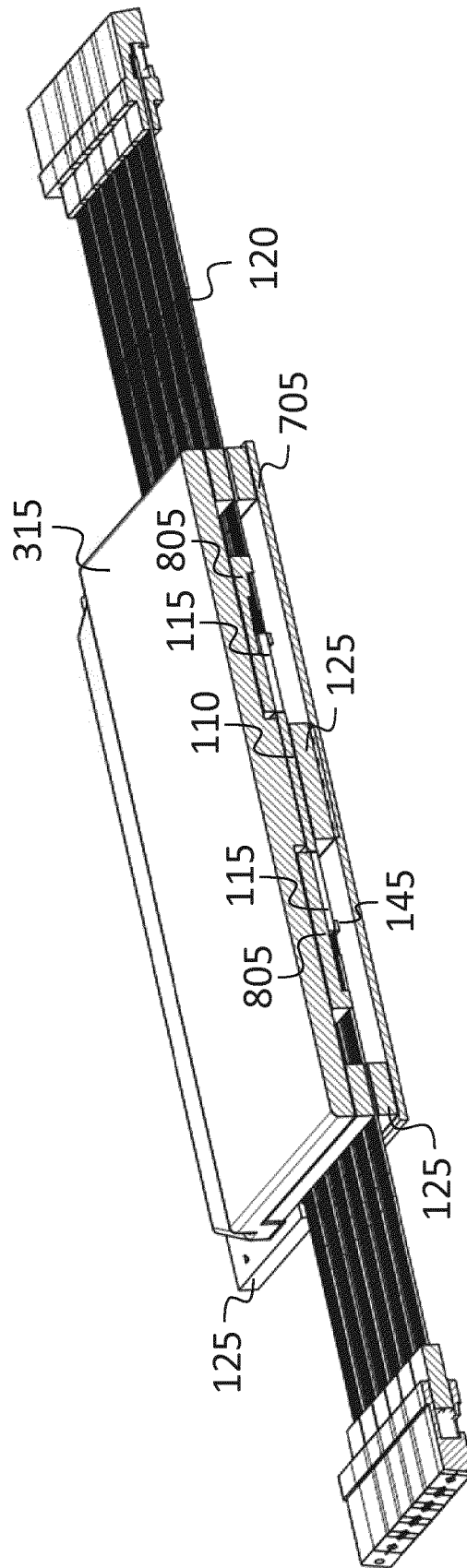


FIG. 18

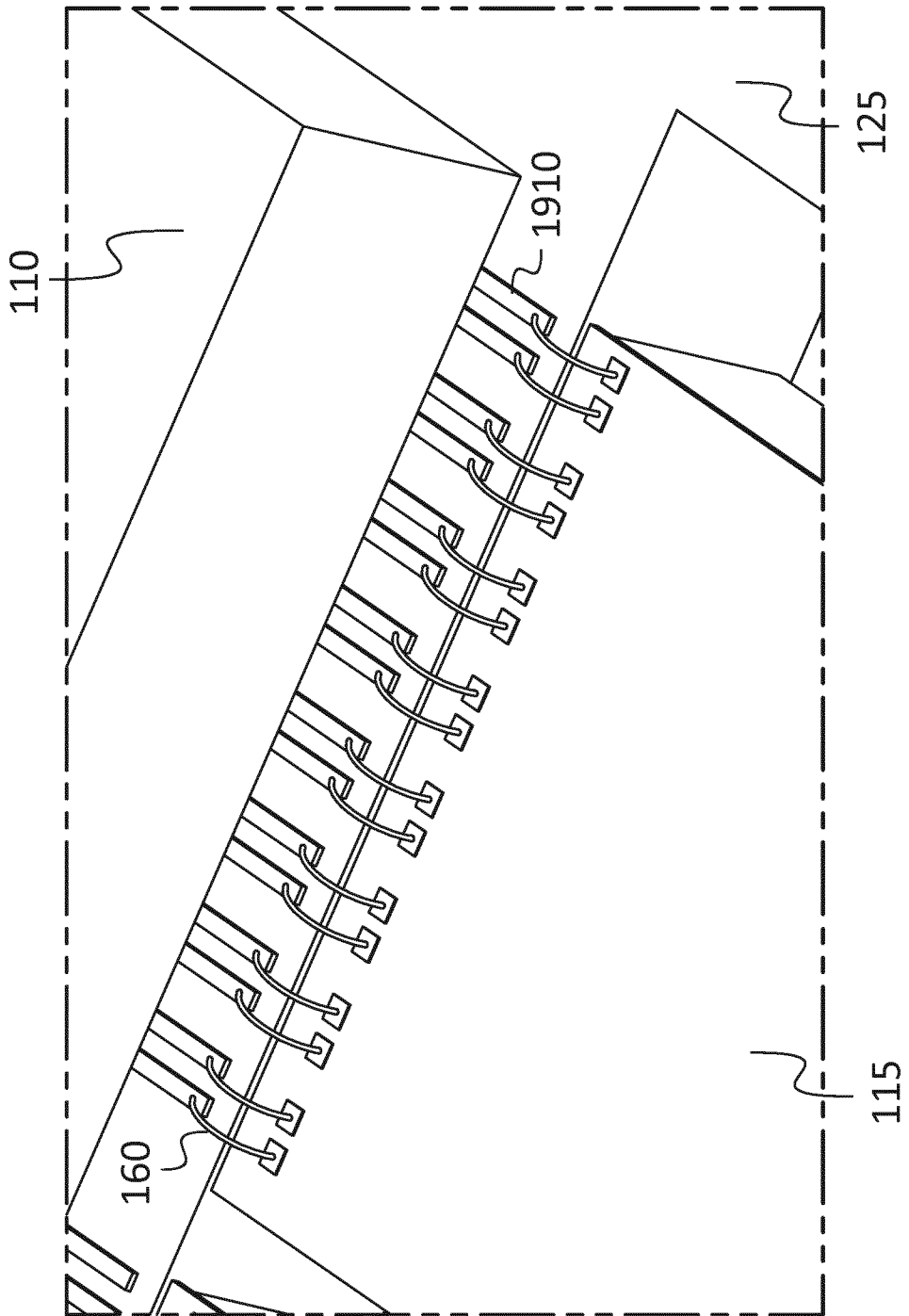


FIG. 19

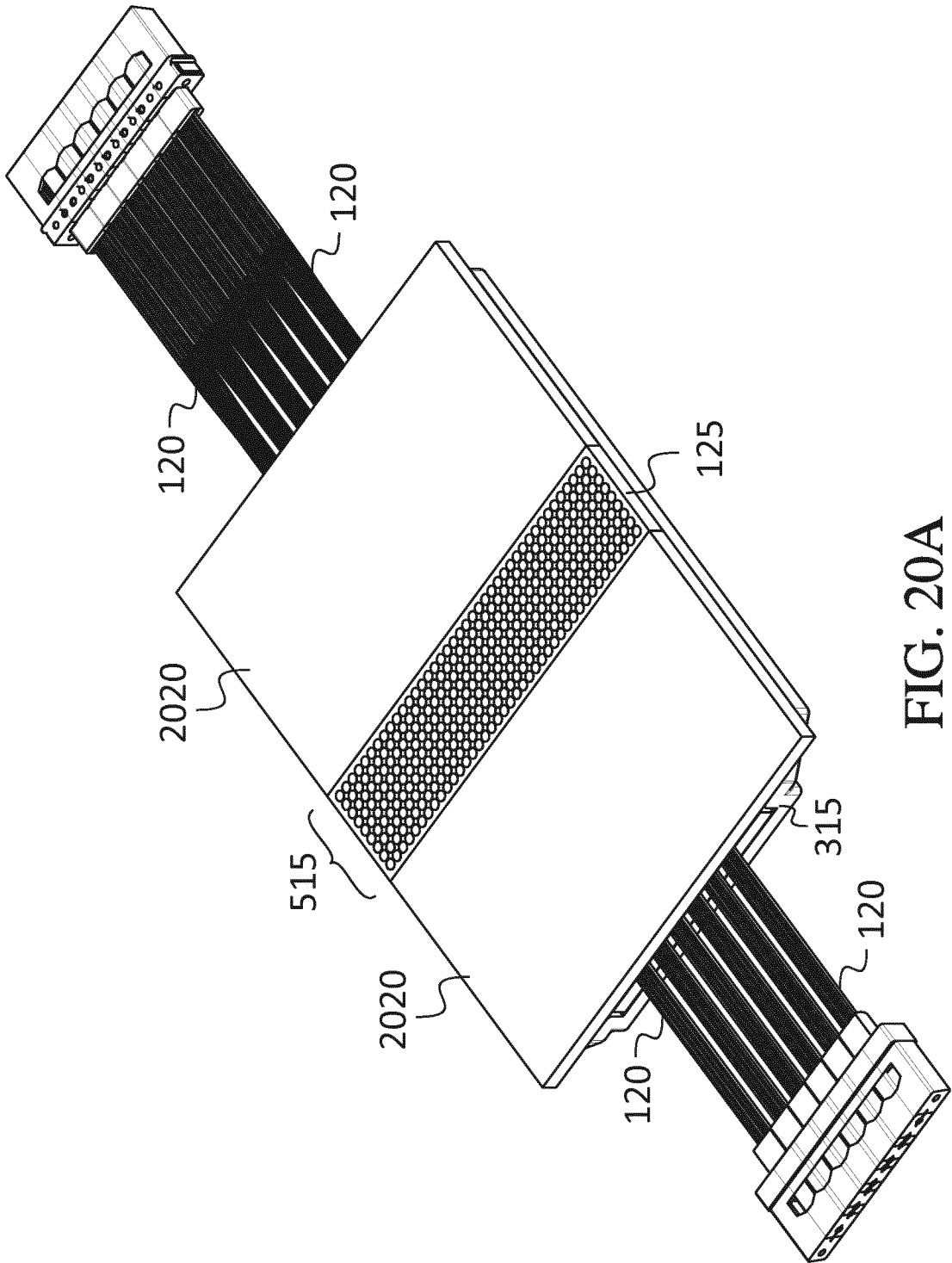


FIG. 20A

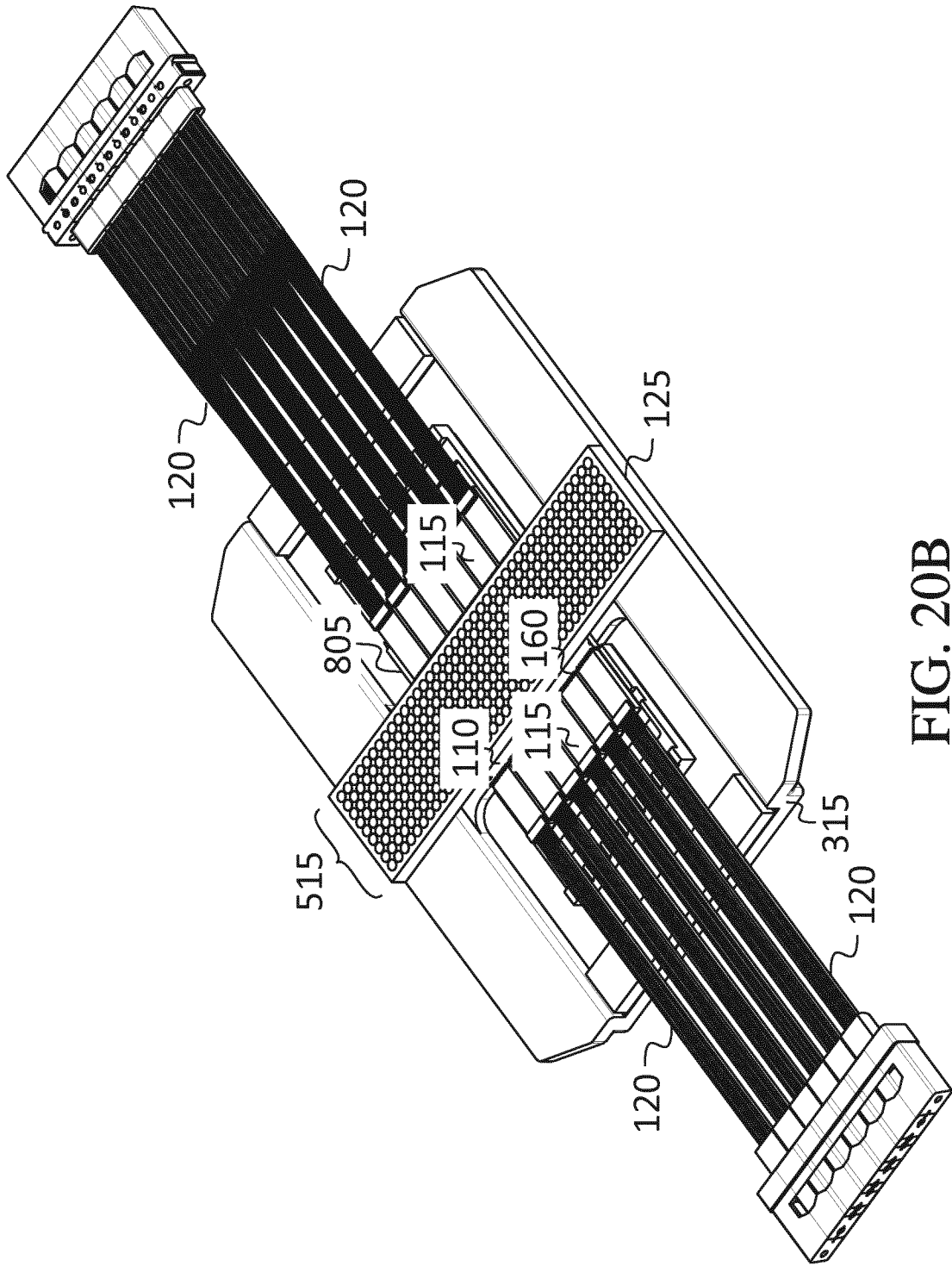


FIG. 20B

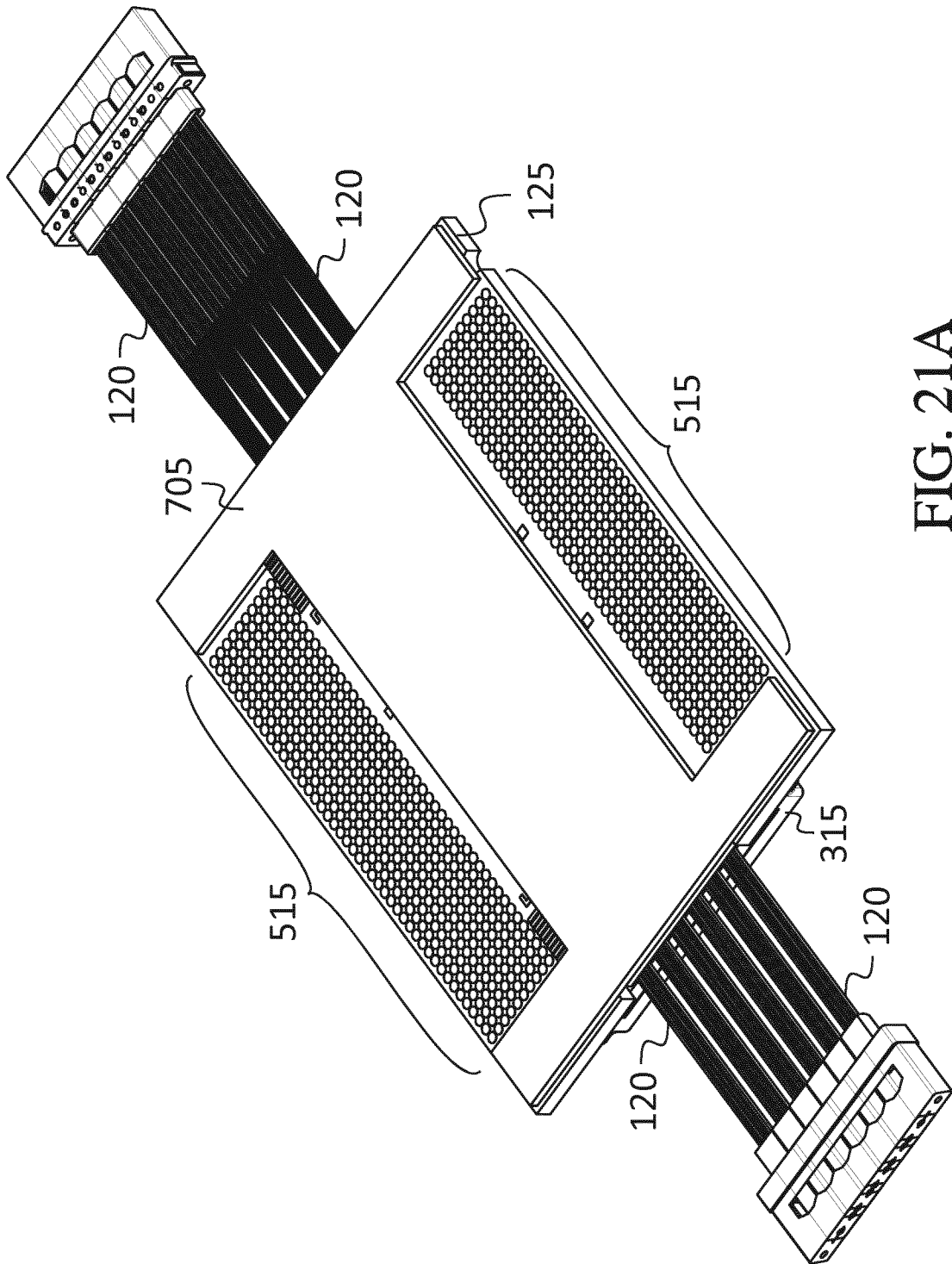


FIG. 21A

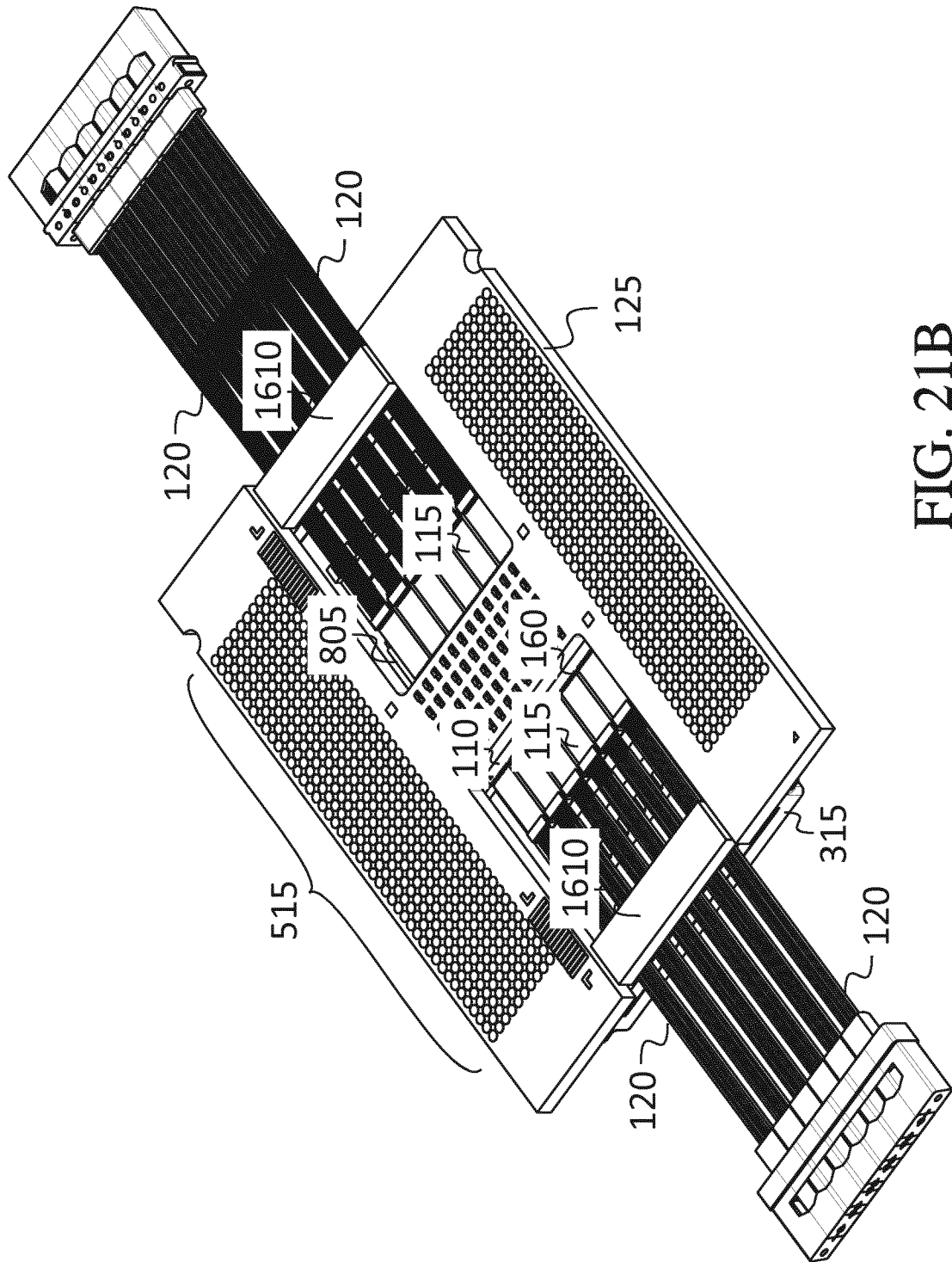


FIG. 21B

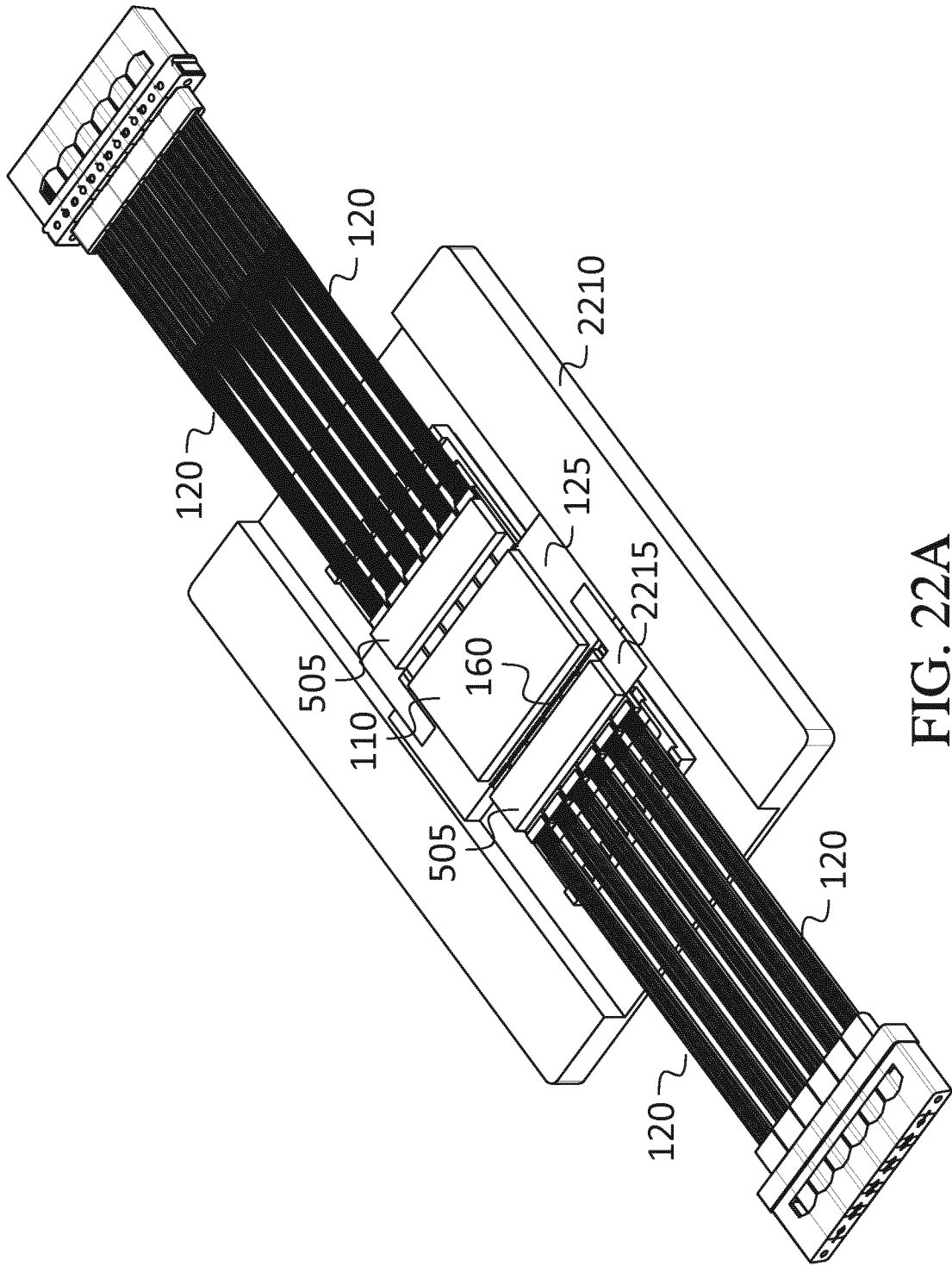


FIG. 22A

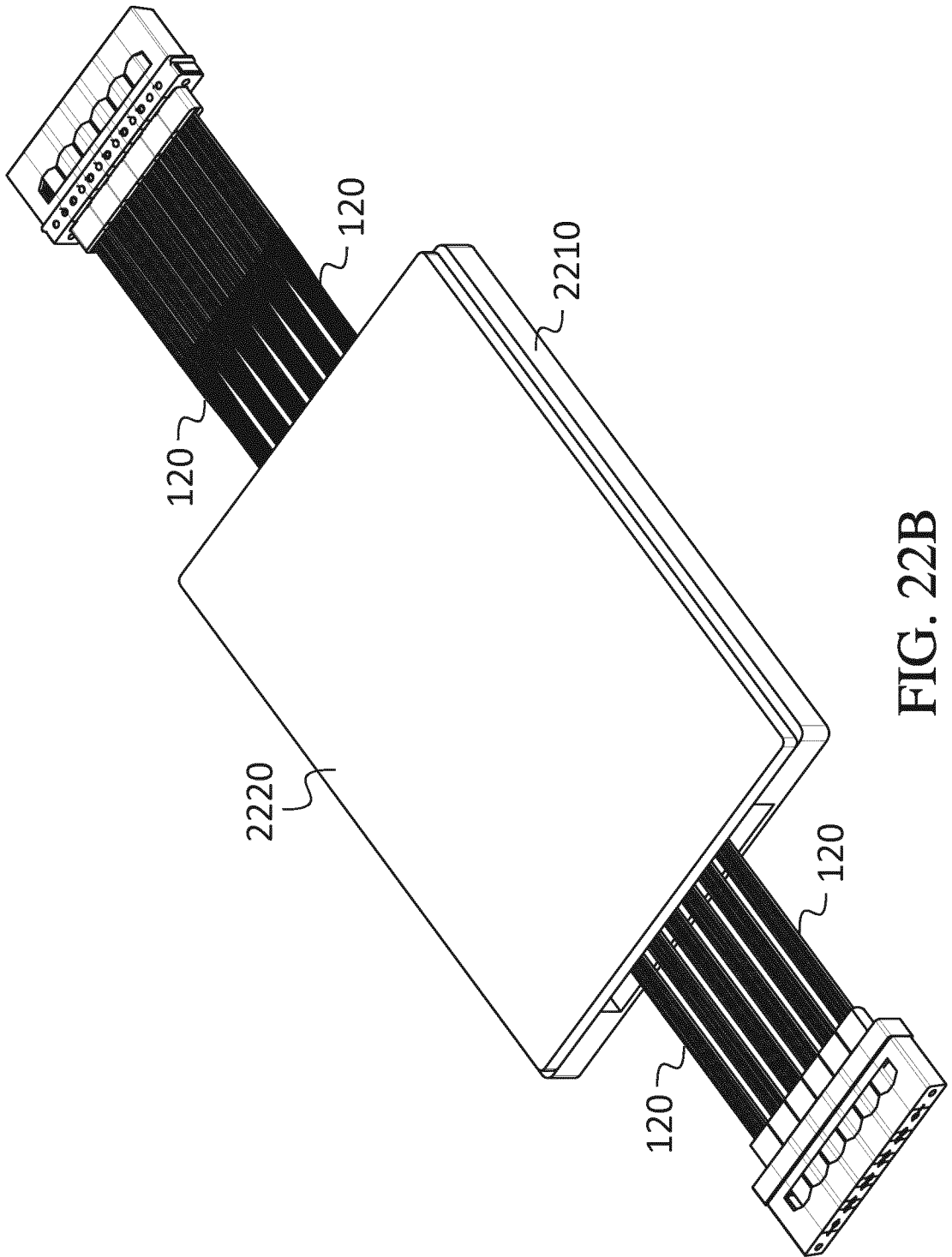


FIG. 22B

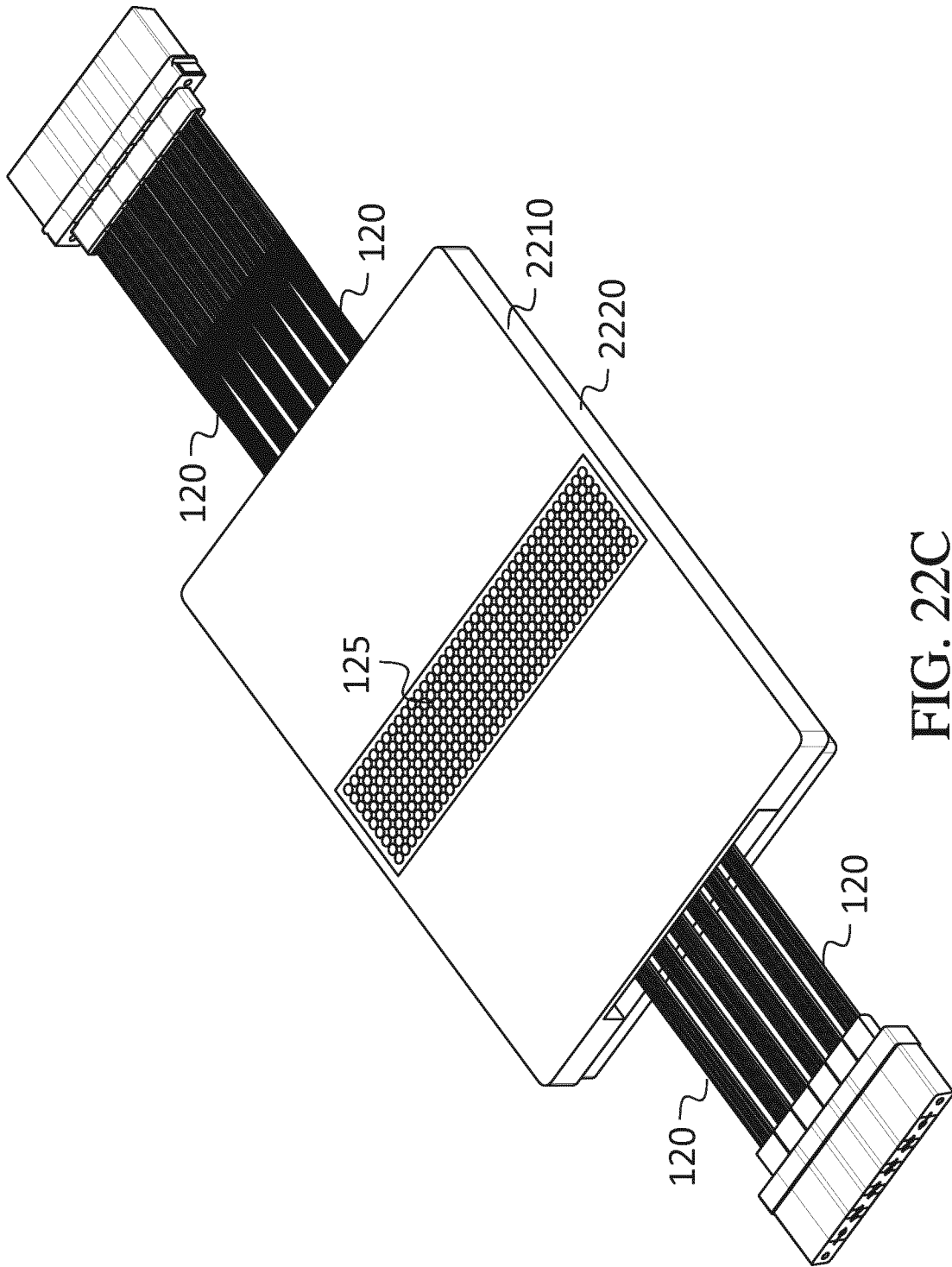


FIG. 22C

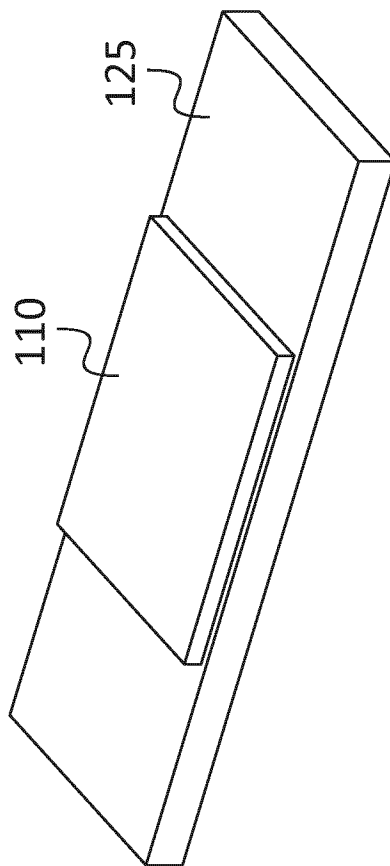


FIG. 22D

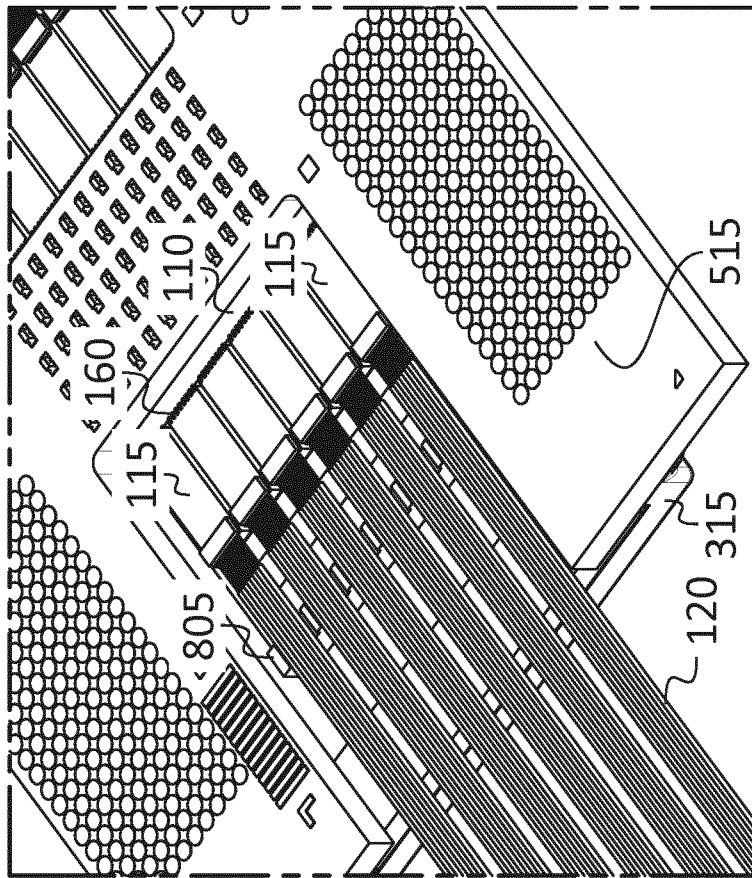


FIG. 23

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/050188

A. CLASSIFICATION OF SUBJECT MATTER
INV. G02B6/42
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2016/085038 A1 (DECKER PATRICK J [US] ET AL) 24 March 2016 (2016-03-24) paragraph [0031] - paragraph [0036]; figure 1	1,2,5-8, 10-12,17 3,4,9, 13-16, 18,19
A	----- US 2005/248019 A1 (CHAO TE-TSUNG [TW] ET AL) 10 November 2005 (2005-11-10) paragraph [0047] - paragraph [0053]; figure 6	1-19
A	----- US 2016/111407 A1 (KRASULICK STEPHEN B [US]) 21 April 2016 (2016-04-21) paragraph [0071]; figure 7C	1-19
A	----- US 8 971 676 B1 (THACKER HIREN D [US] ET AL) 3 March 2015 (2015-03-03) column 7, line 26 - line 67; figure 7 -----	1-19

Further documents are listed in the continuation of Box C.

See patent family annex.

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- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search

19 March 2018

Date of mailing of the international search report

05/04/2018

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Authorized officer

Andreassen, Jon

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2018/050188

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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			CN 101110411 A 23-01-2008
			JP 2005322887 A 17-11-2005
			TW I257162 B 21-06-2006
			US 2005248019 A1 10-11-2005

US 2016111407	A1	21-04-2016	NONE

US 8971676	B1	03-03-2015	US 8971676 B1 03-03-2015
			US 2015098677 A1 09-04-2015
