(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 452 117 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **91303179.5**

(51) Int. Cl.[5]: **G09G 1/16**

(22) Date of filing: **10.04.91**

(30) Priority: **11.04.90 GB 9008279**

(43) Date of publication of application:
16.10.91 Bulletin 91/42

(84) Designated Contracting States:
BE CH DE FR GB IT LI NL

(71) Applicant: **A.F.E. DISPLAYS LIMITED**
62 Anchorage Road, Sutton Coldfield
Birmingham B74 4PG, West Midlands (GB)

(72) Inventor: **Evans, Peter**
9, The Grange Upper Longdon,
Staffordshire, (GB)

(74) Representative: **Lucking, David John et al**
FORRESTER & BOEHMERT
Widenmayerstrasse 4
W-8000 München 22 (DE)

(54) Image display system.

(57) An image display system comprises a screen (10) on which, in use, an image (I) is displayed in the form of a plurality of lines (11,12) of information, a plurality of memory means (14,15) each of which contains information to be displayed on the screen (10), processing means (16,17) to process an input signal from a CPU (21) and to write into the memory means (14,15) the information to be displayed, characterised in that the image (I) is displayed as a plurality of groups of information of N lines where N is the number of memory means (14,15), each memory means (14,15) storing information relating to one line (11,12) only of each group of lines.

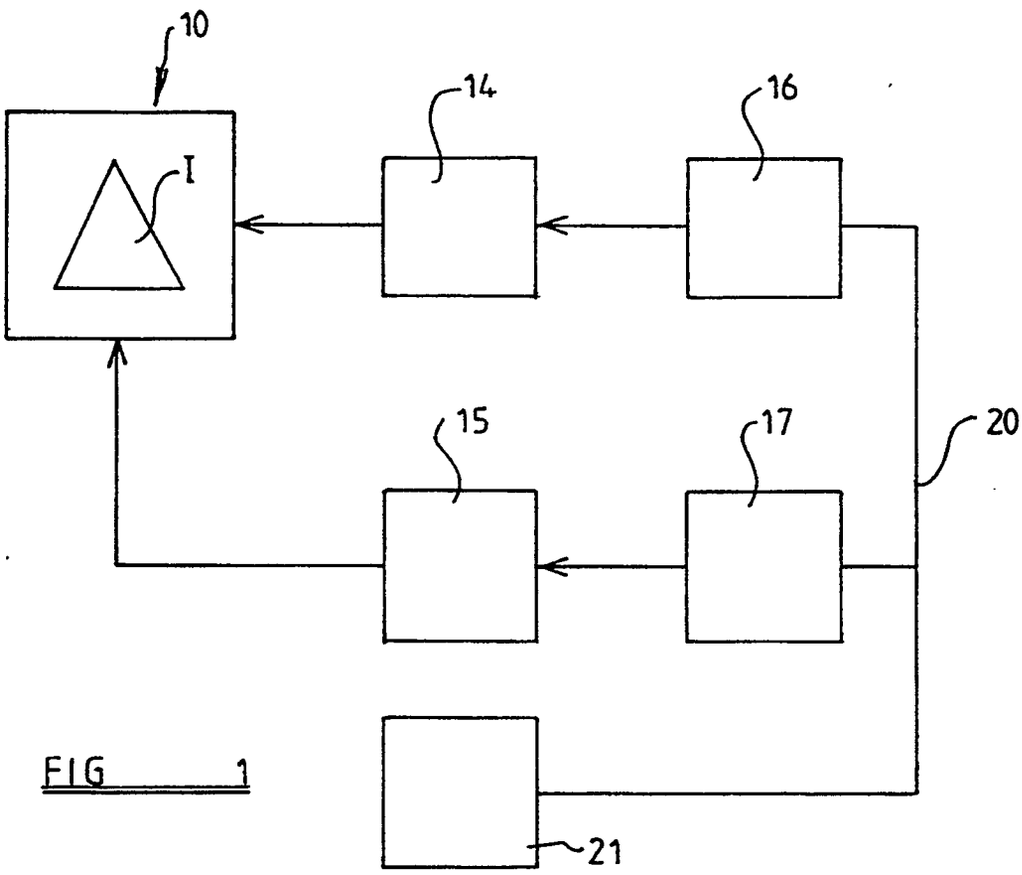

FIG 1

EP 0 452 117 A2

Description of Invention

This invention relates to an image display system. Such systems are known in which a plurality memory means have information written into them by a processing means such that each memory means stores information to enable a portion of an image to be displayed on the screen, the portion containing a plurality of lines less than the total number of lines displayed by the screen, and a plurality of pixels less than the total number of pixels displayed by the screen on each line.

Such systems enable blocks of image to be manipulated on the screen but because the processor means has to process a signal from an upstream central processing unit (CPU) to enable the correct information to be stored in the individual memory means, this is a slow process.

According to one aspect of the invention we provide an image display system comprising a screen on which, in use, an image is displayed in the form of a plurality of lines of information, a plurality of memory means each of which contains information to be displayed on the screen, processing means to process an input signal from a CPU and to write into the memory means the information to be displayed, characterised in that the image is displayed as a plurality of groups of information of N lines where N is the number of memory means, each memory means storing information relating to one line only of each group of lines.

According to a second aspect of the invention we provide a method of operating an image display system according to the first aspect of the invention the method comprising the steps of feeding to the processing means the input signal from the CPU, causing the processing means to write into each of the plurality of memory means information relating to one line of each group of N lines to be displayed on the screen, and feeding the stored information from each of the memory means to the screen where the composite image is displayed.

The invention will now be described with reference to the accompanying drawings in which:

FIGURE 1 is a diagram illustrating the construction of an image display system in accordance with the invention, and,

FIGURE 2 is a view of part of a screen of the system of Figure 1, displaying a composite image.

Referring to the drawings, an image display system comprises a screen 10 (e.g. a visual display unit (VDU)) on which in use an image I is displayed in the form of a plurality of lines 11,12, of information each comprising a row of pixels.

The system further comprises a plurality of memory means, in this example, two memory means indicated at 14 and 15. Each memory means 14,15, stores information which is repeatedly sent to the screen 10 preferably simultaneously, to provide the image I for as long as is required. As will be described in more detail below, memory means 14 stores information relating to part of the image 1 to be displayed, whilst memory means 15 stores information relating to the remainder of the image I to be displayed. For example, each memory means 14,15, may comprise a VRAM comprising a parallel data bus and a serial data bus with the serial data bus being used for the output stream of data to the screen 10.

The information is written into the respective memory means 14,15, by processing means comprising a first processor 16 which writes information into the memory 14, and a second processor 17 which writes information into the memory means 15.

The processors 16,17, are preferably generally identically constructed but alternatively configured such that the processors 16 and 17 are each arranged to respond only to part of an input signal from an upstream central processing unit (CPU) 21 which is also connected to each of the processors 16,17, by a bus 20.

It will be appreciated that the input signal will comprise a stream of information which is to be displayed on the screen 10 as the plurality of lines 11,12.

The system operates so that the processor 16 is responsive to those parts of the input signal relating to every other line 11 of the image I to be displayed, whilst processor 17 is responsive to those parts of the input signal relating to each of the other lines 12 of the image I.

The processor 16 then writes into the memory means 14 information relating only to the lines 11, whilst processor 17 writes into the memory means 15 information relating to the lines 12 only and the memory means 14,15, under the control of their respective processors 16,17, then together provide all the necessary information to the screen 10 to enable the entire composite image I to be displayed.

It has been found that such an arrangement enables the image I to be written faster to memory than has hitherto been possible with arrangements which utilise a plurality of memories but wherein each such memory stores information relating to a block of the image such as the block indicated in dotted lines in figure 2 at B.

As shown in figure 1, the memory means 14,15, may be provided as physically separate units but alternatively, may comprise different areas of a single memory unit which are separately addressable and into which the appropriate line information can individually be written. Also the processors 16,17, may be separate physical units as shown, but alternatively may be provided as a single unit comprising a plurality of processing areas which are each individually responsive to their individual respective line information. However, separate processors 16,17, are preferred.

If desired, instead of the separate processors 16,17, being of identical construction, and being indi-

vidually configured to enable each processor to respond only to the associated part of the input signal, the processors 16,17, may be individually constructed so as to respond to address or scan information contained in the input signal from the CPU 21 so that the processors 16,17, write only the appropriate line information in the corresponding memory 14,15.

In the example described above, only two memory means 14,15, are provided along with a corresponding number of processors 16,17. It will be appreciated that a system in accordance with the invention may have any desired number of memory means and processors such that the processors are able to write into their corresponding memory means 14,15, only that information relating to the lines of the image I for which the memories 14,15, are to store information.

In the generality, where there are N memory means, the screen will display the image I as a plurality of groups of N lines, each memory means storing information relating to one line only of each group of N lines.

The features disclosed in the foregoing description or the accompanying drawings, expressed in their specific forms or in terms of a means for performing the disclosed function, or a method or process for attaining the disclosed result, or a class or group of substances or compositions, as appropriate, may, separately or in any combination of such features, be utilised for realising the invention in diverse forms thereof.

Claims

1. An image display system for displaying an image (I) comprising a screen (10) in the form of a plurality of lines (11,12) of information, wherein a plurality of memory means (14,15) are provided, each of which contains information to be displayed on the screen (10), there being processing means (16,17) to process an input signal from a CPU (21) and to write into the memory means (14,15) the information to be displayed, characterised in that the image (I) is displayed as a plurality of groups of information of N lines where N is the number of memory means (14,15), each memory means (14,15) storing information relating to one line (11,12) only of each group of lines.

2. A system according to claim 1 characterised in that a first memory means (14) stores information relating to the first line (11) of each group of lines, a second memory means (15) stores information relating to the second line (12) of each group of lines and so on for the N memories.

3. A system according to claim 1 or claim 2 characterisd in that the processing means (16,17) comprises a first processor (16)which responds to the input signal from the CPU (21) to write into one of the memory means (14) only the information relating to the respective line (11) information to be stored in that memory means (14), a second processor (17) which responds to the input signal from the CPU (21) to write into another of the memory means (15) only the information relating to the respective line (12) information to be stored in the another memory means (15) and so on for each of the memory means (14,15) whereby there are N processors (16,17), each processor (16,17) writing information into one of the memory means (14,15).

4. A system according to claim 1, claim 2 or claim 3 characterised in that the plurality of memory means (14,15) are provided by a corresponding number of physically separate units.

5. A system according to claim 1, claim 2 or claim 3 characterised in that the plurality of memory means (14,15) are provided by a single memory unit comprising different areas, each area providing one of the memory means (14,15) which is addressable by the processor means (16,17).

6. A system according to any one of the preceding claims characterised in that the processing means (16,17) comprises a plurality of physically separate units to each of which the input signal from the CPU (21) is fed.

7. A system according to any one of claims 3 to 5 appendant to claim 3 characterised in that the processing means (16,17) comprises a single unit which has a plurality of areas which each provide one of the processors (16,17).

8. A system according to claim 7 characterised in that the plurality of separate processor units (16,17) are each of generally identical construction, but each of the processor units (16,17) is arranged to respond only to part of the input signal such that only information relating to the associated image lines (11,12) are written into the corresponding memory means (14,15).

9. A method of operating an image display system according to any one of the preceding claims characterised in that the method comprises the steps of feeding to the processing means (16,17) the input signal from the CPU (21), causing the processing means (16,17) to write into each of the plurality of memory means (14,15) information relating to one line (11,12) of each group of N lines to be displayed on the screen (10), and feed-

ing the stored information from each of the memory means (14,15) to the screen (10) where the composite image is displayed.

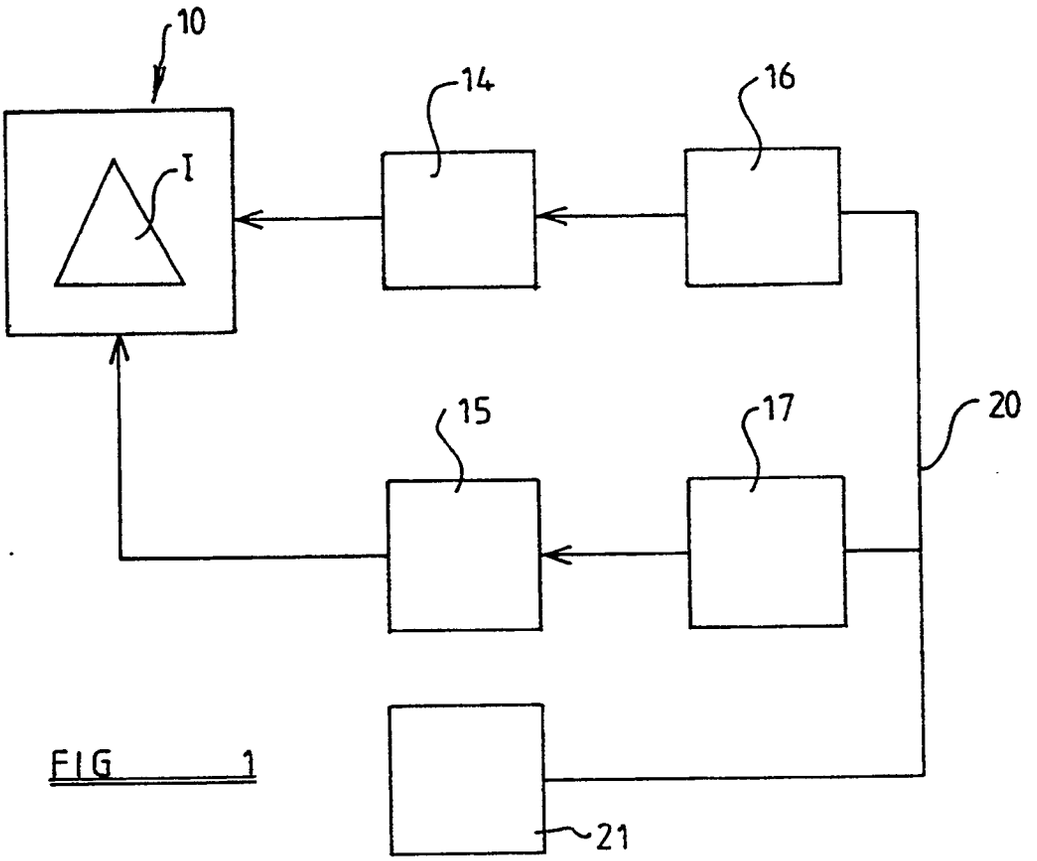

FIG 1

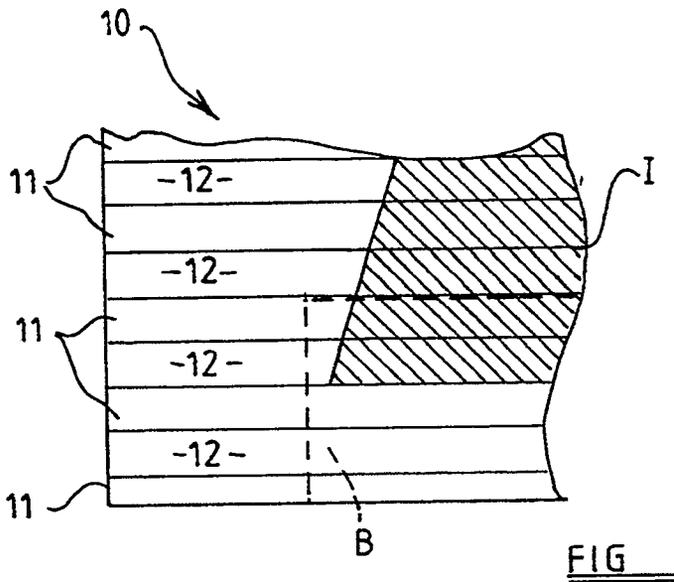

FIG 2