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(54) RESISTANCE VARIABLE MEMORY ELEMENT WITH THRESHOLD DEVICE AND METHOD OF FORMING THE SAME

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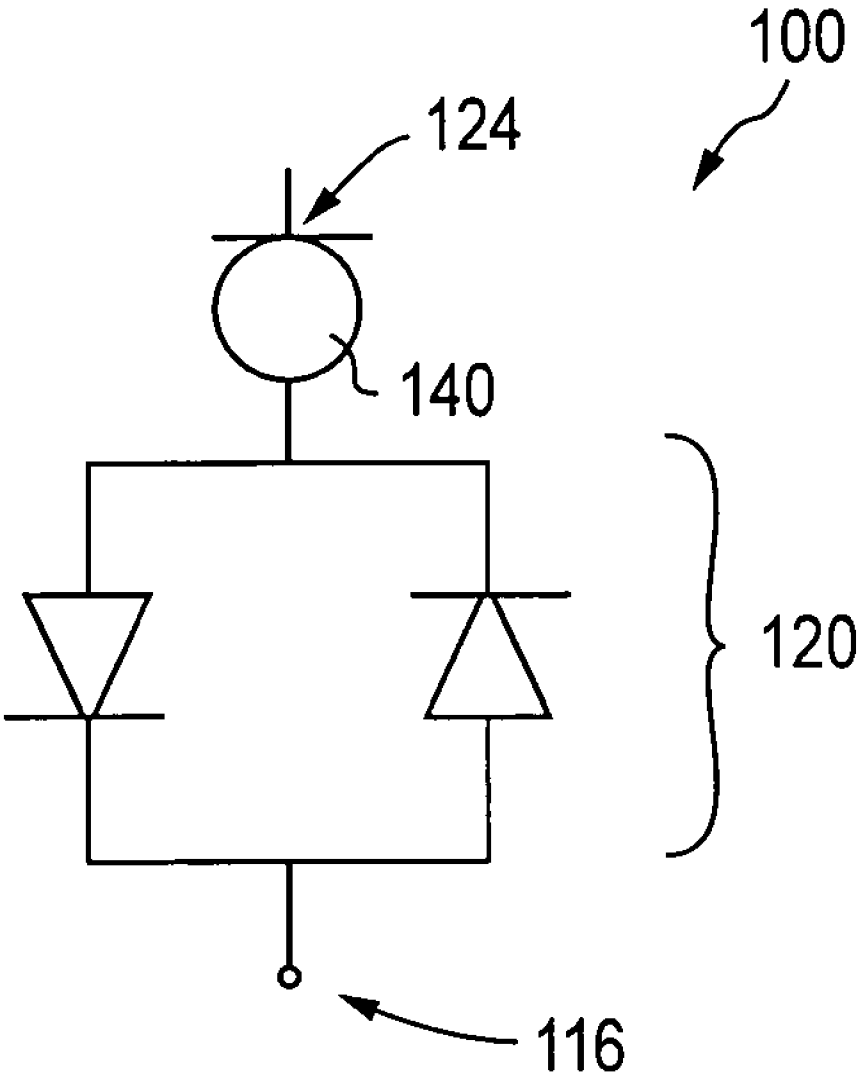
(57) **ABSTRACT**

A memory device having a memory portion connected in series with a threshold device between. The memory portion stores at least one bit of data based on at least two resistance states. The threshold device is configured to switch from a high resistance state to a low resistance state upon application of a voltage and, when the voltage is removed, to re-assume the high resistance state. Additionally, the threshold device can be configured to switch in response to both negative and positive applied voltages across the first and second electrodes. Memory elements having a memory portion and threshold device between first and second electrodes and methods for forming the memory elements are also provided.



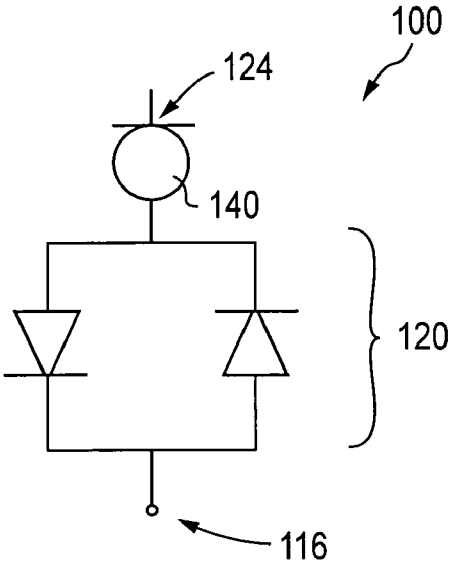

100
124
140
120
116

FIG. 1

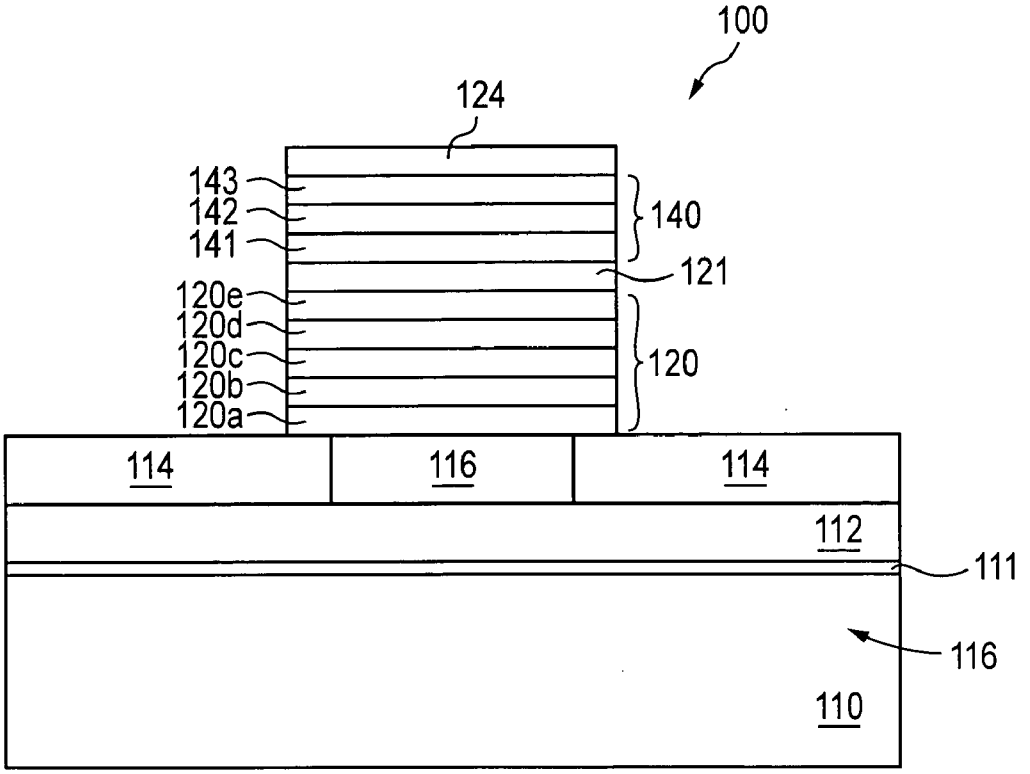

100
124
143
142
141
140
121
120e
120d
120c
120b
120a
120
114
116
114
112
111
116
110

FIG. 2

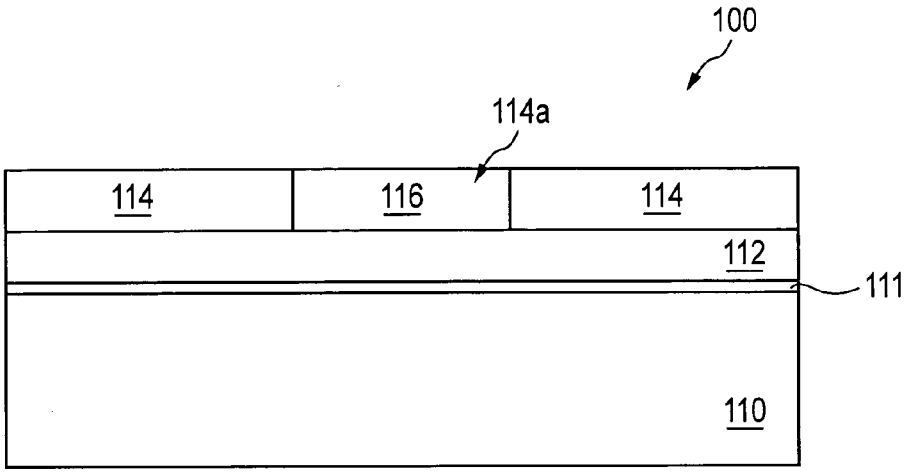

100
114a
114
116
114
112
111
110

FIG. 3A

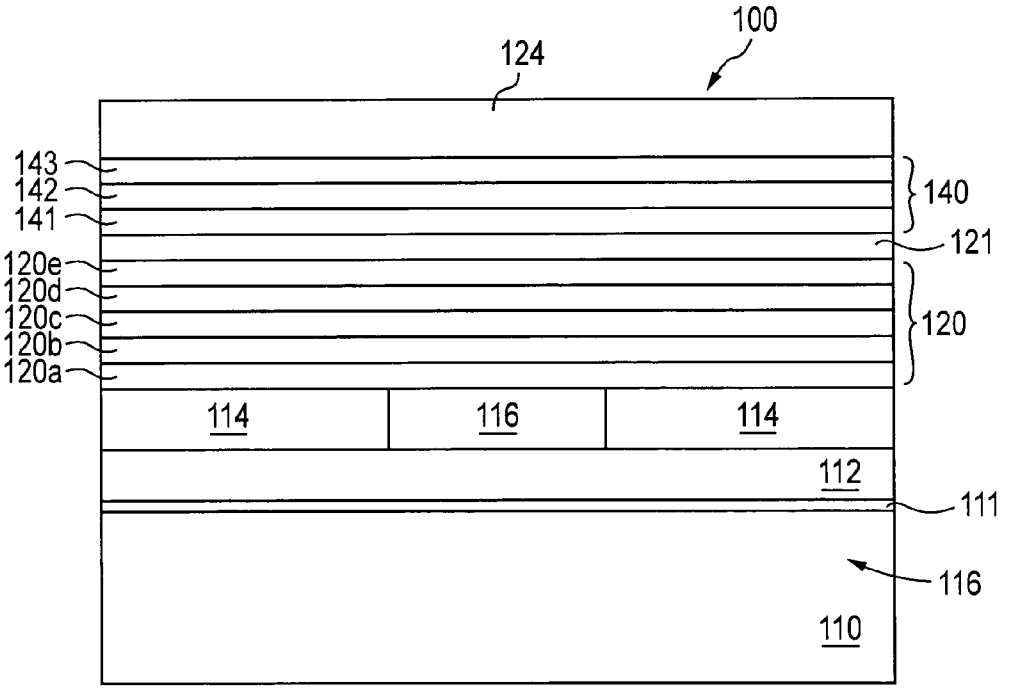

100
124
143
142
141
140
121
120e
120d
120c
120b
120a
120
114
116
114
112
111
116
110

FIG. 3B

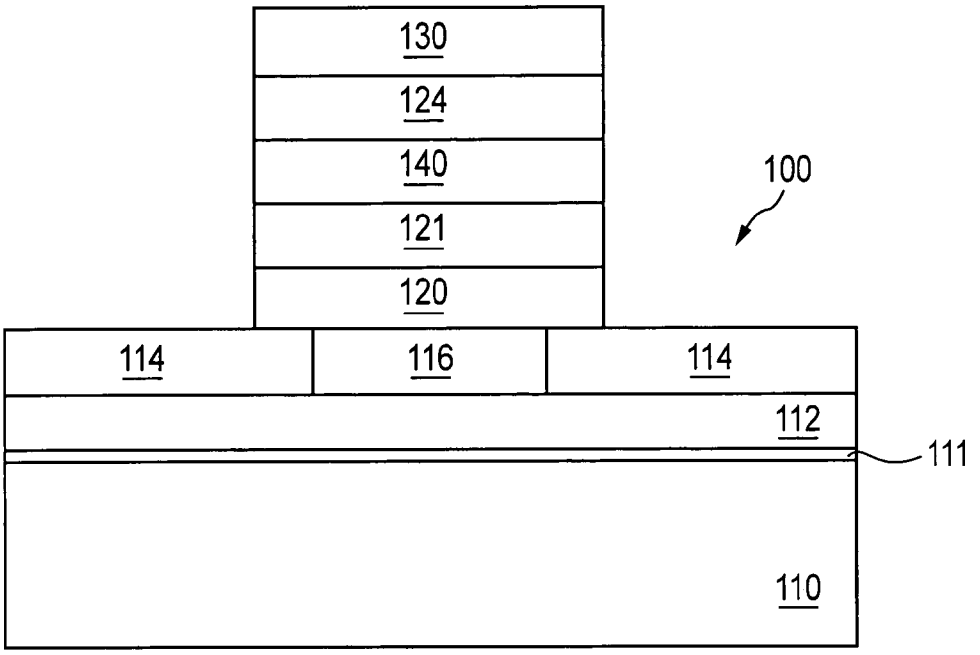

130
124
140
121
120
100
114
116
114
112
111
110

FIG. 3C

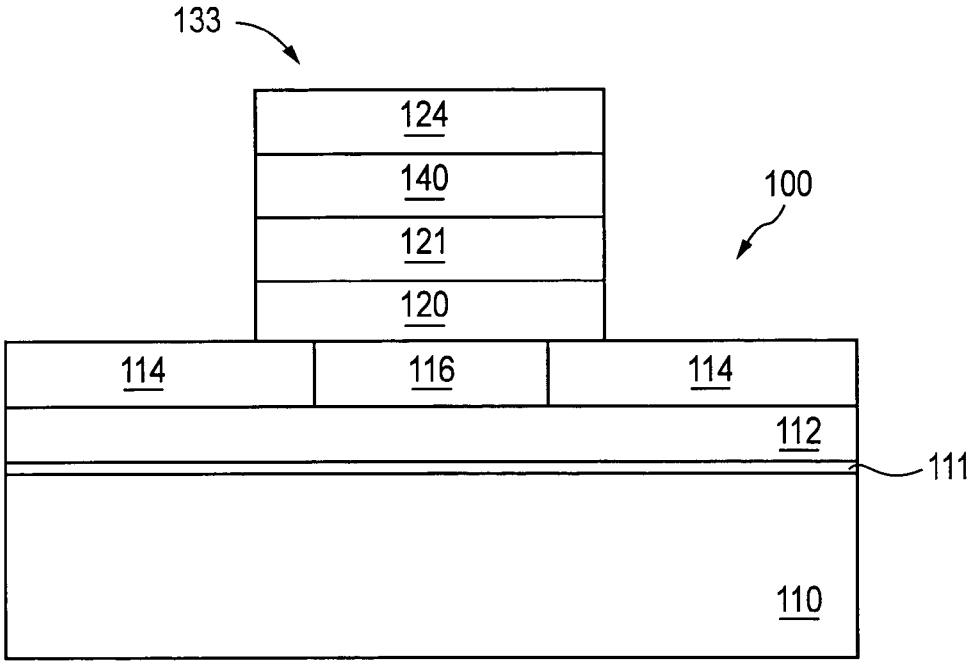

133
124
140
121
120
100
114
116
114
112
111
110

FIG. 3D

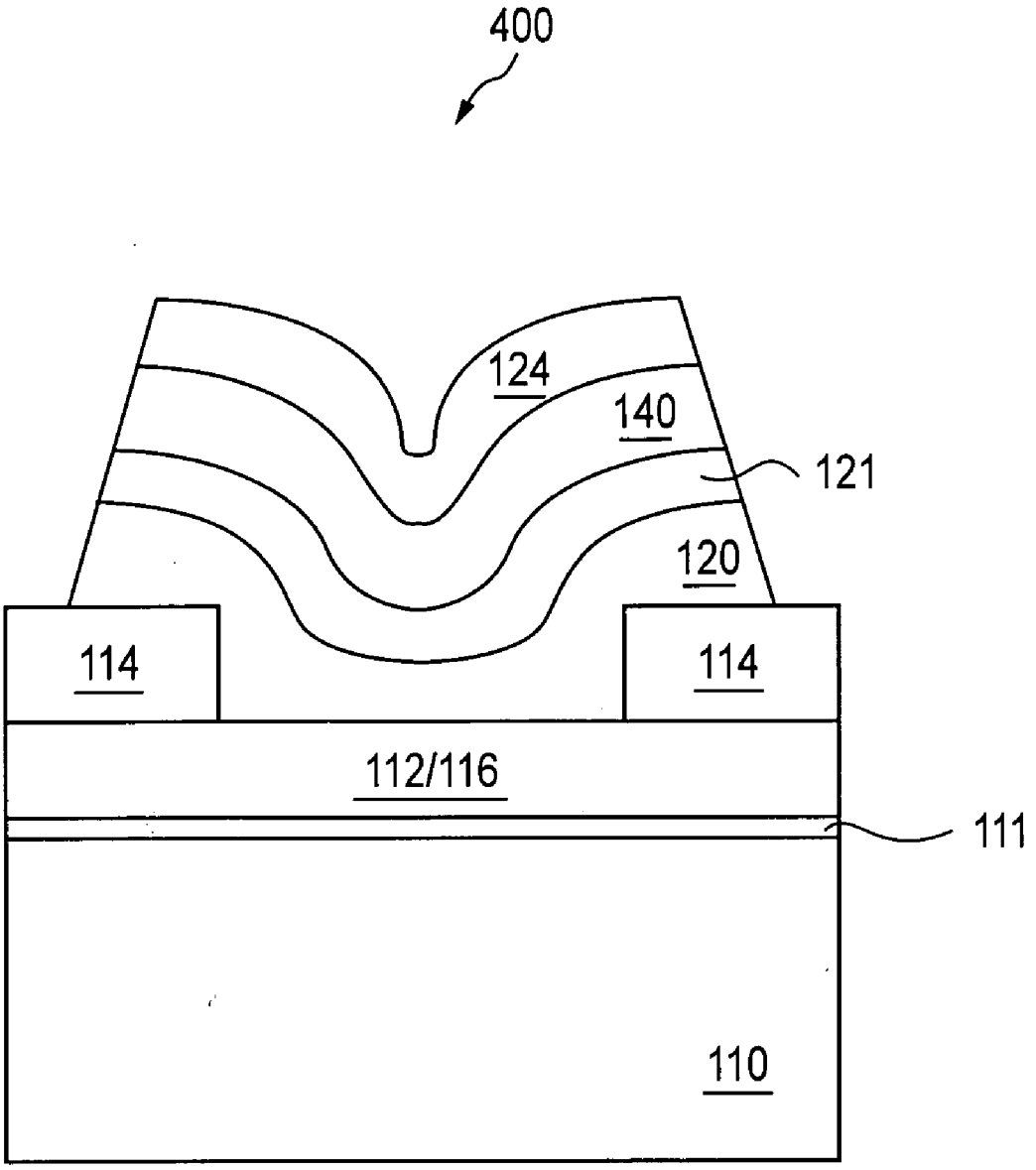


FIG. 4

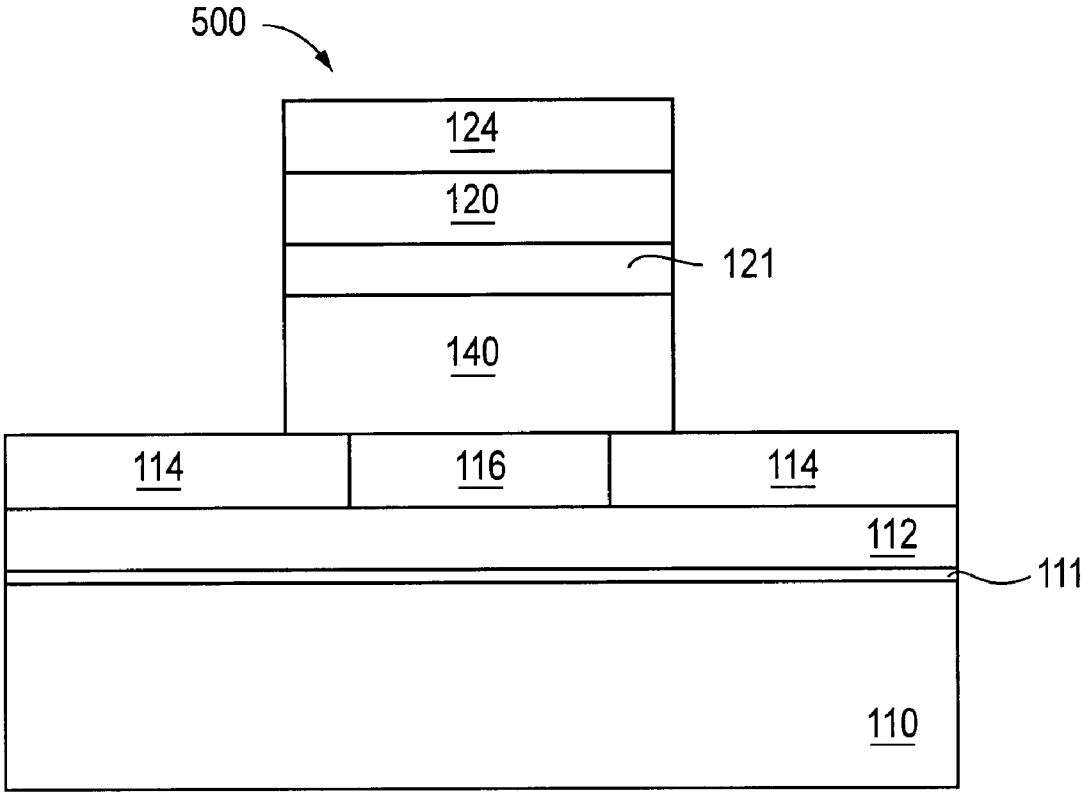


FIG. 5

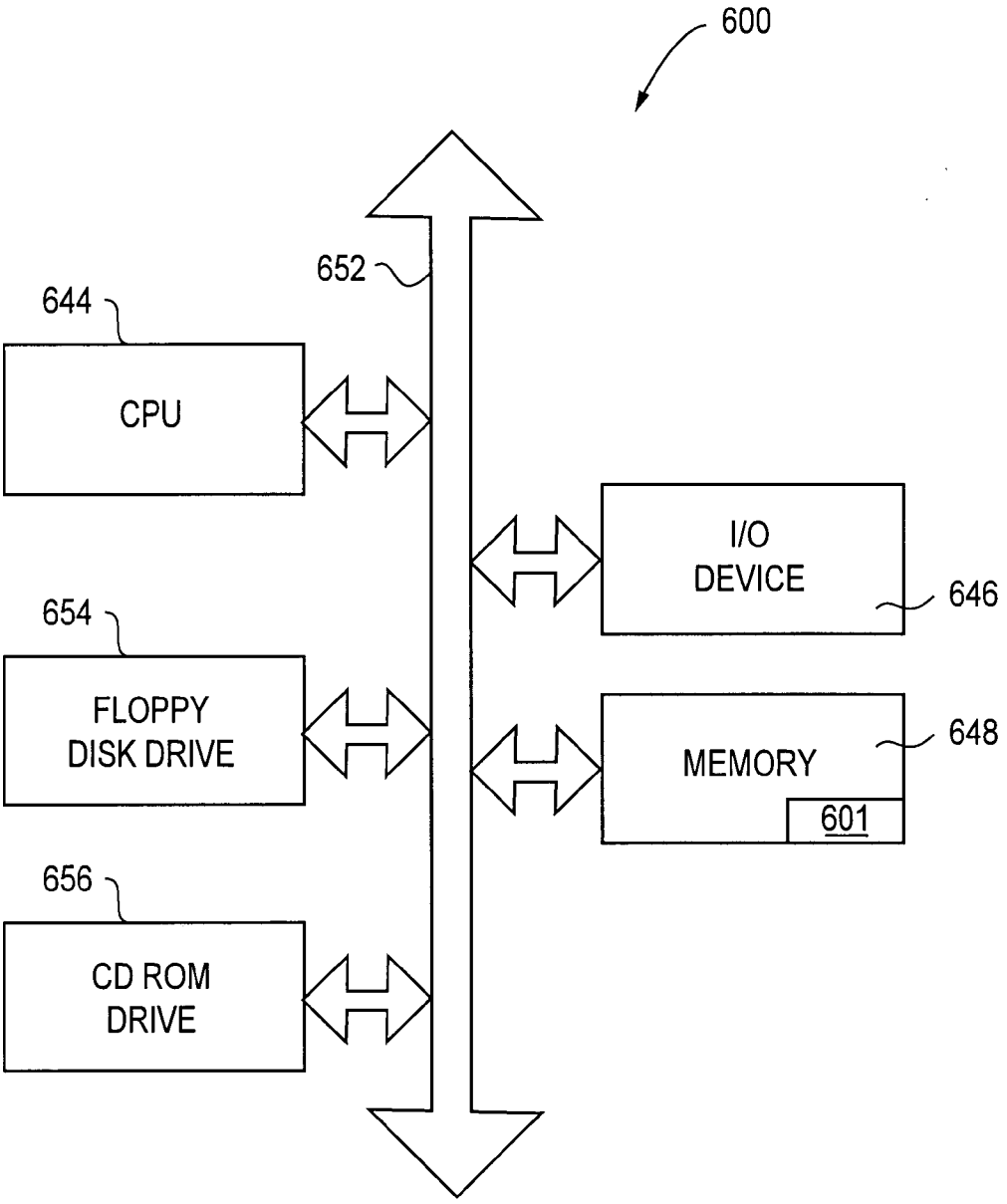

600
652
644
CPU
I/O
DEVICE
646
654
FLOPPY
DISK DRIVE
MEMORY
648
601
656
CD ROM
DRIVE

FIG. 6

RESISTANCE VARIABLE MEMORY ELEMENT WITH THRESHOLD DEVICE AND METHOD OF FORMING THE SAME

FIELD OF THE INVENTION

[0001] The invention relates to the field of random access memory (RAM) devices formed using a resistance variable material.

BACKGROUND OF THE INVENTION

[0002] Resistance variable memory elements, which include electrokinetic memory elements using chalcogenides, have been investigated for suitability as semi-volatile and non-volatile random access memory devices. A representative chalcogenide resistance variable memory element is disclosed in U.S. Pat. No. 6,348,365 to Moore and Gilton.

[0003] In one type of chalcogenide resistance variable memory element, a conductive material, for example, silver and copper, is incorporated into a chalcogenide glass. The resistance of the chalcogenide glass can be programmed to stable higher resistance and lower resistance states. An unprogrammed chalcogenide variable resistance element is normally in a higher resistance state. A write operation programs the element to a lower resistance state by applying a voltage potential across the chalcogenide glass and forming a conductive pathway. The element may then be read by applying a voltage pulse of a lesser magnitude than required to program it; the resistance across the memory device is then sensed as higher or lower to define two logic states.

[0004] The programmed lower resistance state of a chalcogenide variable resistance element can remain intact for an indefinite period, typically ranging from hours to weeks, after the voltage potentials are removed; however, some refreshing may be useful. The element can be returned to its higher resistance state by applying a reverse voltage potential of about the same order of magnitude as used to write the device to the lower resistance state. Again, the higher resistance state is maintained in a semi- or non-volatile manner once the voltage potential is removed. In this way, such an element can function as a semi- or non-volatile variable resistance memory having at least two resistance states, which can define two respective logic states, i.e., at least a bit of data.

[0005] One exemplary chalcogenide resistance variable device uses a germanium selenide (i.e., Ge_xSe_{100-x}) chalcogenide glass as a backbone between first and second electrodes. The germanium selenide glass has, in the prior art, incorporated silver (Ag) and silver selenide ($Ag_{2+/-x}Se$) layers in the memory element. The element is programmed by applying a sufficient voltage across the electrodes to cause the formation of a conductive path between the two electrodes, by virtue of a conductor (i.e., such as silver) that is present in metal ion laced glass layer.

[0006] It would be desirable to have a structure and method for adjusting the programming voltages used for a memory element.

BRIEF SUMMARY OF THE INVENTION

[0007] Embodiments of the invention include memory devices having a memory portion connected in series with a threshold device between the electrodes is provided. The memory portion stores at least one bit of data based on at least two resistance states. The threshold device is configured to switch from a high resistance state to a low resistance state upon application of a voltage and, when the voltage is removed, to re-assume the high resistance state. Additionally, the threshold device can be configured to switch in response to both negative and positive applied voltages across the first and second electrodes. Embodiments of the invention also include memory elements having a memory portion and threshold device between first and second electrodes. Methods for forming the memory elements are also provided.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The foregoing and other advantages and features of the invention will become more apparent from the detailed description of exemplary embodiments provided below with reference to the accompanying drawings in which:

[0009] FIG. **1** illustrates a schematic diagram of a memory element according to the invention;

[0010] FIG. **2** illustrates a cross sectional view of a portion of a memory element according to an exemplary embodiment of the invention;

[0011] FIGS. **3**A-**3**D depict the formation of the memory element of FIG. **2** at different stages of processing;

[0012] FIG. **4** illustrates a cross sectional view of a portion of a memory element according to another exemplary embodiment of the invention;

[0013] FIG. **5** illustrates a cross sectional view of a portion of a memory element according to another exemplary embodiment of the invention; and

[0014] FIG. **6** is a block diagram of a system including a memory element according to an exemplary embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] In the following detailed description, reference is made to various specific embodiments of the invention. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that other embodiments may be employed, and that various structural, logical and electrical changes may be made without departing from the spirit or scope of the invention.

[0016] The term "substrate" used in the following description may include any supporting structure including, but not limited to, a semiconductor substrate that has an exposed substrate surface. A semiconductor substrate should be understood to include silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. When reference is made to a semiconductor substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation. The substrate need not be semiconductor-based, but may be any support structure suitable for supporting an integrated circuit, including, but

not limited to, metals, alloys, glasses, polymers, ceramics, and any other supportive materials as is known in the art.

[0017] The invention is now explained with reference to the figures, which illustrate exemplary embodiments and throughout which like reference numbers indicate like features. FIG. **1** is a schematic diagram of the memory element **100** according to the invention. A threshold device **120** is connected in series with the memory portion **140** of the memory element **100**. Specifically, in FIG. **1**, the threshold device **120** is disposed between a first electrode **116** and a second electrode **124** of the element **100**. Schematically, the threshold device **120** is depicted by two diodes in parallel with opposite orientations.

[0018] The threshold device **120** is configured to have a switching characteristic with respect to both a positive and negative voltage, such that the memory portion **140** of the element **100** can be written and erased when the positive and negative voltages are applied. Upon application of a positive or negative voltage, the threshold device **120** switches from a high resistance state to a stable low resistance state so that the voltage drop across the threshold device **120** is constant. When the positive or negative voltage is removed, the threshold device **120** re-assumes the high resistance state. Preferably, the threshold device **120** does not exhibit any leakage current.

[0019] By placing the threshold device **120** in series with the memory portion **140** of the memory element **100**, it is possible to use a voltage with a greater magnitude to program (i.e., write and erase) the memory portion **140**. For example, if the threshold device **120** has a threshold voltage greater than the voltage needed to write the memory portion **140** to a high or low resistance state, the threshold device **120** would effectively cause an increase in the voltage magnitude needed to write the memory portion **140**. The programming voltage can thus be increased up to about 1 to 2 Volts or more. Additionally, the threshold device **120** can protect the memory portion **140** from spurious noise, since a voltage of a greater magnitude will be needed to write the memory portion **140**.

[0020] According to an exemplary embodiment, the threshold voltage of the threshold device **120** has a greater magnitude in one of the positive or negative directions. For example, where an increase in the write voltage in the positive direction is desired, the voltage of the threshold device **120** is greater in the positive direction and the memory portion is read using a negative voltage. The magnitude of the threshold voltage of the threshold device **120** is sufficiently low in the negative direction to allow the memory portion **140** to be read without causing the resistance state of the memory portion **140** to be changed. Similarly, where an increase in the write voltage in the negative direction is desired, the voltage of the threshold device **120** can be greater in the negative direction and the memory portion can be read using a positive voltage.

[0021] According to an exemplary embodiment of the invention, the threshold device **120** is one or more layers of material. The material or materials selected for the threshold device **120** are preferably configurable to be responsive to both a positive and negative voltage. Alternatively, if a material or set of materials is responsive to only one voltage type (e.g., positive), a pair of the materials or material sets arranged in opposite orientation may be used to achieve a threshold device **120** responsive to both a positive and negative switching voltage, as schematically depicted in FIG. **1**.

[0022] FIG. **2** illustrates a cross-sectional view of the memory element **100** according to an exemplary embodiment of the invention. The element **100** shown in FIG. **2** is supported by a substrate **110**. Over the substrate **110**, though not necessarily directly so, is a conductive address line **112**, which serves as an interconnect for the element **100** shown and a plurality of other similar devices of a portion of a memory array of which the shown element **100** is a part. It is possible to incorporate an optional insulating layer **111** between the substrate **110** and address line **112**, and this may be preferred if the substrate **110** is semiconductor-based. The conductive address line **112** can be any material known in the art as being useful for providing an interconnect line, such as doped polysilicon, silver (Ag), gold (Au), copper (Cu), tungsten (W), nickel (Ni), aluminum (Al), platinum (Pt), titanium (Ti), and other materials. Over the address line **112** is a first electrode **116**, which is defined within an insulating layer **114**, which is also over the address line **112**. This electrode **116** can be any conductive material that will not migrate into the layer formed directly over the electrode **116** (e.g., layer **120***a*, described below), but is preferably tungsten (W). The insulating layer **114** can be, for example, silicon nitride (Si_3N_4), a low dielectric constant material, an insulating glass, or an insulating polymer, but is not limited to such materials.

[0023] In the embodiment shown in FIGS. **1** and **2**, the threshold device **120** is formed over the first electrode **116**. In the illustrated embodiment, the threshold device **120** is a stack of layers **120***a*, **120***b*, **120***c*, **120***d*, **120***e*. For simplicity, in certain figures, the individual component layers of the threshold device **120** are not shown. Layers **120***a*, **120***c* and **120***e* are each a chalcogenide material, for example, germanium selenide (Ge_xSe_{100-x}), and more particularly $Ge_{60}Se_{40}$. Layers **120***a*, **120***c* and **120***e* may be a same chalcogenide material and may have the same stoichiometry, but may also be different. Layer **120***b* is a metal-chalcogenide layer, and in the illustrated embodiment is tin-selenide. Layer **120***d* is a metal layer and in the illustrated embodiment is copper. The threshold device **120**, however, can include additional layers and/or different materials, which are configured as described above.

[0024] An optional conductive layer **121** is formed over the threshold device **120**. The conductive layer **121** can be any suitable conductive material, and in the illustrated embodiment is tungsten.

[0025] The memory portion **140** (i.e., the portion for storing a bit of data based on at least two resistance states, which can define two respective logic states) of the memory element **100** is formed over the optional conductive layer **121**. The memory portion **140** includes one or more layers of resistance variable material and can further include one or more layers of other materials such as, for example, metal. In the illustrated embodiment, the memory portion **140** is a stack of layers and includes, for example, a chalcogenide material layer **141**, a tin-chalcogenide layer **142**, and an optional metal layer **143**. For simplicity, in certain figures the individual component layers of the memory portion **140** are not shown. The invention, however, is not limited to such embodiments, and the memory portion **140** can include

additional or fewer layers of other materials suitable for forming a resistance variable memory element. For example, the portion **140** can include a second chalcogenide material layer (not shown) over the metal layer **143**. The second chalcogenide layer may be a same material as the chalcogenide layer **141** or a different material.

[**0026**] In the illustrated embodiments, the chalcogenide material layer **141** is e.g., germanium selenide (Ge_xSe_{100-x}). The germanium selenide may be within a stoichiometric range of about $Ge_{33}Se_{67}$ to about $Ge_{60}Se_{40}$. The chalcogenide material layer **141** may be between about 100 Å and about 1000 Å thick, e.g., about 300 Å thick. Layer **141** need not be a single layer, but may also be comprised of multiple chalcogenide sub-layers having the same or different stoichiometries.

[**0027**] Over the chalcogenide material layer **141** is an optional layer of metal-chalcogenide **142**, such as tin-chalcogenide (e.g., tin selenide ($Sn_{1+/-x}Se$, where x is between about 1 and about 0)), or silver-chalcogenide (e.g., silver selenide). It is also possible that other chalcogenide materials may be substituted for selenium, such as sulfur, oxygen, or tellurium. The layer **142** in the exemplary embodiment is a layer of tin-chalcogenide layer and may be about 100 Å to about 1000 Å thick; however, its thickness depends, in part, on the thickness of the underlying chalcogenide material layer **141**. The ratio of the thickness of the tin-chalcogenide layer **142** to that of the underlying chalcogenide material layer **141** is preferably between about 5:1 and about 1:3.

[**0028**] An optional metal layer **143** is provided over the tin-chalcogenide layer **142**, with silver (Ag) being the exemplary metal. This metal layer **143** is between about 300 Å and about 500 Å thick. Over the metal layer **143** is the second electrode **124**. The second electrode **124** can be made of the same material as the first electrode **116**, but is not required to be so formed. In the illustrated embodiment, the second electrode **124** is tungsten (W).

[**0029**] FIGS. **3**A-**3**D are cross sectional views of a wafer in various stages of fabrication depicting the formation of the memory element **100** according to an exemplary embodiment of the invention. No particular order is required for any of the actions described herein, except for those logically requiring the results of prior actions. Accordingly, while the actions below are described as being performed in a general order, the order is exemplary only and can be altered if desired. Although the formation of a single memory element **100** is shown, it should be appreciated that the memory element **100** can be one memory element in an array of memory elements, which can be formed concurrently.

[**0030**] As shown by FIG. **3**A, a substrate **110** is initially provided. As indicated above, the substrate **110** can be semiconductor-based or another material useful as a supporting structure. If desired, an optional insulating layer **111** may be formed over the substrate **110**. The optional insulating layer **111** may be silicon oxide, silicon nitride, or other insulating materials. Over the substrate **110** (and optional insulating layer **111**, if desired), the conductive address line **112** is formed by depositing a conductive material, such as doped polysilicon, aluminum, platinum, silver, gold, nickel, titanium, but preferably tungsten. The conductive material is patterned, for instance with photolithographic techniques, and etched to define the address line **112**. The conductive material may be deposited by any technique known in the art, such as sputtering, chemical vapor deposition, plasma enhanced chemical vapor deposition, evaporation, or plating.

[**0031**] An insulating layer **114** is formed over the address line **112**. The insulating layer **114** can be silicon nitride, a low dielectric constant material, or other insulators known in the art, and may be formed by any known method. Preferably, the insulating layer **114** (e.g., silicon nitride) does not allow tin ion migration. An opening **114***a* in the insulating layer **114** is made, for instance by photolithographic and etching techniques, exposing a portion of the underlying address line **112**. A first electrode **116** is formed within the opening **114***a*, by forming a layer of conductive material over the insulating layer **114** and in the opening **114***a*. A chemical mechanical polishing (CMP) step is performed to remove the conductive material from over the insulating layer **114**. Desirably, the first electrode **116** is formed of tungsten.

[**0032**] As shown in FIG. **3**B, the threshold device **120** is formed over the first electrode **116** and insulating layer **114**. In the illustrated embodiment, layer **120***a* is formed over the first electrode **116** and insulating layer **114**, and each of the layers **120***b*, **120***c*, **120***d*, **120***e* of the threshold device **120** is formed consecutively thereafter. Layers **120***a*, **120***c* and **120***e* are each a chalcogenide material, for example, germanium selenide (Ge_xSe_{100-x}), and more particularly $Ge_{60}Se_{40}$. Layers **120***a*, **120***c* and **120***e* may be a same chalcogenide material and may have the same stoichiometry, but may also be different. Formation of the layers **120***a*, **120***c* and **120***e* of the threshold device **120** may be accomplished by any suitable method, for example, by sputtering. Layer **120***b* is a metal-chalcogenide layer, and in the illustrated embodiment is tin-selenide. Layer **120***b* can be formed by any suitable method, e.g., physical vapor deposition, chemical vapor deposition, co-evaporation, sputtering, among other techniques. Layer **120***d* is a metal layer and in the illustrated embodiment is copper and can be formed by any suitable technique.

[**0033**] An optional conductive layer **121** is formed over the threshold device **120**. The conductive layer **121** can be any suitable conductive material and can be formed by any suitable technique. In the illustrated embodiment the conductive layer **121** is copper.

[**0034**] The memory portion **140** of the memory element **100** is formed over the optional conductive layer **121**. In the illustrated embodiment, the memory portion **140** is a stack of layers and includes, for example, a chalcogenide material layer **141**, a tin-chalcogenide layer **142**, and an optional metal layer **143**. In the illustrated embodiments, the chalcogenide material layer **141** is e.g., germanium selenide (Ge_xSe_{100-x}). The germanium selenide may be within a stoichiometric range of about $Ge_{33}Se_{67}$ to about $Ge_{60}Se_{40}$. The chalcogenide material layer **141** is formed to between about 100 Å and about 1000 Å thick, e.g., about 300 Å thick. Layer **141** need not be a single layer, but may also be formed to include multiple chalcogenide sub-layers having the same or different stoichiometries.

[**0035**] An optional layer of metal-chalcogenide **142**, such as tin-chalcogenide (e.g., tin selenide ($Sn_{1+/-x}Se$, where x is between about 1 and about 0)), or silver-chalcogenide (e.g., silver selenide) is formed over the chalcogenide material

layer **141**. The metal-chalcogenide layer **142** can be formed by any suitable method, e.g., physical vapor deposition, chemical vapor deposition, co-evaporation, sputtering, among other techniques. It is also possible that other chalcogenide materials may be substituted for selenium, such as sulfur, oxygen, or tellurium. The layer **142** in the exemplary embodiment is a layer of tin-chalcogenide layer and is formed to be about 100 Å to about 1000 Å thick; however, its thickness depends, in part, on the thickness of the underlying chalcogenide material layer **141**. The chalcogenide material layer **141** and tin-chalcogenide layer **142** are preferably formed such that the ratio of the thickness of the tin-chalcogenide layer **142** to that of the underlying chalcogenide material layer **141** is between about 5:1 and about 1:3.

[**0036**] An optional metal layer **143** is formed by any suitable technique over the tin-chalcogenide layer **142**, with silver (Ag) being the exemplary metal. This metal layer **143** formed to be between about 300 Å and about 500 Å thick.

[**0037**] A conductive material is deposited over the metal layer **143** to form a second electrode **124**. Similar to the first electrode **116**, the conductive material for the second electrode **124** may be any material suitable for a conductive electrode. In one exemplary embodiment the second electrode **124** is tungsten.

[**0038**] Referring to FIG. **3**C, a layer of photoresist **130** is deposited over the second electrode **124** layer, masked and patterned to define a stack **133** of the memory element **100**. An etching step is used to remove portions of layers **120** (**120***a*, **120***b*, **120***c*, **120***d*, **120***e*), **121**, **141**, **142**, **142**, and electrode **124**, with the insulating layer **114** used as an etch stop, leaving stack **133** as shown in FIG. **3**C. The photoresist **130** is removed, leaving the structure shown in FIG. **3**D.

[**0039**] Additional steps may be performed to isolate the memory element **100** from other memory elements and other devices. For example, an insulating layer (not shown) may be formed over the stack **133** of layers **120** (**120***a*, **120***b*, **120***c*, **120***d*, **120***e*), **121**, **141**, **142**, **142**, and electrode **124**. Also, other processing steps can be conducted to electrically couple the element **100** to peripheral circuitry (not shown) and to include the element **100** in an array of memory element, and include such an array in an integrated circuit or processor system, e.g., processor system **600** described below in connection with FIG. **6**.

[**0040**] FIG. **4** illustrates a memory element **400** according to another exemplary embodiment of the invention. In the illustrated memory element **400**, the chalcogenide material (or germanium), tin-chalcogenide, and optional metal layers **120** (**120***a*, **120***b*, **120***c*, **120***d*, **120***e*), **121**, **141**, **142**, **142**, and electrode **124** are formed in a via **128**. The via **128** is formed in an insulating layer **114** over a combined address line and electrode structure **112**/**116**. Layers **120** (**120***a*, **120***b*, **120***c*, **120***d*, **120***e*), **121**, **141**, **142**, **142**, as well as the second electrode **124**, are conformally deposited over the insulating layer **114** and within the via **128**. Layers **120**, **121**, **141**, **142**, **142**, and electrode **124** are patterned to define a stack over the via **128**, which is etched to form the completed memory element **400**. Alternatively, a first electrode **116** that is separate from the underlying address line **112** can be used. Such a separate electrode **116** can be formed in the via **128** prior to the formation of layers **120**, **121**, **141**, **142**, **142**.

[**0041**] FIG. **5** illustrates a memory element **500** according to another exemplary embodiment of the invention. The memory element **500** is similar to the memory element **100**, except that the threshold device **120** and optional conductive layer **121** are formed over the memory portion **140**. The element **500** can be formed as described above in connection with FIGS. **3**A-**3**D, except that the layers **141**, **142**, **143**, **121**, **120** (**120***a*, **120***b*, **120***c*, **120***d*, **120***e*) are formed in a different order to achieve the structure shown in FIG. **5**.

[**0042**] The embodiments described above refer to the formation of only a few possible resistance variable memory element structures in accordance with the invention, which may be part of a memory array. It must be understood, however, that the invention contemplates the formation of other memory structures within the spirit of the invention, which can be fabricated as a memory array and operated with memory element access circuits.

[**0043**] FIG. **6** illustrates a processor system **600** that includes a memory circuit **648**, e.g., a memory device, including a memory array **601**, which employs resistance variable memory elements (e.g., elements **100**, **400**, and/or **500**) according to the invention. The processor system **600**, which can be, for example, a computer system, generally comprises a central processing unit (CPU) **644**, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device **646** over a bus **652**. The memory circuit **648** communicates with the CPU **644** over bus **652** typically through a memory controller.

[**0044**] In the case of a computer system, the processor system **600** may include peripheral devices such as a floppy disk drive **654** and a compact disc (CD) ROM drive **656**, which also communicate with CPU **644** over the bus **652**. Memory circuit **648** is preferably constructed as an integrated circuit, which includes one or more resistance variable memory elements, e.g., elements **100** (FIG. **1**). If desired, the memory circuit **648** may be combined with the processor, for example CPU **644**, in a single integrated circuit.

[**0045**] The above description and drawings are only to be considered illustrative of exemplary embodiments, which achieve the features and advantages of the present invention. Modification and substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the present invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A memory element comprising:

a first electrode;

a second electrode;

a memory portion between the first electrode and the second electrode, the memory portion comprising at least one layer of resistance variable material; and

a threshold device between the first electrode and the second electrode and being connected to the memory portion, the threshold device configured to switch from a high resistance state to a low resistance state upon application of a voltage and, when the voltage is removed, to re-assume the high resistance state.

2. The memory element of claim 1, wherein the threshold device is further configured to switch in response to both negative and positive applied voltages across the first and second electrodes.

3. The memory element of claim 2, wherein the threshold device has a first threshold voltage in response to a positive voltage and a second threshold voltage in response to a negative voltage, and wherein a magnitude of the first threshold voltage is different than a magnitude of the second threshold voltage.

4. The memory element of claim 1, wherein the threshold device comprises a plurality of layers.

5. The memory element of claim 1 wherein the threshold device comprises:

first, second and third layers of germanium selenide;

a layer of tin selenide between the first and second germanium selenide layers; and

a copper layer between the second and third germanium selenide layers.

6. The memory element of claim 5, wherein at least one of the germanium selenide layers comprises $Ge_{60}Se_{40}$.

7. The memory element of claim 1, wherein the memory portion comprises a chalcogenide material layer.

8. The memory element of claim 1, further comprising a conductive layer between the memory portion and the threshold device.

9. The memory element of claim 8, wherein the conductive layer comprises tungsten.

10. The memory element of claim 1, wherein the memory portion is over the threshold device.

11. The memory element of claim 1, wherein the threshold device is over the memory portion.

12. The memory element of claim 1, wherein at least one of the first and second electrodes comprises tungsten.

13. The memory element of claim 1, wherein the memory portion and threshold device are provided within a via in an insulating layer.

14. A memory device, comprising:

an array of memory elements, at least one memory element comprising:

a memory portion for storing at least one bit of data based on two resistance states; and

a threshold device connected in series with the memory portion,

the threshold device configured to switch in response to both negative and positive applied voltages.

15. The memory device of claim 14, wherein the threshold device has a first threshold voltage in response to a positive voltage and a second threshold voltage in response to a negative voltage, and wherein a magnitude of the first threshold voltage is different than a magnitude of the second threshold voltage.

16. The memory device of claim 14, wherein the threshold device is further configured to switch from a high resistance state to a low resistance state upon application of the positive or negative voltage and, when the voltage is removed, to re-assume the high resistance state.

17. The memory device of claim 14, further comprising first and second electrodes, wherein the memory portion and the threshold device are between the first and second electrodes.

18. The memory device of claim 17, wherein the threshold device comprises:

first, second and third layers of germanium selenide;

a layer of tin selenide between the first and second germanium selenide layers; and

a copper layer between the second and third germanium selenide layers.

19. The memory device of claim 18, wherein at least one of the germanium selenide layers comprises $Ge_{60}Se_{40}$.

20. The memory device of claim 17, wherein the memory portion comprises a chalcogenide material layer.

21. The memory device of claim 17, further comprising a conductive layer between the memory portion and the threshold device.

22. The memory device of claim 21, wherein the conductive layer comprises tungsten.

23. The memory device of claim 17, wherein the memory portion is over the threshold device.

24. The memory device of claim 17, wherein the threshold device is over the memory portion.

25. A memory array, comprising:

a plurality of memory elements over a substrate, each memory element comprising:

a first electrode;

a second electrode;

a memory portion between the first electrode and the second electrode, the memory portion comprising at least one layer of resistance variable material; and

a threshold device between the first electrode and the second electrode, the threshold device comprising:

first, second and third layers of germanium selenide;

a layer of tin selenide between the first and second germanium selenide layers; and

a copper layer between the second and third germanium selenide layers.

26. The memory array of claim 25, wherein at least one of the germanium selenide layers comprises $Ge_{60}Se_{40}$.

27. The memory array of claim 25, wherein the memory portion comprises a chalcogenide material layer.

28. The memory array of claim 25, further comprising a conductive layer between the memory portion and the threshold device.

29. The memory array of claim 28, wherein the conductive layer comprises tungsten.

30. The memory array of claim 25, wherein the memory portion is over the threshold device.

31. The memory array of claim 25, wherein the threshold device is over the memory portion.

32. A processor system, comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

a first electrode;

a second electrode;

a memory portion between the first electrode and the second electrode, the memory portion comprising at least one layer of resistance variable material; and

a threshold device between the first electrode and the second electrode and being connected to the memory portion, the threshold device configured to switch from a high resistance state to a low resistance state upon application of a voltage and, when the voltage is removed, to re-assume the high resistance state.

33. The system of claim 32, wherein the threshold device is further configured to switch in response to both negative and positive applied voltages across the first and second electrodes.

34. The system of claim 33, wherein the threshold device has a first threshold voltage in response to a positive voltage and a second threshold voltage in response to a negative voltage, and wherein a magnitude of the first threshold voltage is different than a magnitude of the second threshold voltage.

35. The system of claim 32, wherein the threshold device comprises:

first, second and third layers of germanium selenide;

a layer of tin selenide between the first and second germanium selenide layers; and

a copper layer between the second and third germanium selenide layers.

36. The system of claim 32, wherein the memory portion comprises a chalcogenide material layer.

37. The system of claim 32, further comprising a conductive layer between the memory portion and the threshold device.

38. The system of claim 32, wherein the conductive layer comprises tungsten.

39. The system of claim 32, wherein the memory portion is over the threshold device.

40. The system of claim 32, wherein the threshold device is over the memory portion.

41. A method of forming a memory element, the method comprising the acts of:

forming a first electrode;

forming a second electrode;

forming a memory portion between the first electrode and the second electrode, the memory portion formed comprising at least one layer of resistance variable material; and

forming a threshold device between the first electrode and the second electrode and connected to the memory portion, the threshold device configured to switch from a high resistance state to a low resistance state upon application of a voltage and, when the voltage is removed, to re-assume the high resistance state.

42. The method of claim 41, wherein the threshold device is further configured to switch in response to both negative and positive applied voltages across the first and second electrodes.

43. The method of claim 42, wherein the threshold device is configured to have a first threshold voltage in response to a positive voltage and a second threshold voltage in response to a negative voltage, and wherein a magnitude of the first threshold voltage is different than a magnitude of the second threshold voltage.

44. The method of claim 41, wherein the act of forming the threshold device comprises:

forming first, second and third layers of germanium selenide;

forming a layer of tin selenide between the first and second germanium selenide layers; and

forming a copper layer between the second and third germanium selenide layers.

45. The method of claim 44, wherein at least one of the germanium selenide layers is formed comprising $Ge_{60}Se_{40}$.

46. The method of claim 41, wherein the act of forming the memory portion comprises forming a chalcogenide material layer.

47. The method of claim 41, further comprising the act of forming a conductive layer between the memory portion and the threshold device.

48. The method of claim 47, wherein the conductive layer is formed comprising tungsten.

49. The method of claim 41, wherein the memory portion is formed over the threshold device.

50. The method of claim 41, wherein the threshold device is formed over the memory portion.

51. The method of claim 41, wherein at least one of the first and second electrodes is formed comprising tungsten.

52. The method of claim 41, wherein the memory portion and threshold device are formed within a via in an insulating layer.

53. A method of forming a memory element, the method comprising the acts of:

forming a first electrode;

forming a memory portion over the first electrode, the memory portion formed comprising at least one layer of resistance variable material;

forming a threshold device over the memory portion, the act of forming the threshold device comprising:

forming a first layer of germanium selenide,

forming a layer of tin selenide over the first germanium selenide layer,

forming a second germanium selenide layer over the tin selenide layer,

forming a copper layer over the second germanium selenide layer; and

forming a third germanium selenide layer over the copper layer; and

forming a second electrode over the threshold device.

54. The method of claim 53, wherein at least one of the germanium selenide layers is formed comprising $Ge_{60}Se_{40}$.

55. The method of claim 53, wherein the act of forming the memory portion comprises forming a chalcogenide material layer.

56. The method of claim 53, further comprising the act of forming a conductive layer between the memory portion and the threshold device.

57. The method of claim 56, wherein the conductive layer is formed comprising tungsten.

58. A method of forming a memory element, the method comprising the acts of:

forming a first electrode;

forming a threshold device over the first electrode, the act of forming the threshold device comprising:

forming a first layer of germanium selenide;

forming a layer of tin selenide over the first germanium selenide layer;

forming a second germanium selenide layer over the tin selenide layer;

forming a copper layer over the second germanium selenide layer; and

forming a third germanium selenide layer over the copper layer;

forming a memory portion over the first electrode, the memory portion formed comprising at least one layer of resistance variable material; and

forming a second electrode over the memory portion.

59. The method of claim 58, wherein at least one of the germanium selenide layers is formed comprising $Ge_{60}Se_{40}$.

60. The method of claim 58, wherein the act of forming the memory portion comprises forming a chalcogenide material layer.

61. The method of claim 58, further comprising the act of forming a conductive layer between the memory portion and the threshold device.

62. The method of claim 61, wherein the conductive layer is formed comprising tungsten.

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