(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 January 2022 (20.01.2022)

WIPO | PCT

(10) International Publication Number
WO 2022/013589 A1

(51) International Patent Classification:
G11C 13/00 (2006.01) *G06F 12/02* (2006.01)
G06F 11/10 (2006.01)

(21) International Application Number:
PCT/IB2020/020035

(22) International Filing Date:
14 July 2020 (14.07.2020)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **MICRON TECHNOLOGY, INC** [US/US]; 8000 South Federal Way, Boise, Idaho 83716-9632 (US).

(72) Inventors: **MUZZETTO, Riccardo**; Via Gilera, 134, 20862 Arcore (MB) (IT). **DI VINCENZO, Umberto**; Via Giovanni Falcone, 12a, 24042 Capriate San Gervasio (BG) (IT). **BEDESCHI, Ferdinando**; Via Porta D'Arnolfo, 6, 20853 Biassono (MB) (IT).

(74) Agent: **HARRIS, PHILIP** et al.; Holland & Hart LLP, P.O. Box 11583, Salt Lake City, Utah 84147 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: METHODS AND SYSTEMS FOR IMPROVING ACCESS TO MEMORY CELLS

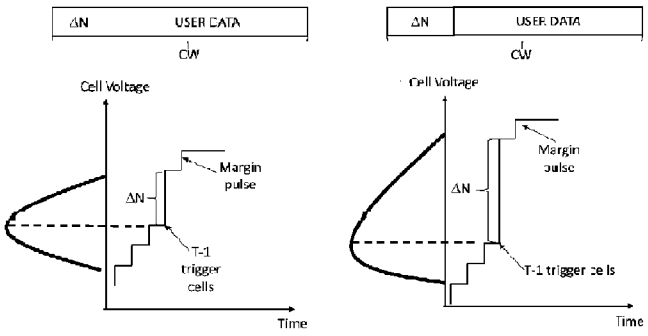

FIG. 5A

(57) Abstract: The present disclosure relates a method for an improved accessing operation of memory cells, the method comprising storing a set of user data and additional data information in a plurality of memory cells of a memory array, the additional data information being representative of a voltage difference between a first threshold voltage and a second threshold voltage of the memory cells of the set of user data programmed to a first logic state, wherein the first threshold voltage is a voltage to activate a preset number of memory cells programmed to the first logic state, and wherein the second threshold voltage is a voltage to activate memory cells programmed to the first logic state having a threshold voltage whose magnitude is higher than the first threshold voltage and is based on the statistical distribution of the threshold voltages of the memory cells of the set of user data.

WO 2022/013589 A1

Title: METHODS AND SYSTEMS FOR IMPROVING ACCESS TO MEMORY CELLS

DESCRIPTION

TECHNICAL FIELD

[001] The present disclosure relates generally to operating an array memory of memory cells, and more particularly to improved write-based methods and systems for accessing memory cells.

BACKGROUND

[002] Memory devices are used in many electronic systems such as mobile phones, personal digital assistants, laptop computers, digital cameras and the like. Various types of memory devices exist, including magnetic hard disks, random access memory (RAM), read only memory (ROM), dynamic RAM (DRAM), synchronous dynamic RAM (SDRAM), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), resistive RAM (RRAM), flash memory, phase change memory (PCM), and others. Memory devices may be volatile or non-volatile. Nonvolatile memories retain their contents when power is switched off, making them good choices in memory devices for storing information that is to be retrieved after a system power-cycle. In particular, non-volatile memory cells may maintain their stored logic state for extended periods of time even in the absence of an external power source. Volatile memory cells may lose their stored state over time unless they are periodically refreshed by an external power source.

[003] Information is stored by programming different states of a memory device. For example, binary devices have two states, often denoted by a logic “1” or a logic “0.” In other systems, more than two states may be stored. To access the stored information, a component of the memory device may read, or sense, the stored state. To store information, a component of the memory device may write, or program, the logic state.

[004] Improving memory devices, generally, may include increasing memory cell density, increasing read/write speeds, increasing reliability, increasing data retention, reducing power consumption, reducing manufacturing costs, as well as scaling smaller than traditional devices (which may lead to relatively high rates of errors), and the like.

[005] A more robust read technique may be desired to increase memory devices performances and reliability when memory cells exhibit variable electrical characteristics, in particular memory devices having a three-dimensional (3D) array of memory cells.

BRIEF DESCRIPTION OF THE DRAWINGS

[006] Figure 1 is an exemplary block scheme illustrating an exemplary memory cell that can be read according to embodiments of the present disclosure;

[007] Figure 2 schematically illustrates a portion of an exemplary memory cell array;

[008] Figure 3 illustrates an example of data pattern supporting a reading operation according to an embodiment of the present disclosure;

[009] Figure 4 schematically illustrates examples of threshold voltage distributions that support the reading operation according to embodiments of the present disclosure;

[010] Figures 5A and 5B schematically illustrate threshold voltage distributions of memory cells programmed to a logic state, as well as the corresponding read voltages according to embodiments of the present disclosure;

[011] Figure 6 is an exemplary scheme illustrating a technique for storing a programming voltage according to an embodiment of the present disclosure;

[012] Figure 7 is a block diagram illustrating an architecture for storing a programming voltage according to an embodiment of the present disclosure;

[013] Figure 8 is a flow diagram representing steps of a method for reading an array of memory cells according to the present disclosure;

[014] Figures 9A and 9B are flow diagrams representing respective steps of a method for programming an array of memory cells according to the present disclosure; and

[015] Figure 10 shows a schematic block diagram of a system including a memory device according to the disclosure.

DETAILED DESCRIPTION

[016] With reference to those drawings, methods and systems for an improved accessing operation of memory cells will be disclosed herein.

[017] In the following detailed description, numerous specific details are set forth to provide a thorough understanding of claimed subject matter. However, it will be understood by those skilled in the art that claimed subject matter may be practiced without these specific details. In other instances, methods, apparatuses and/or systems that would be known by one of ordinary skill have not been described in detail so as not to obscure claimed subject matter.

[018] Nonvolatile memories retain their contents when power is switched off, making them good choices for storing information that is to be retrieved after a system power-cycle. A Flash memory is a type of nonvolatile memory that retains stored data and is characterized by a very fast access time. Moreover, it can be erased in blocks instead of one byte at a time. Each erasable block of memory comprises a plurality of nonvolatile memory cells arranged in a matrix of rows and columns. Each cell is coupled to an access line and/or a data line. The cells are programmed and erased by manipulating the voltages on the access and data lines. Flash memories are well established and well suited for mass storage applications; however, their performances do not meet present day most demanding applications. New technologies, for example 3D Cross Point (3DXPoint) memories and Self-Selecting Memories (SSM) have better

performances, for example in terms of access time and access granularity (data may be programmed and read with page, word or – in principle – even bit granularity). Accessing data during a read operation is more and more challenging with scaled technologies and the present disclosure provides for methods and systems for improved access operations.

[019] Figure 1 illustrates a block scheme of an exemplary assembly 100 comprising a memory cell 100' that can be arranged in an array and then programmed and read according to the present disclosure.

[020] In the embodiment illustrated in figure 1, the memory cell 100' includes a storage material 102 between access lines 104 and 106. The access lines 104, 106 electrically couple the memory cell 100' with circuitry 142 that writes to and reads from the memory cell 100'. The term "coupled" can refer to elements that are physically, electrically, and/or communicatively connected either directly or indirectly, and may be used interchangeably with the term "connected" herein. Physical coupling can include direct contact. Electrical coupling includes an interface or interconnection that allows electrical flow and/or signaling between components. Communicative coupling includes connections, including wired and wireless connections, that enable components to exchange data.

[021] In one embodiment, the storage material 102 includes a self-selecting material that exhibits memory effects. A self-selecting material is a material that enables selection of a memory cell in an array without requiring a separate selector element. Thus, figure 1 illustrates the storage material 102 as a "selector/storage material." A material exhibits memory effects if circuitry for accessing memory cells can cause the material to be in one of multiple states (e.g., via a write operation), and later determine the programmed state (e.g., via a read operation). Circuitry for accessing memory cells (e.g., via read and write operations) is referred to generally as "access circuitry," and is discussed further below with reference to access circuitry 143. Access circuitry can store information in the memory cell 100' by causing the storage material 102 to be in a particular state. The storage material 102 can include, for example, a chalcogenide material such as Te—Se alloys, As—Se alloys, Ge—Te alloys, As—

Se—Te alloys, Ge—As—Se alloys, Te—As—Ge alloys, Si—Ge—As—Se alloys, Si—Te—As—Ge alloys, or other material capable of functioning as both a storage element and a selector, to enable addressing a specific memory cell and determining what the state of the memory cell is. Thus, in one embodiment, the memory cell 100' is a self-selecting memory cell that includes a single layer of material that acts as both a selector element to select the memory cell and a memory element to store a logic state, i.e. a state related to a given polarity of the cell.

[022] In one embodiment, the storage material 102 is a phase change material. A phase change material can be electrically switched between a generally amorphous and a generally crystalline state across the entire spectrum between completely amorphous and completely crystalline states. The memory cell 100' may further include a selection device (not shown) between access lines 104 and 106; the selection device may be serially coupled to the storage material 102. In another embodiment, the storage material 102 is not a phase change material. In one embodiment in which the storage material 102 is not a phase change material, the storage material is capable of switching between two or more stable states without changing phase. The access circuitry 143 is able to program the memory cell 100' by applying a voltage with a particular polarity to cause the storage material 102 to be in the desired stable state.

[023] In one such embodiment, programming the memory cell 100' causes the memory cell 100' to "threshold" or to undergo a "threshold event." When a memory cell thresholds (e.g., during a programming voltage pulse), the memory cell undergoes a physical change that causes the memory cell to exhibit a certain threshold voltage in response to the application of a subsequent voltage (e.g., a read voltage with a particular magnitude and polarity). Programming the memory cell 100' can therefore involve applying a voltage of a given polarity to induce a programming threshold event, which causes the memory cell 100' to exhibit a particular threshold voltage at a subsequent reading voltage of a same or different polarity. In one such embodiment, the storage material 102 is a self-selecting material (e.g., a non-phase change chalcogenide material or other self-selecting material) that can be programmed by inducing a threshold event.

[024] As it is explained in further detail below, the output of such a memory cell when read differs as a function of the polarity used to program the memory cell and the polarity used to read the memory cell. For example, the storage material 102 can exhibit a "lower threshold voltage" or a "higher threshold voltage" in response to a read voltage based on the polarity of both the programming and read voltages. In the context of the present disclosure, exhibiting a threshold voltage means that there is a voltage across the memory cell that is approximately equal to the threshold voltage in response to the application of a voltage with a particular magnitude and polarity to the terminals of the memory cell. The threshold voltage thus corresponds to the minimum voltage that is needed to be applied at the input(s) to produce output(s), i.e. to see a determined electrical response of the cell. In other words, in the context of the present disclosure, the verb "threshold" means that the cells undergo a threshold event, i.e. they have an electrical response in response to the applied voltage that is above a given threshold, thus exhibiting a peculiar threshold voltage.

[025] As mentioned above, the access lines 104, 106 electrically couple the memory cell 100' with circuitry 142. The access lines 104, 106 can be referred to as a bitlines and wordlines, respectively. The wordline is for accessing a particular word in a memory array and the bitline is for accessing a particular bit in the word. In one embodiment, the access lines 104, 106 can be made of one or more suitable metals including: Al, Cu, Ni, Cr, Co, Ru, Rh, Pd, Ag, Pt, Au, Ir, Ta, and W; conductive metal nitrides including TiN, TaN, WN, and TaCN; conductive metal silicides including tantalum silicides, tungsten silicides, nickel silicides, cobalt silicides and titanium silicides; conductive metal silicide nitrides including TiSiN and WSiN; conductive metal carbide nitrides including TiCN and WCN, or any other suitable electrically conductive material.

[026] In one embodiment, electrodes 108 are disposed between storage material 102 and access lines 104, 106. Electrodes 108 electrically couple access lines 104, 106 with storage material 102. Electrodes 108 can be made of one or more conductive and/or semiconductive materials such as, for example: carbon (C), carbon nitride (CxNy); n-doped polysilicon and p-doped polysilicon; metals

including, Al, Cu, Ni, Cr, Co, Ru, Rh, Pd, Ag, Pt, Au, Ir, Ta, and W; conductive metal nitrides including TiN, TaN, WN, and TaCN; conductive metal silicides including tantalum silicides, tungsten silicides, nickel silicides, cobalt silicides and titanium silicides; conductive metal silicides nitrides including TiSiN and WSiN; conductive metal carbide nitrides including TiCN and WCN; conductive metal oxides including RuO2, or other suitable conductive materials.

[027] The stack made of electrodes 108 and storage material 102 is hereinafter referred to as the memory cell 100', without limiting the scope of the disclosure. In various embodiments, the memory cell 100' may comprise more or less elements. Therefore, the memory cell 100' is one example of a memory cell. Other embodiments can include memory cells having additional, less, or different layers of material than the ones illustrated in figure 1 (e.g., a thin dielectric material between the storage material and access lines and the like).

[028] Referring again to the circuitry 142, the access lines 104, 106 communicatively couple the circuitry 142 to the memory cell 100', in accordance with an embodiment. The circuitry 142 includes access circuitry 143 and sense circuitry 145. Circuitry includes electronic components that are electrically coupled to perform analog or logic operations on received or stored information, output information, and/or store information. Hardware logic is circuitry to perform logic operations such as logic operations involved in data processing. In one embodiment, the access circuitry 143 applies voltage pulses to the access lines 104, 106 to write to or read the memory cell 100'. The terms "write" and "program" are used interchangeably to describe the act of storing information in a memory cell. To write to the memory cell 100', the access circuitry applies a voltage pulse with a particular magnitude and polarity to the access lines 104, 106, which can both select memory cell 100' and program memory cell 100'.

[029] For example, the access circuitry 143 applies a read voltage with one polarity to program the memory cell 100' to be in one logic state, and applies a pulse with a different polarity to program the memory cell 100' to be in a different logic state. The access circuitry 143 can then differentiate between different logic states as a consequence of the programming polarity of a memory

cell. For example, in a case of a memory read, the access circuitry 143 applies a voltage pulse with a particular magnitude and polarity to the access lines 104, 106, which results in an electrical response that the sense circuitry 145 can detect. Detecting electrical responses can include, for example, detecting one or more of: a voltage drop (e.g., a threshold voltage) across terminals of a given memory cell of the array, current through the given memory cell, and a threshold event of the given memory cell. In some cases, detecting a threshold voltage for a memory cell can include determining that the cell's threshold voltage is lower than or higher than a reference voltage, for example a read voltage. The access circuitry 143 can determine the logic state of the memory cell 100' based on electrical responses to one or more of the voltage pulses in a read sequence.

[030] The electric current generated upon application of a reading voltage thus depends on the threshold voltage of the memory cell determined by the electrical resistance of the logic state storage element. For example, a first logic state (e.g., SET state) may correspond to a finite amount of current, whereas a second logic state (e.g., RESET state) may correspond to no current or a negligibly small current. Alternatively, a first logic state may correspond to a current higher than a current threshold, whereas a second logic state may correspond to a current lower than the current threshold.

[031] Figure 2 shows a portion of a memory cell array 200, which can include a plurality of memory cells such as the memory cell 100' of figure 1, in accordance with an embodiment. The memory cell array 200 is an example of a three-dimensional cross-point memory structure (3D X Point). The memory cell array 200 includes a plurality of access lines 204, 206, which can be the same or similar as the access lines 104, 106 described with respect to figure 1. Access lines 204, 206 can be referred to as bitlines and wordlines. In the embodiment illustrated in figure 2, the bitlines (e.g., access lines 204) are orthogonal to the wordlines (e.g., access lines 206). A storage material 202 (such as the storage material 102 of figure 1) is disposed between the access lines 204, 206. As disclosed in relation to figure 1, storage material 202 may be a self-selecting storage material, in some examples; storage material 202 may be serially

coupled to a selection device (not shown), in other examples. In one embodiment, a "cross-point" is formed at an intersection between a bitline and a wordline. A memory cell is created from the storage material 202 between the bitline and wordline where the bitline and wordline intersect (it is noted that, in figure 2, additional layers such as electrodes are not shown, so that the cell is schematically represented in said figure by the storage material 202 only, without limiting the scope of the disclosure, and additional layers may be present). Generally speaking, the intersection defines the address of the memory cell. The storage material 202 can be a chalcogenide material such as the storage material 102 described above with respect to figure 1. In one embodiment, the access lines 204, 206 are made of one or more conductive materials such as the access lines 104, 106 described above with respect to figure 1. Although a single level or layer of memory cells is shown in figure 2, memory cell array 200 can include multiple levels or layers of memory cells (e.g., in the z-direction).

[032] A "cross-point" thus refers to a place where a memory cell is formed such that access lines associated with the memory cell topologically "cross" each other as access lines connect to different nodes of the memory cell. Cross-point architecture enables reaching the theoretical minimum cell area determined by the minimum pitch of access lines.

[033] Figures 1 and 2 illustrate an example of a memory cell and array. However, other memory cell structures and arrays may be used, in which the memory cells exhibit electrical responses that vary as a function of programming and read polarity. A memory cell (not shown) may be formed at crossing locations between vertical conductive pillars, acting as bitlines, intersecting horizontal conductive planes, acting as wordlines, in a 3D memory array, for example. This and other array organizations may also lead to a cross-point architecture as described above.

[034] Ideally, all memory cells of a memory device should feature a same (nominal) resistivity and therefore a same threshold voltage for a same logic state, wherein the threshold voltage is the voltage to be applied to the memory

cells for causing them to conduct an electric current, i.e. the minimum value of the voltage that is needed to create a conducting path between the terminals, as above defined. However, since different cells programmed to a same logic state practically exhibit different resistivity values because of several factors (such as for example variations in the electrical characteristics of the phase-change material caused by the execution of a number of read-write operations and/or by manufacturing tolerances), each logic state is actually associated to a respective resistivity distribution (typically a Gaussian-type distribution), and therefore to a respective threshold voltage distribution.

[035] In order to assess the logic state of a cell, a reading operation is carried out to assess to which threshold voltage distribution the threshold voltage of the cell belongs. For example, a reading voltage may be applied to the cell via access lines and the logic state of the cell is assessed based on (the presence or absence of) a current responsive to said reading voltage, the (presence or absence of the) current depending on the threshold voltage of the cell. A cell thresholds (e.g., it becomes conductive) when a suitable voltage difference is applied between its two terminals; such a voltage difference may be obtained in different ways, for example biasing one terminal, such as a wordline terminal, to a negative voltage (e.g. a selection voltage), and the other terminal, such as a bitline terminal, to a positive voltage (e.g. a reading voltage). Other biasing configurations may produce the same effects (e.g., both the word line and the bitline terminal biased to positive voltage, or the wordline terminal biased to a reference voltage, e.g. a ground voltage, and the bitline terminal biased to a positive voltage).

[036] In other words, operations such as programming and reading, which may be referred to as access operations, may be performed on memory cells by activating or selecting a wordline 206 and bitline 204. As known in the field, wordlines 206 may also be known as row lines, sense lines, and access lines. Bitlines 204 may also be known as digitlines, column lines, data lines, as well as access lines. References to wordlines and bitlines, or their analogues, are interchangeable without loss of understanding or operation. For example, the access lines may be wordlines and the data lines may be bitlines. Wordlines 206

and bitlines 204 may be perpendicular (or nearly perpendicular) to one another to create an array, as previously shown with reference to figure 2. Depending on the type of memory cell (e.g., FeRAM, RRAM, etc.), other access lines (not shown in the figures) may be present, such as plate lines, for example. It should be appreciated that the exact operation of the memory device may be altered based on the type of memory cell and/or the specific access lines used in the memory device. Activating or selecting a wordline 206 or a bitline 204 may include applying a voltage to the respective line via a dedicated driver. By activating one wordline and one bitline, a single memory cell 202 may be accessed at their intersection. Accessing the memory cell may include reading or writing the memory cell.

[037] Accessing memory cells may be controlled through a row decoder and a column decoder (not shown). For example, a row decoder may receive a row address from a memory controller and activate the appropriate wordline based on the received row address. Similarly, a column decoder may receive a column address from the memory controller and activate the appropriate bitline.

[038] As mentioned before, in some cases, memory cells 202 may exhibit different electrical characteristics after a number of cycling operations (e.g., a series of read or write operations). For example, a threshold voltage of a memory cell 202 (e.g., PCM cell) corresponding to a logic state of 1, after receiving an identical programming pulse to store the logic state of 1 (e.g., a SET programming pulse), may be different if a memory cell is relatively new (e.g., a PCM cell with a small number of read or write operations) compared to a memory cell having been cycled through an extensive number of read or write operations. In addition, in some cases, a chalcogenide material in the memory cells (e.g., the logic storage element 102 or 202) may experience a change (which may also be referred to as a drift) in its resistance after programming (e.g., crystallizing or quenching) of the chalcogenide material during a write operation. Such change in resistance may result in changes in threshold voltages of memory cells and may hinder accurately reading information from memory cells (e.g., PCM cells) after a certain period of time elapsed. In some embodiments, the amount of change may be a function of ambient temperature. In many

cases, it may be impractical to rely only on error correction mechanisms to handle the errors.

[039] The present disclosure provides a robust and reliable read technique also when memory cells (e.g., PCM cells or SSM cells) exhibit different, non-uniform, variable electrical characteristics that may originate from various factors including statistical process variations, cycling events (e.g., read or write operations on the memory cells), or a drift (e.g., a change in resistance of a chalcogenide alloy), among others. The voltage distributions of the cells may thus drift in time or exhibit shapes deviating from perfect statistical functions, e.g. deviating from a perfect gaussian curve.

[040] More in particular, according to the read technique of the present disclosure, an auto-referenced reading of a set of user data (e.g., a codeword, a page) is performed based on data information previously stored in a codeword, said data information accounting for the statistical properties of the voltage distribution of the cells of the codeword, providing a new and more efficient solution for reading memory cells, in particular in 3D memory devices.

[041] According to the present disclosure, the memory cells may be configured to store encoded user data that include modified user data (or original user data, in some cases) and a number of bits (e.g., flip-bits), which may be added thereto. In some cases, the encoded user data stored in the memory cells have been modified to include a certain number of bits having the logic state of 1. The number of bits having the logic state of 1 may vary within a predetermined range. As it will be disclosed in the following, the auto-referenced read of the present disclosure determines a proper read reference voltage to be applied to the memory cells, namely a voltage that is to be used to discern whether a memory cell exhibits a logic state of 1 (e.g., a SET status) or a logic state of 0 (e.g., a RESET status). The auto-referenced read may determine the read reference voltage for the memory cells by taking into account the statistical distributions of the bits programmed in the memory cells, e.g. of the bits of a codeword CW.

[042] Figure 3 illustrates an exemplary user data pattern diagram 301. The user data pattern diagram 301 includes user data 310a and encoded user data 315a. Encoding process 320a, which is performed in the programming phase of the array of memory cells, may convert the user data 310a into the encoded user data 315a. The encoded user data 315a may be stored in a set of memory cells, which may be, for example, memory cells 100' or 202 described with reference to figures 1 and 2. Each box of the encoded user data 315a may correspond to a memory cell that may exhibit a logic state of 1 or a logic state of 0. During the encoding process 320a, a number of parity bits may be added to the user data 310a to establish a predetermined number of bits of the encoded user data 315a having a given logic value (e.g., a logic value of 1). As a result, a number of bits in the encoded user data 315a may be greater than the number of bits in the user data 310a (e.g., n is larger than m if some bits, e.g. parity bits, are added). Process 325 may convert the encoded user data 315a back to the user data 310a after the encoded user data 315a have been accurately read.

[043] In an embodiment, the plurality of encoded bits to be read represents a codeword (CW). The codeword may be programmed to include various information to be used during the reading phase.

[044] In some embodiments, for each set of user data 310a, corresponding encoded user data 315a may have a same number of memory cells exhibiting a logic state of 1 and a logic state of 0 (which may also be referred to as a balanced encoding scheme, where half of the encoded user data bits have a logic state of 1, and the other half have a logic state of 0). As such, the encoded user data may be referred to have a 50% weight. In some embodiments, for each user data 310a, corresponding encoded user data 315a may have a predetermined number of memory cells exhibiting a given logic state (e.g., a logic state of 1), hence producing a constant weight that may be different than 50% (which may also be referred to as a constant weight encoding scheme). In general, an outcome of the encoding process 320a may be that a predetermined number of memory cells exhibiting a given logic state (e.g., a logic state of 1) in the encoded user data 315a is established.

[045] In other words, according to an embodiment of the present disclosure, the codeword may be manipulated to constrain the number of bits exhibiting a given logic state (e.g. a logic state of 1) to a known desired predetermined value, generally between a minimum value and a maximum value (e.g., between {Min1, Max1}, or within a range), by adding some extra bits of information. Therefore, in some embodiments, the memory cells of the array may be configured to store encoded user data that include modified user data (or original user data, in some cases) and a number of bits which may be added thereto, i.e. a data manipulation is performed to constrain the number of bits having a given logic state (e.g. the number of bits having the logic value 1) in a codeword by few (e.g. 2-4) parity or inversion bits. In this way, the statistics of the codeword is improved by using distributions having a reasonable number of bits in a given logic state, in particular having a predetermined number of bits having a logic state 1, or having a number of bits having a logic state of 1 in a given range, facilitating the reading operation and avoiding extreme cases with very few bits exhibiting the logic state 1. This also allows to statistically track usage (e.g. drift and cycling) of the codeword with few extra bits, as well as improving speed.

[046] In some cases, the encoding scheme may result in the total number of bits in the encoded user data having a given logic state (e.g., a logic value of 1) being in a predetermined weight range (e.g., 48%-50%, 40%-48%, 40%-45%, or 20%-25%, for example) rather than an exact predetermined weight. Some additional bits may be programmed to obtain an exact weight, in some cases.

[047] In the context of the present disclosure, a bit having the logic state of 1 (e.g. corresponding to a cell in the logic state 1) is identified as a bit in a first logic state, whereas a bit having the logic state of 0 (e.g. corresponding to a cell in the logic state 0) is identified as a bit in a second logic state, even if other definitions may be used. According to an embodiment of the present disclosure, the memory cells exhibit a threshold voltage with a lower magnitude when the memory cells are in the first logic state, and a threshold voltage with a higher magnitude when the memory cells are in the second logic state, the logic state of a given cell being determined based on whether the memory cell exhibits a

higher or lower magnitude threshold voltage in response to an applied read voltage.

[048] Summing up, the present disclosure thus provides, in the programming phase, the storage of user data (such as the encoded user data 315a) in a plurality of memory cells of the memory array, these data being subjected to encoding schemes as previously described. More in particular, when storing the user data, they may be encoded in a codeword having a predetermined number of bits exhibiting the first logic value. For example, in an embodiment, the encoded user data may have a same number of bits having the logic value of 1 and the logic value of 0, i.e. the encoded user data have substantially a same number of bits exhibiting the first logic state and the second logic state, even if other configurations in which the encoded user data have a known predetermined number of bits in the first logic value may be used. The present disclosure may thus include an encoding technique that ensures a certain number bits in the set of user data (e.g., a codeword of 128 bits) to have a given logic state (e.g., a logic state of 1) prior to storing the user data in memory cells (e.g., PCM cells, 3DXP memory cells). In some embodiments, a logic state of 1 (e.g., a SET state of cell, which may also be referred to as a SET cell or bit) corresponds to a set of threshold voltages lower than a set of threshold voltages associated with a logic state of 0 (e.g., a RESET state of a cell, which may also be referred to as a RESET cell or bit). The encoding technique may provide a number of bits having the logic state of 1 (e.g., the SET bits) within a certain range which may be established by a predetermined factor k. The ratio between a number of bits having the logic state of 1 (e.g., 32 SET bits) and a total number of bits in the user data (e.g., 128 bits) may be referred to as a weight (e.g., 25% weight) or a weight pattern. In some examples, the encoding technique may ensure the encoded user data to have a particular weight within a range of weights (e.g., between 50% and (50+50/k) %) established by the predetermined factor k. The larger the value of k, the narrower the range may become, which may result in an increased accuracy of the read operation. Further, the encoding technique may track changes in the user data during the encoding operation by storing k number of bits associated with the encoded

user data. The k number of bits, which may also be referred to as flip-bits, may indicate a status of the original user data such that decoding of the encoded user data may be carried out accurately. In other words, the codeword may be encoded as wanted (e.g., to the desired number of bits having the logic state of 1) for improving read reliability or performance.

[049] Figure 4 illustrates examples of threshold voltage (V_{TH}) distribution diagrams 401 and 402 of memory cells that supports read techniques in accordance with embodiments of the present disclosure. Each diagram 401 or 402 represents two groups of threshold voltages corresponding to two logic states (e.g., a logic state of 1, a logic state of 0) of the memory cells. The memory cells (e.g., PCM cells) may be embodiments of the memory cells 100' or 202 described with reference to figures 1 and 2. The logic state of 1 may correspond to a first set of threshold voltages (e.g., a distribution 410, a distribution 420) of the memory cells. In some cases, the logic state of 1 is referred to as a SET state of a PCM cell. The logic state of 0 may correspond to a second set of threshold voltages (e.g., a distribution 430, a distribution 440) of the memory cells. In some cases, the logic state of 0 is referred to as a RESET state of a cell.

[050] Distribution diagram 401 depicts a number of memory cells (y-axis) as a function of threshold voltages V_{TH} (x-axis) of the memory cells. The memory cells of the distribution diagram 401 may represent a set of memory cells storing encoded user data in accordance with the encoding scheme of the present disclosure, as mentioned above. In other words, the encoded user data has a number of bits having the logic state of 1 (e.g., SET cells) within a predetermined range. The distribution 410 illustrates a threshold voltage V_{TH} distribution of memory cells programmed to the logic state of 1. The distribution 430 illustrates a threshold voltage V_{TH} distribution of memory cells having the logic state of 0. The distribution 410 may have a median value (or peak value) denoted as V_{TH1}. A standard deviation (e.g., σSET) of the distribution 410 determines the width of said distribution 410. Similarly, the distribution 430 may have a median value denoted as V_{TH3} and a standard deviation (e.g., σRESET) that determines the width of said distribution 430. The distributions may be gaussian distributions or other statistical functions depending on various factors.

[051] In some embodiments, each distribution may not be symmetrical around its median threshold voltage V_{TH}, as shown below. In some embodiments, each distribution may exhibit a different ranges of threshold voltage V_{TH} values (not shown).

[052] A difference between the highest threshold voltage of the memory cells having the logic state of 1 and the lowest threshold voltage of the memory cells having the logic state of 0 is referred to as a read window budget 450. A desired read reference voltage may be determined to be at or near the middle of the read window budget 450 and is denoted by V_{REF_0} in FIG. 4. The threshold voltage V_{TH} distributions diagram 401 may illustrate voltage distributions of a set of memory cells that are relatively new (e.g., PCM cells with a small number of cycling operations) or recently programmed (e.g., memory cells without a significant drift).

[053] Similarly, threshold voltage V_{TH} distributions diagram 402 depicts a number of memory cells (y-axis) as a function of threshold voltages (x-axis) of the memory cells. The distributions diagram 402 may illustrate distributions of the encoded user data (e.g., the encoded user data represented by the distribution diagram 401) stored in a set of memory cells that may have experienced an extensive number of cycling operations representing a different electrical characteristic. The distribution 420 illustrates a threshold voltage V_{TH} distribution of memory cells having the logic state of 1. The distribution 440 illustrates a threshold voltage V_{TH} distribution of memory cells having the logic state of 0. The distribution 420 may have a median value denoted as V_{TH2} that may be greater than V_{TH1}. The distribution 440 may have a median value denoted as V_{TH4} that may be greater than V_{TH3}, i.e. peak value may drift. A σSET of the distribution 420 may be greater than the σSET of the distribution 410. A σRESET of the distribution 440 may be greater than the σRESET of the distribution 430, i.e. distributions may be larger. As a result, a read window budget 460 of the threshold voltage distributions diagram 402 may be different (e.g., less) than the read window budget 450 of the threshold voltage distributions diagram 401. Therefore, the read reference voltage V_{REF_0} for the distributions diagram 401 may not be appropriate for the distributions diagram

402. A new desired read reference voltage V_{REF_1} may be configured to support accurate reading of the memory cells of the distributions diagram 402. The change in the read window budget and the associated change in the read reference voltage, as well as the change in the shape of distributions, may be a result of memory cells experiencing extensive cycling operations and/or significant drift events, and the present disclosure provides methods and systems to perform an efficient reading operation of these cells.

[054] The use of fixed, defined a priori, reference read voltages V_{REF} may result in read disturb, for instance when the value of a reference voltage used for reading cells in the first logic state 1 is close to the minimum threshold voltage of the cells in the second logic state 0, so that reading may be negatively affected.

[055] The reading of the codeword may be improved according to the present disclosure. More in particular, the present disclosure relies on encoding and programming schemes that provide the storage, for each single codeword, of distribution information enabling the proper setting of the reference voltage, and allowing an accurate subsequent reading of the user data regardless of the different electrical characteristics of memory cells, and thus regardless of possible different voltage distributions of the cells of different codewords.

[056] First of all, according to the present disclosure, a set of user data is stored in a plurality of memory cells of the memory array. As previously mentioned, the user data are generally encoded in a codeword having a number of bits exhibiting the first logic state in a range, the encoding step comprising manipulating the codeword to constrain the number of bits exhibiting the first logic value in the range. In an embodiment, the encoded user data have substantially a same number of bits exhibiting the first logic state and the second logic state.

[057] In an embodiment of a programming method of the present disclosure, the cells are initially programmed to the first logic state 1 (i.e. a programming voltage is initially applied to switch the array cells to All1), even if the present

disclosure is not limited thereto and another suitable configuration may be adopted.

[058] When programming the array of memory cells, a predetermined number of memory cells of the array, hereinafter referred to as "trigger memory cells T", is used to detect the switching of a predetermined number of cells having a given logic state, i.e. the logic state of 1.

[059] More in particular, a programming voltage for programming cells to a first logic state is applied to the memory cells of the array. When it is determined that a predetermined first group of memory cells, i.e. the above mentioned trigger memory cells T, has been switched to an active state based on the application of the programming voltage, this programming voltage corresponding to the activation of all said cells (herein referred to as "first threshold voltage") is stored into a portion of the memory array. The first threshold voltage is thus the programming voltage used to activate the preset number of trigger memory cells T in the first logic state, e.g. in the logic state 1.

[060] In other words, a number T of cells acts as trigger and, once said T (or T-1) trigger cells are switched based on the application of the programming voltage, the desired predetermined number of memory cells is thus activated and the corresponding programming voltage (i.e. the first threshold voltage) is stored. As mentioned above, in an embodiment, T-1 cells are considered in order to avoid a possible fail-cell inside trigger to produce an error.

[061] In an embodiment, the trigger memory cells T are used to store the intrinsic switching value of the voltage distribution of a set of memory cells programmed to the first logic state. More particularly, in an embodiment, the first threshold voltage is the median – i.e. the peak - threshold voltage value of the memory cells in the first logic state, allowing tracking the intrinsic of the distribution without being affected by very slow switching or defects or cells broken with device life. The median threshold voltage may thus be determined based on the activation of the predetermined number of trigger memory cells T in the first logic state, i.e. the logic state of 1.

[062] According to other embodiments of the present disclosure, any point of the cell voltage distribution may be identified and tracked as a reference point, i.e. the first threshold voltage may be a particular threshold voltage value for the cells programmed to the first logic state and it is not necessarily the peak value (i.e. it may be comprised between the minimum expected threshold voltage value and the peak value, or may be greater than the peak value), depending on the circumstances. The present disclosure thus allows a choice of a reference tracking point of the distribution, optimizing the trade-off between reading speed and accuracy, depending on the circumstances.

[063] The applied programming voltage may thus initiate a series of switching events by activating the first group of memory cells, i.e. the trigger memory cells T, and thus programming them to the first logic state 1. In other words, the present disclosure identifies that a particular switching event (e.g., a T-th switching event of the plurality of switching events) correlates to a given threshold voltage value (e.g. a median – or peak – threshold voltage, or other desired values of the distribution) of memory cells having the logic state of 1 (e.g., SET cells) and the corresponding voltage is stored.

[064] After detecting the T-th switching event, corresponding to the activation of the trigger memory cells T, the expected extreme (e.g. maximum) threshold voltage value of the voltage distribution of the memory cells is precisely calculated each time a codeword is programmed into said cells, as each codeword may have its specific distribution, as shown in figures 5A and 5B which illustrate the voltage distributions relating to two different codewords of the memory array. Advantageously, once the voltage used to activate the first group of memory cells is stored, a proper voltage ΔN, which is calculated and defined for each codeword, is stored and associated to the codeword to be subsequently applied to the memory cells.

[065] More in particular, the present disclosure provides the storage, for each codeword of the memory array, of additional data information, said additional data information being representative of a voltage difference ΔN between the first threshold voltage (i.e. the voltage to activate the preset number of trigger

memory cells T programmed to the first logic state) and a second threshold voltage used to program the remaining cells of the array, said second threshold voltage depending on the actual width of the threshold voltage distribution, which may be different from codeword to codeword.

[066] In other words, the second threshold voltage is a programming voltage used to activate the memory cells in the first logic state and whose magnitude is higher than the first threshold voltage, more specifically the second threshold voltage corresponds to the expected maximum threshold voltage of the voltage distribution of the memory cells programmed at the first logic state 1, and is based on the actual statistics of the threshold voltage distribution. As shown in the exemplary embodiments of figures 5A and 5B, the value of ΔN may be a voltage difference between the peak of the voltage distribution (or generally a given value of the distribution) and the maximum expected threshold voltage value, and accounts for the actual width of the voltage distribution of the set of user data.

[067] According to an embodiment of the present disclosure, the calculation of ΔN is based on the difference between the last voltage value (e.g. the last voltage step in case of a staircase ramp) used to program the array and the first threshold voltage (i.e. the trigger switching voltage step), and is stored into some bits related to the codeword.

[068] More in particular, according to an embodiment of the present disclosure, in the programming operation, the user data are encoded according to an Error Correction Code (ECC) scheme.

[069] In an embodiment, during the application of the programming voltage (e.g. during incrementing voltage with a voltage ramp), all the cells are programmed at 1.

[070] As previously mentioned, once it is determined that the predetermined first group of memory cells has been switched to an active state based on the application of the programming voltage (i.e. after switching of the codeword

trigger memory cells T used to detect the switching of the predetermined "1's"), information representative of the corresponding programming voltage value (e.g. the corresponding voltage step value) is stored.

[071] An ECC verify operation is then performed on the programmed data and the value of the syndrome of said ECC is determined. More in particular, after the trigger memory cells T are switched, the ECC is operated simultaneously to the application of the programming voltage to program the remaining cells of the array.

[072] The ECC has the ability to correct data bit errors which occur in memory arrays. ECC syndrome bits are the XOR of computed check bits and read check bits. Non-zero ECC syndrome bits denote an error, while a zero ECC syndrome denotes a correct programming operation.

[073] According to the present disclosure, as schematically illustrated in figure 6, based on the ECC syndrome calculation, the programming voltage values corresponding to an ECC syndrome toggling from a first value (e.g. from 1) to a second value (e.g. to 0, corresponding to a correct programming operation as in steps N+1, N+3 and N+5 of the example of figure 6) are stored, while the programming voltage values corresponding to an ECC syndrome different from the second value (i.e. different from 0) are ignored (in the example N and N+2). The voltage difference between the programming voltage used to program the first group of trigger memory cells T (i.e. the first threshold voltage) and the last programming voltage value used to program the memory cells to the first logic state 1 and resulting in a stable ECC syndrome equal to zero (i.e. the second threshold voltage causing the last toggling from the first value of 1 to the second value of 0) is then stored in a portion of the memory array. The second threshold voltage is thus the programming voltage corresponding to the activation of all the cells in the first logic state, i.e. in the logic state 1, within the ECC correction capability. In other words, in the programming phase, the memory cells are programmed at 1 with a program and verify "on the fly", up to a stable ECC output (corresponding to a zero syndrome).

[074] In an embodiment, the programming voltage may be a voltage staircase up to the maximum threshold voltage value, in case plus a margin voltage.

[075] In this way, during the application of the programming voltage (which may be a voltage staircase ramp comprising N steps), anytime the syndrome is zero, the staircase up step N(i) is stored into a latch or a register (as schematically shown in figure 7), while, when the syndrome is 1, the corresponding N(i) voltage value is ignored. The syndrome will toggle between 1 and 0 across the whole staircase up until it is stabilizing to zero, indicating that all the cells have been properly programmed to the first logic state 1 within the ECC correction capability, and the corresponding N(i) voltage step value is then stored.

[076] More in particular, in an embodiment shown in figure 7, the programming technique of the present disclosure may be executed by an ECC calculation unit 701 configured to produce, from the encoded set of user data, a syndrome value, and, when the syndrome value is zero, the corresponding programming voltage value (e.g. the N(i) voltage step) is stored in a register and/or latch 702 while, when the syndrome is different from zero, the corresponding programming voltage is ignored. The programming voltage is updated in said register or latch 702 anytime the ECC syndrome is toggling from a value different from zero to zero. A logic circuit 703 is configured to generate the N voltage steps value that are used by a voltage generator 704 to apply the proper voltage to the array.

[077] Therefore, at any new zero of the ECC syndrome, the equivalent N(i) voltage value is stored, updating into the register its last value. The last stored value is equivalent to the staircase up step at which the distribution is all written to All1 within the ECC correction capability. In fact, the syndrome is stable at 0 when the data pattern is correctable by the ECC, which means that all the memory cells are programmed to the logic state 1 except for at most its correcting power. In other words, the second threshold voltage is the last programming voltage corresponding to a switching of the ECC syndrome to 0 and, when saved, updates all the previous stored programming voltages. A verify process based on ECC feedback is thus used during the programming phase to

retrieve information about the distribution width by waiting for the last used voltage value. The last used voltage value is updated to the current step of the voltage staircase if ECC syndrome is toggling from 1 to 0; in other words, anytime the ECC syndrome is toggling from a value different from zero to zero, the corresponding programming voltage value is stored updating the previous value thereof.

[078] Advantageously, this technique takes into account also cells with very high switch voltage or defective cells (e.g. stuck at 0).

[079] In other words, a programming write operation is herein disclosed which firstly writes the memory cells of the array to All1 and then measures the distribution width and stores the measured distribution information in the form of the voltage ΔN into the codeword CW.

[080] In an embodiment, once the cells have been programmed to the first logic state 1 and ΔN has been stored in the codeword, a programming write operation writes-back cells in the second logic state 0. In general, if there are 0's to be written, write-back of the user data is performed by changing the decoder polarity. In other words, after the programming of the cells to the first logic state 1, the present disclosure provides for a write-back operation for programming memory cells of the array to the second logic state 0. According to an embodiment of the present disclosure, the cells that have to be programmed to the second logic state are initially masked in such a way that, during the application of the programming voltage for programming the cells to the first logic state, said masked cells are regarded as memory cells already programmed to said second logic state, so as not to affect the operation of the ECC during the programming operation of the cells in the first logic state.

[081] At the end of the programming operation, drift is reset and also reset disturb is reset because write back to 0 is applied.

[082] The stored information representative of voltage difference (ΔN) is then used as additional data information for properly reading the codewords of the

array. Specifically, a particular ΔN value is adapted and stored for each particular codeword, improving the reading operation by adding to a read voltage said voltage difference ΔN, as disclosed in the following, said ΔN being read before reading the data of the codeword. The present disclosure thus provides for an advantageous programming method and a corresponding reading method of an array of memory cells, and therefore provides for an improved access operation to the array of memory cells.

[083] In order to read user data, a read voltage is applied to the memory array, said voltage being configured to activate a group of memory cells containing the encoded user data. In some embodiments, the read voltage has a constant rate of increase with respect to time. In other embodiments, the read voltage has a monotonically increasing staircase shape such that a first step is applied for a first period of time followed by a second (possibly different) step for a second period of time.

[084] In a preferred and non-limiting embodiment of the present disclosure, the read voltage is a staircase voltage ramp comprising N steps, as shown in figures 5A and 5B.

[085] The applied read voltage initiates a series of switching events by activating the first group of memory cells storing the encoded user data, i.e. activating the above-described trigger memory cells T. The switching event may be attributed to a memory cell turning on ("activating"), e.g., conducting an appreciable amount of current, when the applied voltage across the memory cell exceeds its threshold voltage V_{TH}. Hence, initiating the series of switching events in response to the increasing read voltage may be similar to identifying memory cells in an ascending order in terms of their threshold voltage values.

[086] Referring again to figures 5A and 5B, the present disclosure identifies that a particular switching event (e.g., a Tth switching event of the plurality of swathing events) correlates to a given threshold voltage value (e.g., a median – or peak – threshold voltage) of memory cells having the logic state of 1 (e.g., SET cells). In an embodiment, the memory cells that have been activated, including

the memory cell that exhibited the Tth switching event, may be determined to have the logic state of 1 (e.g., SET cells).

[087] In some embodiments, the present disclosure identifies a memory cell having a V_{TH} value close to the median V_{TH} value (e.g., V_{TH1} of distribution 410, V_{TH2} of distribution 420 of figure 4), or, in other embodiments, close to other different voltage values. The read operation may determine such memory cell (e.g., a memory cell having a T-th threshold voltage value in ascending order) based on a knowledge that encoded user data has a number of bits having the logic state of 1 (e.g., SET cells) within a predetermined range. The read operation may apply a read voltage (e.g., an activation voltage) to the memory cells in order to detect the memory cell turning on (e.g., the memory cell exhibiting the T-th switching event) while the read voltage amplitude increases with respect to time.

[088] The read of the array is thus performed by applying to the memory array a read voltage to activate the first group of memory cells corresponding to the preset number of trigger memory cells T, and then determining that said first group of memory cells has been activated based on applying the read voltage, wherein said read voltage is equal to the first threshold voltage when the first group of memory cells has been activated.

[089] After detecting the T-th switching event, corresponding to the above-mentioned activation of the trigger memory cells T, it would be desirable to apply a read voltage (i.e. a read pulse) accounting for the correct statistical distribution of the threshold voltages of the memory cells, avoiding the application of a preset fixed read voltage, as instead performed in the prior art solutions not accounting for different distributions of different codewords in the memory array.

[090] Advantageously according to the present disclosure, once a read voltage is applied to the memory array to activate the first group of memory cells (i.e. after the application of the first threshold voltage), the voltage difference ΔN, representing a proper voltage step defined for each codeword and calculated as

above, is applied to the memory cells to complete the reading operation. The present disclosure may thus provide a proper read technique for the memory cells, e.g. also for both situations 401 and 402 of figure 4.

[091] Therefore, depending on the voltage difference ΔN stored into the codeword, a voltage step offset equal to ΔN is applied to the array to complete reading after the application of the first threshold voltage.

[092] More in particular, the present disclosure provides, based on the stored additional data information (which are read from the codeword before reading the user data in said codeword), the application of the voltage difference ΔN to the memory array to activate a second group of memory cells programmed to the first logic state, i.e. to the logic state 1. The second group of activated memory cells corresponds to the cells having a threshold voltage whose magnitude is comprised between the first threshold voltage and the maximum expected threshold voltage of the cells in the first logic state 1.

[093] Advantageously, the voltage ΔN is specific for each codeword and is associated to each particular codeword so that the value thereof may be properly used during the reading operation. In this way, the voltage ΔN corresponds to a voltage used to properly read all the cells in the first logic state (e.g. up to 5σ from the intrinsic value of the distribution, i.e. up to the last statistically significant value within the ECC correction capability, said value being different for each codeword), without affecting the cells programmed in the second logic state, thus eliminating read disturb.

[094] According to an embodiment of the present disclosure, an additional margin read voltage may be applied after the application of the voltage difference ΔN, e.g. in order to account for voltage threshold distributions enlarging with time.

[095] In this case, a corresponding margin may be taken while storing the last programming voltage value (for example, if the program value is a staircase voltage ramp and N is the last step, the saved value is N-1). This allows to not

consider a possible very high threshold cell and decide with the ECC if continue or not.

[096] Since the last programming voltage has reset the drift and the reset disturb (the distribution window is quite enlarged) and it has written the required ΔN to program the cells at 1 into the ECC correction capability, the extra margin pulses may account only for distribution enlarging with time (e.g. a standard deviation increasing from 95mV to 140mV max). This means that a value of 6σ corresponds to less than 300mV, which is comparable with a pulse step. A single pulse can thus be accounted for the tail bits. This single pulse amplitude is then subtracted by the total available window (which has been enlarged because of the per-page reading and the program strategy which is avoiding the reset read disturb).

[097] According to another embodiment of the present disclosure, as shown in figure 5B, an ECC verify operation is performed after the application of the voltage difference ΔN; in this case, a further read voltage (e.g. one or more voltage steps) is applied in case the ECC verify operation yields an error to be corrected in the set of user data. In other words, a Try and Repeat ECC verify is started until the errors are corrected.

[098] Moreover, according to an embodiment of the present disclosure, the additional data information ΔN comprises bits protected using an ECC and/or a differential cells scheme. For example, ΔN may comprise 3 bits (and 3 parity bits), resulting in 12 bits differential and protected by ECC1.

[099] According to an embodiment of the present disclosure, ECC is checked at each new read pulse.

[0100] According to the present disclosure, the read operation is thus based on switching the array cells to All1. The applied read voltage is firstly based on a predetermined number of trigger memory cells T and then an additional pulse step (i.e. the voltage difference ΔN) based on the additional information stored into the codeword CW during the write phase. In other

words, the voltage spread ΔN is measured starting from a predefined distribution point (in an embodiment, the number T of cells read as 1 in an All1 distribution, limited to cells that are going not to be programmed to 0) and during the read operation the T-th switching event may be dynamically determined (therefore compensating for any drift) and ΔN applied.

[0101] The remaining memory cells of the encoded user data (e.g., the inactive memory cells after the application of the read voltage) may be determined to be the memory cells having the logic state of 0 (e.g., RESET cells).

[0102] In an embodiment, cells are programmed back to 1 (and then to 0). However, in other embodiments, such as embodiments comprising vertical 3D memories, a read only command may be allowed.

[0103] The techniques disclosed herein have several advantages, since the reading operation does not require a counter and relies just on the trigger memory cells T traking a point of the distribution and on the stored information ΔN from the last write operation to track the width of the distribution. The operation is fast since the total number of steps is almost divided by two.

[0104] Advantageously, the disclosed reading operation allows tracking the distribution tails and reset the drift and reset disturb. The voltage represented by ΔN corresponds to a voltage to read all the cells in the first logic state (e.g. up to 5σ from the intrinsic value of the distribution, i.e. up to the last statistically significant value within the ECC correction capability). The voltage (e.g., ΔN) is adaptive to codeword and its usage, it has not to be decided at probe: the larger the distribution width, the larger is ΔN. It is also observed that, in case of large distributions, the greater read reference voltage resulting from a greater ΔN will not affect the bits programmed with opposite polarity, as the probability of having a bit programmed with opposite polarity close to said reference voltage is extremely low (as the result of a product of probabilities), within the ECC correction capability.

[0105] Advantageously, each codeword stored in the memory array comprises respective additional data information associated thereto.

[0106] Figure 8 is flow chart representing steps of a method 800 for accessing memory cells according to the present disclosure. The processes described can be performed by hardware logic and circuitry. For example, the following processes are described as being performed by access circuitry and sense circuitry, as disclosed herein. However, other embodiments can include different circuitry configurations suitable for performing the processes.

[0107] The method of the present disclosure is a method for improving read operations of memory cells. Prior to reading the memory cells, access circuitry writes data to a plurality of memory cells. For example, access circuitry writes logic 0s and logic 1s to a plurality of memory cells such as the memory cell 100' of figure 1. In one embodiment, access circuitry can write logic 0s by applying programming pulses with a negative polarity and logic 1s by applying programming pulses with a positive polarity. The opposite convention can also be adopted. After writing data to the plurality of memory cells, access circuitry can read the plurality of memory cells using the read sequence of the present disclosure.

[0108] More in particular, at step 810, user data are stored in a plurality of memory cells of a memory array, e.g. are stored in a codeword.

[0109] At step 820, additional data information ΔN are stored in a portion of the memory array, the additional data information representative of a voltage difference between a first threshold voltage and a second threshold voltage of the memory cells of the set of user data programmed to a first logic state, wherein the first threshold voltage is a voltage to activate a preset number of memory cells programmed to the first logic state, and wherein the second threshold voltage is a voltage to activate memory cells programmed to the first logic state having a threshold voltage whose magnitude is higher than the first threshold voltage and is based on the statistical distribution of the threshold voltages of the memory cells of said set of user data.

[0110] A further step, not shown, provides for reading the additional data information ΔN stored in the codeword to use them to perform the data reading operation.

[0111] At step 830, a read voltage is applied to activate a first group of memory cells corresponding to the preset number of memory cells. At step 840 it is determined that the first group of memory cells has been activated based on applying the read voltage. In other words, based on the application of the read voltage, it is determined if the trigger memory cells have been activated.

[0112] In case said trigger memory cells T have been activated, the voltage difference represented by ΔN is applied at step 850 to the memory array to activate a second group of memory cells programmed to the first logic state, therefore properly reading all the cells programmed to the first logic state.

[0113] Figure 9A illustrates steps of a method for programming an array of memory cells. At step 910, user data are encoded according to an Error Correction Code (ECC) scheme. A programming voltage is applied for programming to a first logic state the memory cells of the array, as in step 920 (e.g. voltage is incremented following a staircase voltage ramp or the like). At step 930, it is determined that a predetermined first group of memory cells has been switched to an active state based on the application of the programming voltage. In particular, when it is determined that all the trigger memory cells T have been activated, the programming voltage, i.e. the first threshold voltage, corresponding to the switching to the active state of all said cells is stored.

[0114] At this stage, a parallel process 900', as illustrated in figure 9B, is started by performing, at step 910', an ECC verify operation on the programmed bits and determining the value of the syndrome of said ECC.

[0115] More in particular, based on the syndrome of the ECC, the programming voltage values corresponding to an ECC syndrome toggling from a first value (e.g. 1) to a second value (e.g. 0) are stored, while the programming voltage values corresponding to an ECC syndrome different from the second

value are ignored, as shown at step 920'. The voltage values corresponding to syndrome 0 are stored and updated into a register of the array at step 930'

[0116] Referring again to figure 9A, the process of figure 9B is then invoked at step 950 and the stored programming voltages are used at step 960 to establish whether the actual programming voltage is lower than the maximum expected threshold voltage. More in particular, the last voltage value resulting in a stable syndrome equal to the 0 is regarded as the maximum threshold value and is used to calculate, at step 970, information ΔN representative of the voltage difference between the programming voltage (e.g. the last voltage step of a ramp) used to program the first group of memory cells and said last programming voltage value (i.e. the voltage step of a ramp) used to program the memory cells to the first logic state within the ECC correction capability, obtaining the data information ΔN to be stored in the codeword to improve the reading operation.

[0117] Figure 10 is a high-level scheme of a system 1000 that can perform the read algorithm of the present disclosure. The system 1000 includes a memory device 1010 in turn including an array of memory cells 1020 and a circuit 1030 operatively coupled to the memory cells 1020; the memory cells 1020 and the circuit 1030 form a memory portion, herein referred to as memory portion 1000'.

[0118] The memory device 1010 comprises a memory controller 1040, which represents control logic that generates memory access commands, for example in response to command by a host 1050. Memory controller 1040 accesses memory portion 1000'. In one embodiment, memory controller 1040 can also be implemented in the host 1050, in particular as part of a host processor 1060, even if the present disclosure is not limited by a particular architecture. The controller 1040 can include an embedded firmware and is adapted to manage and control the operation of the memory portion 1000'.

[0119] In general, the memory controller 1040 may receive user data through input/output IO. As shown before, in some embodiments, the memory

controller encodes the user data to satisfy a condition prior to storing the user data in memory cells. The condition may be satisfied when encoded user data have a predetermined number of bits exhibiting a given logic value (e.g., a logic value of 1). As a way of example, the encoded user data may be configured to have 50% of the memory cells storing the encoded user data to exhibit the logic state of 1 while the other 50% of the memory cells to exhibit a logic state of 0 (i.e. the balanced encoding scheme, where half of the encoded user data bits have a logic state of 1, and the other half have a logic state of 0). During the encoding process, the memory controller 1040 may add a certain number of bits (e.g., parity bits) to the user data to establish the predetermined number of memory cells to exhibit the given logic state. As a result of adding the parity bits, the encoded user data may have more bits than the user data. In some embodiments, a different percentage value (e.g., 40%, 60%, 75%) of the memory cells exhibiting the logic state of 1 may be employed during the encoding process.

[0120] The value of the voltage difference ΔN may be stored by the memory controller 1040 in the array as a codeword portion.

[0121] The memory device 1010 can also comprise other components, such as processor units coupled to the controller 1040, antennas, connection means (not shown) with the host device, and the like.

[0122] Multiple signal lines couple the memory controller 1040 with the memory portion 1000'. For example, such signal lines may include clock, command/address and write data (DQ), read DQ, and zero or more other signal lines. The memory controller 1040 is thus operatively coupled to the memory portion 1000' via suitable buses.

[0123] The memory portion 1000' represents the memory resource for the system 1000. In one embodiment, the array of memory cells 1020 is managed as rows of data, accessed via wordline (rows) and bitline (individual bits within a row) control. In one embodiment, the array 1020 of memory cells includes a 3D crosspoint array such as the memory cell array 200 of figure 2. The array 1020

of memory cells can be organized as separate channels, ranks, and banks of memory. Channels are independent control paths to storage locations within memory portion. Ranks refer to common locations across multiple memory devices (e.g., same row addresses within different devices). Banks refer to arrays of memory locations within a memory device. In one embodiment, banks of memory are divided into sub-banks with at least a portion of shared circuitry (e.g., drivers, signal lines, control logic) for the sub-banks. It will be understood that channels, ranks, banks, or other organizations of the memory locations, and combinations of the organizations, can overlap physical resources. For example, the same physical memory locations can be accessed over a specific channel as a specific bank, which can also belong to a rank. Thus, the organization of memory resources will be understood in an inclusive, rather than exclusive, manner.

[0124] In one embodiment, the memory controller 1040 includes refresh (REF) logic 1041. In one embodiment, refresh logic 1041 indicates a location for refresh, and a type of refresh to perform. Refresh logic 1041 can trigger self-refresh within memory, and issue external refreshes by sending refresh commands to trigger the execution of a refresh operation.

[0125] In one embodiment, access circuitry 1031 of the circuit 1030 performs a refresh (e.g., reprogramming) of any of the accessed memory cells that were not refreshed during the read sequence. Therefore, a complete refresh of memory cells can be achieved as mostly a side effect of the memory read sequence with minimal additional refresh operations.

[0126] In an embodiment, the circuit can also be embedded in the memory controller, even if the present disclosure is not limited by a particular architecture.

[0127] In the exemplary embodiment illustrated in figure 10, the memory controller 1040 includes error correction circuitry 1042. The error detection/correction circuitry 1042 can include hardware logic to implement an error correction code (ECC) to detect errors occurring in data read from memory

portion. In one embodiment, error detection/correction circuitry 1042 also corrects errors (up to a certain error rate based on the implemented ECC code). However, in other embodiments, error detection/correction circuitry 1042 only detects but does not correct errors.

[0128] More in particular, the controller 1040 may be configured to encode user data according to an Error Correction Code (ECC) scheme, and may comprise a syndrome calculation unit configured to produce, from the encoded set of user data, a syndrome value, the controller being configured so that, when the syndrome value is zero, the corresponding programming voltage value is stored in a register and/or latch of the array and, when the syndrome is different from zero, the corresponding programming voltage is ignored, wherein the second threshold voltage is the last programming voltage corresponding to a syndrome equal to zero, the controller being configured to update in said register or latch the programming voltage anytime the ECC syndrome is toggling from a value different from zero to zero, according to an architecture analogous to the one shown in figure 7.

[0129] In an embodiment, the first threshold voltage is the median threshold voltage value of the memory cells in the first logic state, the controller being configured to track said median value.

[0130] In the illustrated embodiment, the memory controller 1040 includes command (CMD) logic 1043, which represents logic or circuitry to generate commands to send to memory portion. The memory controller 1040 may also include a counter 1044, such as the per-codeword counter disclosed above and configured to count the number of bits switched during the read operation. Clearly, also other architectures can be employed, for example the counter can be embedded in the host 1050 or also in the circuit 1030.

[0131] Based on the received command and address information, access circuitry 1031 of the circuit 1030 performs operations to execute the commands, such as the read operation of the present disclosure. In one such embodiment, the circuit 1030 includes sense circuitry 1032 to detect electrical

responses of the one or more memory cells to the applied read voltage. In one embodiment, the sense circuitry 1032 include sense amplifiers. Figure 10 illustrates the access circuitry 1031 and sense circuitry 1032 as being embedded in the memory portion 1000', however, other embodiments can include access circuitry and/or sense circuitry that is separate from the memory portion 1000'. For example, access circuitry and sense circuitry can be included in a memory controller such as the memory controller 1040.

[0132] Sense circuitry may be configured to detect a current through a given memory cell in response to the read voltage, wherein the access circuitry is configured to determine that the given memory cell is in the first logic state based on detection that a magnitude of the current is greater than or equal to a threshold current.

[0133] In one embodiment, memory portion 1000' includes one or more registers 1033. The registers 1033 represent one or more storage devices or storage locations that provide configuration or settings for the operation of the memory portion. Furthermore, in one embodiment, the circuit 1030 includes also decode circuitry 1034.

[0134] The host device 1050 is a computing device in accordance with any embodiment described herein, and can be a laptop computer, a desktop computer, a server, a gaming or entertainment control system, a scanner, copier, printer, routing or switching device, embedded computing device, or other electronic device such as a smartphone. The memory device 1010 may also be embedded in the host device 1050.

[0135] In one embodiment, the system 1000 includes an interface 10100 coupled to the processor 1060, which can represent a higher speed interface or a high throughput interface for system components that needs higher bandwidth connections, and/or graphics interface components. Graphics interface interfaces to graphics components for providing a visual display to a user of system 1000. In one embodiment, graphics interface generates a display

based on data stored in the memory device or based on operations executed by processor or both.

[0136] The system may also comprise network interface 1080 communicatively coupled to the host or to memory device for example for connecting with other systems, and/or a battery coupled to provide power to said system.

[0137] In conclusion, the present disclosure provides a read and programming method based on the switching of a predetermined and the subsequent application of a read pulse determined, codeword by codeword, according to the actual statistical distribution of bits in the codeword, improving the performances of the array.

[0138] According to an exemplary embodiment, a method for operating (accessing) an array of memory cells comprises the steps of storing a set of user data in a plurality of memory cells of the memory array, storing, in a portion of the memory array, additional data information, these additional data information being a voltage difference between a first threshold voltage and a second threshold voltage of the memory cells of the set of user data programmed to a first logic state, wherein the first threshold voltage is a voltage to activate a preset number of memory cells programmed to the first logic state, and wherein the second threshold voltage is a voltage to activate memory cells programmed to the first logic state having a threshold voltage whose magnitude is higher than the first threshold voltage and is based on the statistical distribution of the threshold voltages of the memory cells of the set of user data, applying to the memory array a read voltage to activate a first group of memory cells corresponding to the preset number of memory cells, determining that the first group of memory cells has been activated based on applying the read voltage, wherein said read voltage is equal to the first threshold voltage when the first group of memory cells has been activated, and, based on the additional data information (i.e. after reading the additional data information), applying the voltage difference to the memory array to activate a second group of memory cells programmed to the first logic state.

[0139] According to another exemplary embodiment, a method for programming an array of memory cells comprises the steps of encoding user data according to an Error Correction Code (ECC) scheme, applying a programming voltage for programming to a first logic state the memory cells of the array (i.e. storing the user data in the first logic state), determining that a predetermined first group of memory cells has been switched to an active state based on the application of the programming voltage, storing, in a portion of the memory array, the programming voltage corresponding to the switching to the active state of all the cells of the predetermined first group of memory cells, performing, while applying the programming voltage to the array to program all cells to the first logic state, an ECC verify operation and determining the value of the syndrome of said ECC, based on the syndrome of the ECC, storing the programming voltage values corresponding to an ECC syndrome toggling from a first value to a second value and ignoring the programming voltage values corresponding to an ECC syndrome different from the second value, storing, in a portion of the memory array, the voltage difference between the programming voltage used to program the first group of memory cells and the last programming voltage value used to program the memory cells to the first logic state within the ECC correction capability, said last voltage value resulting in a toggling to a stable ECC syndrome equal to the second value. In an embodiment, the first value of the syndrome is different from zero and the second value is zero.

[0140] If not explicitly indicated, method steps are not necessarily in the indicated sequence.

[0141] The present disclosure also discloses a memory device comprising an array of memory cells, at least a codeword in the memory array including a set of user data and additional data information, these additional data information being a voltage difference between a first threshold voltage and a second threshold voltage of the memory cells of the set of user data programmed to a first logic state, wherein the first threshold voltage is a voltage to activate a preset number of memory cells programmed to the first logic state, and wherein the second threshold voltage is a voltage to activate memory cells programmed

to the first logic state having a threshold voltage whose magnitude is higher than the first threshold voltage and is based on the statistical distribution of the threshold voltages of the memory cells of the set of user data, the device further comprising a memory controller configured to execute instructions for accessing the memory cells, and a circuit for accessing the memory cells, the circuit being operatively coupled with the array of memory cells and comprising at least an access circuit configured to apply to the memory array a read voltage to activate a first group of memory cells corresponding to the preset number of memory cells, a sense circuit configured to determine that the first group of memory cells has been activated based on applying the read voltage, wherein said read voltage is equal to the first threshold voltage when the first group of memory cells has been activated, wherein, based on the additional data information stored in the memory array, the controller is configured to control the access circuit to apply the voltage difference to the memory array to activate a second group of memory cells programmed to the first logic state. In an embodiment, the array of memory cells comprises a Self-Selecting Memory (SSM) or a 3D cross point (3D X Point) memory.

[0142] A related system, comprising a host device and a memory device as above is also disclosed, the system comprising for example any of a display communicatively coupled to the memory device or to the host, a network interface communicatively coupled to the memory device or to the host, and a battery coupled to provide power to said system.

[0143] In the preceding detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, specific examples. In the drawings, like numerals describe substantially similar components throughout the several views. Other examples may be utilized, and structural, logical and/or electrical changes may be made without departing from the scope of the present disclosure. In addition, as will be appreciated, the proportion and the relative scale of the elements provided in the figures are intended to illustrate the embodiments of the present disclosure and should not be taken in a limiting sense.

[0144] As used herein, "a," "an," or "a number of" something can refer to one or more of such things. A "plurality" of something intends two or more. As used herein, the term "coupled" may include electrically coupled, directly coupled, and/or directly connected with no intervening elements (e.g., by direct physical contact) or indirectly coupled and/or connected with intervening elements. The term coupled may further include two or more elements that co-operate or interact with each other (e.g., as in a cause and effect relationship).

[0145] Although specific examples have been illustrated and described herein, those of ordinary skill in the art will appreciate that an arrangement calculated to achieve the same results can be substituted for the specific embodiments shown. This disclosure is intended to cover adaptations or variations of one or more embodiments of the present disclosure. It is to be understood that the above description has been made in an illustrative fashion, and not a restrictive one. The scope of one or more examples of the present disclosure should be determined with reference to the appended claims, along with the full range of equivalents to which such claims are entitled.

CLAIMS

1. A method for accessing an array of memory cells, comprising the steps of:

- storing a set of user data in a plurality of memory cells of the memory array;

- storing, in a portion of the memory array, additional data information, said additional data information being representative of a voltage difference between a first threshold voltage and a second threshold voltage of the memory cells of the set of user data programmed to a first logic state, wherein the first threshold voltage is a voltage to activate a preset number of memory cells programmed to the first logic state, and wherein the second threshold voltage is a voltage to activate memory cells programmed to the first logic state having a threshold voltage whose magnitude is higher than the first threshold voltage and is based on the statistical distribution of the threshold voltages of the memory cells of said set of user data;

- applying to the memory array a read voltage to activate a first group of memory cells corresponding to the preset number of memory cells;

- determining that the first group of memory cells has been activated based on applying the read voltage, wherein said read voltage is equal to the first threshold voltage when the first group of memory cells has been activated; and

- based on the additional data information, applying the voltage difference to the memory array to activate a second group of memory cells programmed to the first logic state.

2. The method of claim 1, wherein the memory cells of the second group of memory cells have threshold voltages whose magnitude is comprised between the first threshold voltage and the second threshold voltage, said second read voltage being the expected maximum magnitude threshold voltage of the memory cells programmed to the first logic state.

3. The method of claim 1, wherein the second threshold voltage is the programming voltage corresponding to an activation of all the cells in the first logic state, within Error Correction Code (ECC) correction capability.

4. The method of claim 3, wherein storing the user data comprises a step of computing a syndrome of the ECC, wherein:

- when the syndrome is toggling from a value different from zero to zero, the corresponding programming voltage value is stored;

- when the syndrome is different from zero, the corresponding programming voltage is ignored, and

wherein the second threshold voltage is the last programming voltage corresponding to a syndrome equal to zero.

5. The method of claim 1, comprising the step of applying an additional margin read voltage after the application of the voltage difference to account for voltage threshold distributions enlarging with time.

6. The method claim 1, comprising performing an Error Correction Code (ECC) verify operation after the application of the voltage difference, and comprising applying a further read voltage in case the ECC verify operation results in an error to be corrected in the set of user data.

7. The method of claim 1, wherein the first threshold voltage is the median threshold voltage value of the memory cells in the first logic state.

8. The method according to claim 1, wherein the user data are encoded in a codeword having a number of bits exhibiting the first logic state in a range, the encoding step comprising manipulating the codeword to constrain the number of bits exhibiting the first logic value in the range.

9. The method according to claim 8, wherein the encoded user data have substantially a same number of bits exhibiting the first logic state and a second

logic state, and wherein the memory cells exhibit a threshold voltage with a lower magnitude when the memory cells are in the first logic state, and a threshold voltage with a higher magnitude when the memory cells are in the second logic state, and wherein a logic state of a given cell is determined based on whether the memory cell exhibits a higher or lower magnitude threshold voltage in response to the applied read voltage.

10. The method according to claim 1, wherein the additional data information comprises bits protected using an Error Correction Code (ECC) and/or a differential cells scheme.

11. The method of claim 1, wherein the read voltage is a staircase voltage ramp.

12. A method for programming an array of memory cells, comprising the steps of:

- encoding user data according to an Error Correction Code (ECC) scheme;

- applying a programming voltage for programming to a first logic state the memory cells of the array;

- determining that a predetermined first group of memory cells has been switched to an active state based on the application of the programming voltage;

- storing, in a portion of the memory array, the programming voltage corresponding to the switching to the active state of all the cells of the predetermined first group of memory cells;

- performing an ECC verify operation and determining the value of the syndrome of said ECC;

- based on the syndrome of the ECC, storing the programming voltage values corresponding to an ECC syndrome toggling from a first value to a second value and ignoring the programming voltage values corresponding to an ECC syndrome different the second value; and

- storing, in a portion of the memory array, the voltage difference between the programming voltage used to program the first group of memory cells and the last programming voltage value used to program the memory cells to the first logic state resulting in a toggling of ECC syndrome to the second value.

13. The method of claim 12, wherein the first value of the syndrome is different from zero and the second value is zero.

14. The method of claim 12, wherein, during the application of the programming voltage, anytime the ECC syndrome is toggling from a value different from zero to zero, the corresponding voltage value is stored updating the previous value thereof.

15. The method of claim 12, wherein the memory cells to be programmed are included in vertical 3D memory devices.

16. The method of claim 12, wherein user data are encoded in a codeword having a number of bits exhibiting the first logic state in a range, the encoding step comprising manipulating the codeword to constrain the number of bits exhibiting the first logic value in the range, and wherein the encoded user data have substantially a same number of bits exhibiting the first logic value and a second logic value.

17. The method of claim 12, wherein the programming voltage is a staircase voltage ramp.

18. The method of claim 12, comprising, after programming the cells to the first logic state, a step of write-back for programming further memory cells of the array to a second logic state, wherein the cells that have to be programmed to the second logic state are initially masked in such a way that, during the application of the programming voltage for programming the cells to the first logic state, said masked cells are regarded as memory cells already programmed to said second logic state.

19. The method of claim 12, wherein each codeword stored in the memory array comprises respective additional data information associated thereto.

20. A memory device comprising:

- an array of memory cells;

- at least a codeword in the memory array including a set of user data and additional data information, said additional data information being representative of a voltage difference between a first threshold voltage and a second threshold voltage of the memory cells of the set of user data programmed to a first logic state, wherein the first threshold voltage is a voltage to activate a preset number of memory cells programmed to the first logic state, and wherein the second threshold voltage is a voltage to activate memory cells programmed to the first logic state having a threshold voltage whose magnitude is higher than the first threshold voltage and is based on the statistical distribution of the threshold voltages of the memory cells of said set of user data;

- a memory controller configured to execute instructions for accessing the memory cells; and

- a circuit for accessing the memory cells, the circuit being operatively coupled with the array of memory cells and comprising at least:

- an access circuit configured to apply to the memory array a read voltage to activate a first group of memory cells corresponding to the preset number of memory cells; and

- a sense circuit configured to determine that the first group of memory cells has been activated based on applying the read voltage, wherein said read voltage is equal to the first threshold voltage when the first group of memory cells has been activated,

wherein, based on the additional data information stored in the memory array, the controller is configured to control the access circuit to apply the voltage

difference to the memory array to activate a second group of memory cells programmed to the first logic state.

21. The memory device of claim 20, wherein the sense circuitry is configured to detect a current through a given memory cell in response to the read voltages, and wherein the access circuitry is configured to determine that the given memory cell is in the first logic state based on detection that a magnitude of the current is greater than or equal to a first threshold current.

22. The memory device of claim 20, wherein the read voltage is a staircase voltage ramp.

23. The memory device of claim 20, wherein the array of memory cells comprises a Self-Selecting Memory (SSM) or a 3D cross point (3D X Point) memory.

24. The memory device of claim 20, wherein the controller is configured to encode user data according to an Error Correction Code (ECC) scheme.

25. The memory device of claim 24, comprising a syndrome calculation unit configured to produce, from the encoded set of user data, a syndrome value, the controller being configured so that, when the syndrome value is toggling from a value different from zero to zero, the corresponding programming voltage value is stored in a register and/or latch of the array and, when the syndrome is different from zero, the corresponding programming voltage is ignored, wherein the second threshold voltage is the last programming voltage corresponding to a syndrome equal to zero, the controller being configured to update in said register and/or latch the programming voltage anytime the ECC syndrome is toggling from a value different from zero to zero.

26. The memory device of claim 20, wherein the access circuity is configured to apply an additional margin read voltage after the application of the second read voltage to account for voltage threshold distributions enlarging with time, and/or to perform an Error Correction Code (ECC) verify operation after the application of the second read voltage and to apply a further read voltage in case

the ECC verify operation results in an error to be corrected in the set of user data.

27. The memory device of claim 20, wherein the first threshold voltage is the median threshold voltage value of the memory cells in the first logic state, the controller being configured to track said median value.

28. A system comprising:

- a host device; and

- a memory device according to claim 20.

29. The system of claim 28, further comprising any of a display communicatively coupled to the memory device or to the host, a network interface communicatively coupled to the memory device or to the host, and a battery coupled to provide power to said system.

.

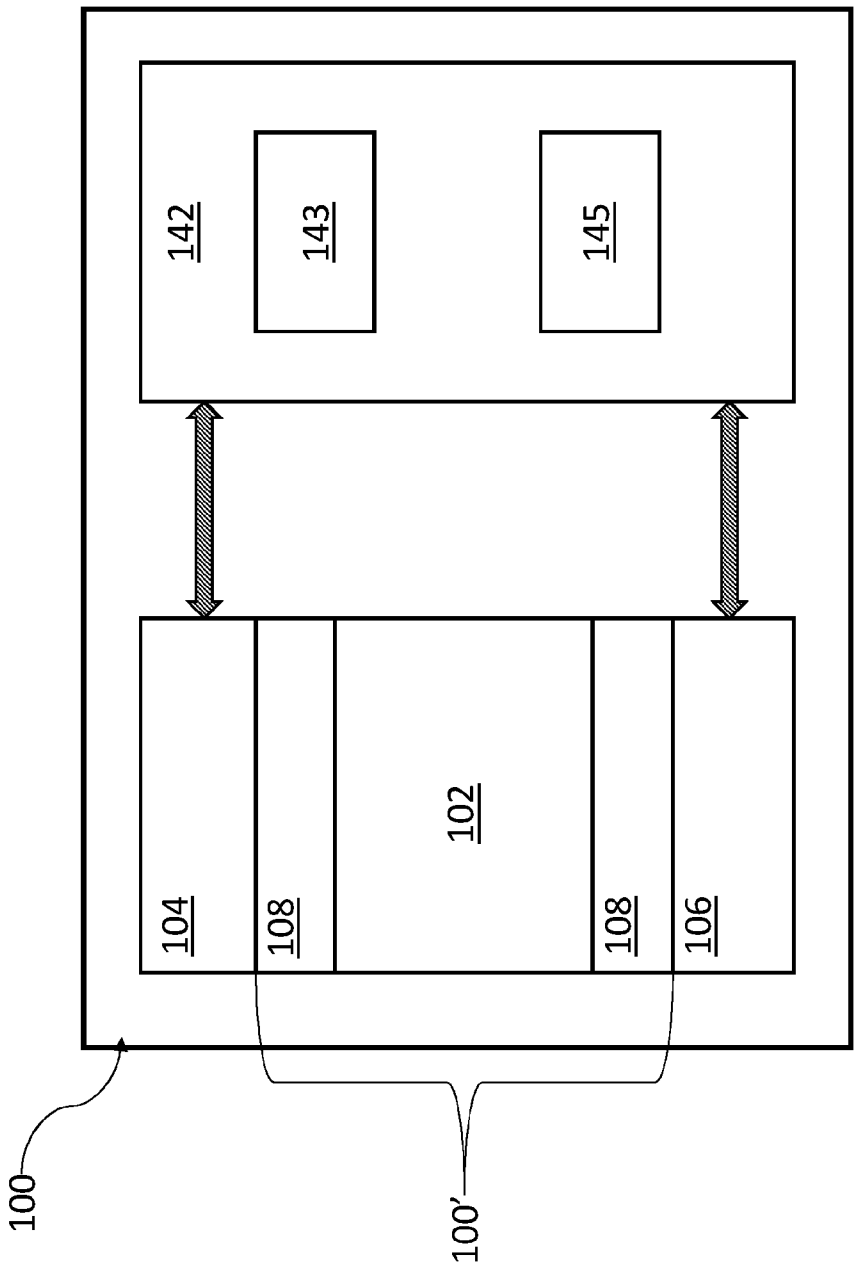

FIG. 1

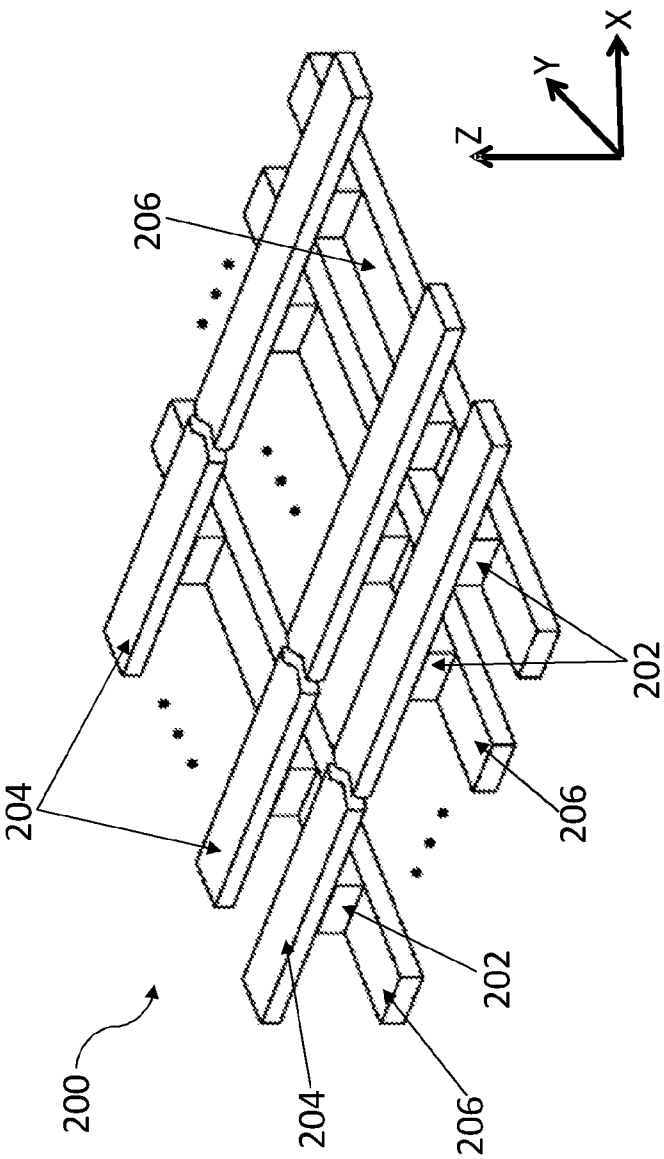

FIG. 2

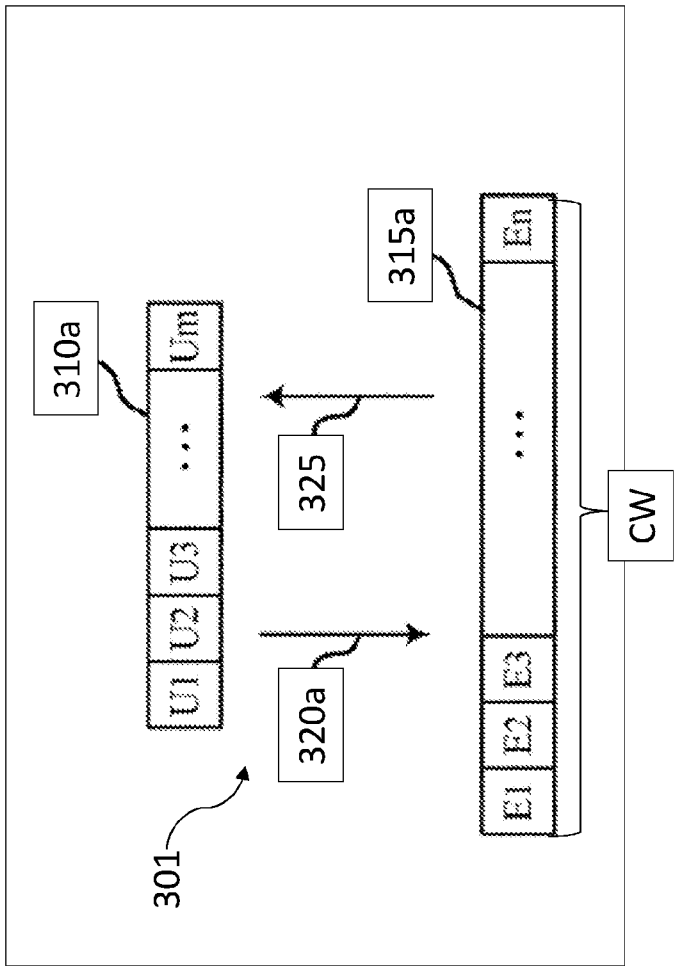

FIG. 3

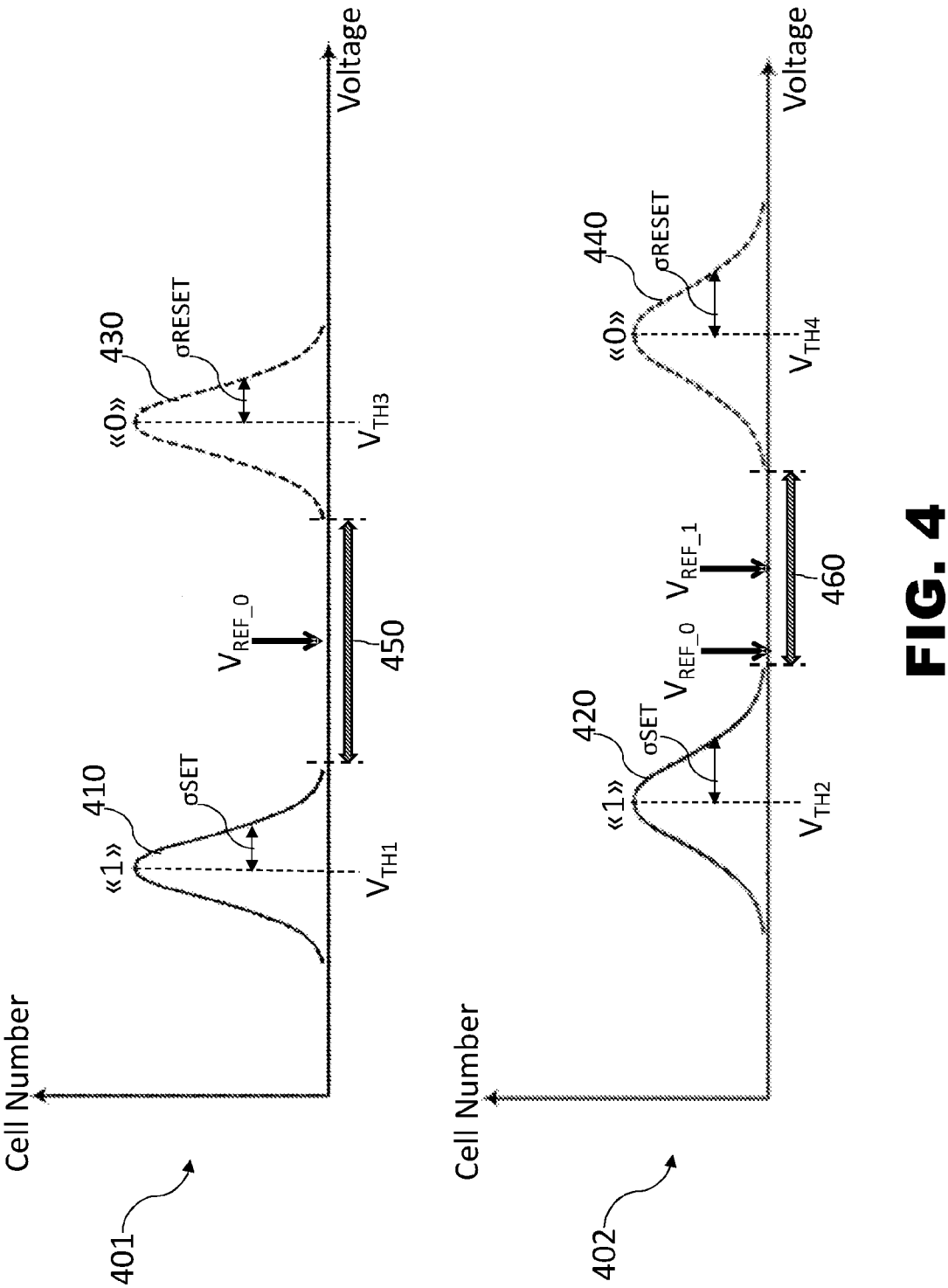
Cell Number
Voltage
401
«1»
«0»
410
420
430
440
σSET
σRESET
V_{TH1}
V_{TH2}
V_{TH3}
V_{TH4}
V_{REF_0}
V_{REF_1}
450
460
402

FIG. 4

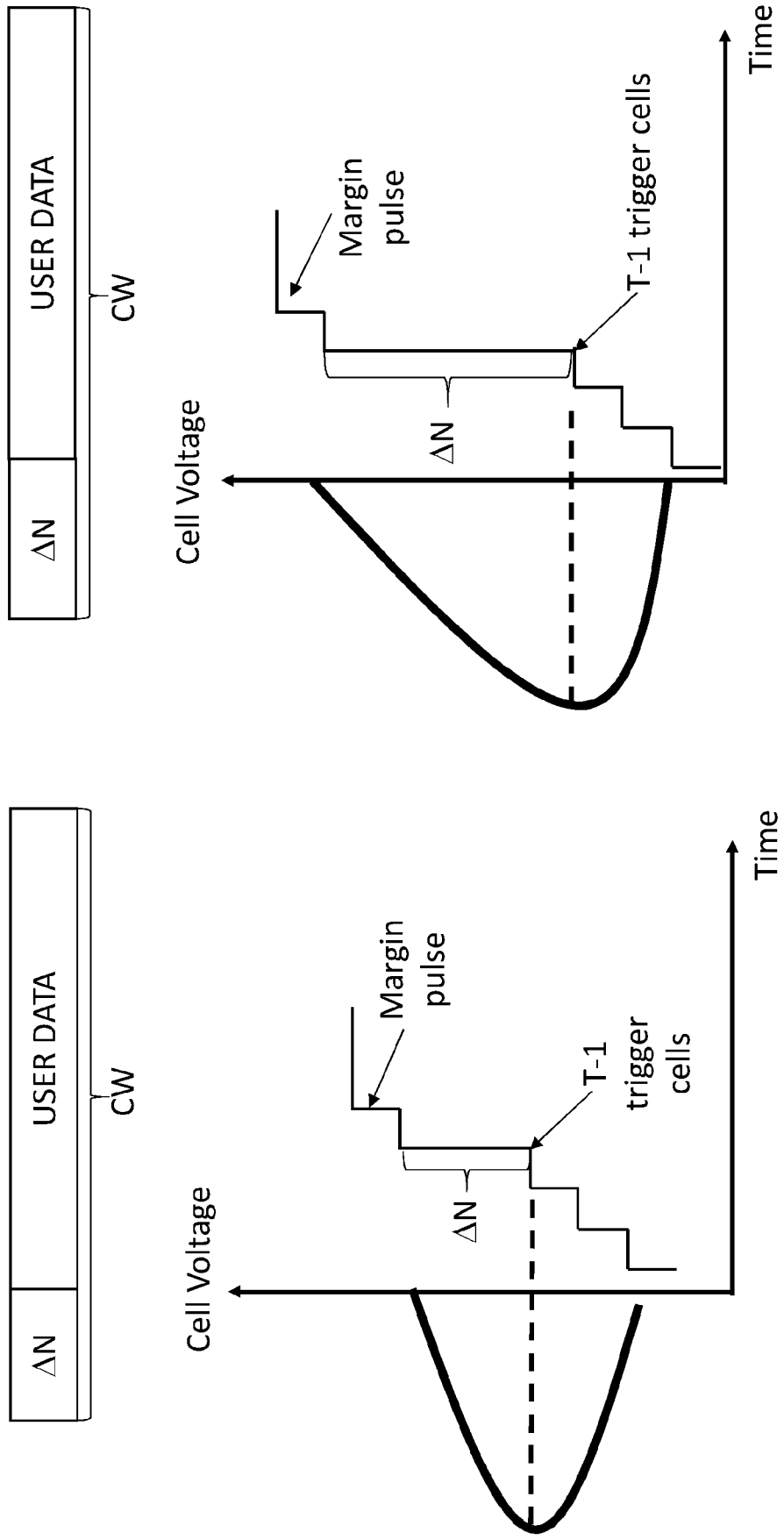
USER DATA
CW
ΔN
Cell Voltage
Margin pulse
T-1 trigger cells
ΔN
Time
USER DATA
CW
ΔN
Cell Voltage
Margin pulse
T-1 trigger cells
ΔN
Time

FIG. 5A

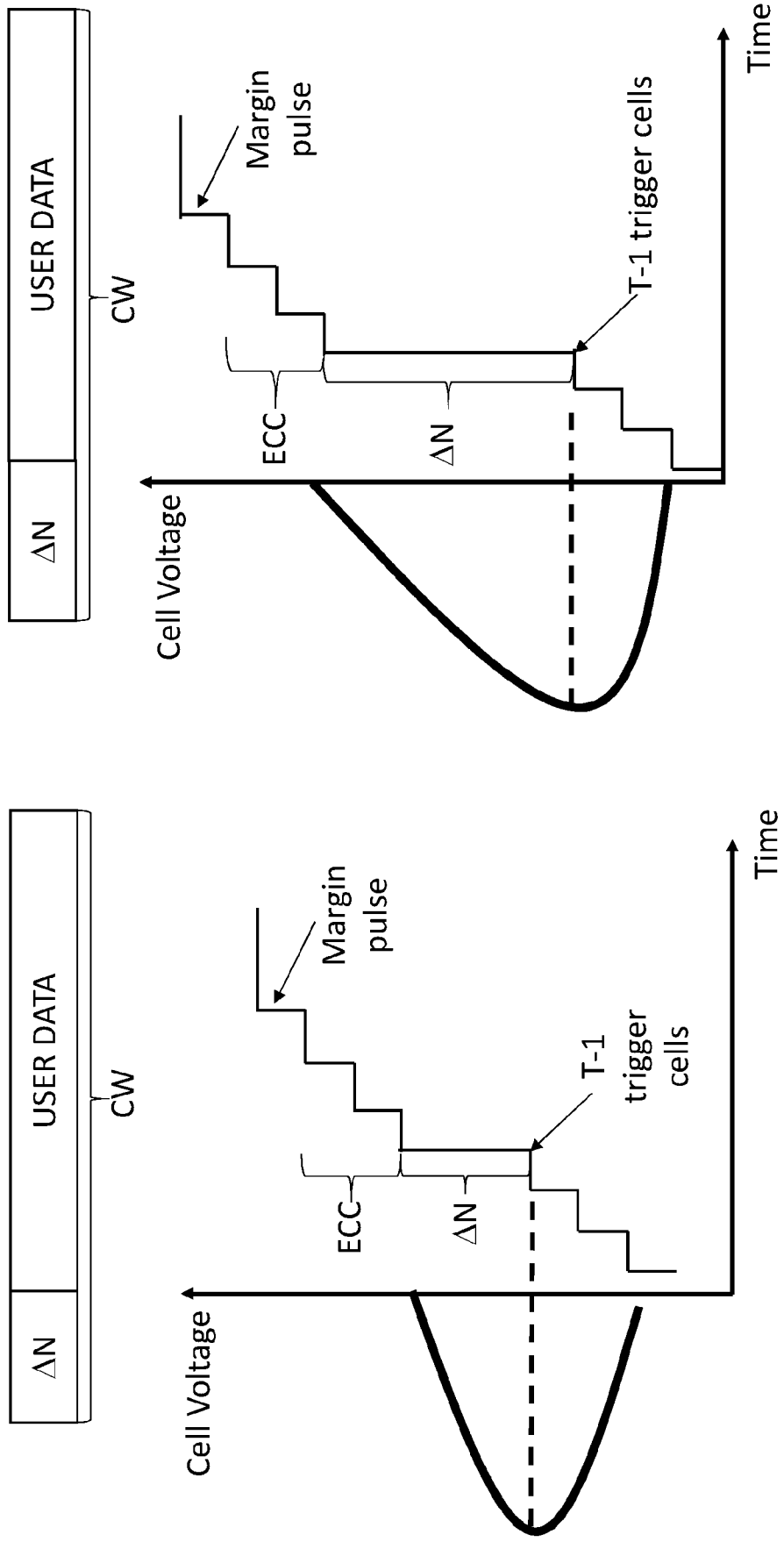
USER DATA
ΔN
CW
Margin pulse
T-1 trigger cells
ECC
ΔN
Cell Voltage
Time
USER DATA
ΔN
CW
Margin pulse
T-1 trigger cells
ECC
ΔN
Cell Voltage
Time

FIG. 5B

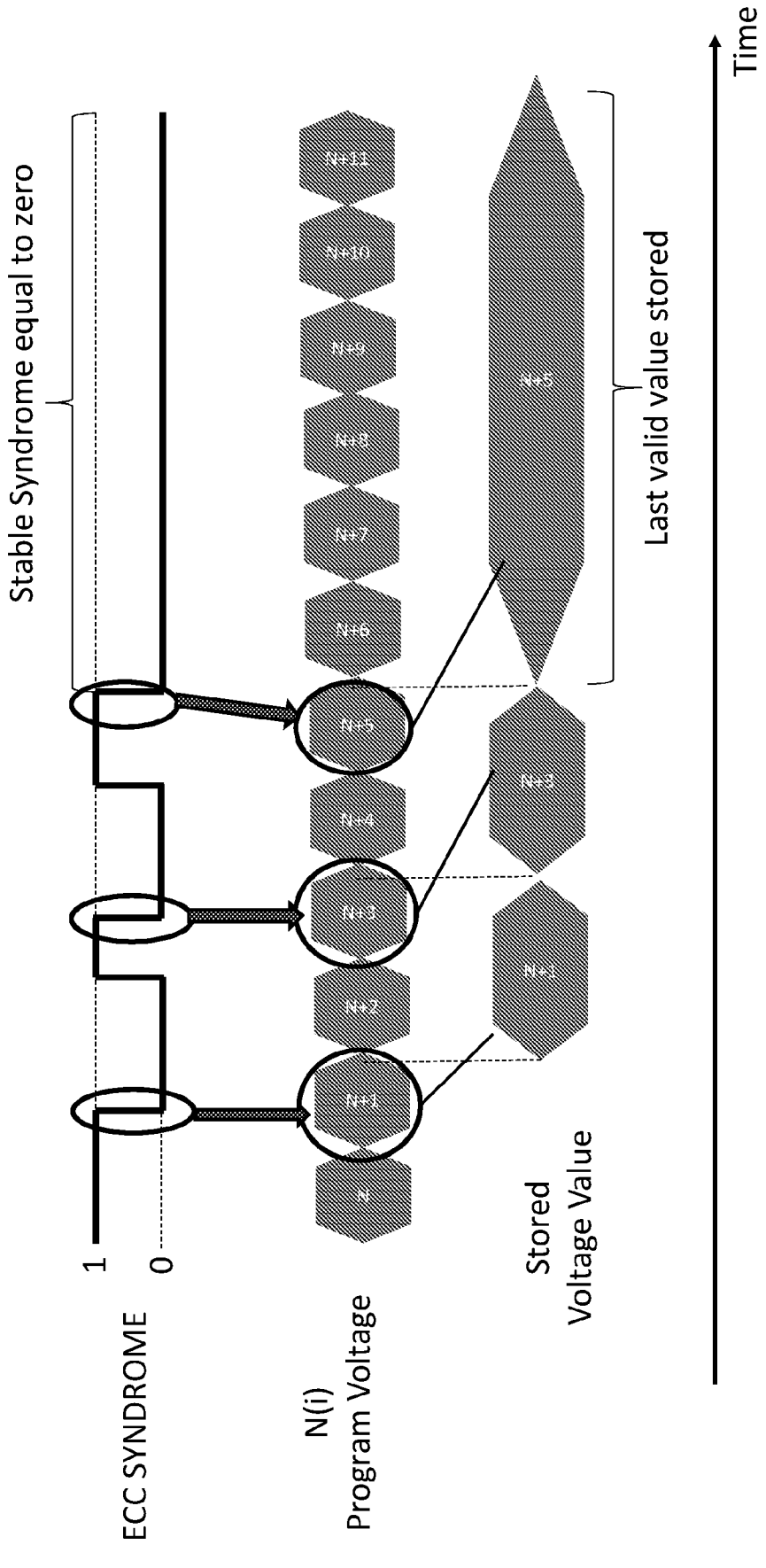
Stable Syndrome equal to zero
ECC SYNDROME
1
0
N(i)
Program Voltage
N+11
N+10
N+9
N+8
N+7
N+6
N+5
N+4
N+3
N+2
N+1
N
Stored
Voltage Value
N+5
N+3
N+1
Last valid value stored
Time

FIG. 6

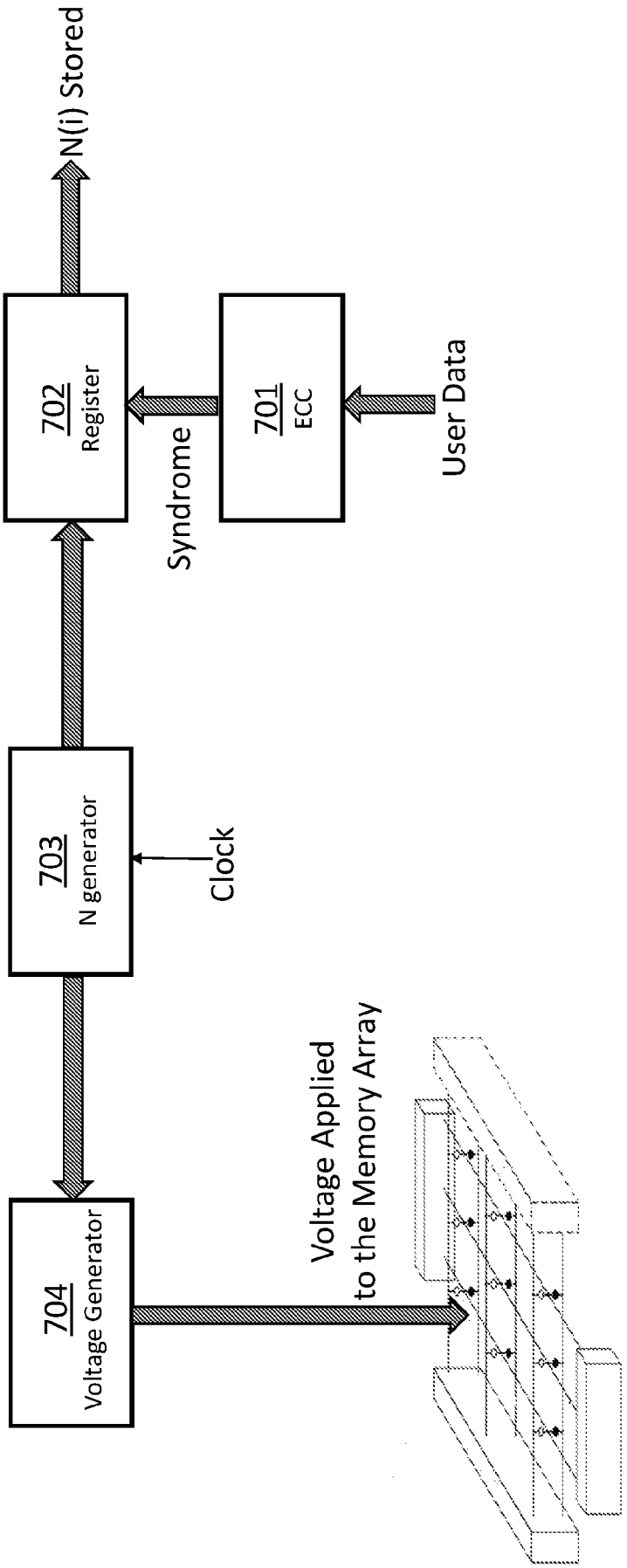
N(i) Stored
702
Register
701
ECC
User Data
Syndrome
703
N generator
Clock
704
Voltage Generator
Voltage Applied
to the Memory Array

FIG. 7

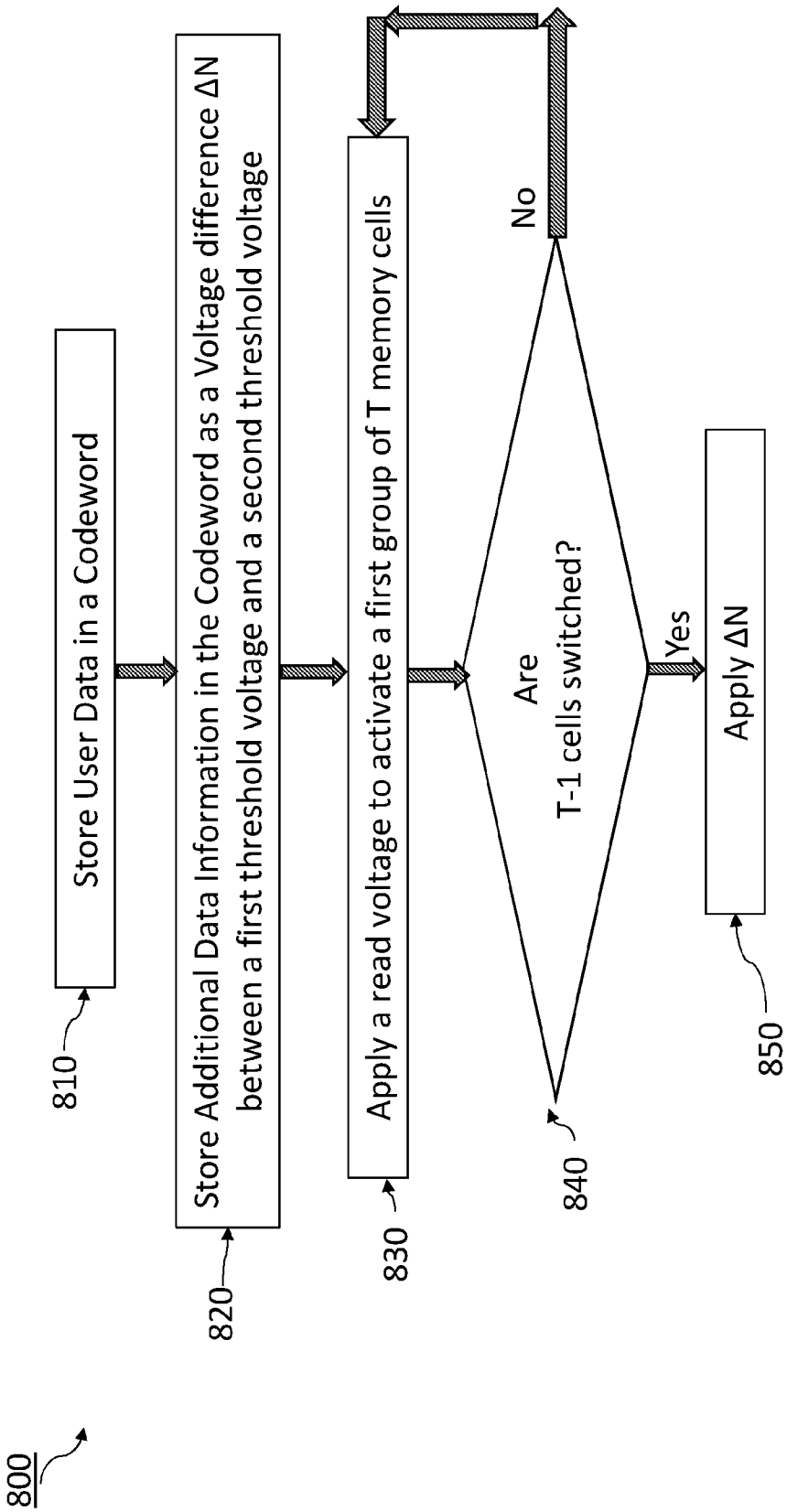
800
Store User Data in a Codeword
810
Store Additional Data Information in the Codeword as a Voltage difference ΔN between a first threshold voltage and a second threshold voltage
820
Apply a read voltage to activate a first group of T memory cells
830
Are T-1 cells switched?
840
No
Yes
Apply ΔN
850

FIG. 8

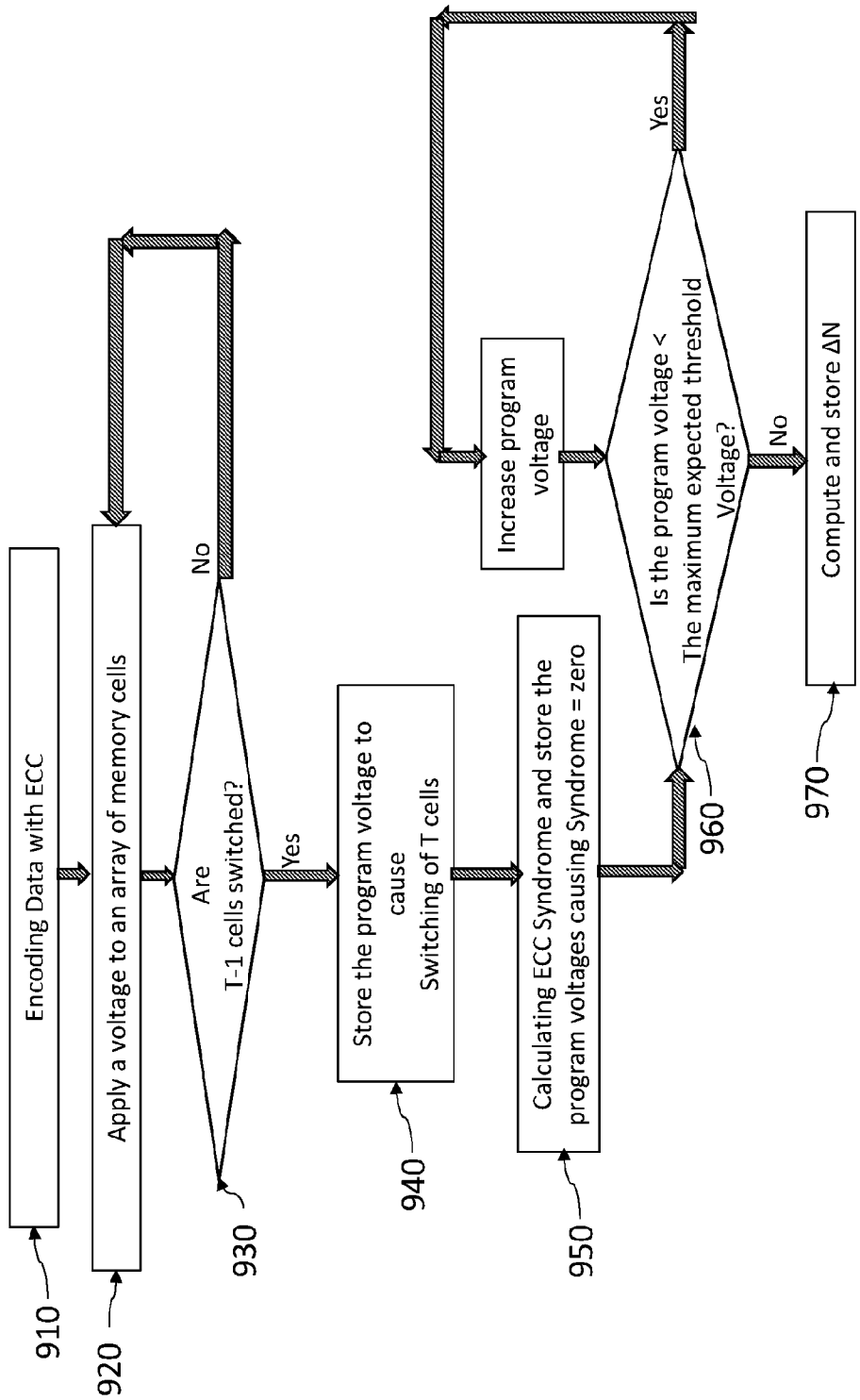
900
910
Encoding Data with ECC
920
Apply a voltage to an array of memory cells
930
Are T-1 cells switched?
No
Yes
940
Store the program voltage to cause Switching of T cells
950
Calculating ECC Syndrome and store the program voltages causing Syndrome = zero
960
Is the program voltage < The maximum expected threshold Voltage?
Yes
Increase program voltage
No
970
Compute and store ΔN

FIG. 9A

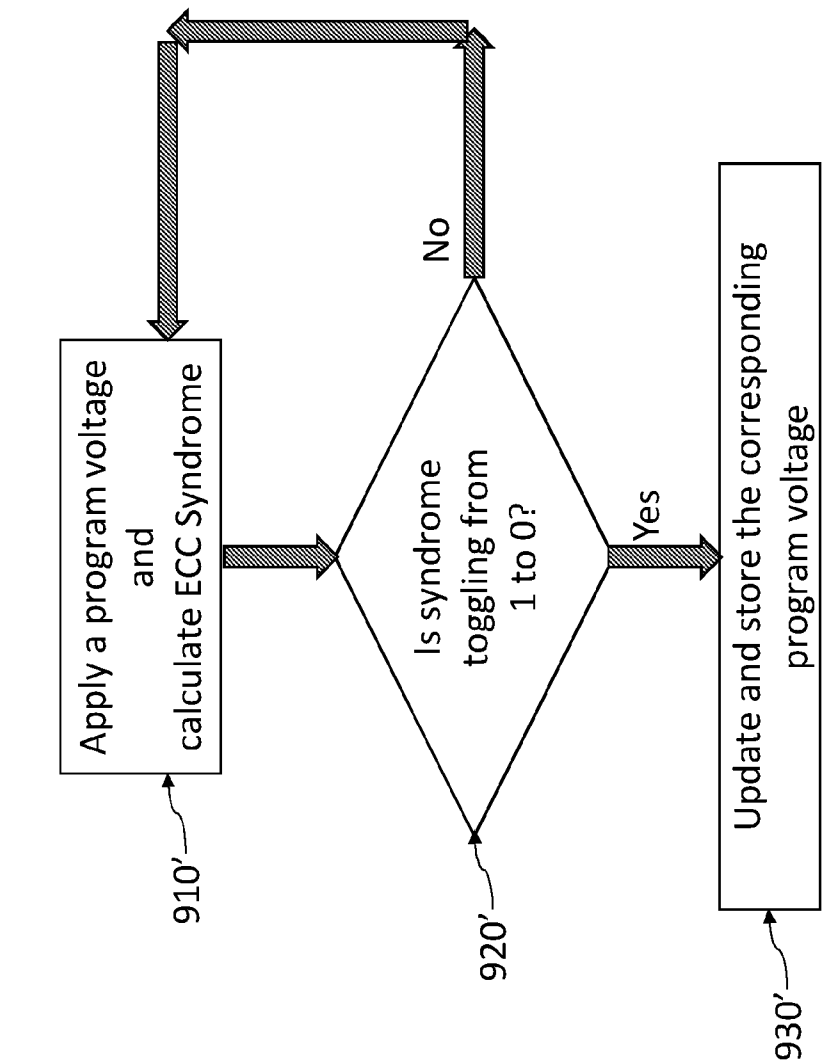
900'
Apply a program voltage and calculate ECC Syndrome
910'
Is syndrome toggling from 1 to 0?
920'
No
Yes
Update and store the corresponding program voltage
930'

FIG. 9B

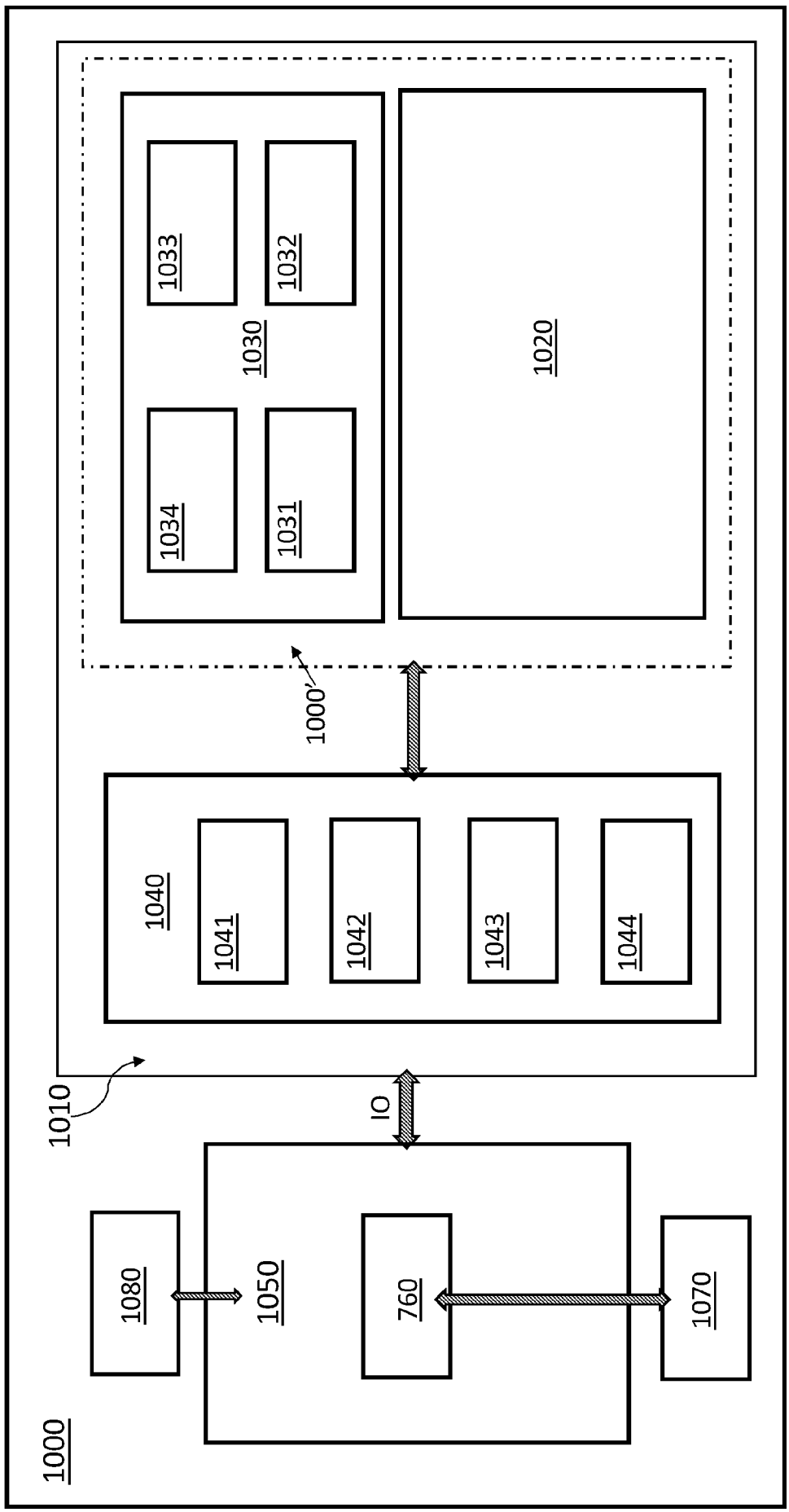
1000
1080
1050
760
1070
IO
1010
1040
1041
1042
1043
1044
1000'
1030
1033
1032
1034
1031
1020

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2020/020035

A. CLASSIFICATION OF SUBJECT MATTER

G11C 13/00(2006.01)i; **G06F 11/10**(2006.01)i; **G06F 12/02**(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 13/00(2006.01); G06F 11/10(2006.01); G11B 20/10(2006.01); G11C 11/56(2006.01); G11C 13/02(2006.01); G11C 16/04(2006.01); G11C 16/28(2006.01); G11C 29/50(2006.01); G11C 7/12(2006.01); G11C 7/14(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: additional data, threshold voltage, Error Correction Code (ECC), activate, distribution, access, read

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2019-126746 A1 (MICRON TECHNOLOGY, INC.) 27 June 2019 (2019-06-27) paragraphs [0018]-[0079]; and figures 1-6	1-29
A	US 7957187 B2 (NIMA MOKHLESI et al.) 07 June 2011 (2011-06-07) column 3, line 60 - column 11, line 62; claims 1-2; and figures 1-11	1-29
A	US 2017-0140802 A1 (SK HYNIX INC.) 18 May 2017 (2017-05-18) paragraphs [0025]-[0107]; claim 1; and figures 1-13	1-29
A	US 2015-0178158 A1 (MICRON TECHNOLOGY, INC.) 25 June 2015 (2015-06-25) paragraphs [0017]-[0055]; and figures 1-6B	1-29
A	US 2019-0122726 A1 (SEAGATE TECHNOLOGY LLC) 25 April 2019 (2019-04-25) paragraphs [0022]-[0111]; and figures 1-6	1-29

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 March 2021	**31 March 2021**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office **189 Cheongsa-ro, Seo-gu, Daejeon** **35208, Republic of Korea**	**YANG, JEONG ROK**
Facsimile No. **+82-42-481-8578**	Telephone No. **+82-42-481-5709**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/IB2020/020035

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
WO 2019-126746 A1	27 June 2019	CN 111480200 A	31 July 2020
		EP 3729429 A1	28 October 2020
		KR 10-2020-0089761 A	27 July 2020
		SG 11202005283 A	29 July 2020
		US 10566052 B2	18 February 2020
		US 10741243 B2	11 August 2020
		US 2019-0198096 A1	27 June 2019
		US 2020-0211641 A1	02 July 2020
		US 2020-0335159 A1	22 October 2020
US 7957187 B2	07 June 2011	US 2009-0282186 A1	12 November 2009
		US 2011-0194348 A1	11 August 2011
		US 8154921 B2	10 April 2012
US 2017-0140802 A1	18 May 2017	CN 106710631 A	24 May 2017
		KR 10-2017-0058066 A	26 May 2017
		TW 201719377 A	01 June 2017
		US 9741402 B2	22 August 2017
US 2015-0178158 A1	25 June 2015	CN 104871142 A	26 August 2015
		CN 104871142 B	15 December 2017
		EP 2923270 A1	30 September 2015
		EP 2923270 B1	01 August 2018
		JP 2016-504658 A	12 February 2016
		JP 6059358 B2	11 January 2017
		KR 10-1752987 B1	03 July 2017
		KR 10-2015-0087337 A	29 July 2015
		TW 201432706 A	16 August 2014
		TW I536391 B	01 June 2016
		US 2014-0143631 A1	22 May 2014
		US 8984369 B2	17 March 2015
		US 9405622 B2	02 August 2016
		WO 2014-081632 A1	30 May 2014
US 2019-0122726 A1	25 April 2019	CN 107039079 A	11 August 2017
		KR 10-2017-0054277 A	17 May 2017
		US 10192614 B2	29 January 2019
		US 10347343 B2	09 July 2019
		US 10755776 B2	25 August 2020
		US 2017-0125089 A1	04 May 2017
		US 2017-0125110 A1	04 May 2017