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(19) **United States**(12) **Patent Application Publication**
RITTAKU(10) **Pub. No.: US 2011/0212594 A1**(43) **Pub. Date: Sep. 1, 2011**(54) **SEMICONDUCTOR DEVICE HAVING
ELEMENT ISOLATION REGION****Publication Classification**(75) Inventor: **Satoshi RITTAKU**, Tokyo (JP)(51) **Int. Cl.**
H01L 21/20 (2006.01)(73) Assignee: **RENESAS ELECTRONICS
CORPORATION**, Kanagawa (JP)(52) **U.S. Cl.** **438/416; 257/E21.09**(21) Appl. No.: **13/106,914**(57) **ABSTRACT**(22) Filed: **May 13, 2011****Related U.S. Application Data**

(62) Division of application No. 12/273,163, filed on Nov. 18, 2008, now Pat. No. 7,960,796, which is a division of application No. 10/011,774, filed on Dec. 11, 2001, now Pat. No. 7,462,530.

Foreign Application Priority Data

(30) Jun. 28, 2001 (JP) 2001-197190

An n-type buried diffusion layer is formed on the surface layer of the prescribed area of a p-type silicon substrate, and a p-type first high-concentration isolation diffusion layer is formed in the silicon substrate so as to surround the buried diffusion layer. An n-type epitaxial layer is formed on the silicon substrate, the buried diffusion layer, and the first high-concentration isolation diffusion layer. A p-type second high-concentration isolation diffusion layer is formed in the epitaxial layer on the first high-concentration isolation diffusion layer. A p-type low-concentration isolation diffusion layer for isolating the epitaxial layer into a plurality of island regions is formed in the epitaxial layer on the second high-concentration isolation diffusion layer.

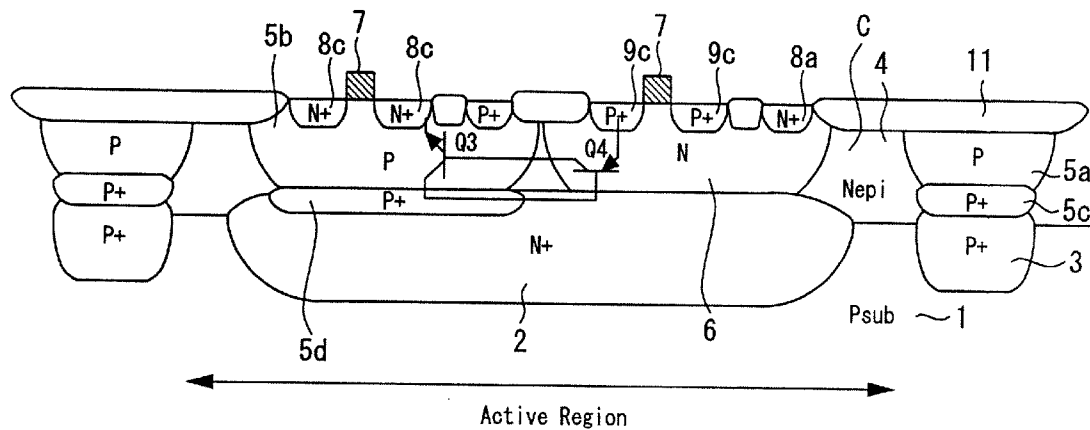


Fig. 1

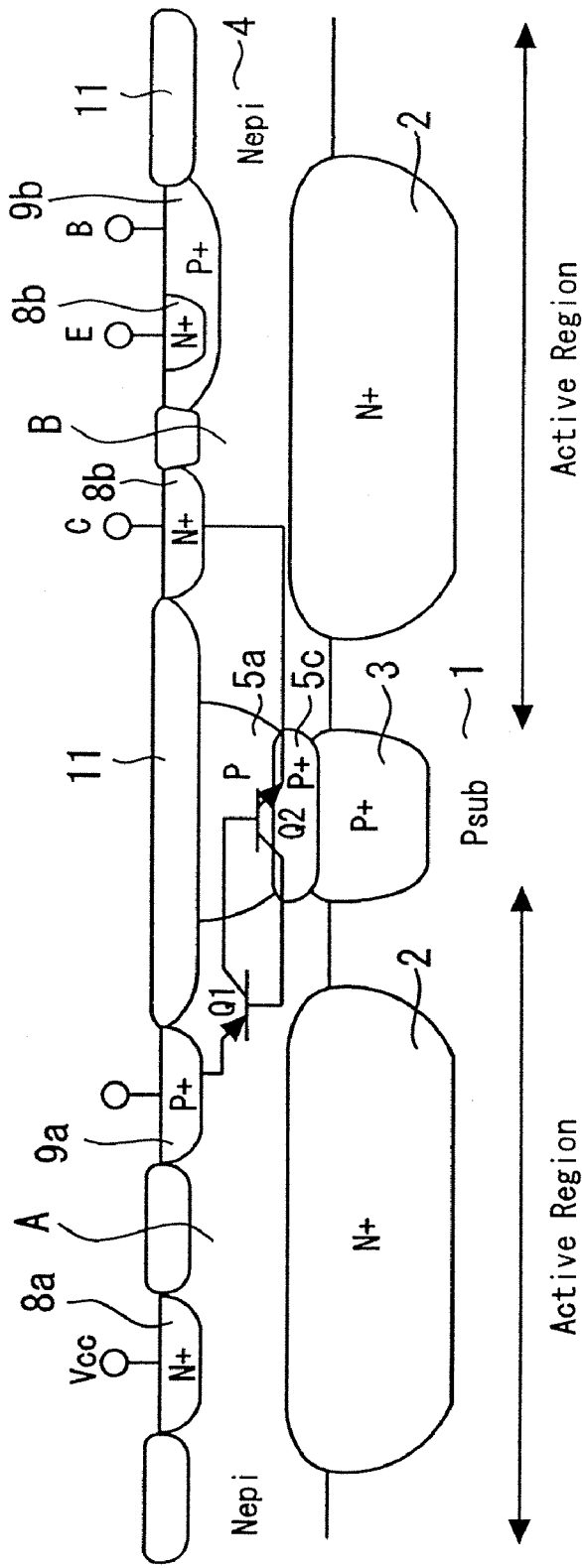


Fig. 3

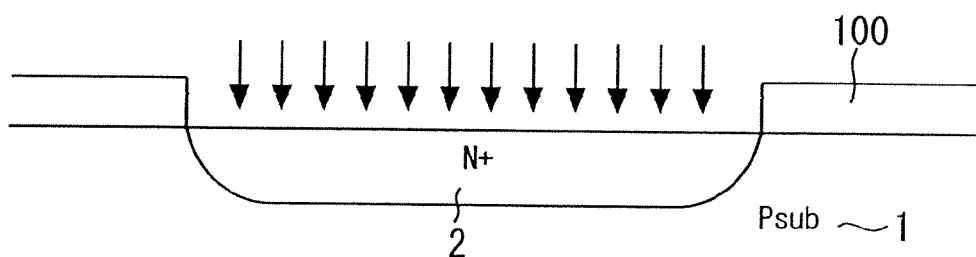


Fig. 4

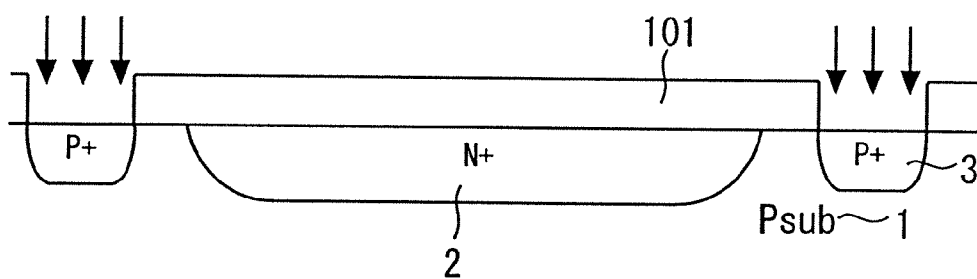


Fig. 5

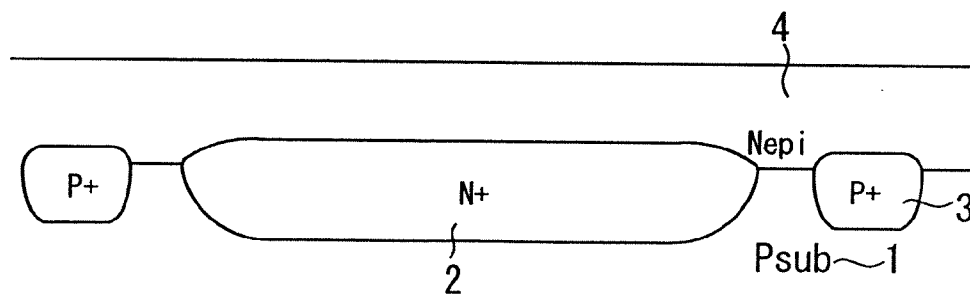


Fig. 6

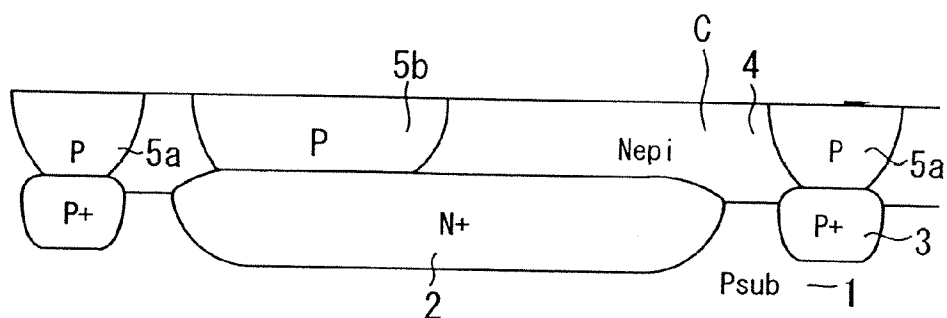


Fig. 7

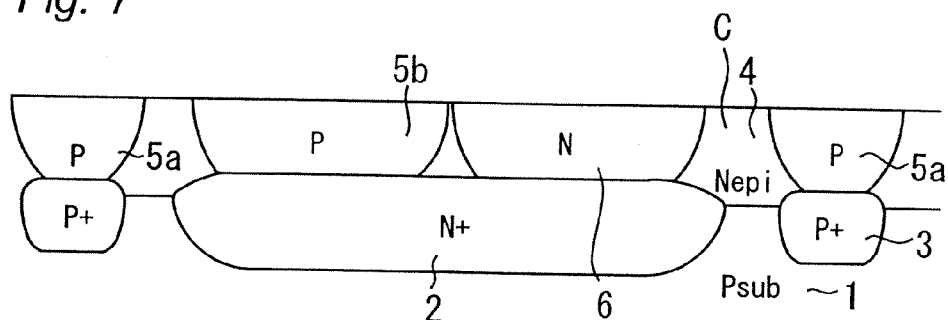


Fig. 8

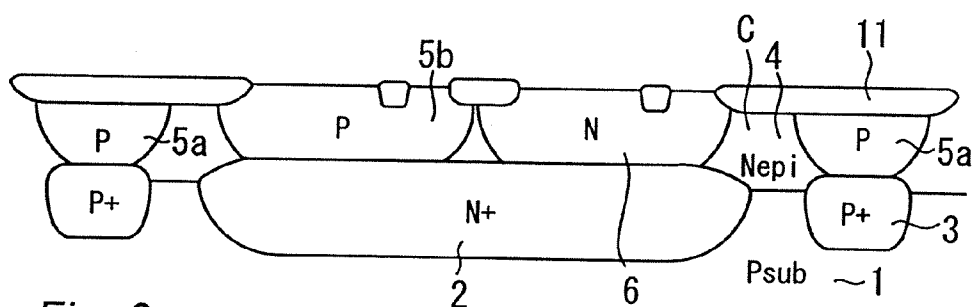


Fig. 9

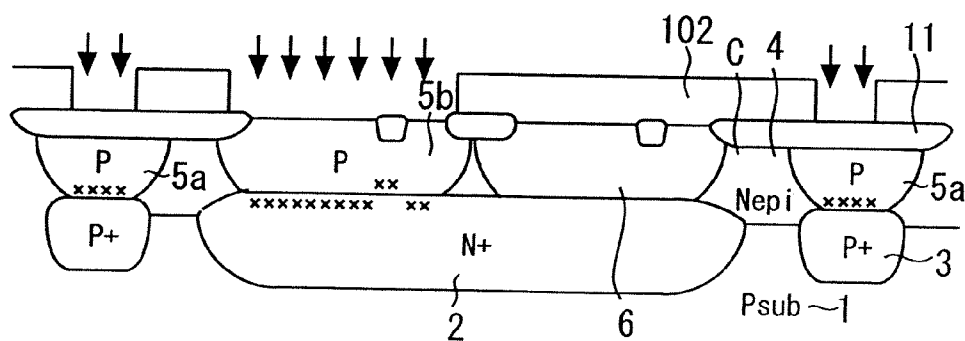


Fig. 11

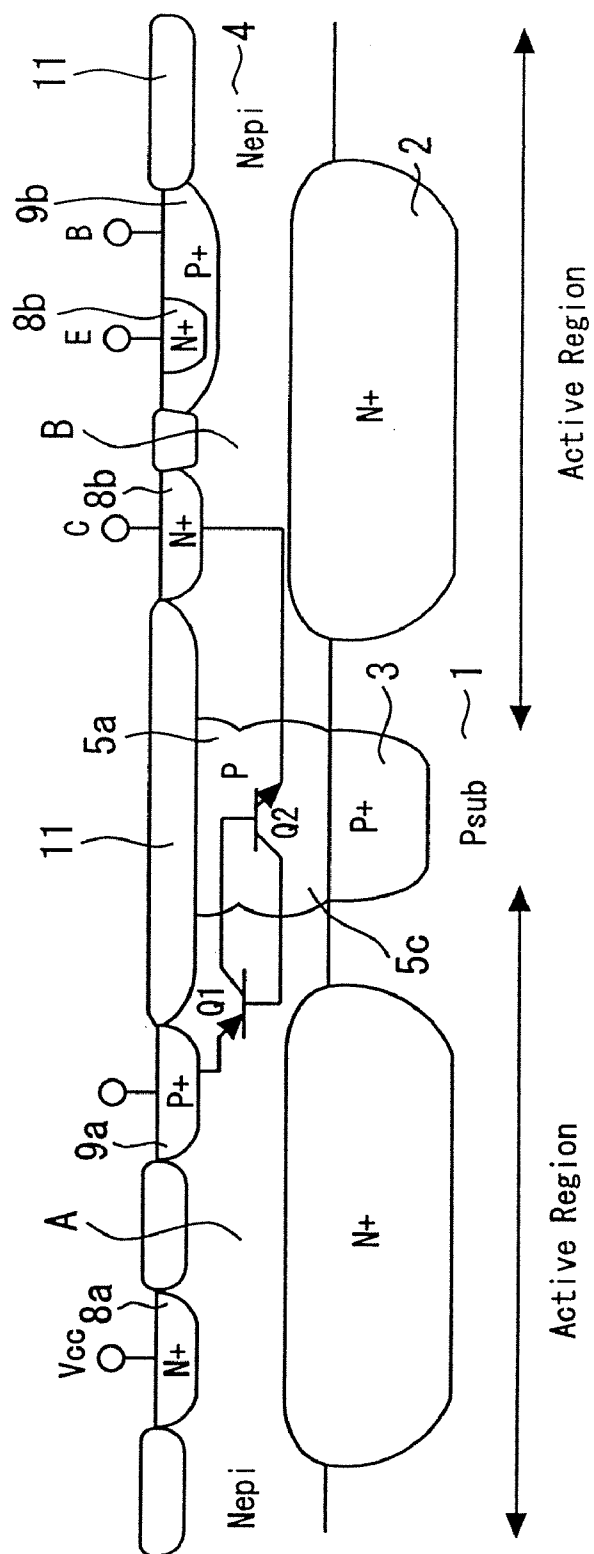


Fig. 12

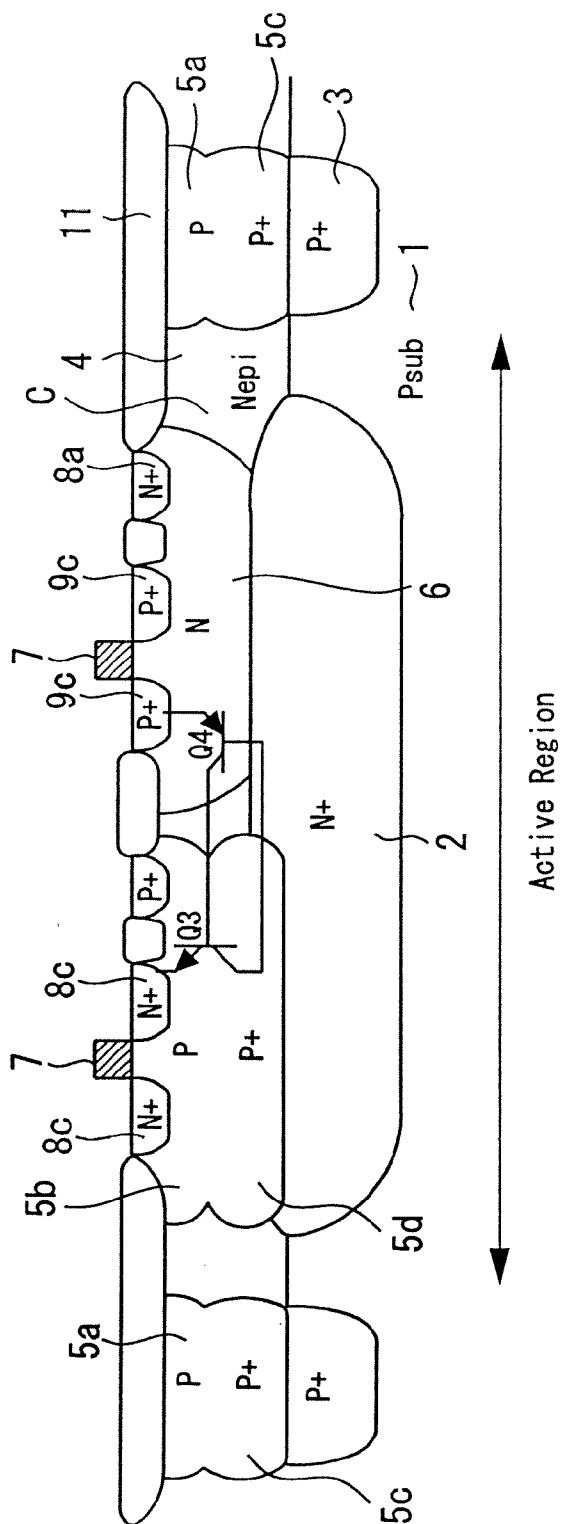


Fig. 13

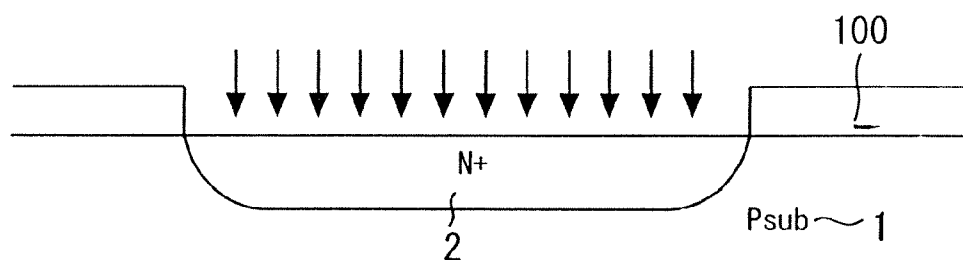


Fig. 14

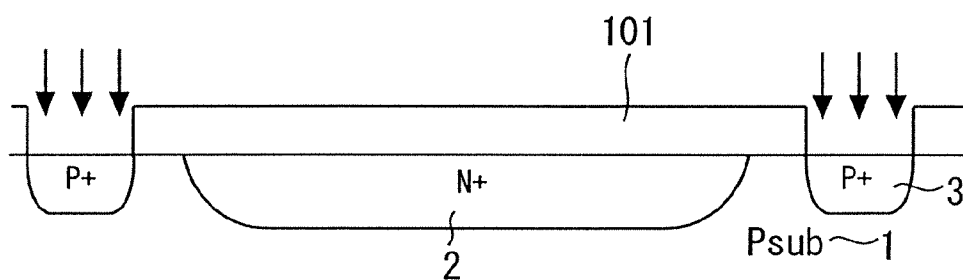


Fig. 15

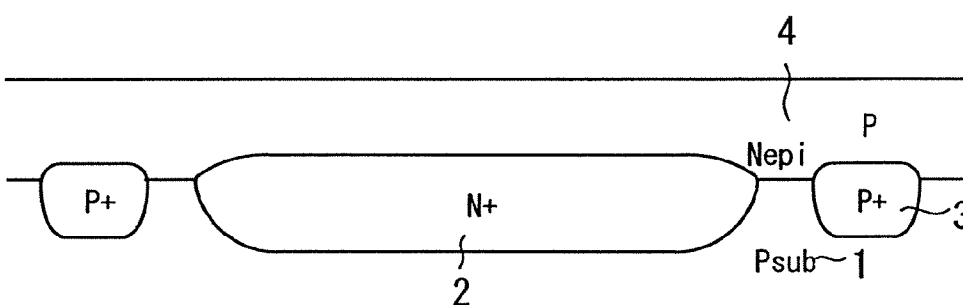


Fig. 16

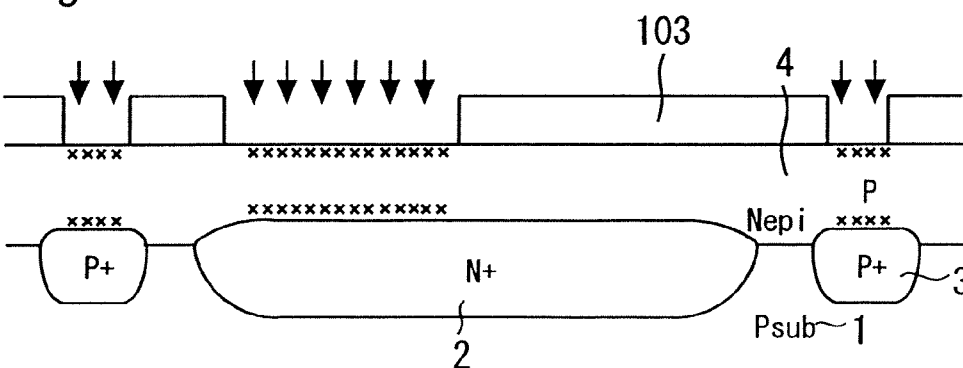


Fig. 17

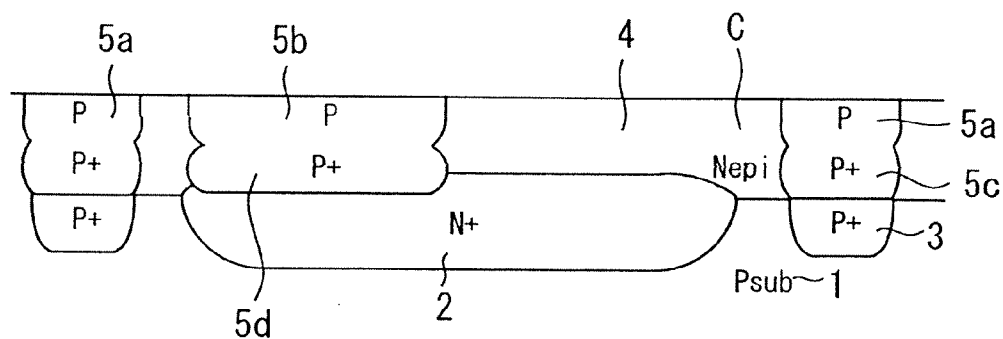


Fig. 18

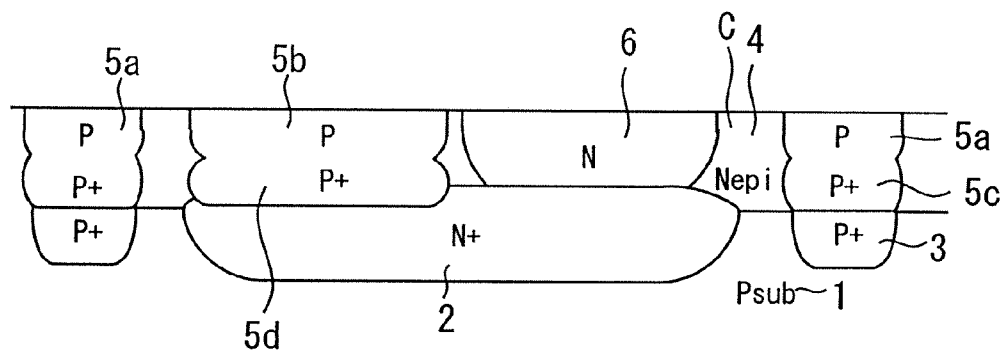
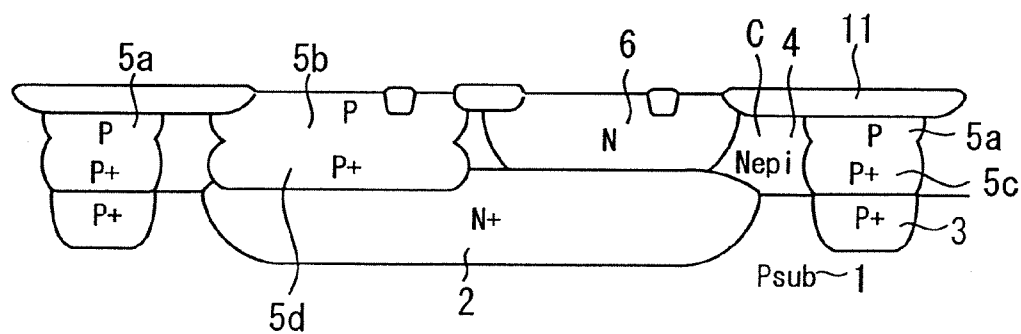


Fig. 19



Background Art

Fig. 24

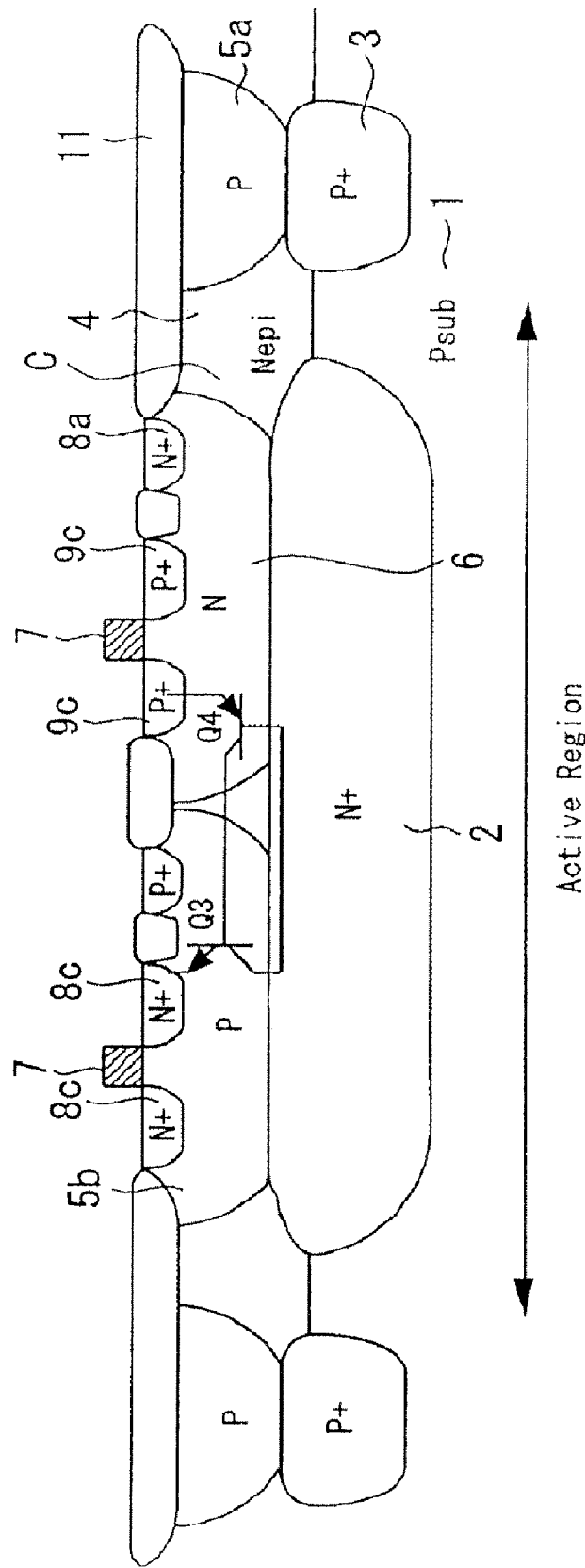


Fig. 25

Background Art

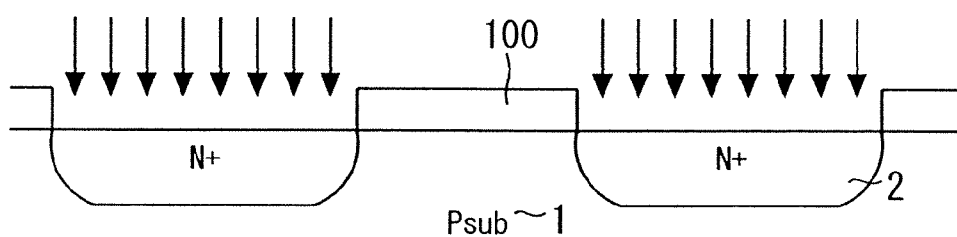


Fig. 26

Background Art

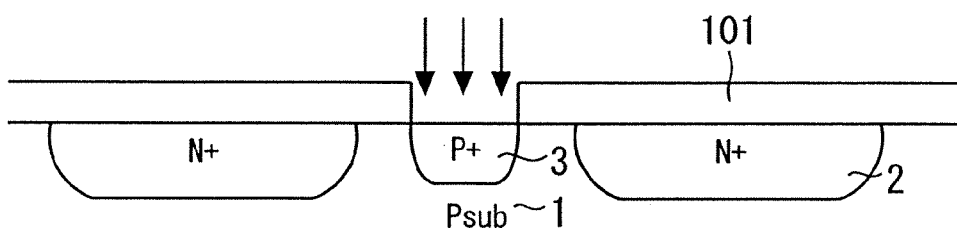


Fig. 27

Background Art

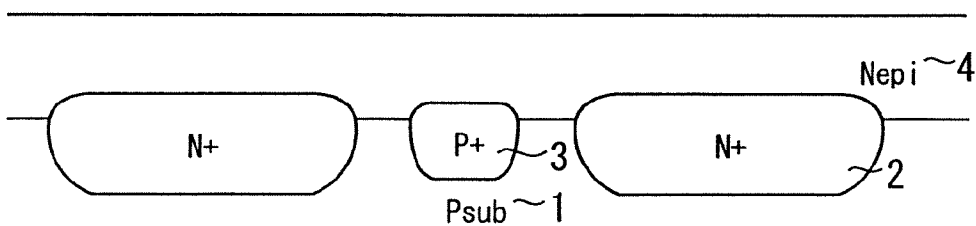


Fig. 28

Background Art

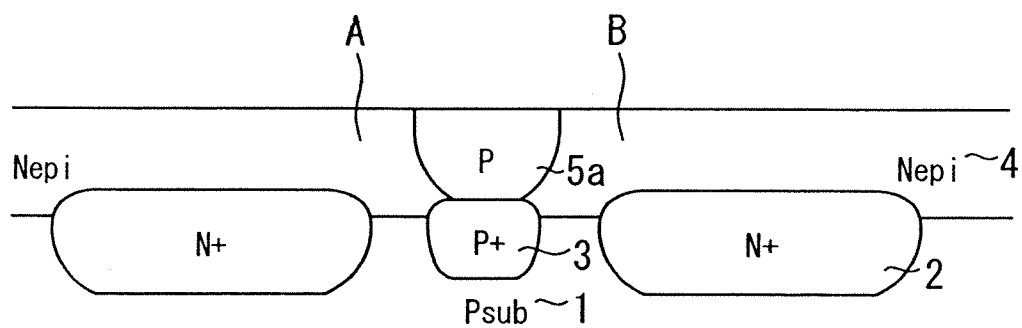
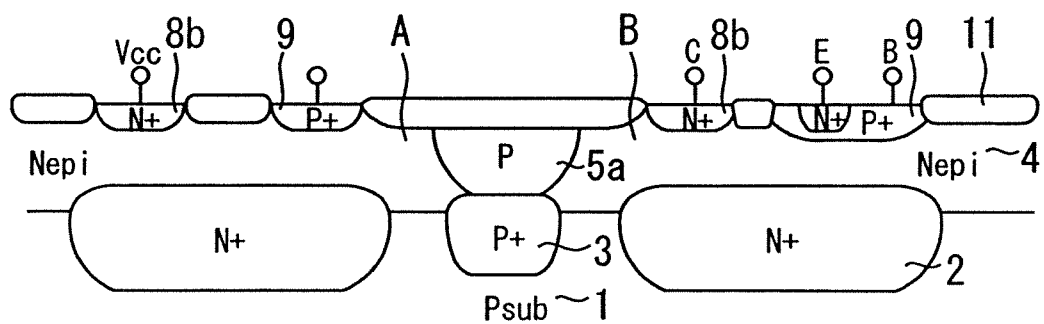


Fig. 29

Background Art



SEMICONDUCTOR DEVICE HAVING ELEMENT ISOLATION REGION

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a semiconductor device and a method for the manufacture thereof. More specifically, the present invention relates to the improvement of latch-up resistance of Bi-CMOS integrated circuits.

[0003] 2. Description of the Background Art

[0004] A Bi-CMOS integrated circuit, in which bipolar transistors and CMOS transistors are formed on a single substrate, has been manufactured.

[0005] In recent years, techniques for reducing the size of Bi-CMOS integrated circuits, in particular, techniques for reducing the size of bipolar transistors have been proposed. For example, in order to solve the problem of high occupying ratio of element isolation region in the area where bipolar transistors are formed, there have been proposed a large number of techniques for reducing the size of Bi-CMOS integrated circuits by element isolation using trench forming techniques. However, since trench forming techniques have problems of technical difficulties or manufacturing costs, separation techniques by junction forming have still been used.

[0006] A conventional semiconductor device and a method for the manufacture thereof will be described below.

[0007] First, a conventional semiconductor device (Bi-CMOS integrated circuit) will be described. FIGS. 23 and 24 are cross-sectional views for illustrating a conventional semiconductor device. Specifically, FIG. 23 shows a first island region in which a p-type diffusion resistor element is formed, a second island region in which an npn transistor is formed, and an element isolation region for isolating these island regions in a conventional Bi-CMOS integrated circuit. FIG. 24 shows a third island region in which a CMOS transistor is formed in a conventional Bi-CMOS integrated circuit.

[0008] In FIGS. 23 and 24, the reference numeral 1 represents a p-type silicon substrate, 2 represents an n-type buried diffusion layer, 3 represents a p-type first high-concentration isolation diffusion layer framed in the silicon substrate 1 and for isolating lower layer (deep layer) elements, and 4 represents an n-type epitaxial layer.

[0009] The reference numeral 5a represents a p-type low-concentration isolation diffusion layer formed in the epitaxial layer 4 and for isolating upper layer elements. The reference numeral 5b represents a p-type well region, which is formed in a third island region C of the epitaxial layer 4 simultaneously with the low-concentration isolation diffusion layer 5a, and in which an NMOS transistor is formed. The reference numeral 6 represents an n-type well region, which is formed in the third island region C, and in which a PMOS transistor is formed.

[0010] The reference numeral 7 represents gate electrodes of the MOS transistors, 8a represents an n-type diffusion region constituting an electrode forming region, 8b represents an n-type diffusion region constituting the bipolar transistor, 8c represents an n-type diffusion region constituting the source-drain region of the NMOS transistor; 9a represents a p-type diffusion region constituting a p-type diffused resistor element, 9b represents a p-type diffusion region constituting the bipolar transistor, 9c represents a p-type diffusion region constituting the source-drain region of the PMOS transistor, and 11 represents a field insulating film.

[0011] The reference symbol A represents an n-type first island region, B represents an n-type second island region, C represents a third island region, and Q1, Q2, Q3, and Q4 represent parasitic transistors.

[0012] As shown in FIGS. 23 and 24, the epitaxial layer 4 is separated into a plurality of island regions A, B, and C by the low-concentration isolation diffusion layer 5a and the first high-concentration isolation diffusion layer 3 formed in the element-isolation region. The n-type diffusion region 8b is fixed to the normal (ON) potential Vcc. The p-type silicon substrate 1 is fixed to GND (not shown).

[0013] Next, a method for manufacturing the above-described semiconductor device will be described below. FIGS. 25 to 29 are cross-sectional views for illustrating a conventional method for manufacturing a semiconductor device.

[0014] First, as FIG. 25 shows, a silicon oxide film 100 is formed on a p-type silicon substrate 1. Next, the silicon oxide film 100 is patterned. Then, an n-type impurity is implanted using the silicon oxide film 100 as a mask (hard mask), and the substrate 1 is subjected to annealing (heat treatment). Then the silicon oxide film 100 is removed. Thereby, an n-type buried diffusion layer 2 is formed.

[0015] Next, as shown in FIG. 26, a silicon oxide film 101 is formed on the silicon substrate 1. Then, the silicon oxide film 101 is patterned. Furthermore, a p-type impurity is implanted using the silicon oxide film 101 as a mask, and the substrate 1 is subjected to annealing. Then the silicon oxide film 101 is removed. Thereby, a first high-concentration isolation diffusion layer 3 is formed.

[0016] Next, as shown in FIG. 27, an n-type epitaxial layer 4 is formed on the silicon substrate 1, the buried diffusion layer 2, and the first high-concentration isolation diffusion layer 3 using the epitaxial method.

[0017] Next, as shown in FIG. 28, a low-concentration isolation diffusion layer 5a and a p-type well region 5b (see FIG. 24) are selectively and simultaneously formed using photolithography, the implantation of a p-type impurity, and annealing at a high temperature.

[0018] Then, in the same manner as the above-described p-type well region 5b, an n-type well region 6 (see FIG. 24) is selectively formed using photolithography, the implantation of a p-type impurity, and annealing at a high temperature.

[0019] Next, as shown in FIG. 29, a field insulating film 11 is formed on the prescribed area of the epitaxial layer 4. Then, gate electrodes 7 (see FIG. 24) are formed on the epitaxial layer 4, and n-type diffusion regions 8a, 8b, and 8c are selectively formed in the epitaxial layer 4. Next, p-type diffusion regions 9a, 9b, and 9c are selectively formed in the epitaxial layer 4. Thereby, a p-type diffused resistor element having the p-type diffusion regions 9a is formed in the first island region A, and a bipolar transistor having the n-type diffusion region 8b is formed in the second island region B.

[0020] Also at the same time, an NMOS transistor is formed in the p-type well region 5b, and a PMOS transistor is formed in the n-type well region 6 (see FIG. 24). Thus, a CMOS transistor is formed in the third island region C.

[0021] However, the recent downsizing of semiconductor devices has inevitably shortened the distance between junctions, and in the operation of circuits, the operation of parasitic transistors induced in junction separation has not been ignored.

[0022] In the above-described conventional semiconductor device, the potential of the p-type diffusion region 9a becomes momentarily higher than the potential of the first

island region A in the transient state between ON and OFF of V_{cc}, and current flows from the p-type diffusion region 9a to the first island region A. Thereby the parasitic pnp transistor Q1 that uses the p-type diffusion region 9a as the emitter, the first island region A as the base, and the low-concentration isolation diffusion layer 5a as the collector operates, and current flows into the low-concentration isolation diffusion layer 5a. Here, when the current flows into the low-concentration isolation diffusion layer 5a, the potential of the low-concentration isolation diffusion layer 5a elevates due to the resistance of the low-concentration isolation diffusion layer 5a itself. Due to the elevation of the potential, the parasitic npn transistor Q2 that uses the second island region B as the emitter, the low-concentration isolation diffusion layer 5a as the base, and the first island region A as the collector conducts.

[0023] As described above, when parasitic transistors Q1 and Q2 operate, a continuous excessive current flows between the p-type diffusion region 9 and the second island region B. Thus, the problem of a latch-up phenomenon arises.

[0024] Similarly in the third island region C shown in FIG. 24, there is a parasitic pnp transistor Q4 that uses the p-type diffusion region 9c, which is the source-drain region of the PMOS transistor, as the emitter, the n-type well region 6 as the base, and the p-type well region 5b as the collector; and there is a parasitic npn transistor Q3 that uses the buried diffusion layer 2 as the collector, the p-type well region 5b as the base, and the n-type well region 8c, which is the source-drain region of the NMOS transistor, as the emitter. In the transient state between ON and OFF of V_{cc}, current flows from the p-type diffusion region 9 to the n-type well region 6, and the parasitic pnp transistor Q4 operates. Thereby, current flows in the p-type well region 5b, and the potential of the p-type well region 5b elevates. Since the current gain of parasitic bipolar transistors Q3 and Q4 increases at this time, a continuous excessive current flows between (the source-drain region 9c of) the PMOS transistor and (the source-drain region 8c of) NMOS transistor. Thus, the problem of a latch-up phenomenon arises.

[0025] Although increase in the distance between the p-type diffusion region 9 and the low-concentration isolation diffusion layer 5a, or increase in the width of the low-concentration isolation diffusion layer 5a is effective to inhibit the operation of the above-described parasitic transistors, any of these goes against the current requirement of downsizing.

[0026] Also in a semiconductor device manufactured by the conventional manufacturing method, the concentration gradient of impurities is formed in the junction between the first high-concentration isolation diffusion layer 3 and the low-concentration isolation diffusion layer 5a, and in the junction between the buried diffusion layer 2 and the p-type well region 5b, depending on the thickness and impurity content of the epitaxial layer 4, and on the conditions of heat treatment (temperature, time). Lowering the temperature and reducing the time of heat-treatment to meet the current requirement of downsizing may result in insufficient diffusion of the impurities in the above-described junctions, and may cause a high-resistance layer to be formed in the above-described junctions.

[0027] Therefore, the conduction of the above-described parasitic pnp transistor Q1 causes the potential of the low-concentration isolation diffusion layer 5a to elevate easily. Similarly in the third island region C, the conduction of the parasitic pnp transistor Q4 causes the potential of the p-type

well region 5b to elevate easily. Thus, the problem of a high possibility of a latch-up phenomenon arises.

[0028] Alternatively, a method for lowering the resistance of the above-described junctions can be considered by increasing the impurity content for forming the low-concentration isolation diffusion layer 5a, or by increasing the time for heat treatment after the implantation of impurities. However, since the low-concentration isolation diffusion layer 5a is formed simultaneously with the p-type well region 5b of the NMOS transistor, the driving ability of the NMOS transistor takes precedence. Furthermore, since the low-concentration isolation diffusion layer 5a is formed considering the control of side diffusion to inhibit the isolating width. In other words, since increase in impurity content or heat-treatment time leads to the deterioration of the performance of the NMOS transistor, and to increase in the element area of the bipolar transistor, the problem of going against the improvement of performance by downsizing.

SUMMARY OF THE INVENTION

[0029] The present invention has been conceived to solve the previously-mentioned problems and a general object of the present invention is to provide a novel and semiconductor device and to provide a novel and useful method for manufacturing a semiconductor device.

[0030] A more specific object of the present invention is to provide a semiconductor device with improved latch-up resistance by inhibiting the operation of parasitic transistors without increasing the element area, and is to form an element separation of low resistance that does not depend on the thickness and impurity content of the epitaxial layer, and on the conditions of heat treatment.

[0031] The above object of the present invention is attained by a following method of manufacturing a semiconductor device and a following semiconductor device.

[0032] According to a first aspect of the present invention, the semiconductor device comprises: a substrate of a first conductivity type; a buried diffusion layer of a second conductivity type formed in the surface layer of the prescribed area of the substrate; a first high-concentration isolation diffusion layer of the first conductivity type formed in the substrate so as to surround the buried diffusion layer; an epitaxial layer of the second conductivity type formed on the substrate, the buried diffusion layer, and the first high-concentration isolation diffusion layer; a second high-concentration isolation diffusion layer of the first conductivity type formed in the epitaxial layer on the first high-concentration isolation diffusion layer; and a low-concentration isolation diffusion layer of the first conductivity type formed on the second high-concentration isolation diffusion layer, for isolating the epitaxial layer into a plurality of island regions.

[0033] According to a second aspect of the present invention, the semiconductor device comprises: a substrate of a first conductivity type; a buried diffusion layer of a second conductivity type formed in the surface layer of the prescribed area of said substrate; an epitaxial layer of the second conductivity type formed on the substrate and the buried diffusion layer; a high-concentration diffusion layer of the first conductivity type formed on the prescribed area of the buried diffusion layer; a first diffusion layer of the first conductivity type formed in the epitaxial layer on the high-concentration diffusion layer; and a second diffusion layer of the second conductivity type formed in the epitaxial layer on the buried diffusion layer adjacent to the first diffusion layer.

[0034] According to a third aspect of the present invention, the method for manufacturing a semiconductor device, comprises the steps of: forming a buried diffusion layer of a second conductivity type in the surface layer of the prescribed area of a substrate of a first conductivity type; forming a first high-concentration isolation diffusion layer of the first conductivity type in the substrate so as to surround the buried diffusion layer; forming an epitaxial layer of the second conductivity type on the substrate, the buried diffusion layer, and the first high-concentration isolation diffusion layer; forming a low-concentration isolation diffusion layer of the first conductivity type in the epitaxial layer on the first high-concentration isolation diffusion layer, the low-concentration isolation diffusion layer isolating the epitaxial layer into a plurality of island regions; and forming a second high-concentration isolation diffusion layer of the first conductivity type in the junction area between the first high-concentration isolation diffusion layer and the low-concentration isolation diffusion layer.

[0035] Other objects and further features of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0036] FIGS. 1 and 2 are cross-sectional views for describing a semiconductor device according to a first embodiment of the present invention;

[0037] FIGS. 3 to 10 are cross-sectional views for illustrating a method for manufacturing a semiconductor device according to a first embodiment of the present invention;

[0038] FIGS. 11 and 12 are cross-sectional views for illustrating a semiconductor device according to a second embodiment of the present invention;

[0039] FIGS. 13 to 20 are cross-sectional views for illustrating a method for manufacturing a semiconductor device according to a second embodiment;

[0040] FIGS. 21 and 22 are cross-sectional views for illustrating a semiconductor device according to a third embodiment of the present invention;

[0041] FIGS. 23 and 24 are cross-sectional views for illustrating a conventional semiconductor device;

[0042] FIGS. 25 to 29 are cross-sectional views for illustrating a conventional method for manufacturing a semiconductor device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0043] In the following, principles and embodiments of the present invention will be described with reference to the accompanying drawings. The members and steps that are common to some of the drawings are given the same reference numerals and redundant descriptions therefore may be omitted.

First Embodiment

[0044] First a semiconductor device will be described. FIGS. 1 and 2 are cross-sectional views for illustrating a semiconductor device according to a first embodiment of the present invention. Specifically, FIG. 1 shows, in a Bi-CMOS integrated circuit according to the first embodiment, a first island region A in which a p-type diffused resistor element is formed, a second island region B in which an npn transistor is

formed, and an element isolation region for isolating the first and second island regions. FIG. 2 shows, in a Bi-CMOS integrated circuit according to the first embodiment, a third island region C in which a CMOS transistor is formed.

[0045] In FIGS. 1 and 2, the reference numeral 1 represents a substrate, for example, a p-type silicon substrate; 2 represents an n-type buried diffusion layer, 3 represents a p-type first high-concentration isolation diffusion layer formed in the silicon substrate 1 and for isolating lower layer (deep layer) elements, and 4 represents an n-type epitaxial layer. In the present embodiment, “p-type” corresponds to “first conductivity”, and “n-type” corresponds to “second conductivity” (the same also applies to the second and third embodiments to be described later).

[0046] The reference numeral 5a represents a p-type low-concentration isolation diffusion layer formed in the epitaxial layer 4 on a second high-concentration isolation diffusion layer 5c (described below) and for isolating upper layer elements. The reference numeral 5b represents a p-type well region, which is formed in a third island region C of the epitaxial layer 4 on the high-concentration isolation diffusion layer 5d and for forming an NMOS transistor. The reference numeral 5c represents a p-type second high-concentration isolation diffusion layer formed in the epitaxial layer 4 on the first high-concentration diffusion layer 3; 5d represents a p-type high-concentration isolation diffusion layer formed on the upper layer of the prescribed area of the buried diffusion layer 2. The reference numeral 6 represents an n-type well region, which is formed in the third island region C adjacent to the p-type well region 5b, and in which a PMOS transistor is formed.

[0047] The reference numeral 7 represents gate electrodes of the MOS transistors, 8a represents an n-type diffusion region constituting an electrode forming region, 8b represents an n-type diffusion region constituting the bipolar transistor, 8c represents an n-type diffusion region constituting the source-drain region of the NMOS transistor, 9a represents a p-type diffusion region constituting a p-type diffused resistor element, 9b represents a p-type diffusion region constituting the bipolar transistor, 9c represents a p-type diffusion region constituting the source-drain region of the PMOS transistor, and 11 represents a field insulating film.

[0048] As shown in FIGS. 1 and 2, the epitaxial layer 4 is separated into a plurality of island regions A, B, and C by the low-concentration isolation diffusion layer 5a, the first high-concentration isolation diffusion layer 3, and the second high-concentration isolation diffusion layer 5c. The silicon substrate 1 is fixed to GND (not shown), and the n-type diffusion region 8a formed in the first island region A is fixed to the normal (ON) potential Vcc. The n-type diffusion region 8a formed in the n-type well region 6 is also fixed to the normal (ON) potential Vcc.

[0049] As described above, the above-described semiconductor device comprises a second p-type high-concentration isolation diffusion layer 5c in the junction between the low-concentration isolation diffusion layer 5a and the first high-concentration isolation diffusion layer 3. The second high-concentration isolation diffusion layer 5c has a higher impurity content and a lower resistance than the low-concentration isolation diffusion layer 5a. Therefore, even if a current flows in the low-concentration isolation diffusion layer 5a due to the operation of the parasitic pnp transistor Q1, the second high-concentration isolation diffusion layer 5c allows the current to flow in the silicon substrate 1 connected to GND

while inhibiting the elevation of the potential of the first high-concentration isolation diffusion layer 3 and the low-concentration isolation diffusion layer 5a. In other words, the elevation of potential at the above-described junction can be inhibited. The operation of the parasitic npn transistor Q2 is inhibited, thereby preventing latch-up. Therefore, continuous excessive current flowing between the p-type diffusion region 9 and the active island region B is inhibited, and the latch-up resistance can be improved.

[0050] The above-described semiconductor device also comprises a p-type high-concentration diffusion layer 5d in the junction between the n-type buried diffusion layer 2 and the p-type well region 5b. The high-concentration diffusion layer 5d has a higher impurity content and a lower resistance than the p-type well region 5b. Therefore, even if a current flows in the p-type well region 5b due to the operation of the parasitic npn transistor Q4, the high-concentration diffusion layer 5d allows the current to flow in the silicon substrate 1 connected to GND while inhibiting the elevation of the potential of the p-type well region 5b. That is, the elevation of potential at the above-described junction can be inhibited. The operation of the parasitic npn transistor Q4 is inhibited, thereby preventing latch-up between the first island region A and the second island region B. In other words, the current gain of the parasitic transistors Q3 and Q4 can be minimized, and the latch-up resistance can be improved.

[0051] Next, a method for manufacturing the above-described semiconductor device will be described below. FIGS. 3 to 10 are cross-sectional views for illustrating a method for manufacturing a semiconductor device according to a first embodiment.

[0052] First, as shown in FIG. 3, a silicon oxide film 100 is formed on a silicon substrate 1. Next, the silicon oxide film 100 is patterned using photolithography. Then, an n-type impurity is implanted into the silicon substrate 1 using the patterned silicon oxide film 100 as the mask. Furthermore, the silicon substrate 1 is annealed to diffuse the n-type impurity. Then, the silicon oxide film 100 is removed. Thereby, an buried diffusion layer 2 is formed in the upper layer of the prescribed area of the silicon substrate 1.

[0053] Next, as shown in FIG. 4, a silicon oxide film 101 is formed on the silicon substrate 1. Then, the silicon oxide film 101 is patterned using photolithography. Furthermore, a p-type impurity is implanted into the silicon substrate 1 using the patterned silicon oxide film 101 as the mask. Then, the silicon substrate 1 is annealed to diffuse the p-type impurity. Then, the silicon oxide film 101 is removed. Thereby, a first high-concentration isolation diffusion layer 3 is formed in the silicon substrate 1 so as to surround the buried diffusion layer 2.

[0054] Then, as shown in FIG. 5, an epitaxial layer 4 of a thickness of, for example, 1.0 to 4.0 μm is formed on the silicon substrate 1, the buried diffusion layer 2, and the first high-concentration isolation diffusion layer 3 using the epitaxial method.

[0055] Next, as shown in FIG. 6, a low-concentration isolation diffusion layer 5a is formed in the epitaxial layer 4 on the first high-concentration isolation diffusion layer 3 by photolithography, the implantation of a p-type impurity, and annealing. At the same time, a p-type well region 5b, in which an NMOS transistor is formed, is formed in the epitaxial layer 4 on the prescribed area of the buried diffusion layer 2.

[0056] Then, as shown in FIG. 7, an n-type well region 6, in which a PMOS transistor is formed, is formed in the epitaxial

layer 4 on the buried diffusion layer 2 adjacent to the p-type well region 5b by photolithography, the implantation of an n-type impurity, and annealing.

[0057] Next, as shown in FIG. 8, field-insulating films 11 for isolating elements are formed on the surface layer of a prescribed areas of the epitaxial layer 4 using the LOCOS method.

[0058] Next, as shown in FIG. 9, a resist pattern 102 of a thickness of, for example, 1.0 to 3.0 μm is formed on the epitaxial layer 4 using photolithography. At this time, the photo mask for forming the above-described low-concentration isolation diffusion layer 5a and p-type well region 5b is used as a photo mask for forming the resist pattern 102.

[0059] Then, a p-type impurity, such as boron, is implanted into the epitaxial layer 4 using the resist pattern 102 as the mask at an accelerating voltage of 350 to 500 keV, and a dose of 1.0 E12 to 3.0 E13/cm.

[0060] Furthermore, the silicon substrate 1 is annealed to diffuse the p-type impurity.

[0061] Thereby, a high-concentration diffusion layer 5d is formed in the junction between the p-type well region 5b and the buried diffusion layer 2, and a second high-concentration isolation diffusion layer 5c is formed in the junction between the low-concentration isolation diffusion layer 5a and the first high-concentration isolation diffusion layer 3 (see FIG. 10).

[0062] Next, as shown in FIG. 10, a gate electrode 7 is formed, and n-type diffusion regions 8a, 8b, and 8c are selectively formed. Next, p-type diffusion regions 9a, 9b, and 9c are selectively formed. Thereby, an NMOS transistor is formed in the p-type well region 5b, and a PMOS transistor is formed in the n-type well region 6. In other words, a CMOS transistor is formed in the third island region C.

[0063] At the same time, a p-type diffused resistor element having a p-type diffusion region 9a is also formed in the first island region A, and a bipolar transistor having an n-type diffusion region 8b is formed in the second island region B (see FIG. 1).

[0064] As described above, in the first embodiment, a p-type high-concentration diffusion layer 5c of a low resistance is formed in the junction between the low-concentration isolation diffusion layer 5a and the first high-concentration isolation diffusion layer 3. Thereby when a junction separation is formed by low-temperature heat treatment to meet downsizing, even if annealing is performed at a low temperature after implanting an impurity for forming the low-concentration isolation diffusion layer 5a, the elevation of the resistance of the junction seen in the conventional semiconductor device can be prevented, and an element separation of a low resistance can be formed. Therefore, an element separation of a low resistance, which does not depend on the thickness and the impurity content of the epitaxial layer 4 and on heat-treatment conditions, can be formed.

[0065] Also, since the element separation can be formed by a low-temperature heat treatment, the element separation width does not increase, and the element area does not enlarge. Therefore, the operation of parasitic transistors can be inhibited, and resistance to latch-up can be improved.

[0066] In the first embodiments, a high-concentration diffusion layer 5d of a low resistance is also formed in the junction between the p-type well region 5b and the buried diffusion layer 2 in the third island region C. Thereby, even when the p-type well region 5b is formed by low-temperature heat treatment to meet downsizing, the elevation of the resistance of the junction seen in the conventional semiconductor

device can be prevented. Therefore, the elevation of the potential of the junction between the p-type well region **5b** and the buried diffusion layer **2** can be inhibited. For this reason, even if a parasitic transistor **Q4** operates, the operation of the parasitic transistor **Q3** can be inhibited, and resistance to latch-up can be improved.

[0067] Even if the low-concentration isolation diffusion layer **5a** is not necessarily joined with the first high-concentration isolation diffusion layer **3** by low-temperature heat treatment to meet downsizing, the present invention is effective, and is an essential technique for forming fundamental element separation.

[0068] Here, as an example of the low-temperature heat treatment, the maximum temperature of the heat treatment is lowered to 850° C. or below from 950° C. employed in the prior art. However, the above-described low-temperature heat treatment is not only lowering the maximum temperature, but also lowering the temperature of the entire heat treatment. Therefore, the heat treatment at a lower temperature than the maximum temperature is included, and the integral sum with the heat-treatment time is decreased compared with the prior art.

[0069] Also in the first embodiment, the photo mask for forming the low-concentration isolation diffusion layer **5a** and the p-type well region **5b** can be used as the photo mask for forming the second high-concentration isolation diffusion layer **5c** and the high-concentration diffusion layer **5d**. Therefore, no additional photo masks are required, and the elevation of manufacturing costs can be inhibited.

[0070] Also, a method for manufacturing a semiconductor device, comprises the steps of: forming an buried diffusion layer of a second conductivity type in the surface layer of the prescribed area of a first conductivity type; forming a first high-concentration isolation diffusion layer of the first conductivity type in said substrate so as to surround the buried diffusion layer; forming an epitaxial layer of the second conductivity type on the substrate, the buried diffusion layer, and the first high-concentration isolation diffusion layer; forming a low-concentration isolation diffusion layer of the first conductivity type in the epitaxial layer on the first high-concentration isolation diffusion layer, and simultaneously forming a first diffusion layer of the first conductivity type in the epitaxial layer on the buried diffusion layer; forming a second diffusion layer of the second conductivity type in the epitaxial layer on the buried diffusion layer adjacent to the first diffusion layer; and forming a second high-concentration isolation diffusion layer of the first conductivity type in the junction area between the first high-concentration isolation diffusion layer and the low-concentration isolation diffusion layer, and simultaneously forming a high-concentration diffusion layer of the first conductivity type in the junction area between the buried diffusion layer and the first diffusion layer.

[0071] The method for manufacturing a semiconductor device, further comprises the steps of: forming, after formation of the high-concentration diffusion layer, a first circuit element having a diffusion region of the second conductivity type in the first diffusion layer; and forming a second circuit element having a diffusion region of the first conductivity type in the second diffusion layer.

Second Embodiment

[0072] FIGS. **11** and **12** are cross-sectional views for illustrating a semiconductor device according to a second embodiment of the present invention. Specifically, FIG. **11** shows, in

a Bi-CMOS integrated circuit according to the second embodiment, a first island region A in which a p-type diffused resistor element is formed, a second island region B in which an npn transistor is formed, and an element isolation region for isolating the first and second island regions. FIG. **12** shows, in a Bi-CMOS integrated circuit according to the second embodiment, a third island region C in which a CMOS transistor is formed.

[0073] In the above-described first embodiment, the low-concentration isolation diffusion layer **5a** and the p-type well region **5b**, and the second high-concentration isolation diffusion layer **5c** and the high-concentration diffusion layer **5d** are formed in separate processes. However, in the second embodiment, they are formed in the same process.

[0074] Therefore, the structure of the semiconductor device according to the second embodiment is substantially the same as the structure according to the first embodiment. Consequently, the same effect as the first embodiment can be obtained. The description of the semiconductor device according to the second embodiment will be omitted.

[0075] Next, a method for manufacturing a semiconductor device according to a second embodiment will be described below.

[0076] FIGS. **13** to **20** are cross-sectional views for illustrating a method for manufacturing a semiconductor device according to a second embodiment.

[0077] First, the process steps shown in FIGS. **13** to **15** are carried out. Since the process steps shown in FIGS. **13** to **15** are the same as the process steps shown in FIGS. **3** to **5**, no descriptions will be required.

[0078] Next, as shown in FIG. **16**, a resist pattern **103** of a thickness of, for example, 1.0 to 3.0 μm is formed on the epitaxial layer **4**.

[0079] Then, a p-type impurity, such as boron, is implanted into the upper layer of the epitaxial layer **4** using the resist pattern **103** as the mask at an accelerating voltage of 300 to 400 keV or below, and a dose of $1.0 \text{ E}12$ to $1.0 \text{ E}13/\text{cm}^2$ or below.

[0080] Furthermore, a p-type impurity, such as boron, is implanted into the lower layer of the epitaxial layer **4** using the resist pattern **103** as the mask at an accelerating voltage of 350 to 500 keV, and a dose of $1.0 \text{ E}12$ to $3.0 \text{ E}13/\text{cm}^2$. Thereby, the second impurity is implanted into the location 0.2 to 0.3 μm deeper than the location where the first impurity has been implanted.

[0081] The conditions of the above-described two impurity implantations are determined depending on the optimization of characteristics of the MOS transistor.

[0082] Next, the silicon substrate **1** is annealed to diffuse the p-type impurity that has been implanted in two implantation steps.

[0083] Thereby, as shown in FIG. **17**, a low-concentration isolation diffusion layer **5a** and a p-type well region **5b** are formed in the upper layer of the epitaxial layer **4**, and a second high-concentration isolation diffusion layer **5c** and a high-concentration diffusion layer **5d** are formed in the lower layer of the epitaxial layer **4**.

[0084] Next, as shown in FIG. **18**, an n-type well region **6** is formed in the epitaxial layer **4** on the n-type buried diffusion layer **2** adjacent to the p-type well region **5b** by photolithography, the implantation of an n-type impurity, and high-temperature annealing.

[0085] Then, as shown in FIG. 19, field-insulating films 11 for isolating elements are formed on the prescribed areas of the epitaxial layer 4 using the LOCOS method.

[0086] Next, as shown in FIG. 20, a gate electrode 7 is formed, and n-type diffusion regions 8a, 8b, and 8c are selectively formed. Next, p-type diffusion regions 9a, 9b, and 9c are selectively formed. Thereby, an NMOS transistor is formed in the p-type well region 5b, and a PMOS transistor is formed in the n-type well region 6. In other words, a CMOS transistor is formed in the third island region C.

[0087] At the same time, a p-type diffused resistor element having a p-type diffusion region 9a is also formed in the first island region A, and a bipolar transistor having an n-type diffusion region 8b is formed in the second island region B (see FIG. 11).

[0088] As described above, in the second embodiment, after the epitaxial layer 4 has been formed, an impurity is implanted twice using the same resist pattern 103 in two different heights, and the impurity implanted in different locations is simultaneously diffused by heat. Thereby, the low-concentration isolation diffusion layer 5a, the p-type well region 5b, the second high-concentration isolation diffusion layer 5c, and the high-concentration diffusion layer 5d can be formed simultaneously.

[0089] Therefore, one resist pattern forming step, and one annealing step can be decreased from the first embodiment. Thereby, the manufacturing costs can be reduced.

Third Embodiment

[0090] FIGS. 21 and 22 are cross-sectional views for illustrating a semiconductor device according to a third embodiment of the present invention. Specifically, FIG. 21 shows, in a Bi-CMOS integrated circuit according to the third embodiment, a first island region A in which a p-type diffused resistor element is formed, a second island region B in which an npn transistor is formed, and an element isolation region for isolating the first and second island regions. FIG. 22 shows, in a Bi-CMOS integrated circuit according to the third embodiment, a third island region C in which a CMOS transistor is formed.

[0091] In the third embodiment, the method for manufacturing the second high-concentration isolation diffusion layer 5c and the high-concentration diffusion layer 5d according to the first embodiment, and the method for manufacturing the second high-concentration isolation diffusion layer 5c and the high-concentration diffusion layer 5d according to the second embodiment are used in combination.

[0092] According to the third embodiment, the second high-concentration isolation diffusion layer 5c is formed between the low-concentration isolation diffusion layer 5a and the first high-concentration isolation diffusion layer 3. Also, the high-concentration diffusion layer 5d is formed between the p-type well region 5b and the buried diffusion layer 2. Therefore, the same effect as the first embodiment can be obtained.

[0093] This invention, when practiced illustratively in the manner described above, provides the following major effects:

[0094] According to the present invention, the operation of parasitic transistors can be inhibited without increasing the element area, and resistance to latch-up can be improved. Also, the element separation of a low resistance that does not depend on the thickness and impurity content of the epitaxial layer, and the conditions of heat treatment can be formed.

[0095] Further, the present invention is not limited to these embodiments, but variations and modifications may be made without departing from the scope of the present invention.

[0096] The entire disclosure of Japanese Patent Application No. 2001-197190 filed on Jun. 28, 2001 containing specification, claims, drawings and summary are incorporated herein by reference in its entirety.

1-20. (canceled)

21. A method for manufacturing a semiconductor device, comprising the steps of:

forming a buried diffusion layer of a second conductivity type in the surface layer of a prescribed area of a substrate of a first conductivity type;

forming a first high-concentration isolation diffusion layer of the first conductivity type in the substrate so as to surround the buried diffusion layer;

forming an epitaxial layer of the second conductivity type on the substrate, the buried diffusion layer, and the first high-concentration isolation diffusion layer;

forming a low-concentration isolation diffusion layer of the first conductivity type in the epitaxial layer on the first high-concentration isolation diffusion layer, the low-concentration isolation diffusion layer isolating the epitaxial layer into a plurality of island regions;

forming a second high-concentration isolation diffusion layer of the first conductivity type in the junction area between the first high-concentration isolation diffusion layer and the low-concentration isolation diffusion layer; and

forming a high-concentration diffusion layer of the first conductivity type in direct physical contact with an upper layer of said buried diffusion layer.

22. The method for manufacturing a semiconductor device according to claim 21, further comprising the steps of:

forming, after formation of the second high-concentration isolation diffusion layer, a first circuit element having a diffusion region of the first conductivity type in a first island region of the epitaxial layer; and

forming a second circuit element having a diffusion region of the second conductivity type in a second island region of the epitaxial layer.

23. The method for manufacturing a semiconductor device according to claim 21, further comprising the steps of:

forming, after formation of the epitaxial layer, a first diffusion layer of the first conductivity type in a third island region of the epitaxial layer on the buried diffusion layer;

forming a second diffusion layer of the second conductivity type in the third island region adjacent to the first diffusion layer; and

forming a high-concentration diffusion layer of the first conductivity type in the junction area between the buried diffusion layer and the first diffusion layer.

24. The method for manufacturing a semiconductor device according to claim 23, further comprising the steps of:

forming, after formation of the high-concentration diffusion layer, a third circuit element having a diffusion region of the second conductivity type in the first diffusion layer; and

forming a fourth circuit element having a diffusion region of the first conductivity type in the second diffusion layer.