METHOD TO REDUCE MIDRANGE RESONANCE DURING OPERATION OF A MULTI-PHASE STEP MOTOR

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ABSTRACT

The frequency of the pulse width modulator within a step motor control circuit is increased above a base frequency under defined conditions to enable more accurate construction of the phase current waveform for reducing mid-range resonance. The PWM frequency is stepped between frequencies by a fixed amount above the base frequency, to reduce the excitation of system harmonics and prevent step motor operational instability.
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BACKGROUND OF THE INVENTION

[0001] Step motor systems sometimes experience an operational instability known as “mid-frequency” or “mid-range” resonance.

[0002] This instability which often causes loss of motor torque and leads to motor stall, is caused by an interaction between the step motor drive, power supply and step motor load. When observing the step motor phase current, the shape and magnitude thereof are unstable.

[0003] Previous methods to prevent mid-range resonance include modifications to the power supply, connection of choke coils to the step motor and circuits designed to produce signals indicative of error. The drawbacks to these methods lie in the extra complexity involved. These methods also may need to be tuned to the specific system of step motor, step motor drive, power supply and load.


[0005] One purpose of the present invention is to reduce midrange resonance in a multiphase step motor for improved step motor performance.

SUMMARY OF THE INVENTION

[0006] The frequency of the pulse width modulator, “PWM”, within a step motor control circuit is increased above a base frequency under defined conditions to enable more accurate construction of the phase current waveform for reducing mid-range resonance. The PWM frequency is stepped between frequencies by a fixed amount above the base frequency, to reduce the excitation of system harmonics.

[0007] The PWM is synchronized to the incoming step input once per cycle to prevent the motor step clock from ‘beating’ against the PWM frequency. Improved current control leads to less phase current lag resulting in greater stability.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 is a schematic representation of the step motor control circuit in accordance with the invention;

[0009] FIG. 2 is a diagrammatic representation of the signal waveforms within the circuit of FIG. 1 showing the PWM OSC frequency change;

[0010] FIG. 3 is a diagrammatic representation of the signal waveforms showing the synchronization of the PWM oscillator within the control circuit of FIG. 1; and

[0011] FIG. 4 is a flow chart diagram depicting the logic for changing the PWM-OSC frequency in accordance with the teachings of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0012] The SET POINT GENERATOR 11, within the step motor control circuit 10 of FIG. 1, creates a FRONT SLOPE signal 24 (FIG. 2) on conductor 12 and a SIGN signal 29 (FIG. 3) on conductor 13 in response to the STEP signal input on conductor 14. The FRONT SLOPE signal on conductor 12 occurs when the SIGN signal is present on conductor 13 and the STEP signal on conductor 14 causes the step motor phase current to increase for one quarter of a cycle.

[0013] These signals connect to and influence the operation of a PWM OSCILLATOR, “PWM OSC” 15 that creates the PWM OSC signal 26 (FIG. 2) on conductor 16. These signals, along with others (not shown), are inputted to the BRIDGE CONTROL LOGIC, “LOGIC” 17. The PWM OSC signal on conductor 16 along with others (not shown) direct the operation of the LOGIC, 17. The LOGIC 17, through conductors 18-21 operate the BRIDGE 22 that controls the flow of step motor phase current through MOTOR PHASE COIL “COIL” 23. Although one COIL 23 is shown, the other COILS (not shown) are connected in a similar manner.

[0014] Referring now to FIGS. 1-3, the PWM OSC 15 creates the PWM OSC signal 26 at frequencies that range between a low or base frequency up to a specified maximum frequency. The PWM OSC 15 starts at the base frequency and increases the frequency, if required, to maintain a specified minimum number of edges 27 of the PWM OSC signal 26 during the FRONT SLOPE period until the specified maximum frequency is reached. Having a minimum number of edges enables more accurate construction of the phase current for reducing mid-range resonance.

[0015] The PWM-OSC 15 counts the number of PWM OSC edges 27 during the occasion of the FRONT SLOPE signal 24. If there are fewer than the minimum number of edges specified and the maximum frequency has not been reached, the PWM OSC frequency is increased by a fixed amount when the FRONT SLOPE signal ends as indicated at 25. If the number of edges 27 of the PWM OSC signal 26 is greater than or equal to the number specified during the occasion of the FRONT SLOPE signal 24, the PWM OSC frequency is decreased by a fixed amount when the FRONT SLOPE signal ends as indicated at 25.

[0016] When the FRONT SLOPE signal 24 is stable or changing slowly and the PWM frequency is above the base, the PWM frequency will repetitively step between two frequencies. This step between frequencies occurs when the frequency, in one cycle, is increased creating more PWM OSC edges 27. In the next cycle, (not shown) the number of edges 27 of the PWM OSC signal 26 will be greater than or equal to the minimum number of edges specified, therefore causing the frequency to decrease. The stepping between frequencies reduces the excitation of system harmonics, thereby reducing mid-range resonance.

[0017] In the case where the signal period of the FRONT SLOPE signal 24 is decreasing rapidly, the PWM OSC 15 will increase the frequency by a fixed amount each cycle until the maximum frequency is reached or the period of the FRONT SLOPE signal 24 becomes stable, whichever occurs first.
In the case where the period of the FRONT_SLOPE signal 24 is increasing rapidly and the frequency of the PWM_OSC signal 26 is above the base, the PWM_OSC 15 will increase the frequency by a fixed amount each cycle until the base frequency is reached or the period of the FRONT_SLOPE signal becomes stable, whichever occurs first.

If at the end of a cycle, the frequency of the PWM_OSC signal 26 is increased to the maximum, the frequency of the PWM_OSC signal will be decreased at the end of the next cycle, even though there may be fewer than the number of specified edges 27 of the PWM_OSC signal 26. On the following cycles, the PWM_OSC frequency is increased back to the maximum frequency. This continues the beneficial stepping between PWM_OSC frequencies even at the maximum frequency limit.

It is to be noted that the counting of PWM_OSC edges 27 could be performed during any portion of the motor operating cycle.

The phase current 28 transitions through zero, as indicated in phantom, twice per cycle, although only one cycle is shown in FIG. 3. At one of the transitions, indicated by the SIGN signal 29 on conductor 13, the PWM oscillator 15 resets its frequency generator as indicated 30 thereby synchronizing the PWM oscillator to the phase current. The phase current changes in response to a step input, such that the PWM oscillator is synchronized once per sine cycle to the incoming step input. This synchronization prevents the frequency of the step input from "beating" against the PWM oscillator frequency, reducing the potential of midrange resonance. It is to be noted the synchronization could occur at any point within the sine cycle.

A flow chart diagram 31 is depicted in FIG. 4 for the control of the PWM oscillator logic 15 of FIG. 1.

A count is made of the number of PWM-Osc edges during FRONT-SLOPE (32) and a determination is made as to whether the number of PWM-Osc edges is less than a predetermined minimum (33). If the number of PWM-Osc edges is less than a predetermined minimum, a determination is made as to whether the PWM-Osc frequency is at a predetermined maximum (34). If the PWM-Osc is not at a predetermined maximum, the PWM-Osc frequency is increased (36) and the number of PWM-Osc edges during FRONT-SLOPE is re-counted (32).

If the PWM-Osc frequency is at a predetermined maximum, the PWM-Osc frequency is decreased (37) and the number of PWM-Osc edges during FRONT-SLOPE is re-counted (32).

If the number of PWM-Osc edges is not less than a predetermined minimum, a determination is made as to whether the PWM-Osc frequency is above a base value (35) and if not, the number of PWM-Osc edges during FRONT-SLOPE is re-counted (32). If the PWM-Osc frequency is above a base value, the PWM-Osc frequency is decreased (37) and the number of PWM-Osc edges during FRONT-SLOPE is re-counted (32).

It has herein been shown that careful control of the PWM-Osc frequency to construct the phase current waveform in a step motor reduces mid-range resonance and helps to eliminate motor stall.

1. A method for reducing midrange resonance in a step motor system comprising:
   determining a present operating frequency of a pwm oscillator within a motor controller circuit;
   comparing said present operating frequency to a predetermined pwm oscillator base frequency; and
   increasing said present pwm oscillator operating frequency above said predetermined pwm oscillator base frequency when said present operating frequency is below said predetermined pwm oscillator base frequency and decreasing said present pwm oscillator operating frequency when said present pwm oscillator operating frequency is above base frequency to thereby improve creation of phase current within said motor controller circuit;
   2. (canceled)
   3. The method of claim 1 wherein said present pwm oscillator operating frequency defines a signal having a front slope.
   4. The method of claim 3 wherein said present operating frequency is determined upon occurrence of said front slope.
   5. The method of claim 3 wherein said pwm oscillator frequency is adjusted upon cessation of said front slope.
   6. A method for reducing midrange resonance in a step motor system comprising:
   synchronizing a pwm oscillator signal within a motor controller circuit to a step motor operating current waveform generated by said controller circuit to thereby prevent interaction between an input signal to said motor controller circuit and said pwm oscillator signal thereby reducing midrange step motor operating current resonance.
   7. A circuit for constructing a phase current waveform in a step motor comprising:
   a set point generator connecting with a pwm oscillator for providing front-slope and sign data to said pwm oscillator;
   a bridge control logic connecting with said pwm oscillator and an H bridge, said bridge control logic-arranged for providing a step motor operating current defining an operating current waveform, for connecting a pwm signal with said step motor bridge control logic, for determining a pwm frequency during a portion of said operating current waveform, for decreasing said pwm frequency when said pwm frequency exceeds a predetermined value, for increasing said pwm frequency when said frequency is less than said predetermined value, and
   synchronizing said pulse width modulator to said step motor operating current thereby controlling step motor phase current through said H bridge to a step motor coil to thereby reduce occurrence of system harmonics of said step motor phase current.
   8. (canceled)