

PACKAGE SUBSTRATES WITH MULTIPLE DICE

5

Priority Application

[0001] This application claims the benefit to U.S. Application Serial No. 13/537,445, filed June 29, 2012, which is incorporated herein by reference in its entirety.

10

Technical Field

[0002] The disclosure herein relates generally to semiconductor dice and die packages.

Background Art

[0003] Stacked die semiconductor configurations may use connector pathways that pass through one or more dice to transmit data or connect power to the dice. As the scale of semiconductor devices continually shrinks, efficient designs are desired to improve signals and power transmissions.

Brief Description of the Drawings

20 [0004] FIG. 1 is a block diagram of a die assembly according to an example embodiment.

[0005] FIG. 2 is a block diagram of a multiple die assembly according to an example embodiment.

[0006] FIG. 3 is a block diagram of another multiple die assembly
25 according to an example embodiment.

[0007] FIG. 4 is a block diagram of another multiple die assembly according to an example embodiment.

[0008] FIG. 5 is a block diagram of another multiple die assembly according to an example embodiment.

30 [0009] FIG. 6 is a flow diagram of a method according to an example embodiment.

[0010] FIG. 7 is a block diagram of an electronic device according to an example embodiment.

Description of the Embodiments

[0011] The following description and the drawings sufficiently illustrate specific embodiments to enable those skilled in the art to practice them. Other embodiments may incorporate structural, logical, electrical, process, or other changes. Portions and features of some embodiments may be included in, or substituted for, those of other embodiments. Embodiments set forth in the claims encompass all available equivalents of those claims.

FIG. 1 is an illustration of an embedded die assembly 100. The embedded die assembly 100 consists of a package substrate 102, a first die 104, a second die 106, and a number of connections 108. A connection 110 may be routed through the first die 104 to connect from the second die 106 to a bus 112 in the package substrate 102. Thus, a connection 110 passes through the first die 104. Having the connection 110 through the first die 104 may eliminate valuable space in the first die 104 and may complicate routing. Having the connection 110 through the first die 104 may cause unwanted electrical interference with data signals. A connection such as connection 110 may be a through silicon via (TSV). A TSV is limited in the amount of power that can be transmitted due to geometry available with known manufacturing methods. It is desired to have a device that can have multiple dice embedded in a package substrate wherein all of the dice can connect directly to the package substrate without using connections routed through a die in a package substrate.

[0013] FIG. 2 is an illustration of a device 200 according to an example embodiment. Device 200 may include first and second dice 204 and 206 and at least one first die to substrate connection 208, at least one second die to substrate connection 210, and at least one second die to first die connection 212 included in a package substrate. In certain examples, the first and second dice 204 and 206 are flip-chip dice.

[0014] In certain examples, package substrate 202 may be a bumpless build-up layer (BBUL) package substrate, with one or more of the dice 204, 206 embedded in the package substrate. A BBUL package substrate includes a die or dice embedded in a substrate, which has one or more build-up layers formed underneath the die. In certain examples, a standard micro via formation process such as laser drilling may form connections between build-up layers and die or

dice bond pads. The build-up layers may be formed using a standard high-density integration patterning technology.

[0015] Package substrate 202 may include the first and second dice 204 and 206 embedded therein. In certain examples, the second die 206 may be stacked on the first die 204 at a top surface of the first die. In certain examples, the second die 206 may be coupled to the first die 204 at a top surface of the first die. The first or second dice 204 or 206 may be analog, digital, or a combination thereof. An analog die is a die which uses predominately analog components, whereas a digital die is a die which uses predominately digital components. Some examples of types of dice are memory, radio, processor, arithmetic unit, or any combination thereof, among many others.

[0016] Package substrate 202 may include one or more buses. In the illustrated example of FIG. 2, package substrate 200 includes two buses 214a and 214b. Buses 214a or 214b may include a power bus or a data bus. In certain examples, bus 214a is a power bus and bus 214b is a ground bus. In certain examples, bus 214a is a power bus and bus 214b is a data bus.

[0017] The second die 206 may include a footprint that includes a dimension (e.g. a width) that is larger than a corresponding dimension of a footprint of the first die 204. In certain examples, the larger dimension of the second die 206 may allow for connections between the second die 206 and the package substrate outside the periphery of the first die 204, without requiring a TSV. Including a second die 206 that has a larger footprint than a first die 204, at least in one dimension, may allow cost savings by dividing circuitry between each die based upon how well they scale/reduce in size with fabrication processes. For example, the use of a lower cost technology for circuitry that does not scale well into the reduced size, higher cost technology fabrication processes may be used to make the second die 206, and newer generation, higher cost technology may reduce die size for circuitry that scales well to be included in the first die 204. Including a second die 206 that has a larger footprint than a first die 204, at least in one dimension, may allow for separation of functionality and manufacturing flexibility. In certain examples, a first embedded die 204 may be used in all manufactured assemblies, but a second die 206 may include

different types of functionality or logic, thus allowing for the creation of different systems.

5 [0018] In certain examples, the first die 204 is an analog die and the second die 206 is a digital die. In certain examples, the first die 204 is a digital die and the second die 206 is an analog die. Including an analog die stacked on a top surface of a digital die may help reduce noise and electromagnetic interference issues since the analog die may be closer to the external environment and may not be as susceptible to noise or electromagnetic interference as the digital die.

10 [0019] Device 200 may include at least one first die to substrate connection 208 located at an interface between the first die 204 and the package substrate 202. In certain examples, the at least one first die to substrate connection 208 may be included in a first level interconnect. In certain examples, the at least one first die to substrate connection 208 may be coupled
15 between the first die 204 and the package substrate bus 214a or 214b.

[0020] Device 200 may include at least one second die to substrate connection 210 located at an interface between the second die 206 and the package substrate 202. In certain examples, the at least one second die to substrate connection 210 may be outside the periphery of the first die 204. In
20 certain examples, the at least one second die to substrate connection 210 may be coupled between the second die 206 and the package substrate bus 214a or 214b. In certain examples, the at least one first die to substrate connection 208 and second die to substrate connection 210 may be connections that transfer power or data from the package substrate to the first or second die 204 or 206.

25 [0021] Device 200 may include at least one second die to first die connection 212 located at an interface between the first and second dice 204 and 206. In certain examples, the at least one second die to first die connection 212 may be included in a logic to logic interconnect. In certain examples, the at least one second die to first die connection 212 is a data connection that passes data
30 between the first and second dice 204 and 206.

[0022] In certain examples, it may be beneficial to pre-stack first and second dice 204 and 206 before embedding dice in the package substrate 202. In certain examples, pre-stacking the dice may be accomplished using a flip chip,

wire bonding, or other technique. In certain examples, pre-stacking dice before embedding them in the package substrate may be accomplished using a thermal compression bonding technique. In certain examples, pre-stacking first and second dice using thermal compression bonding may help preserve the dimensions of the dice. In certain examples, the dice may be pre-stacked and then a bumpless build-up layer (BBUL) package substrate may be built around the pre-stacked dice.

[0023] FIG. 3 is an illustration of first and second pre-stacked dice 300. In certain examples, the first and second dice may be pre-stacked (i.e. stacked before they are embedded in a package substrate) using thermal compression bonding. In certain examples the first die 204 may include at least one first die to substrate contact 308 operable to connect the first die 204 to a package substrate. In certain examples, the at least one first die to substrate contact 308 may be included in a first level interconnect. In certain examples, the second die 206 includes at least one second die to substrate contact 310 operable to connect directly to a package substrate. The at least one second die to substrate contact 310 may be outside the periphery of the first die 204. In certain examples, the pre-stacking may create at least one second die to first die connection 212 located at an interface between the first and second dice 204 and 206. In certain examples, the at least one second die to first die connection 212 may be included in a logic to logic interconnect. In certain examples, the second die includes at least one third die to second die contact 302 operable to connect the second die 206 to a third die that may be stacked above a top surface of the second die. In certain examples, the at least one third die to second die contact 302 may be included in a logic to memory interconnect. While FIG. 3 shows two dice stacked, it should be appreciated that any number of dice may be stacked and embedded in accord with the present disclosure.

[0024] FIG. 4 is an illustration of a device 400 according to an example embodiment. Device 400 may include a package substrate with multiple embedded dice 402 and a second package substrate (e.g. third die) 404 stacked above a top surface of the substrate with multiple embedded dice 402. The package substrate with multiple embedded dice may be substantially similar to device 200 of FIG. 2. The package substrate with multiple embedded dice 402

may include a second die coupled to a top surface of a first die such as is described with regard to FIG. 2 or 3. The package substrate with multiple embedded dice 402 may include at least one first die to substrate, second die to substrate, and second die to first die connection such as is described with regard to FIG. 2. The package substrate with multiple embedded dice 402 may include first and second busses operable to transmit power or data such as is described with regard to FIG. 2.

[0025] Device 400 may include a second package substrate 404 stacked above a top surface of the package substrate with multiple embedded dice 402. The second package substrate 404 may include a third die. In certain examples, the third die may be a memory. In certain examples, the memory may be a dual data rate (e.g. DDR2 or DDR3) memory. The stacking of the second package substrate 404 above the top surface of the package substrate with multiple embedded dice 402 may create a device 500 with a package on package architecture. In certain examples, the second package substrate 404 may be connected to the package substrate with multiple embedded dice 402 using a wire bonding, flip chip, or other connection technique.

[0026] Device 400 may include at least one second package substrate (e.g. third die) to first package substrate connection 408 located at an interface between the second package substrate 404 and the substrate of the package substrate with multiple embedded dice 402. The at least one second package substrate to first package substrate connection 408 may be connected between the second package substrate 404 and a bus included in the package substrate with multiple embedded dice. In certain examples, the at least one second package substrate to first package substrate connections may be outside the periphery of the second die of the package substrate with multiple embedded dice 402. In certain examples, the at least one second package substrate to first package substrate connection 408 transmits power to the second package substrate 404. In certain examples, the at least one second package substrate to first package substrate connection 408 transmits data to/from the second package substrate 404.

[0027] FIG. 5 is an illustration of a device 500 according to an example embodiment. Device 500 may include a package substrate with multiple

embedded dice 502 and a second package substrate (e.g. third die) 504 stacked above a top surface of the substrate with multiple embedded dice 502. The package substrate with multiple embedded dice may be substantially similar to device 200 of FIG. 2. The package substrate with multiple embedded dice 502 may include a second die coupled to a top surface of a first die such as is described with regard to FIG. 2 or 3. The package substrate with multiple embedded dice 502 may include at least one first die to substrate, second die to substrate, and second die to first die connection such as is described with regard to FIG. 2. The package substrate with multiple embedded dice 502 may include first and second busses operable to transmit power or data such as is described with regard to FIG. 2.

[0028] Device 500 may include a second package substrate 504 stacked above a top surface of the package substrate with multiple embedded dice 502. The second package substrate 504 may include a third die. In certain examples, the third die may be a memory. In certain examples, the memory may be a dual data rate (e.g. DDR2 or DDR3) memory. The stacking of the second package substrate 504 above the top surface of the package substrate with multiple embedded dice 502 may create a device 500 with a package on package architecture. In certain examples, the second package substrate 504 may be stacked above the package substrate with multiple embedded dice 502 using thermal compression bonding. In certain examples, the second package substrate 504 may be connected to the package substrate with multiple embedded dice 502 using a wire bonding, flip chip, or other connection technique. In certain examples, the second package substrate 504 may include a memory device that communicates to the second die using a logic to memory interface such as the logic to memory interface of FIG. 3. In certain examples the third die may communicate to the first die, the second die, or the package substrate, using a ball grid array (BGA) interface. In certain examples, the second package substrate 504 may be coupled to the package substrate with multiple embedded dice 502 at a top surface of the package substrate with multiple embedded dice.

[0029] Device 500 may include at least one second package substrate (e.g. third die) to second die connection 506 located at an interface between the

second die of the package substrate with multiple embedded dice 502 and the second package substrate 504. In certain examples, the device 500 may include a logic to memory interface including the at least one second package substrate to second die connection 506. The at least one second package substrate to second die connection 506 may transmit data between the second die and the second package substrate 504. In certain examples, the second package substrate to second die connection 506 may be configured as a package on package connection.

[0030] Device 500 may include at least one second package substrate (e.g. third die) to first package substrate connection 508 located at an interface between the second package substrate 504 and the substrate of the package substrate with multiple embedded dice 502. The at least one second package substrate to first package substrate connection 508 may be connected between the second package substrate 504 and a bus included in the package substrate with multiple embedded dice. In certain examples, the at least one second package substrate to first package substrate connections may be outside the periphery of the second die of the package substrate with multiple embedded dice 502. In certain examples, the at least one second package substrate to first package substrate connection 508 transmits power to the second package substrate 504. In certain examples, the at least one second package substrate to first package substrate connection 408 transmits data to/from the second package substrate 504.

[0031] FIG. 6 illustrates a flow diagram of a method 600 of making a device according to an example embodiment. Method 600 may include pre-stacking first and second dice 602. The first or second die may be primarily analog, primarily digital, or a combination thereof. The second die may include a width (e.g. a footprint with a dimension) greater than a corresponding width (e.g. a corresponding dimension of a footprint) of the first die. The second die may be stacked above a top surface of the first die. The pre-stacking may be accomplished using a flip chip process, a wire bonding process, thermal compression bonding process, or other bonding process. At 604 a substrate may be formed around the first and second dice. The substrate may be a bumpless build-up layer substrate. At least one second die to substrate connection may be

formed at an interface between the second die and the substrate at 606. The at least one second die to substrate connection may be formed outside the periphery of the first die. The at least one second die to substrate connection may be between the second die and a bus included in the substrate. The bus may carry power or data signals. At 608 at least one first die to substrate connection may be formed at an interface between the first die and the substrate. The at least one first die to substrate connection may be between the first die and a bus included in the substrate.

[0032] At 610 a third die (e.g. a second package substrate) may be stacked above the second die. The third die may be coupled to the second die at a top surface of the second die. The third die may be analog, digital, or a combination thereof. In certain examples, the third die is a memory die. The third die may include a width greater than the corresponding width of the second die. At 612 at least one third die to second die connection may be formed at an interface between the third die and the second die. The at least one third die to second die connection may transmit data between the second and third dice. At least one third die to substrate connection located at an interface between the third die and the substrate may be formed at 614. The at least one third die to substrate connection (e.g. a second substrate package to first substrate package connection) may be formed outside the periphery of the second die. The at least one third die to substrate connection may be between the third die and a bus included in the substrate. At 616 at least one first to second die connection may be formed between the first and second dice. The at least one second die to first die connection may transfer data between the first and second dice.

[0033] An example of an electronic device using a die as described in the present disclosure is included to show an example of a higher level device application for the present disclosure. FIG. 7 is a block diagram of an electronic device 700 incorporating at least one die in accordance with at least one embodiment of the invention. Electronic device 700 is merely one example of an electronic system in which embodiments of the present invention can be used. Examples of electronic devices 700 include, but are not limited to personal computers, tablet computers, mobile telephones, personal data assistants, MP3 or other digital music players, radios, etc. In this example, electronic device 700

comprises a data processing system that includes a system bus 702 to couple the various components of the system. System bus 702 provides communications links among the various components of the electronic device 700 and can be implemented as a single bus, as a combination of busses, or in any other suitable manner.

[0034] An electronic assembly 710 is coupled to system bus 702. The electronic assembly 710 can include any circuit or combination of circuits. In one embodiment, the electronic assembly 710 includes a processor 712 which can be of any type. As used herein, “processor” means any type of computational circuit, such as but not limited to a microprocessor, a microcontroller, a complex instruction set computing (CISC) microprocessor, a reduced instruction set computing (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, a graphics processor, a digital signal processor (DSP), multiple core processor, or any other type of processor or processing circuit.

[0035] Other types of circuits that can be included in electronic assembly 710 are a custom circuit, an application-specific integrated circuit (ASIC), or the like, such as, for example, one or more circuits (such as a communications circuit 714) for use in wireless devices like mobile telephones, pagers, personal data assistants, portable computers, two-way radios, and similar electronic systems. The IC can perform any other type of function.

[0036] The electronic device 700 can also include an external memory 720, which in turn can include one or more memory elements suitable to the particular application such as a main memory 722 in the form of random access memory (RAM), one or more hard drives 724, and/or one or more drives that handle removable media 726 such as compact disks (CD), digital video disk (DVD), and the like.

[0037] The electronic device 700 can also include a display device 716, one or more speakers 718, and a keyboard and/or controller 730, which can include a mouse, trackball, touch screen, voice-recognition device, or any other device that permits a system user to input information into and receive information from the electronic device 700.

Additional Notes and Examples

[0038] In Example 1, a device includes a first die within a package substrate, a second die, having a width greater than the first die, coupled to a top surface of the first die, at least one first die to substrate connection located at an interface between the first die and the package substrate, and at least one second die to substrate connection located at an interface between the second die and the package substrate outside the periphery of the first die.

[0039] In Example 2, the device of Example 1 includes a second die to first die connection located at an interface between the first die and the second die.

10 [0040] In Example 3, the second die to first die connection of any one or more of Examples 1-2 is a data connection.

[0041] In Example 4, the first die to substrate and second die to substrate connection of any one or more of Examples 1-3 are power connections.

[0042] In Example 5, the at least one first die to substrate connection of any one or more of Examples 1-4 include at least one data connection and at least one power connection.

[0043] In Example 6, the first die of any one or more of Examples 1-5 is a digital die.

20 [0044] In Example 7, the second die of any one or more of Examples 1-6 is an analog die.

[0045] In Example 8, the package substrate of any one or more of Examples 1-7 is configured as a bumpless build-up layer package substrate.

[0046] In Example 9, a device includes a first die embedded within a first package substrate, a second die, having a width greater than the first die, coupled to a top surface of the first die, a second die to first die connection located at an interface between the first die and the second die, a second die to substrate connection located at an interface between the second die and the package substrate outside the periphery of the first die, a second package substrate, having a width greater than the second die, coupled to a top surface of the second die, and a second package substrate to first package substrate connection located at an interface between the second package substrate and the first package substrate outside the periphery of the second die.

25
30

- [0047] In Example 10, the device of any one or more of Examples 1-9 includes a second package substrate to second die connection located at an interface between the second die and the second package substrate.
- [0048] In Example 11, the second package substrate of any one or more of Examples 1-10 is a memory die.
- [0049] In Example 12, the second package substrate to second die connection of any one or more of Examples 1-11 is a dual data rate connection.
- [0050] In Examples 13, the second die to first die connection of any or more of Examples 1-12 is a data connection.
- 10 [0051] In Example 14, the first and second dice of any one or more of Examples 1-13 are digital and analog, respectively.
- [0052] In Example 15, the first package substrate of any one or more of Examples 1-14 is configured as a bumpless build-up layer substrate.
- [0053] In Example 16, the second die of any or more of Examples 1-15 is embedded in the first package substrate.
- 15 [0054] In Example 17, a device includes a first die embedded within a first package substrate, a second die embedded within the first package substrate, wherein the second die includes a width greater than the first die and is coupled to a top surface of the first die, a first die to second die connection located at an interface between the first die and the second die, a second die to substrate connection located at an interface between the second die and the first package substrate outside the periphery of the first die, a second package substrate having a width greater than the second die coupled to a top surface of the second die, and a second package substrate to first package substrate connection located at an interface between the first package substrate and the second package substrate outside the periphery of the second die.
- 20 [0055] In Example 18, the first package substrate of any one or more of Examples 1-17 is configured as a bumpless build-up layer substrate.
- [0056] In Example 19, the second package substrate of any one or more of Examples 1-18 is configured as a bumpless build-up layer substrate.
- 25 [0057] In Example 20, the device of any one or more of Examples 1-19 includes a second package substrate to second die connection located at an interface between the second die and the second package substrate.

[0058] In Example 21, the second package substrate to second die connection of any one or more of Examples 1-20 is configured as a package on package connection.

5 [0059] In Example 22, the first die, the second die, and the second package substrate of any one or more of Examples 1-21 is a digital die, an analog die, and a memory package, respectively.

[0060] In Example 23, a method includes pre-stacking first and second dice, wherein the second die includes a width greater than the first die, and wherein the second die is stacked above the first die, forming a first package
10 substrate around the first and second dice, and forming a second die to substrate connection located at an interface between the second die and the first package substrate outside the periphery of the first die.

[0061] In Example 24, forming the first package substrate of any one or more of Examples 1-23 includes forming a bumpless build-up layer substrate.

15 [0062] In Example 25, pre-stacking of first and second dice of any one of Examples 1-24 includes thermal compression bonding.

[0063] In Example 26, the method of any one or more of Examples 1-25 includes forming a first die to substrate connection located at an interface between the first die and the first package substrate.

20 [0064] In Example 27, the method of any one or more of Examples 1-26 includes stacking a second package substrate on the second die, wherein the second package substrate includes a width greater than the second die, forming a second package substrate to second die connection located at an interface between the second die and the second package substrate, and forming a second
25 package substrate to first package substrate connection located at an interface between the first package substrate and the second package substrate outside the periphery of the second die.

[0065] The above detailed description includes references to the accompanying drawings, which form a part of the detailed description. The
30 drawings show, by way of illustration, specific embodiments in which the invention can be practiced. These embodiments are also referred to herein as “examples.” Such examples can include elements in addition to those shown or described. However, the present inventors also contemplate examples in which

only those elements shown or described are provided. Moreover, the present inventors also contemplate examples using any combination or permutation of those elements shown or described (or one or more aspects thereof), either with respect to a particular example (or one or more aspects thereof), or with respect
5 to other examples (or one or more aspects thereof) shown or described herein.

[0066] In this document, the terms “a” or “an” are used, as is common in patent documents, to include one or more than one, independent of any other instances or usages of “at least one” or “one or more.” In this document, the term “or” is used to refer to a nonexclusive or, such that “A or B” includes “A
10 but not B,” “B but not A,” and “A and B,” unless otherwise indicated. In this document, the terms “including” and “in which” are used as the plain-English equivalents of the respective terms “comprising” and “wherein.” Also, in the following claims, the terms “including” and “comprising” are open-ended, that is, a system, device, article, composition, formulation, or process that includes
15 elements in addition to those listed after such a term in a claim are still deemed to fall within the scope of that claim. Moreover, in the following claims, the terms “first,” “second,” and “third,” etc. are used merely as labels, and are not intended to impose numerical requirements on their objects.

[0067] The above description is intended to be illustrative, and not
20 restrictive. For example, the above-described examples (or one or more aspects thereof) may be used in combination with each other. Other embodiments can be used such as by one of ordinary skill in the art upon reviewing the above description. The Abstract is provided to comply with 37 C.F.R. §1.72(b), to allow the reader to quickly ascertain the nature of the technical disclosure. It is
25 submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. Also, in the above Detailed Description, various features may be grouped together to streamline the disclosure. This should not be interpreted as intending that an unclaimed disclosed feature is essential to any claim. Rather, inventive subject matter may lie in less than all features of a
30 particular disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment, and it is contemplated that such embodiments can be combined with each other in various combinations or permutations. The scope

of the invention should be determined with reference to the appended claims,
along with the full scope of equivalents to which such claims are entitled.

CLAIMS

What is claimed is:

- 5 1. A device, comprising:
 a first die within a package substrate;
 a second die, having a width greater than the first die, coupled to a top
 surface of the first die;
 at least one first die to substrate connection located at an interface
10 between the first die and the package substrate; and
 a second die to substrate connection located at an interface between the
 second die and the package substrate outside the periphery of the first die.
2. The device of claim 1, wherein the device comprises a first die to second
15 die connection located at an interface between the first die and the second die.
3. The device of claim 2, wherein the first die to second die connection is a
 data connection.
- 20 4. The device of claim 1, wherein the first die to substrate and second die to
 substrate connections are power connections.
5. The device of claim 1, wherein the at least one first die to substrate
 connection includes at least one data connection and at least one power
25 connection.
6. The device of claim 1, wherein the first die is digital.
7. The device of claim 1, wherein the second die is analog.
- 30 8. The device of claim 1, wherein the package substrate is configured as a
 bumpless build-up layer package substrate.

9. A device, comprising:
a first die embedded within a first package substrate;
a second die, having a width greater than the first die, coupled to a top surface of the first die;
- 5 a second die to first die connection located at an interface between the first die and the second die;
a second die to first package substrate connection located at an interface between the second die and the first package substrate outside the periphery of the first die;
- 10 a second package substrate, having a width greater than the second die, coupled to a top surface of the second die; and
a second package substrate to first substrate package connection located at an interface between the second package substrate and the first package substrate outside the periphery of the second die.
- 15
10. The device of claim 9, comprising a second package substrate to second die connection located at an interface between the second die and the second package substrate.
- 20 11. The device of claim 9, wherein the second package substrate includes a memory die.
12. The device of claim 11, wherein the second package substrate to second die connection is a dual data rate data connection.
- 25
13. The device of claim 9, wherein the first die to second die connection is a data connection.
14. The device of claim 9, wherein the first die is digital and the second die
- 30 is analog.
15. The device of claim 9, wherein the first package substrate is configured as a bumpless build-up layer package substrate.

16. The device of claim 9, wherein the second die is embedded in the first package substrate.
- 5 17. A device, comprising:
a first die embedded within a first package substrate;
a second die embedded within the first package substrate, wherein the second die includes a width greater than the first die and is coupled to a top surface of the first die;
- 10 a first to second die connection located at an interface between the first die and the second die;
a second die to first package substrate connection located at an interface between the second die and the first package substrate outside the periphery of the first die;
- 15 a second package substrate, having a width greater than the second die coupled to a top surface of the second die; and
a second package substrate to first package substrate connection located at an interface between the first package substrate and the second package substrate outside the periphery of the second die.
- 20 18. The device of claim 17, wherein the first package substrate is a bumpless build-up layer substrate.
19. The device of claim 18, wherein the second package substrate is a bumpless build-up layer substrate.
- 25 20. The device of claim 17, comprising a second package substrate to second die connection located at an interface between the second die and the second package substrate.
- 30 21. The device of claim 18, wherein the second package substrate to second die connection is configured as a package on package connection.

22. The device of claim 17, wherein the first die is digital, the second die is analog, and the second package is a memory package.
23. A method comprising:
- 5 pre-stacking first and second dice, wherein the second die includes a width greater than the first die, and wherein the second die is stacked above the first die;
- forming a first package substrate around the first and second dice; and
- forming a second die to substrate connection located at an interface
- 10 between the second die and the first package substrate outside the periphery of the first die.
24. The method of claim 23, wherein forming the first package substrate includes forming a bumpless build-up layer substrate.
- 15
25. The method of claim 23, wherein pre-stacking first and second dice includes thermal compression bonding.
26. The method of claim 23, comprising forming a first die to substrate
- 20 connection located at an interface between the first die and the first package substrate.
27. The method of claim 23, comprising:
- stacking a second package substrate above a top surface of the second
- 25 die, wherein the second package substrate includes a width greater than the second die;
- forming a second package substrate to second die connection located at an interface between the second package substrate and the second die; and
- forming a second package substrate to first package substrate connection
- 30 located at an interface between the second package substrate and the first package substrate outside the periphery of the second die.

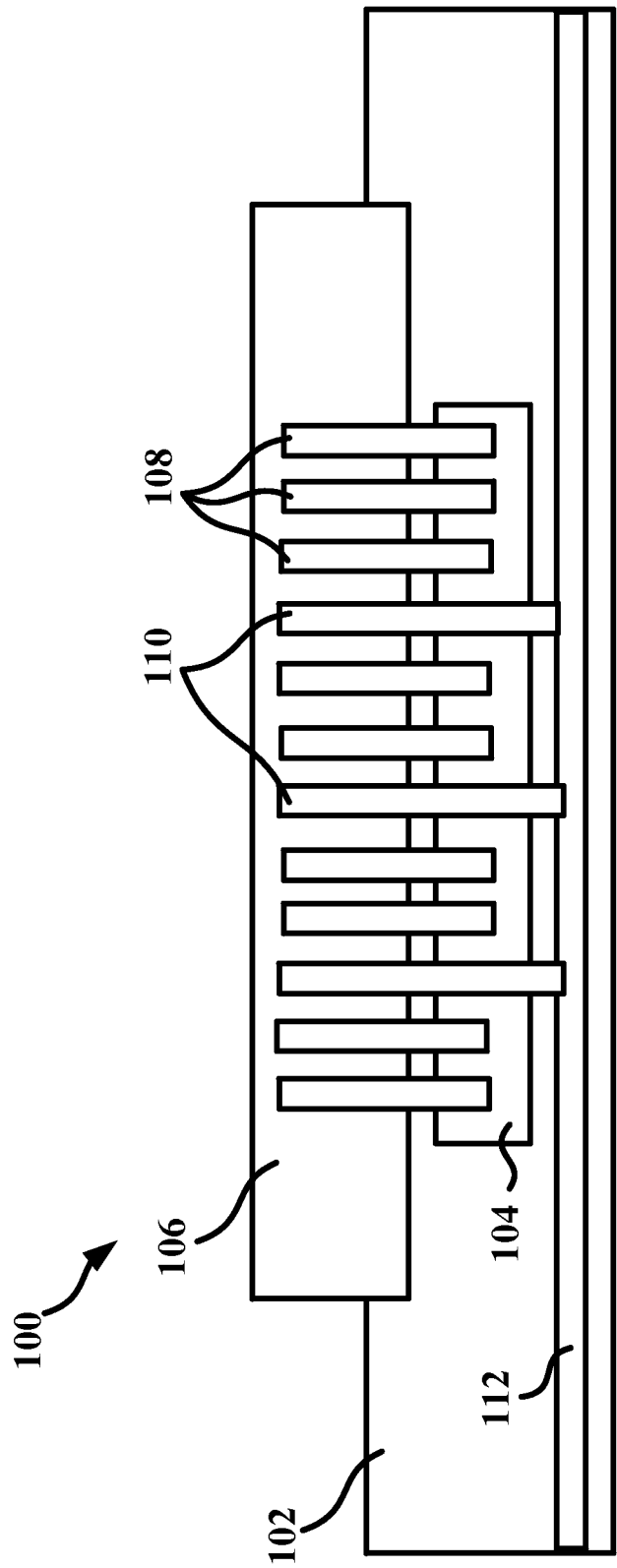


FIG. 1

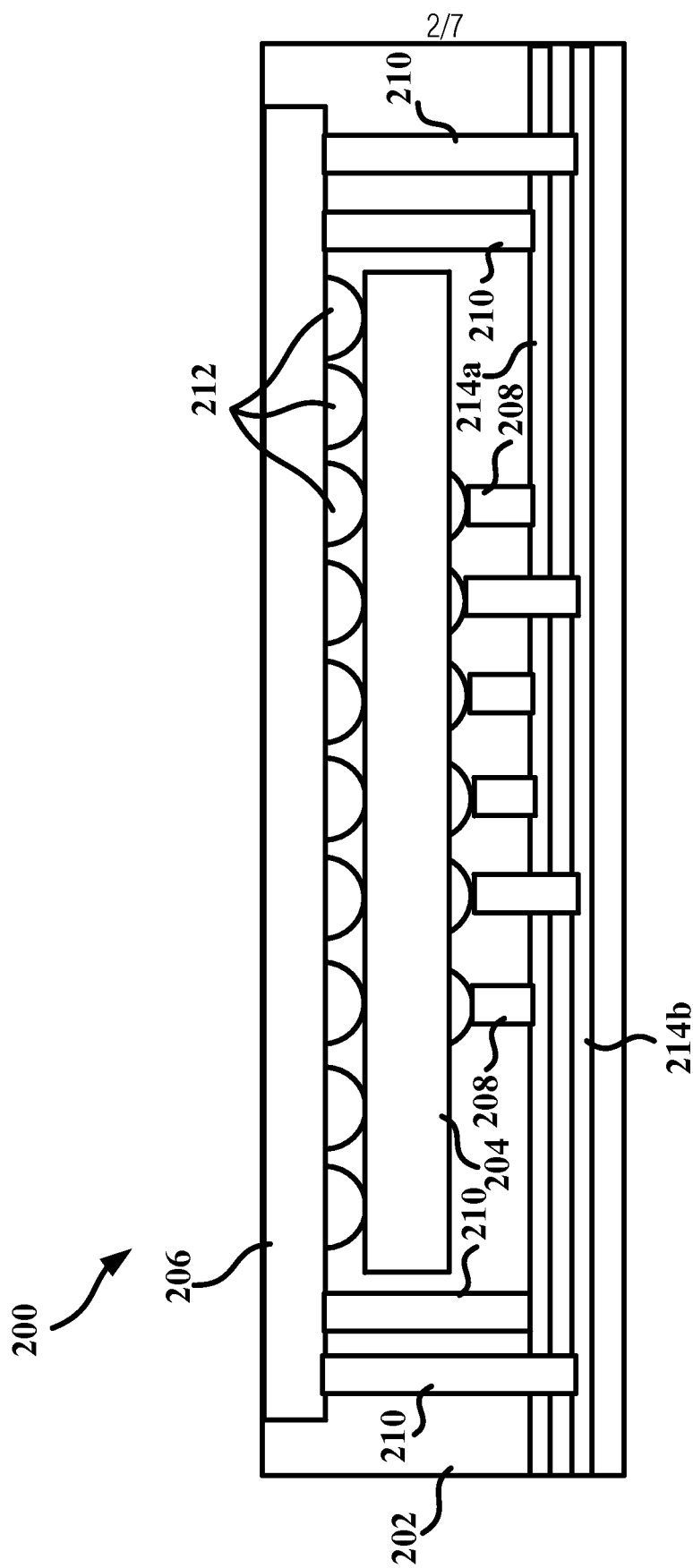
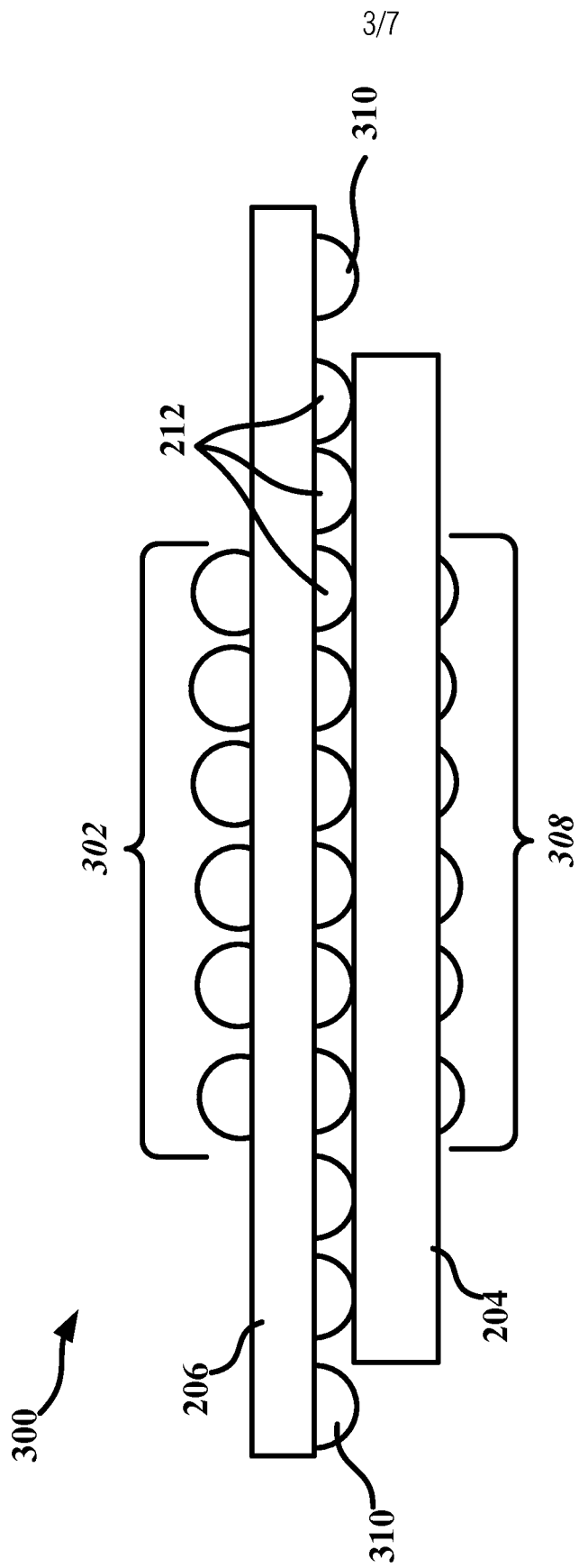


FIG. 2



3/7

FIG. 3

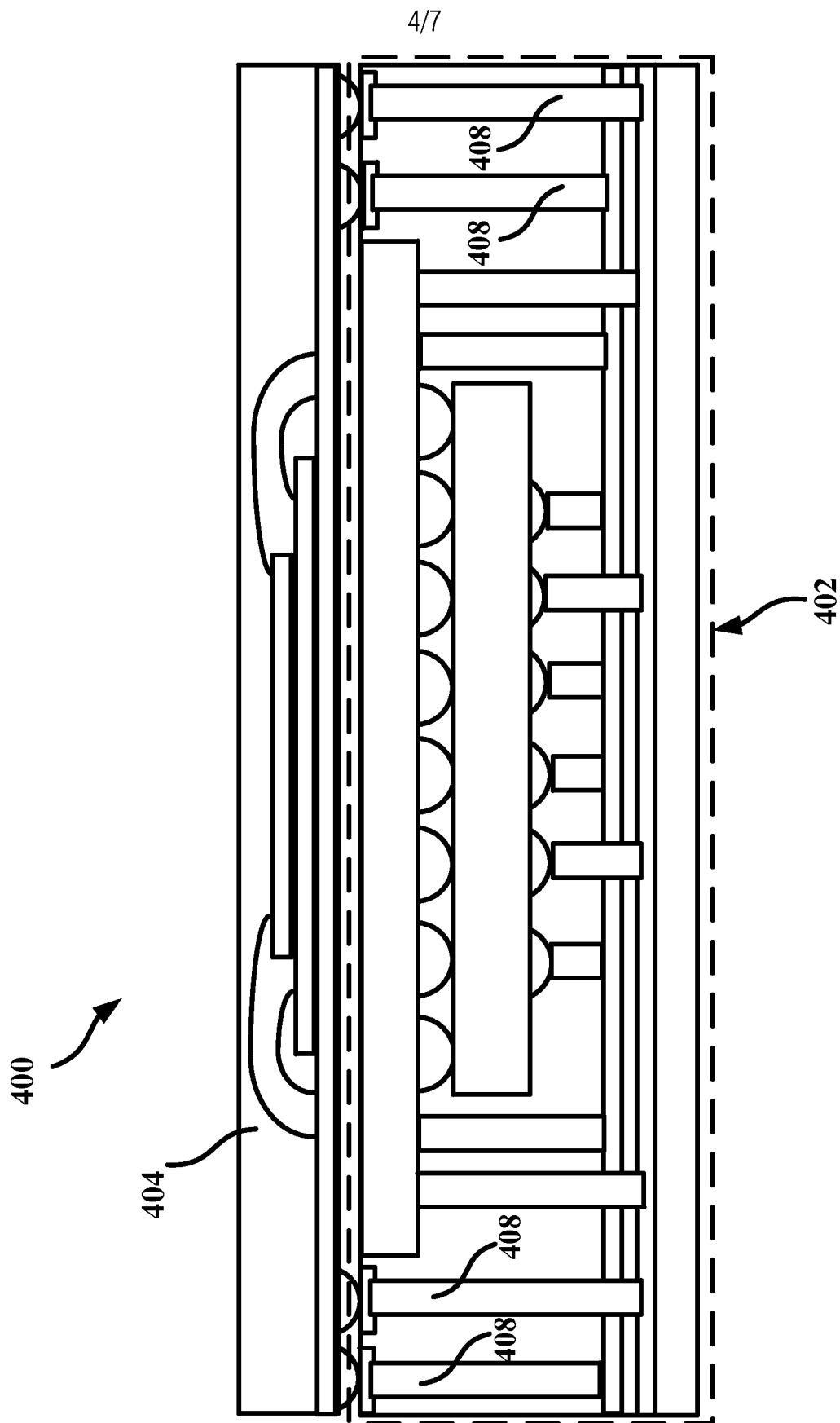


FIG. 4

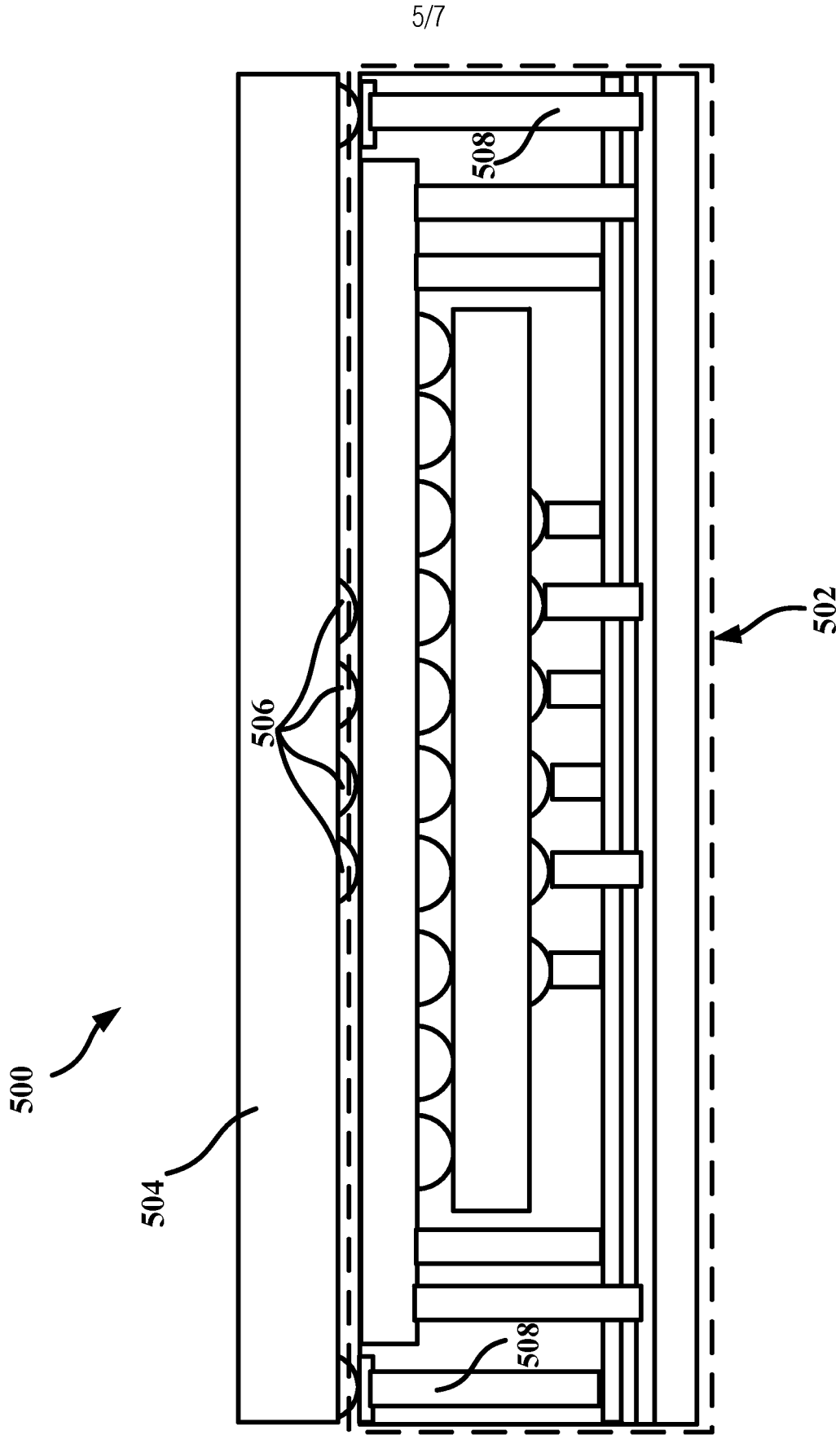


FIG. 5

6/7

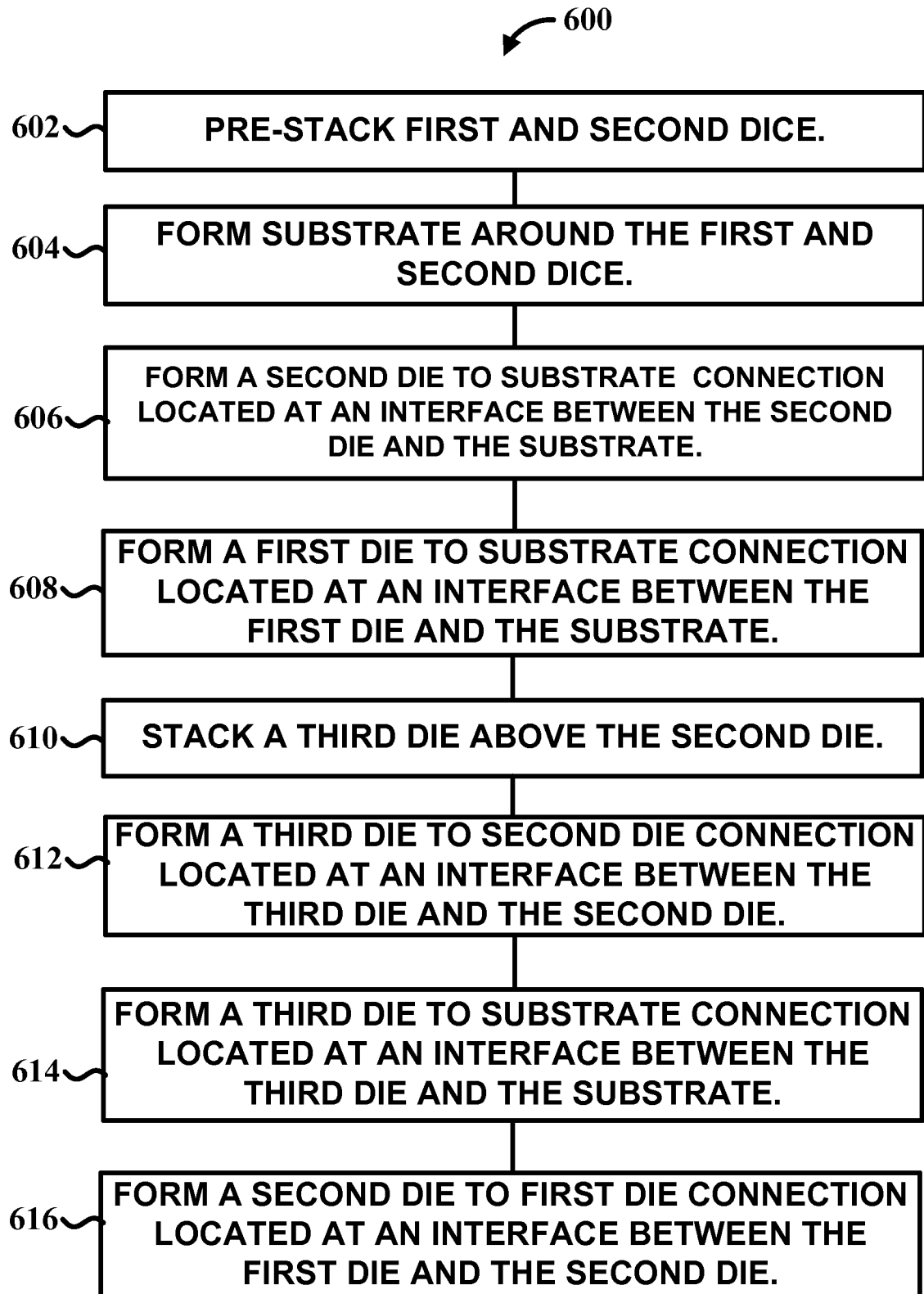


FIG. 6

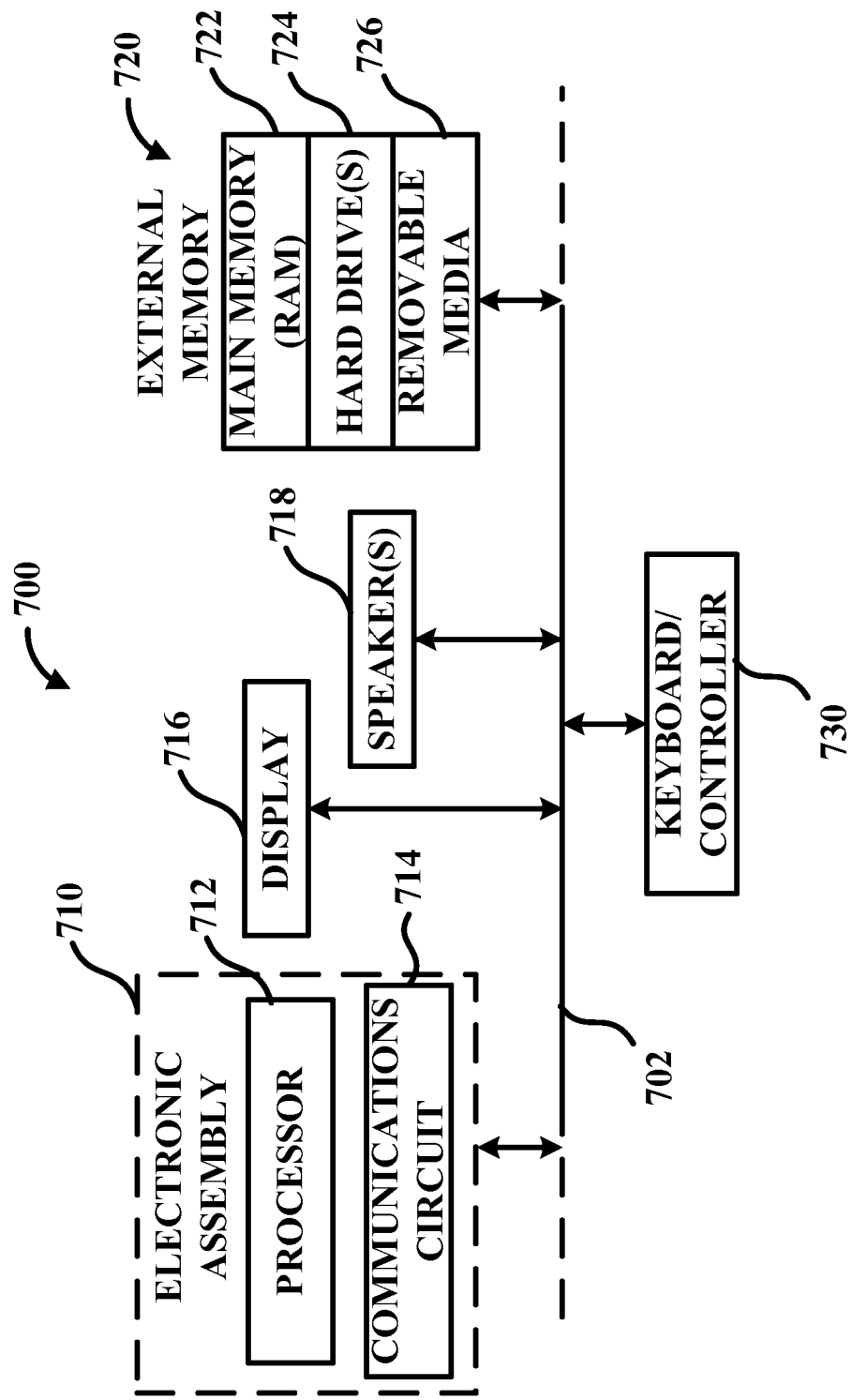


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/047647**A. CLASSIFICATION OF SUBJECT MATTER****H01L 23/12(2006.01)i, H01L 23/48(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
H01L 23/12; H01L 21/50; H01L 23/48; H01L 23/02; H01L 25/065; H01L 23/28; H01L 25/07Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: multiple dice, periphery ,BULL, package, width**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012-0091575 A1 (YI-SHAO LAI et al.) 19 April 2012 See paragraphs [0002]-[0028], claim 12 and figures 2-9.	1-7, 23, 25-26
A		8-22, 24, 27
A	US 2004-0212069 A1 (YU-WEN CHEN et al.) 28 October 2004 See abstract, paragraphs [0019]-[0023] and figures 2-4.	1-27
A	US 5977640 A (CLAUDE LOUIS BERTIN et al.) 02 November 1999 See abstract, column 4, lines 1-37 and figure 7.	1-27
A	KR 10-2011-0108136 A (SAMSUNG ELECTRONICS CO., LTD.) 05 October 2011 See abstract, paragraphs [0054]-[0063] and figures 2, 15-18.	1-27
A	JP 2008-016519 A (RENESAS TECHNOLOGY CORP.) 24 January 2008 See abstract, paragraphs [0023]-[0046] and figures 1-9.	1-27



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 September 2013 (27.09.2013)

Date of mailing of the international search report

27 September 2013 (27.09.2013)

Name and mailing address of the ISA/KR

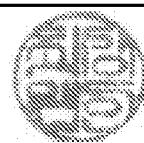
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan City,
302-701, Republic of Korea

Facsimile No. +82-42-472-7140

Authorized officer

CHOI Sang Won

Telephone No. +82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/047647

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0091575 A1	19/04/2012	None	
US 2004-0212069 A1	28/10/2004	TW 231977 A TW 231977 B TW 1231977 B	01/05/2005 01/05/2005 01/05/2005
US 5977640 A	02/11/1999	CN 1148804 C0 CN 1241032 A0 JP 2000-156461 A JP 3096459 B2 KR 10-0404373 B1 US 6294406 B1	05/05/2004 12/01/2000 06/06/2000 10/10/2000 05/11/2003 25/09/2001
KR 10-2011-0108136 A	05/10/2011	US 2011-0233755 A1 US 8436462 B2	29/09/2011 07/05/2013
JP 2008-016519 A	24/01/2008	CN 101101909 A CN 101101909 C0 JP 5259059 B2 KR 10-2008-0004356 A TW 200816435 A US 2008-0006947 A1 US 7847413 B2	09/01/2008 09/01/2008 07/08/2013 09/01/2008 01/04/2008 10/01/2008 07/12/2010