



(51) International Patent Classification:

H02M 1/08 (2006.01) *H02M 3/337* (2006.01)
H02M 3/325 (2006.01) *H05K 1/00* (2006.01)

(21) International Application Number:

PCT/US2016/043919

(22) International Filing Date:

25 July 2016 (25.07.2016)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

62/195,865 23 July 2015 (23.07.2015) US
15/073,964 18 March 2016 (18.03.2016) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:

US 15/073,964 (CON)
Filed on 18 March 2016 (18.03.2016)

(71) Applicant: TEXAS INSTRUMENTS INCORPORATED [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant (for JP only): TEXAS INSTRUMENTS JAPAN LIMITED [JP/JP]; 24-1, Nishi-shinjuku 6-chome, Shinjuku-ku, Tokyo, 160-8366 (JP).

(72) Inventor: SEEMAN, Michael, D.; 1314 Fremont St., San Jose, CA 95126 (US).

(74) Agents: DAVIS, Michael A., Jr. et al.; Texas Instruments Incorporated, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

[Continued on next page]

(54) Title: HYSTERETIC CONTROL FOR TRANSFORMER BASED POWER CONVERTERS

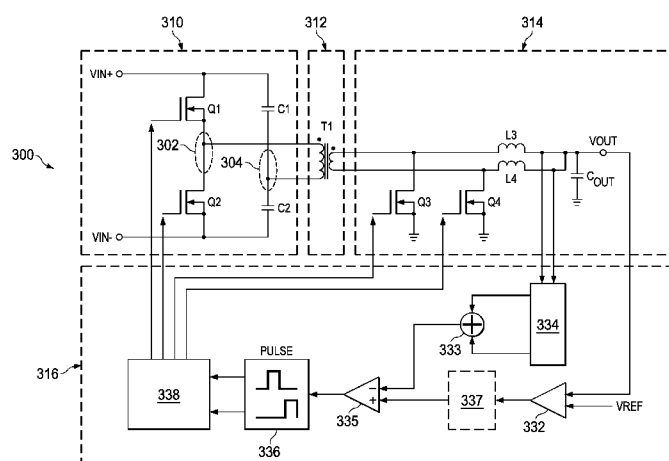


FIG. 3

(57) Abstract: In described examples, a converter arrangement (300) converts an input voltage (VTN) to an output voltage (VOUT). The arrangement (300) includes: a transformer (312); at least one primary side driver switch (Q1) coupled to supply current from an input voltage terminal (VIN+) to the primary side of the transformer (312); at least one inductor (L3) coupled between the secondary side of the transformer (312) and the output voltage terminal (VOUT); at least one secondary side switch (Q3) coupled between the inductor (L3) and a ground potential; and a hysteretic controller (316) coupled to supply a first on-time signal to the at least one primary side switch (Q1) and a second on-time signal to the at least one secondary side switch (Q3). The hysteretic controller is configured to sense the output voltage and has at least one current input coupled for sensing current flowing in the inductor (L3) and generating primary side driver switch on-time pulses to control the output voltage (VOUT).



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- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))* — *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*
- Published:**
- *with international search report (Art. 21(3))*

HYSTERETIC CONTROL FOR TRANSFORMER BASED POWER CONVERTERS

[0001] This relates generally to power conversion, and more particularly to a hysteretic control mechanism for power converters.

BACKGROUND

[0002] Complex electronic systems commonly contain a quantity of subassemblies on printed circuit boards (PCBs) or other modules that are typically located and interconnected in a rack connected via a back plane, or in an enclosure connected via wire. As the core voltage of integrated circuits has continued to fall to below 3.3 volts to 2 volts and even less, power distribution to these subassemblies conventionally uses an architecture where each subassembly creates its own specific power, using an intermediate system power as an input. This is commonly referred to as a distributed power architecture (DPA), and it a more efficient architecture for getting regulated power to the various subassemblies when compared to the centralized power architectures (CPA) of conventional assemblies.

[0003] In a conventional approach for a DPA, the primary system power supply will receive an input voltage and reduce it to one or more intermediate system voltages to be bussed to each of the PCBs subassemblies. Each PCB subassembly typically includes a DC-DC converter that will convert the system supply voltage to one (or more) well-regulated supply voltages for the subassembly PCB. With the addition of power regulation, the DC-DC converters are commonly referred to as switching regulators (SRs) or point-of-load (PoL) converters. Electrical isolation may be provided by either the primary system power supply or the individual switching regulators. The switching regulator is a commonly used and versatile element allowing the various subassembly components to receive the power supply voltages required without requiring adding a specific voltage and buss to the system power architecture. In the case of a high current, low voltage PoL converter, such as one rated at 30A, 1V, the PoL converter significantly reduces the line losses and cost that would otherwise be needed when distributing a 30A current by allowing the power to be distributed as a high voltage, low current, such as 3A, 12V to the various subassemblies. This approach allows the power to be distributed in a smaller sized, lower cost and lighter weight wire or buss than would otherwise be needed.

[0004] FIG. 1 depicts a distributed power architecture. DPA 100 has an input voltage 101, which feeds the system power supply 103. The system power supply is connected to a power buss 105, which (in this example) distributes voltages such as 24V and 12V within the system. The DC-DC switching regulators 107a, 107b ... 107n located on the subassembly PCBs (not shown) are connected to the system power buss 105 and may use one or both of the system power supplies. Illustrating the versatility of the onboard switching regulators, regulator 107a has outputs of 10V and 3.3Vs; regulator 107b has outputs of 1.0V and 1.5V; and regulator 107n has a single output of 8V. In consumer and commercial electronic applications, the input voltage 101 could be 100Vac to 240Vac. In telecom applications, such as where the system is run from standard battery voltages, the input voltage could be between 36Vdc to 72Vdc, with a 48V DC input being a typical input voltage in conventional systems.

[0005] Progress has been made in improving the efficiency of the two stage DPA including allowing the intermediate voltage to be a semi-unregulated voltage, running in an open loop manner. This approach is disclosed in U. S. Pat. No. 7,187,562, titled “Two Stage Power Conversion Circuit” to Stojcic et. al. (the “’562 Patent”). As explained in the ‘562 Patent, allowing a semi-unregulated intermediate voltage in the distributed power architecture reduces complexity of the first stage and does not have an adverse effect on the individual switching regulators on the subassemblies, because each subassembly is configured to regulate the output voltages. For the second stage switching regulators, the multi-phase buck converter has become a commonly used converter architecture for the point-of-load (PoL) converters where high currents and low voltages, such as 1V at 40A, are required.

[0006] FIG. 2 is a simple schematic of a two phase buck converter 200 with a synchronous rectifier, current doubler output stage, and a controller. FIG. 2 illustrates a buck converter 200, which is a rectifier that uses transistor switches Q1, Q2 as high side drivers and transistor switches Q3 and Q4 as synchronous rectifiers. The output voltage VOUT is coupled to the switching node through two inductors L3 and L4, which serve to double the output current while halving the voltage (when compared to a buck converter with a single inductor and single phase). The switching controller 201 receives output voltage information in a feedback loop, which is used to allow the controller 201 to synchronously switch Q1, Q2 and to use Q3, Q4 to act as synchronous rectifiers and to regulate the output voltage or current.

[0007] Regulation modes are divided into two basic types, which are: pulse width modulation

(PWM); and hysteretic. The PWM type includes voltage-mode control (VMC) and current-mode control (CMC) controllers. From various manufacturers, various off-the-shelf integrated circuits implement these conventional converter control modes. For example, VMC is implemented by the SG3524 “Pulse Width IC” commercially available from Microsemi. CMC is implemented by the UC3843 current mode PWM controller manufactured by Unitrode (now available from Texas Instruments Incorporated). Hysteretic control is implemented by the TPS53632 integrated circuit available from Texas Instruments Incorporated.

[0008] The selected control mode depends on the requirements of the power supply, but hysteretic control inherently provides lower quiescent current and excels in extreme down conversion applications common in modern PoL converters. Several types of hysteretic control exist. The original hysteretic approach provided a very simple circuit with fast regulation, but also with a widely varying switching frequency and a variable pulse width. Modified hysteretic control has since been developed to improve converter performance. In one example approach, a semi-fixed duration on-pulse is used to turn on a high side driver switch at each trigger event. By adjusting the duration of the pulse, and triggering the pulses based on the output voltage and on the input voltage, regulation can be achieved. Also, hysteretic control achieves good regulation when compared to other approaches and can provide a sufficiently fast voltage and current slew rate to supply processor cores, DSP cores and other low voltage, power hungry ICs. The use of power savings and sleep modes in integrated circuits, coupled with a very fast transition to a full voltage or high speed clocking rate, makes the need for a fast response from the PoL converter critical to system performance when supplying power to these high performance ICs. Hysteretic controllers can provide cycle by cycle control with fast response to changes in output or load conditions, making these controllers popular for providing power supplies to these advanced integrated circuits.

[0009] The two-stage approach to DPA is commonly used, because the conversion of a high input voltage (such as a DC input of 36-75 volts) to a sub 3.3V level with a single buck converter stage has a typical conversion efficiency in the low 80% range or even worse for some conventional systems. As indicated in FIG. 1, a typical efficiency of the first stage system power supply is 95% to 98%, and a typical efficiency of the second stage switching regulators in conventional converters is 90% to 95%, resulting in an overall system efficiency in the 85% to 93% range when using the two-stage approach. For a given power level, the efficiency of the

converter typically decreases with decreasing output voltage. For example, a 12V, 30W switching regulator converter providing 6V @ 5A would be more efficient than the same converter providing 1V @ 30A at the output. Accordingly, the typical overall efficiency of a conventional approach low-voltage output PoL converter is normally closer to the 85% end of the overall efficiency range.

SUMMARY

[0010] Arrangements that form aspects of example embodiments incorporate circuitry for power converters to provide highly efficient, single stage conversion from large input voltages to low voltage, high current outputs. In these arrangements, bridge topology converters such as half-bridge, and alternatively full-bridge and forward topologies, are used with a transformer situated between an input stage circuit and an output stage circuit, and hysteretic control is used to generate switching pulses for switches in the input and output stage circuits. Some arrangements use a hysteretic controller integrated circuit (previously used for controlling a buck converter), in a modified manner, to provide the hysteretic control. In some arrangements, a current doubler is used in the output stage to provide the output current. In other arrangements, a half-bridge input stage is used with the current doubler and the hysteretic controller. In still additional arrangements, a full-bridge input stage is used with the hysteretic controller.

[0011] In an example arrangement, an apparatus includes a power converter for converting an input voltage to an output voltage, the power converter further including: a transformer having a primary side and a secondary side coupled between an input voltage terminal and an output voltage terminal, respectively; at least one primary side driver switch coupled to supply current from the input voltage terminal to the primary side of the transformer; at least one inductor coupled between the secondary side of the transformer and the output voltage terminal; at least one secondary side switch coupled between a node coupled to the inductor and the secondary side of the transformer and a ground potential; and a hysteretic controller coupled to supply a first on-time signal to the at least one primary-side switch and a second on-time signal to the at least one secondary side switch, the hysteretic controller having a feedback input coupled to the output voltage and configured for sensing the voltage at the output and having at least one current input coupled to the at least one inductor and further configured for receiving a signal corresponding to the current flowing in the at least one inductor.

[0012] In a further example arrangement, in the apparatus above, the power converter further

includes a half-bridge converter with a current doubler output. In yet another further arrangement, in the apparatus above, the power converter further includes a second primary side driver switch coupled between the primary side of the transformer and a negative voltage input; a second inductor coupled between the secondary side of the transformer and the output voltage terminal; and a second secondary side switch coupled between a second node coupled to the second inductor and the secondary side of the transformer, and a terminal for receiving a ground potential. The hysteretic controller is further configured to supply on-time signals to the second primary side driver switch and the second secondary side switch.

[0013] In still another example arrangement, the power converter (of the apparatus described above) further includes two alternating cycles and the first and second inductors form a current doubler at the output voltage terminal. In still another example arrangement, in the apparatus described above, the power converter is a forward converter.

[0014] In still another example arrangement, in the apparatus described above, the hysteretic converter further includes a differential amplifier configured to compare the output voltage received to a reference voltage and to output an amplified error signal and/or a filtered droop signal, the hysteretic controller outputting the on-time signal to the at least one primary side driver switch responsive to the error signal or to the droop signal.

[0015] In a further example arrangement, in the above described apparatus, the hysteretic converter further includes a pulse sequencer to generate the at least one on-time signal to the at least one primary side driver switch responsive to a comparator that receives a voltage corresponding to average current in the at least one inductor, and the droop signal, and outputs an on-time pulse to the at least one primary side driver switch responsive to the comparison.

[0016] In still a further example arrangement, in the apparatus described above, the at least one primary side driver switch and the synchronous rectifier switch further include FET transistors. In still another alternative arrangement, in the apparatus described above the FET transistors further include silicon MOSFET devices. In yet another example arrangement, in the apparatus described above, the transistors further include GaN devices.

[0017] In still another example arrangement, in the apparatus described above, the power converter further includes a hard switched full-bridge converter with a current doubler output.

[0018] In still a further example arrangement, in the above described apparatus, the hard switched full-bridge converter further includes a second primary side driver switch coupled

between the primary side of the transformer and a negative input voltage terminal, a third driver switch coupled between the input voltage terminal and the primary side of the transformer, and a fourth driver switch coupled between the primary side of the transformer and the negative voltage input terminal.

[0019] In yet another alternative arrangement, in the above described apparatus, the first and second primary side driver switches and the third and the fourth driver switch further include GaN transistors.

[0020] In a further example arrangement, a half-bridge transformer-based power converter includes a transformer having a primary side with a first terminal and a second terminal and a secondary side with a third terminal and a fourth terminal; a first primary side driver transistor having a current conduction path coupled between a first voltage input terminal for receiving a positive input voltage and the first terminal of the primary side of the transformer, and having a gate terminal; a second primary side driver transistor having a current conduction path coupled between a second voltage terminal for receiving a negative input voltage and the first terminal of the primary side of the transformer, and having a gate terminal; a first capacitor coupled between the first voltage input terminal for receiving the positive input voltage and the first terminal of the primary side of the transformer; a first secondary side driver transistor having a current conduction path between the first terminal of the secondary side of the transformer and a terminal for a ground potential, and having a gate input; a second secondary side driver transistor having a current conduction path coupled between the second terminal of the secondary side of the transformer and the terminal for a ground potential, and having a gate input; a first inductor coupled between the first terminal of the secondary side of the transformer and an output terminal for an output voltage; a second inductor coupled between the second terminal of the secondary side of the transformer and the output terminal for an output voltage; and a hysteretic controller coupled to the output voltage and having inputs for receiving sensed current signals for the first and second inductors, and having outputs for driving the gate signals for each of the first and second primary side driver transistors, and for driving each of the first and second secondary side transistors, configured to output on-time pulses on the gate signals of the first and second primary side driver transistors at a nearly constant switching frequency to create an output voltage at the output voltage terminal.

[0021] In a further arrangement, the hysteretic controller (of the half-bridge power converter

described above) further includes a first comparator for comparing the output voltage to a reference voltage and for outputting an error voltage. The error voltage can further be filtered through a dynamic filter to form the droop voltage, which will adjust the dynamic performance of the power converter.

[0022] In still another arrangement of the half-bridge power converter described above, the hysteretic controller further includes a summer configured to add the sensed current signals, and a second comparator comparing the sum of the sensed current signals to the droop voltage, and configured to output a switch signal responsive to the comparison.

[0023] In yet another arrangement of the half-bridge power converter described above, first and second primary side driver transistors each include a GaN transistor.

[0024] In another alternative arrangement of the half-bridge power converter described above, the first and second low side driver transistors each include a MOSFET.

[0025] In still another example arrangement, an integrated circuit includes primary side driver transistors for a transformer based power converter, and further includes a hysteretic controller circuit having output signals for driving the gate terminals of primary side driver transistors and secondary side driver transistors to form a step down output voltage converter, the hysteretic controller circuit having an input for receiving a feedback output voltage, and having inputs for receiving signals corresponding to sensed inductor currents; at least one primary side driver transistor having a current conduction path coupled between a terminal for receiving a positive input voltage and a terminal for coupling to the primary side of a transformer and having a gate input coupled to the hysteretic controller; and at least one secondary side driver transistor having a current conduction path coupled between a terminal for coupling to the secondary side of the transformer and a terminal for a ground potential, and having a gate terminal coupled to an output of the hysteretic converter. The hysteretic controller is configured to output on-time pulses to the first primary side driver to control an output voltage using an approximately constant switching frequency.

[0026] In still a further example arrangement, the hysteretic controller (of the integrated circuit described above) is adapted to provide gate signals to control a hard switched half-bridge isolated power converter.

[0027] Use of these arrangements incorporating an transformer based topology for a power converter and using hysteretic control to provide the switching signals for the power converter

enables highly efficient, single stage power converters with low output voltages and high output currents, thus reducing cost, reducing operating temperature and reducing board area, and simultaneously increasing reliability of the systems where these arrangements are used. Use of these arrangements allows elimination of costly intermediate stage converters that were required by conventional solutions for power converters.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] FIG. 1 is a simple block diagram of a distributed power architecture.

[0029] FIG. 2 is a simple schematic of a conventional approach two phase buck converter and controller.

[0030] FIG. 3 is an illustration of a half bridge converter arrangement forming an aspect of example embodiments.

[0031] FIG. 4 is a timing diagram of hysteretic control in the arrangement of FIG. 3.

[0032] FIG. 5 illustrates a simulated timing diagram of the converter arrangement of FIG. 3.

[0033] FIG. 6 is a graph of measured data illustrating the efficiency of an example half bridge converter arrangement with varying output voltages using an aspect of example embodiments.

[0034] FIG. 7 is a graph of measured data illustrating the efficiency of a half bridge converter arrangement with varying input voltages using an aspect of example embodiments.

[0035] FIG. 8 illustrates a prototype device incorporating an aspect of example embodiments.

[0036] FIG. 9 depicts schematics of additional converter topologies that are useful to form additional arrangements of example embodiments.

[0037] FIG. 10 depicts a simplified circuit diagram of a full bridge power converter arrangement incorporating aspects of example embodiments.

[0038] FIG. 11 depicts a simplified block diagram of a hysteretic controller circuit that can be used with example embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0039] Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are not necessarily drawn to scale.

[0040] Improvements in the size and efficiency of power converters are helpful to reduce the size of electronic products and to increase efficiency without adversely increasing the device operating temperatures.

[0041] The term “coupled” may include connections made with intervening elements, and

additional elements and various connections may be used between any elements that are described as “coupled.”

[0042] An aspect of example embodiments provides for hysteretic control of a transformer based power converter that is configured in a manner that is similar in some characteristics to a buck or step down converter topology, but these arrangements further use a transformer to reduce a high input voltage to a low voltage, while also simultaneously multiplying the current based on the turn ratio of the transformer. Using the transformer for voltage reduction reduces the stress and switching inefficiencies in the high side switches which can be implemented as FET transistors. Further, as is described further below, the efficiency of this conversion is about 10% above the efficiency for a conventional single stage buck converter reducing voltages in a similar range. In sharp contrast to conventional approaches for power distribution, the use of the high efficiency, single stage PoL converter in example embodiments results in eliminating the need for intermediate step down voltages, along with eliminating the corresponding cost and board area for the components used to generate and isolate the intermediate voltages. Elimination of these components also increases overall system reliability and reduces weight and size of the system. The transformer based converter arrangements of example embodiments are also useful to form a step up converter, increasing an input voltage to a higher output voltage, and alternative arrangements of example embodiments may be formed with a step up transformer.

[0043] FIG. 3 illustrates an example of a half bridge PoL converter arrangement 300 that forms an aspect of example embodiments. The example converter 300 is “hard switched” because the transistors Q1, Q2 (which are the primary side drivers for two alternating cycles of conversion) may be turned on during the converter operations with a voltage already across them, such as VIN. In FIG. 3, an input section 310 of converter 300 is coupled via transformer section 312 to an output section 314.

[0044] In FIG. 3, hysteretic control is used to supply the switch enable signals (gate signals) for FETs that form the switches Q1, Q2, Q3, and Q4. A hysteretic control section 316 receives voltage feedback from the output section. The hysteretic control section 316 provides for the regulation of the PoL converter through regulating the on and off times for switches Q1, Q2, Q3 and Q4. The hysteretic control section 316 also receives current sense inputs from the inductors L3, L4 in the output section.

[0045] The input section 310 includes an input voltage Vin+ coupled to the drain or source

terminal of a switching transistor Q1 and to the first terminal of capacitor C1. The source or drain terminal of the transistor forming switch Q1 is coupled to node 302. In an example application where the switch Q1 is implemented using an enhancement mode MOSFET transistor of the N-type, the input voltage V_{IN+} would be coupled to the drain, and the node 302 would be coupled to the source, of the MOSFET that forms Q1. Node 302 is also coupled to a first primary side terminal of transformer T1 and to a drain or source terminal of transistor Q2. The second terminal of C1 is coupled to node 304. Node 304 is also coupled to a second terminal on the primary side of transformer T1 and a first terminal of capacitor C2. A reference voltage V_{in-} , which could be a ground reference voltage for a DC input voltage, is connected to the source or drain terminal of transistor Q2 and the second terminal of capacitor C2. The capacitors C1, C2 provide current balancing between the two output inductors in the half-bridge converter topology of FIG. 3. If alternative topologies are chosen, as is further described below, the capacitors C1, C2 may be omitted. For those additional alternative arrangements, current balancing can be performed by the control features of the circuitry. The use of the transformer enables the power converter to be an isolated bridge converter, where the voltages on the primary side of the transformer are electrically isolated from the voltages on the secondary or output side of the transformer. However, in some alternative arrangements, voltage isolation is not provided. Further, the transformer can be used, as described in this example, as a step-down voltage converter. However, in alternative arrangements, the transformer can be used to form a step-up voltage converter, and the illustrative examples described herein are not limiting on the broader aspects of the application.

[0046] The output section 314 in FIG. 3 includes an output terminal for the voltage V_{OUT} which is coupled to a first terminal of output capacitor C_{OUT} and to the first terminals of inductors L3 and L4. The second terminal of inductor L3 is coupled to the transformer T1 secondary side and to a drain (or source) terminal of transistor Q3. The second terminal of L4 is coupled to another terminal on the secondary side of transformer T1 and to the drain (or source) terminal of transistor Q4. The source (or drain) terminals of transistors Q3 and Q4 are connected to low side ground and the second terminal of C_{OUT} is connected to low side ground.

[0047] The hysteretic control section 316 includes a differential amplifier 332 that receives voltage V_{OUT} in a feedback loop and receives or locally generates a reference voltage V_{REF} . The output of amplifier 332, the error between the output voltage and a reference voltage, is

coupled to a first terminal of a comparator 335. This output optionally may pass through a compensator block 337, shown as a dashed component to emphasize that it is optional, which may further amplify or apply a dynamic filter to the output of amplifier block 332. The second terminal of the comparator 335 is coupled to a summing block 333. In some arrangements, to further overcome noise and possible erroneous comparator results due to switching on transients, the comparator 335 can be implemented using a hysteretic comparator, which is a comparator that has a hysteresis threshold that must be overcome to trigger a change at the output, thereby reducing noise and errors. The summing block 333 is coupled to a current input block 334 which gets current sense information for both of the inductors L3, L4 from the output section 314. The comparator 335 output is coupled to a pulse sequencer 336 which is further coupled to a dead time generation block 338. The dead-time generation block is coupled to the control terminal of the four transistor switches Q1, Q2, Q3 and Q4. In the example of FIG. 3, the switches Q1, Q2, Q3, Q4 can be implemented as enhancement mode FET transistors, and the control section 316 outputs gate signals to turn on, or turn off, these transistors. In alternative arrangements, other transistor types can be used. Dead-time generation is used to prevent excess current when a primary-side transistor such as Q1 and a corresponding secondary side transistor, such as Q3, are both active at the same time. The dead time generation block 338 ensures that the switch pulses are spaced in time and that only the primary-side, or corresponding secondary side, transistor is active at a given point in time. In this example arrangement, Q3, coupled to the secondary side of the transformer, acts as a synchronous rectifier corresponding to Q1, and Q4, also coupled to the secondary side of the transformer, acts as the synchronous rectifier corresponding to Q2. Other arrangements are possible to provide the advantages of the example in FIG. 3.

[0048] In the example PoL converter 300 of FIG. 3, in addition to optionally providing galvanic isolation, the transformer T1 provides an efficient voltage step-down and current multiplication needed in a low voltage / high current PoL converter. Examining the converter 300 in FIG. 3, with the current doubler in the output, this PoL converter 300 can be directly compared to the two-phase buck converter topology illustrated in FIG. 2. In both examples the switching transistors Q1 and Q2 are comparable in function, and the secondary side switching transistors Q3 and Q4 are comparable in function. Lastly the output inductors L3 and L4 are treated similarly to the buck inductors in the buck converter of FIG. 2, providing current doubling and voltage halving (as compared to a single inductor output in a conventional

half-bridge converter).

[0049] In FIG. 3, the hysteretic control receives signals corresponding to current sensing in the L3 and L4 inductors through conventional sensing methods, such as using a shunt resistor in each of the L3 and L4 lines, or alternatively by using a resistor-capacitor filter to sense the current using direct current resistance (DCR) methods, or by measuring the $V_{DS(on)}$ of the low side transistors Q3 and Q4. These current sensing methods may use temperature compensated components to compensate for expected temperature dependent effects.

[0050] In operation, a trigger event for the selected one of the primary side drivers Q1, Q2 is determined by the comparison of a droop voltage V_{DROOP} and a signal corresponding to the sum of the currents for inductors L2 and L3. The voltage V_{DROOP} is an amplified, filtered error signal between the output voltage V_{out} and the reference voltage V_{ref} . In operation, when the droop voltage signal exceeds the signal representing the sum of the inductor currents, a semi-fixed duration on-time pulse is sent to the switches Q1, Q2, in an alternating fashion, corresponding to the high side and low side drivers, respectively. When the specified on-time elapses, the on-time ends. The hysteretic controller 338 in FIG. 3 adjusts the on-time duration of the primary side drivers to achieve a desired steady-state frequency by monitoring the input voltage and the output voltage obtained. The converter 300 operates at an approximately fixed frequency in current conduction mode, reducing noise and putting any EMI noise at a known frequency. In this way the fast transient response of the hysteretic controller can be achieved along with acceptable EMI noise, and using controlled switching frequencies at a more or less constant frequency for a particular input voltage and output voltage level.

[0051] FIG. 4 is a simplified timing diagram 400 of operation of the hysteretic control section 316 using the droop voltage signal labeled V_{DROOP} , which is an amplified and filtered voltage signal corresponding to the difference between the reference voltage V_{REF} and the observed output voltage V_{OUT} . For example, the controller uses V_{DROOP} and the current sum signal output by the summer 333 in FIG. 3 labeled I_{SUM} to generate trigger events for on-time pulses for the switches. In FIG. 4, the output voltage is shown as the top trace, labeled V_{CORE} . The voltage V_{DROOP} rises as the output voltage V_{CORE} falls. A voltage corresponding to the sum, or average, of the two inductor currents I_{SUM} is output by the summer 333 in FIG. 3, in FIG. 4 the trace line for I_{SUM} is shown dashed to separate it from V_{DROOP} .

[0052] In operation, when a voltage corresponding to the inductor current sum I_{SUM} crosses the

voltage V_{DROOP} , this is a trigger event and an on-time pulse of a predetermined duration is generated by the pulse sequencer 336 in FIG. 3. This pulse is shown as SW_CLK. This on-time pulse turns on the appropriate primary-side driver (in FIG. 3, either Q1, or alternatively, Q2, in alternating cycles) to apply the input voltage to the transformer primary side. The reflected applied voltage that appears on the secondary side of the transformer will increase the current in one of the output inductors, and will charge the output voltage V_{CORE} . For a multiple cycle converter, the appropriate primary side driver is enabled in sequence. In FIG. 4, the gate signals to the four switches in FIG. 3 are shown, labeled Q1, Q2, Q3, and Q4. The gate signals to the primary side driver switches Q1, Q2 are driven with on-time pulses of a duration that is determined by the controller, while the gate signals to the secondary side driver switches Q3, Q4 are inverted signals with a dead time spacing. For example, the gate signal to Q3 is the inverse of the gate signal to Q1. In the example converter 300 of FIG. 3, only two primary side driver transistors Q1, Q2 are implemented, but (in alternative arrangements) additional primary side drivers can also be supported by adding additional high side and low side transistors and a corresponding inductor in the output section. In an alternative arrangement, additional drivers could be arranged such as a four phase arrangement formed by doubling all the power stages in parallel. These alternative arrangements form additional aspects of example embodiments. The pulse sequencer and dead time controller of FIG. 3 will then be configured to cycle the pulses through the phases in a cyclical fashion, allocating one on-time pulse to the appropriate primary side driver device for each cycle.

[0053] In an example arrangement, the on-time pulse duration is determined by an adaptive on time control mechanism and is proportional to the ratio of the output voltage to the input voltage, so that the switching frequency remains roughly constant regardless of variations of the input and output voltage. For a constant input voltage with a constant target output voltage V_{OUT} , the resulting switching frequency is therefore more or less constant, making EMI noise and converter loss predictable, enabling use of the hysteretic controller to facilitate robust system design.

[0054] The example arrangement of FIG. 3 implements two primary side drivers, which are: one using primary side driver Q1 and inductor L3; and one an additional primary side driver Q2 and inductor L4. The on-time for the secondary side transistors Q3, Q4, which act as synchronous rectifiers, are complementary to the on-time signals corresponding primary-side

driver transistors. The dead time circuitry 338 ensures that the primary-side driver transistors such as Q1, and the corresponding secondary-side transistors, such as Q3, will not be turned on simultaneously, operating in a manner similar to the operation of the dead time circuitry in conventional buck converter controllers. Also, the dead time circuitry 338 also ensures that the primary-side drivers Q1 and Q2 are not turned on simultaneously. The secondary-side transistors Q3, Q4 can and will be on simultaneously at different stages of the circuit operation.

[0055] In one example arrangement, a hysteretic step down controller integrated circuit labeled TPS53632G from Texas Instruments Incorporated is useful to control the switches Q1, Q2, and to output the complementary gate signals to switches Q3 and Q4. However, in an alternative arrangement, the hysteretic controller can be formed as part of a highly integrated circuit including other components such as some or all of the driver transistors Q1-Q4, and a system-on-a-chip approach (SOIC or SOC) can be used. Other arrangements can be formed where the hysteretic controller is implemented using programmable logic (such as CPLDs, FPGAs and ASICs), or using programmable digital devices (such as microcontrollers, DSPs, MCUs and CPUs).

[0056] If an output capacitor with sufficient equivalent series resistance (ESR) is used, the hysteretic controller can operate using the ripple voltage at the output to provide the timing signal for the on-time pulses. However, in some converter implementations capacitors are used with extremely low ESR. In those applications, additional resistance such as a series resistance can be added. In alternative implementations, additional resistor and capacitor networks can be formed around the inductors to add a ripple voltage to the output voltage. Texas Instruments Incorporated provides various hysteretic controllers that use direct access to the output capacitor, referred to as “D-CAP” or “DCAP” which are useful to control the transformer arrangements of example embodiments with some modifications. Additional hysteretic controllers from Texas Instruments Incorporated are useful and are labeled “DCAP+” and “DCAP2” type hysteretic controllers. Internal circuitry in these advanced controllers make the use of low ESR output capacitors with no or few additional external components possible. The internal circuitry can add a ripple to the feedback voltage from the output even for cases where the output capacitance has very low ESR and thus presents minimum ripple at the output. The TPS53632G device described above is an example of a “D-CAP+” type hysteretic controller.

[0057] Various manufacturers offer hysteretic or hysteretic-styled controllers for step-down or

buck converters that can also be used to form additional arrangements of example embodiments to control the half-bridge power converter arrangements. Also, other circuit topologies using transformers are useful to form additional alternative arrangements for a single stage converter to output a low voltage, high current output, such as less than 3.5 volts, from a relatively high supply voltage, such as an AC input of 110-240 volts, or a DC input of greater than 30 volts. These other topologies can also be controlled using an existing hysteretic controller chip, a programmable controller or processor, or by using dedicated circuitry for implementing hysteretic control. For example a full-bridge arrangement can be used instead of the half-bridge arrangement. In a full-bridge arrangement, the input stage of the primary side of the transformer has four symmetrically arranged driver transistors that have complementary control signals, so no additional control circuitry is required. In another alternative arrangement, the current doubler in the output stage can be replaced with a feed-forward arrangement. In this case, only a single inductor may be used instead of the two inductors in the current doubler.

[0058] In an example alternative arrangement, the system 300 can be implemented using a mixed signal integrated circuit that includes the primary side and secondary side switches Q1-Q4, the hysteretic controller 316, and the capacitors C1, C2. The transformer T1 and the output inductors L3, L4, can be implemented external to the integrated circuit. In this way the system 300 can be made smaller and board area can be saved. In an alternative arrangement, the mixed signal integrated circuit may include additional driver devices that are arranged to drive external switches Q1-Q4, which can be large, high power capable components, such as power MOSFETs and GaN transistors.

[0059] In another alternative arrangement, the hysteretic controller 316 can be implemented as a dedicated integrated circuit similar to the TPS53632G but modified for use with example embodiments, such as by removing functions not needed for the selected arrangement. For example, a dedicated 2-phase hysteretic controller could be implemented with fewer transistors than the up to three phase circuitry currently provided in the TPS53632G device, while retaining the hysteretic control features.

[0060] FIG. 5 illustrates a simulated timing diagram 500 of the switches of the example hard-switched half bridge PoL converter from FIG. 3. In graph 500, the vertical axis in graphs 501, 502, 503, and 504, represent increasing voltage values. The vertical axis of graph 505 represents a voltage corresponding to inductor current. The horizontal axis on all the graphs

represents increasing time, with each representing the same time values. The data in graph 501 represents the gate timing of transistors Q1 (solid line) and Q3 (dashed line) as shown in FIG. 3. The data depicted in 502 represents the gate timing of transistors Q2 (solid line) and Q4 (dashed line) shown in FIG. 3. The data depicted in 503 represents the voltage across transistor Q2 (V_{Q2}) shown in FIG. 3. The data depicted in 504 represents the voltage across transistors Q3 (V_{Q3}) and Q4 (V_{Q4}) shown in FIG. 3. The data depicted in 505 represents voltages corresponding to the current through inductors L4 (I_{L4}) and L3 (I_{L3}) shown in FIG. 3.

[0061] In time duration 510, the switch Q1 is turned on as shown by the positive pulse on 501, switch Q3 is complementary to the gate signal for switch Q1, while switches Q2 and Q4 remain off. V_{Q2} rises to V_{IN+} as indicated in 503 during time period 510. On the secondary side, V_{Q3} is at zero and V_{Q4} rises as shown in 504 during time period 510. The current I_{L3} rises in the duration 510 while I_{L4} is falling. Time duration 520 is the duration between on-time pulses during which none of the primary-side switches is on, but both secondary side transistors Q3, Q4, the synchronous rectifiers, are on during time 520. The controller ensures this time is always positive by preventing overlapping on-time pulses to prevent an undesired short between V_{IN+} and V_{IN} . A dead time is inserted between when a primary-side switch, such as Q1, is on and when a corresponding secondary-side switch, such as Q3, is on. This dead-time is used to prevent any primary-side switch and corresponding secondary-side switch from turning on at the same time. The leakage inductance of the transformer T1 will react with the primary side output capacitance and result in a slight oscillation observed in V_{Q2} during the dead time. The inductor currents I_{L4} and I_{L3} are both declining during this period, because no power is being applied to the primary. The following time period 512 shows transistor Q2 being turned on, because another cycle is being performed, and the cycles alternate between Q1 and Q2 supplying energy to the secondary side, and Q4 has a gate signal that is complementary to Q2, with Q1 being off and Q3 being on. V_{Q2} goes to zero as shown in trace 503 during the time period 512. On the secondary side, V_{Q3} increases as shown in 504 during the time period 512. I_{L4} increases during the time that Q2 and Q4 are on. The summing of I_{L4} and I_{L3} at the V_{OUT} node provides power to the load at that point. The controller 316 in FIG. 3 monitors the output voltage compared to a reference voltage and also monitors the sum of the currents through the inductors L3 and L4. The controller varies the duty cycle of the transistor switches to regulate the output voltage, with a longer duty cycle increasing output power and a lower duty cycle lowering the output power, that

is, the on-time for the driver transistors Q1, Q2 is adapted as the output voltage (or input voltage) varies.

[0062] FIG. 6 is a graph illustrating the efficiency of an example arrangement for a hard-switched half bridge PoL converter such as shown in FIG. 3 with varying output voltages, using an aspect of example embodiments. In the efficiency graph 600, the horizontal axis represents increasing current in amps increasing from left to right, and the vertical axis represents increasing converter efficiency moving up. Data curve 610 with circle data points represents the efficiency of the PoL converter with an output voltage of 1.5V, data curve 612 with triangle data points represents the efficiency of the PoL converter with an output voltage of 1.2V, data curve 614 with square data points represents the efficiency of the PoL converter with an output voltage of 1.0V and data curve 616 with diamond data points represents the efficiency of the PoL converter with an output voltage of 0.8V. This data was recorded with a V_{IN+} of about 48V with a switching frequency of about 600KHz. Use of these arrangements with hysteretic control of a half bridge converter using GaN transistors for the switches Q1, Q2, Q3 and Q4 has surprisingly enabled a single stage power converter with an input voltage of 48V, and an output voltage of less than 1.0 V at efficiencies around and greater than 90%, an efficiency that was not available in a single stage power converter using conventional approaches.

[0063] A typical output current range for an example PoL converter of this nature is indicated by 620 and is the range of 10A to 35A. Curve 616 at point 622 indicates that the lowest efficiency is 86% when the output voltage was 0.8V and the best efficiency at point 624 is about 91% when the output voltage is 1.5V.

[0064] FIG. 7 is a data graph illustrating the efficiency of a half bridge PoL converter such as shown in FIG. 3, with varying input voltages, using an aspect of example embodiments. In the efficiency graph 700, the horizontal axis represents increasing current in amps moving from left to right and the vertical axis represents increasing converter efficiency moving up. Data line 710 with diamond data points represents the efficiency of the PoL converter with an input voltage of 36V, data line 712 with square data points represents the efficiency of the PoL converter with an input voltage of 48V and data line 714 with circular data points represents the efficiency of the PoL converter with an input voltage of 60V. This data was recorded with a V_{OUT} of about 1.2V with a switching frequency of about 600 KHz. A typical current range for a PoL converter of

this nature is indicated by the span labeled 720 and is the range of 10A to 35A. Data line 714 indicates that the lowest efficiency at point 722 is 87% found when the input voltage was 60V and the best efficiency at point 724 is about 91% when the input voltage is 36V. Again, the use of example embodiments has surprisingly enabled a single stage converter to operate with high efficiencies while providing a low voltage, high current output from a relatively high input voltage, efficiencies not possible with a single stage converter using conventional approaches.

[0065] FIG. 8 illustrates an example prototype device that forms an aspect of example embodiments. The top side view 801 of the prototype device contains a Gallium Nitride (GaN) half bridge integrated circuit 810 LMG5200 manufactured by and available from Texas Instruments Incorporated which forms the input stage transistors Q1 and Q2 such as shown in section 310 of FIG. 3. The primary side of transformer 812 with a 5:1 turn ratio such as shown in section 312 of FIG. 3 and a pair of output inductors 814 manufactured by Coilcraft is comparable to the inductors L3 and L4 from FIG. 3. The back side of the printed circuit board is depicted in 802 and contains the secondary side of the transformer 812 as shown as transformer T1, corresponding to section 312 of FIG. 3, a pair of 30V GaN transistors 820 used in parallel for secondary switch Q3 as shown in section 314 of FIG. 3 and a pair of 30V GaN transistors 822 used in parallel for secondary switch Q4 as shown in section 314 of FIG. 3.

[0066] This example prototype design of FIG. 8 uses a TPS53632G hysteretic controller manufactured by Texas Instruments Incorporated (not shown) to perform hysteretic control including on-time control to stabilize the switching frequency during steady state or continuous conduction mode conditions. In this particular example, although prototype GaN driver transistors are used, silicon power MOSFETs and other semiconductor transistor types (such as GaAs and SiGe transistors) are also useful. The arrangements herein are not limited to a particular device type for the transistors, and use of alternative types of transistors form additional alternative arrangements that form additional aspects of example embodiments.

[0067] Use of these arrangements enable a single stage power converter to be used as an efficient point of load power supply, without the intervening intermediate stage required by conventional approaches, such as for input voltages greater than 30 volts, and output voltages less than 3.5V, and as low as 1 volt or lower, for a range of output currents, at high efficiencies. Using conventional approaches, these single stage power converters are not available at high efficiencies in such a single stage arrangement. Thus, the use of example embodiments

surprisingly enables elimination of the intermediate power supply converters of conventional systems, while maintaining high efficiencies.

[0068] FIG. 9 depicts circuit schematics 900 and 902 which illustrate portions of additional converter topologies that are useful to form additional arrangements of example embodiments. These input 900 and output 902 stages can be substituted for the input and output stages of the example in FIG. 3, to form a total of four possible transformer based converter topologies. Half-bridge and full-bridge converter topologies have various options for the input stage and output stage depending on the design goals of the power supply that can be used with these arrangements. The portions of circuits shown in FIG. 9 and other input and output stages may be configured around a transformer in such a manner as to create an architecture that appears, in some respects, to be similar to a single or multiphase buck converter and that can therefore be controlled with a hysteretic control mechanism using example embodiments. For example, the full bridge input stage 900 including transistors Q1, Q1A, Q2, Q2A could be substituted for the half bridge input stage 310 of FIG. 3, and the Q1A and Q2A transistor switches can be switched with the same timing of the transistor switches Q1 and Q2 from FIG. 3. Also, the output stage 902 could be substituted for the output stage of the half bridge PoL converter example of FIG. 3, with the Q3 and Q4 transistor switches retaining the timing of the Q3 and Q4 switches described in FIG. 3. Additional arrangements for using hysteretic control with an isolated converter to form a single stage PoL power supply are possible.

[0069] FIG. 10 depicts a particular illustrative example arrangement of a full bridge converter incorporating the hysteretic control of these arrangements to form a single stage power converter.

[0070] In FIG. 10, converter 1000 is shown in a simplified circuit diagram. In converter 1000, an input section 1010, a transformer 1012, and an output section 1014 are arranged to receive an input voltage, couple the input voltage in an isolated bridge topology, and transfer energy to the output section 1014, which in this example is shown as a current doubler such as in FIG. 3.

[0071] The full bridge power converter 1000 in FIG. 10 incorporates the hysteretic controller 1016 which operates as described above. The gate switching signals to the input section 1010 can be applied in a manner similar to the gate switching signals to the input section of the half-bridge topology of FIG. 3. The gate signal to the switch Q1A has the same timing as the gate signal to Q1 and has the same on-time signal. The gate signal to the switch Q2A has the same timing as the Q2 switch. Therefore the full bridge converter 1000 can be arranged using

the same hysteretic control section 1016 as is used in FIG. 3 without the need for additional modification. The full bridge converter 1000 does not have the capacitors C1, C2 used in the half bridge converter 300 in FIG. 3. As a result, the inherent current balancing of the half bridge converter topology of FIG. 3 does not exist in the converter 1000, and active current balancing by the controller will need to be performed. In one example approach, the current balancing can be accomplished by using the techniques disclosed in U.S. Patent No. 7,903,435, issued March 8, 2011, entitled “Current Balancing for Multi-Phase Converters”, to Carpenter et. al., which is hereby incorporated by reference herein in its entirety. By sensing current in each of the inductors in the current doubler, the on-time signals to the switches Q1, Q1A, Q2, Q2A and Q3 and Q4 can be varied to balance current between the cycles.

[0072] FIG. 11 is a simplified block diagram of an example hysteretic controller 1116. For example, this can be implemented as an integrated circuit or as discrete circuitry. Also, portions of 1116 could be integrated together, while other portions remain discrete, as additional possible alternative arrangements. Software and hardware combinations can be used to implement the blocks of FIG. 11. For the blocks of FIG. 11 that are also described as part of FIG. 10, the block numbers are kept the same except that the block numbers now start with “11” instead of “10”. In FIG. 11, a reference voltage is input to a control interface 1145, and a digital to analog converter labeled DAC outputs an analog reference voltage DAC. A differential amplifier receives and filters the output voltage V_{out} , which is compared to the reference voltage signal DAC at an amplifier 1132 and outputs the result as signal VDROOP. The current sense signals ISENSE1 and ISENSE2 are input to a block 1134 and output to summer 1133, which outputs the signal ISUM. The voltage VDROOP and the summed current signal ISUM are compared at comparator 1135 and when a trigger condition exists as described above, a clock signal CLK is output. A phase manager 1136 outputs a clock to the currently active driver circuit in pulse generator 1138, which receives the input voltage VBAT and determines the duration of an on-time signal output as PWM1 for switching transistor Q1, and PWM2 to switching transistor Q2, using the ratio of the output voltage VOUT to the input VBAT, as described above, in response to a trigger event. A frequency select signal FSEL is also used to output the pulses at a constant predetermined frequency.

[0073] Also, aspects of example embodiments can be applied to other converter topologies such as forward converter topologies. A hysteretic controller can be adapted to control a forward

converter to provide a single stage power converter that is highly efficient. Because in this arrangement, only a single switch is used in the input section, only a single phase on-time signal is needed. Also, because only a single inductor exists in the output section for these topologies, no current averaging is needed.

[0074] Various modifications can also be made in the order of steps and in the number of steps to form additional aspects of example embodiments.

[0075] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. Apparatus, comprising:

a power converter for converting an input voltage to an output voltage, the power converter further including:

a transformer having a primary side and a secondary side coupled between an input voltage terminal and an output voltage terminal, respectively;

at least one primary side power switch coupled to supply current from the input voltage terminal to the primary side of the transformer;

at least one inductor coupled between the secondary side of the transformer and the output voltage terminal;

at least one secondary side switch coupled between a node coupled to the inductor and the secondary side of the transformer, and a ground potential; and

a hysteretic controller coupled to supply a first on-time signal to the at least one primary side switch and a second on-time signal to the at least one secondary side switch, the hysteretic controller having a feedback input coupled to the output voltage and configured for sensing the voltage at the output and having at least one current input coupled to the at least one inductor, and further configured for receiving a signal corresponding to the current flowing in the at least one inductor.

2. The apparatus of claim 1, wherein the power converter further includes a half-bridge converter with a current doubler output.

3. The apparatus of claim 2, wherein the power converter further includes:

a second primary side power switch coupled between the primary side of the transformer and a negative voltage input;

a second inductor coupled between the secondary side of the transformer and the output voltage terminal; and

a second secondary side switch coupled between a second node coupled to the second inductor and the secondary side of the transformer, and a terminal for receiving a ground potential;

wherein the hysteretic controller is further configured to supply on-time signals to the second primary side power switch and the second secondary side switch.

4. The apparatus of claim 3, wherein the power converter further includes two alternating cycles and the at least one inductor and second inductor form a current doubler at the output voltage terminal.
5. The apparatus of claim 1, wherein the power converter further includes an amplifier configured to compare the output voltage received to a reference voltage and to output an error signal, the hysteretic controller outputting the on-time signal to the at least one primary side power switch responsive to the error signal.
6. The apparatus of claim 5 wherein the power converter further includes a compensator amplifier which amplifies and filters the error signal, and outputs a droop voltage signal.
7. The apparatus of claim 6, wherein the power converter further includes a pulse sequencer to generate the at least one on-time signal to the at least one primary side driver switch responsive to a comparator that receives a voltage corresponding to summed current in the at least one inductor, and at least one of the error signal and droop voltage signal, and outputs an on-time pulse responsive to a comparison.
8. The apparatus of claim 1, wherein the at least one primary side power switch and the secondary side switch further include field effect transistors (FETs).
9. The apparatus of claim 8, wherein the FET transistors further include silicon MOSFET devices.
10. The apparatus of claim 1, wherein the at least one primary side power switch and the secondary side switch further include GaN devices.
11. The apparatus of claim 1, wherein the power converter further includes a full-bridge converter with a current doubler output.
12. The apparatus of claim 11, wherein the full-bridge converter further includes a second primary side driver switch coupled between the primary side of the transformer and a negative input voltage terminal, a third driver switch coupled between the input voltage terminal and the primary side of the transformer, and a fourth driver switch coupled between the primary side of the transformer and the negative input terminal.
13. The apparatus of claim 12, wherein the first, second, third, and fourth switches further include GaN transistors.
14. A half-bridge transformer-based power converter; comprising:
a transformer having a primary side with a first terminal and a second terminal and a

secondary side with a third terminal and a fourth terminal;

a first primary side driver transistor having a current conduction path coupled between a first voltage input terminal for receiving a positive input voltage and the first terminal of the primary side of the transformer, and having a gate terminal;

a second primary side driver transistor having a current conduction path coupled between a second voltage terminal for receiving a negative input voltage and the first terminal of the primary side of the transformer, and having a gate terminal;

a first secondary side driver transistor having a current conduction path between the first terminal of the secondary side of the transformer and a terminal for a ground potential, and having a gate terminal;

a second secondary side driver transistor having a current conduction path coupled between the second terminal of the secondary side of the transformer and the terminal for a ground potential, and having a gate terminal;

a first inductor coupled between the first terminal of the secondary side of the transformer and an output terminal for an output voltage;

a second inductor coupled between the second terminal of the secondary side of the transformer and the output terminal for an output voltage; and

a hysteretic controller coupled to the output voltage and having inputs for receiving sensed current signals for the first and second inductors, and having outputs for driving gate signals for each of the first and second primary side driver transistors, and for driving gate signals for each of the first and second secondary side transistors, configured to output on-time pulses on the gate terminals of the first and second primary side driver transistors to create an output voltage at the output voltage terminal.

15. The half-bridge power converter of claim 14, wherein the hysteretic controller further includes a first amplifier for comparing the output voltage to a reference voltage and for outputting an error voltage.

16. The half-bridge power converter of claim 15, wherein the hysteretic controller further includes a summer configured to add the sensed current signals and a second comparator comparing the sum of the sensed current signals to the error voltage, and configured to output a switch signal responsive to a comparison.

17. The half-bridge power converter of claim 14, wherein the first and second primary side

driver transistors each include a GaN transistor.

18. The half-bridge power converter of claim 14, wherein the first and second primary side driver transistors each include a MOSFET.

19. A circuit for controlling driver transistors for a transformer based power converter, comprising:

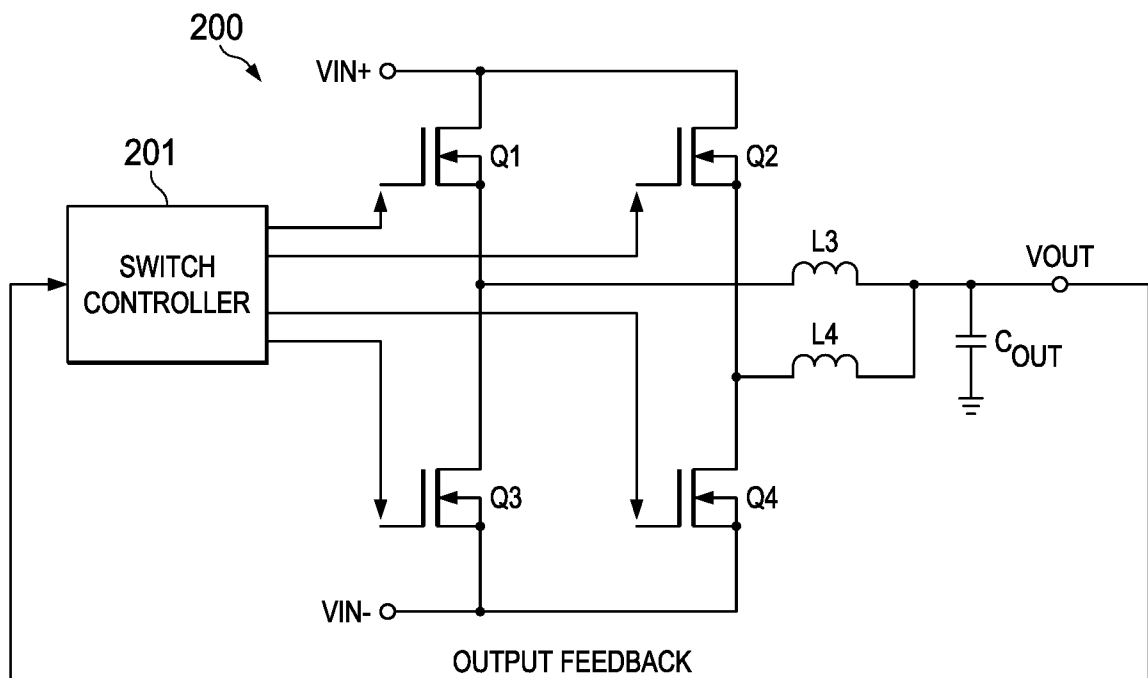
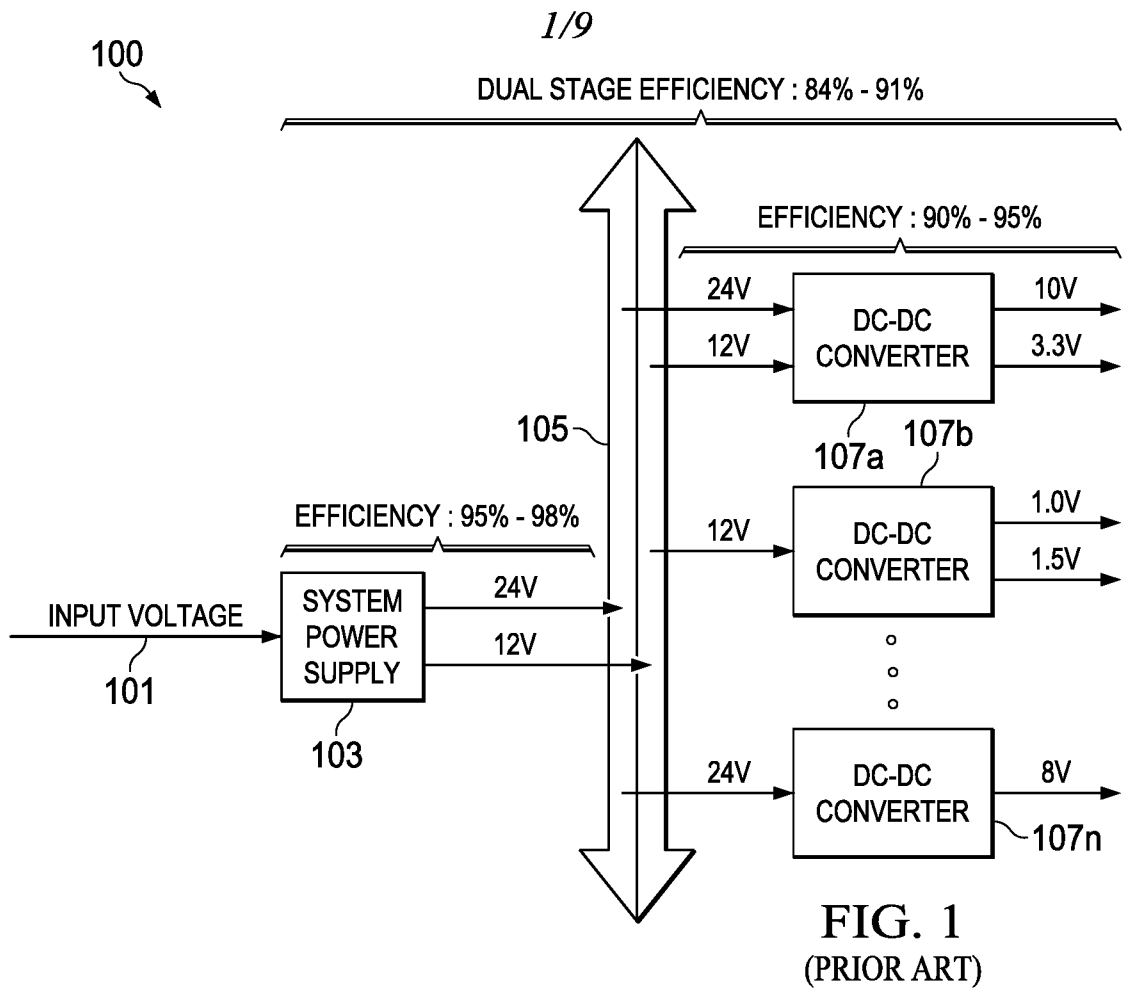
a hysteretic controller integrated circuit having output signals for driving gate terminals of primary side driver transistors and secondary side driver transistors to form a voltage converter, the hysteretic controller circuit having an input for receiving a feedback output voltage, and having inputs for receiving signals corresponding to sensed inductor currents;

the hysteretic controller integrated circuit outputting a first gate signal to at least one primary side driver transistor having a current conduction path coupled between a terminal for receiving a positive input voltage and a terminal for coupling to the primary side of a transformer; and

the hysteretic controller integrated circuit outputting a second gate signal to at least one secondary side driver transistor having a current conduction path coupled between a terminal for coupling to the secondary side of the transformer and a terminal for a ground potential;

wherein the hysteretic controller integrated circuit is configured to output on-time pulses to the at least one primary side driver to control an output voltage using an approximately constant switching frequency.

20. The circuit of claim 19, wherein the hysteretic controller integrated circuit is adapted to provide gate signals to control a half-bridge isolated power converter.



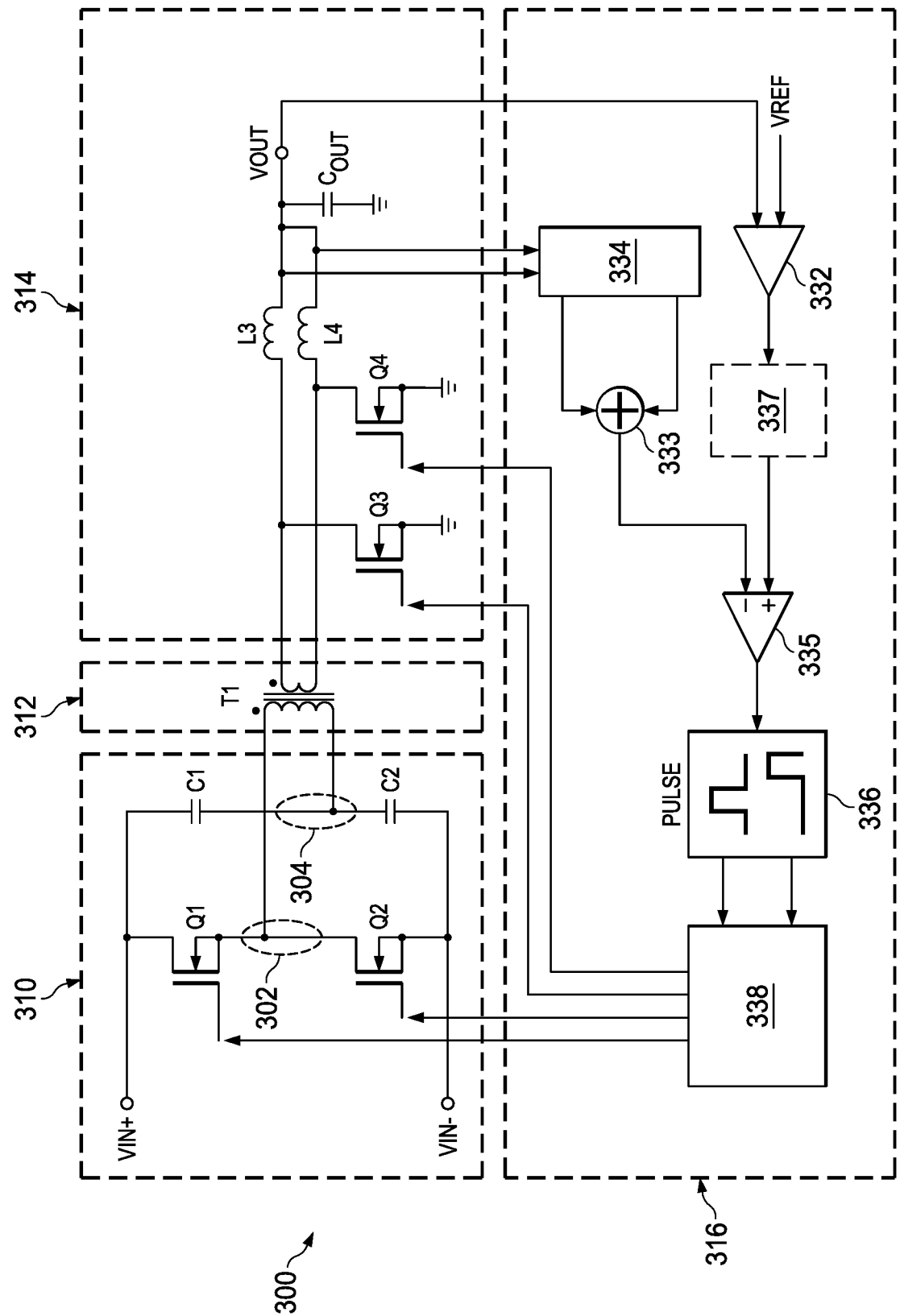


FIG. 3

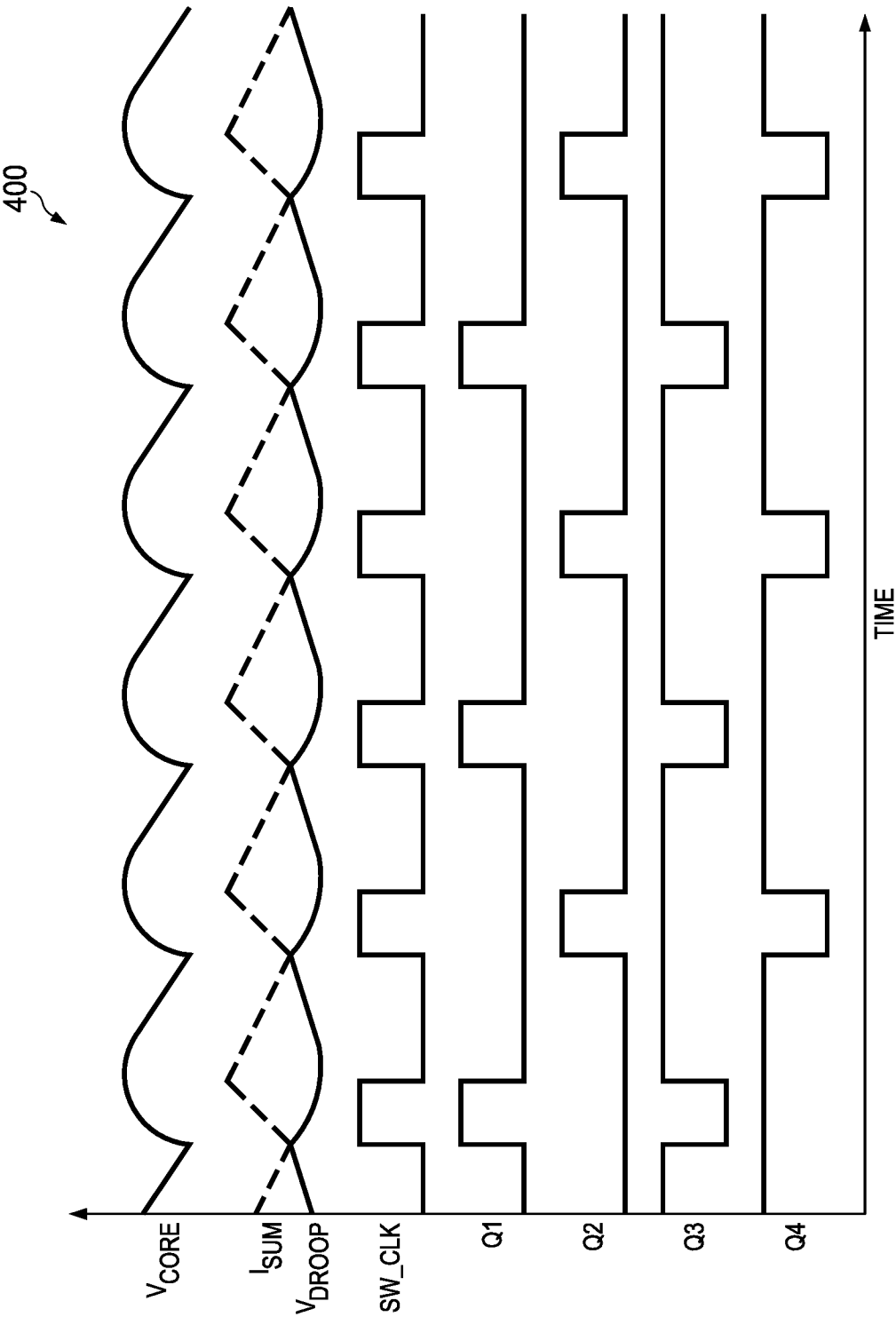


FIG. 4

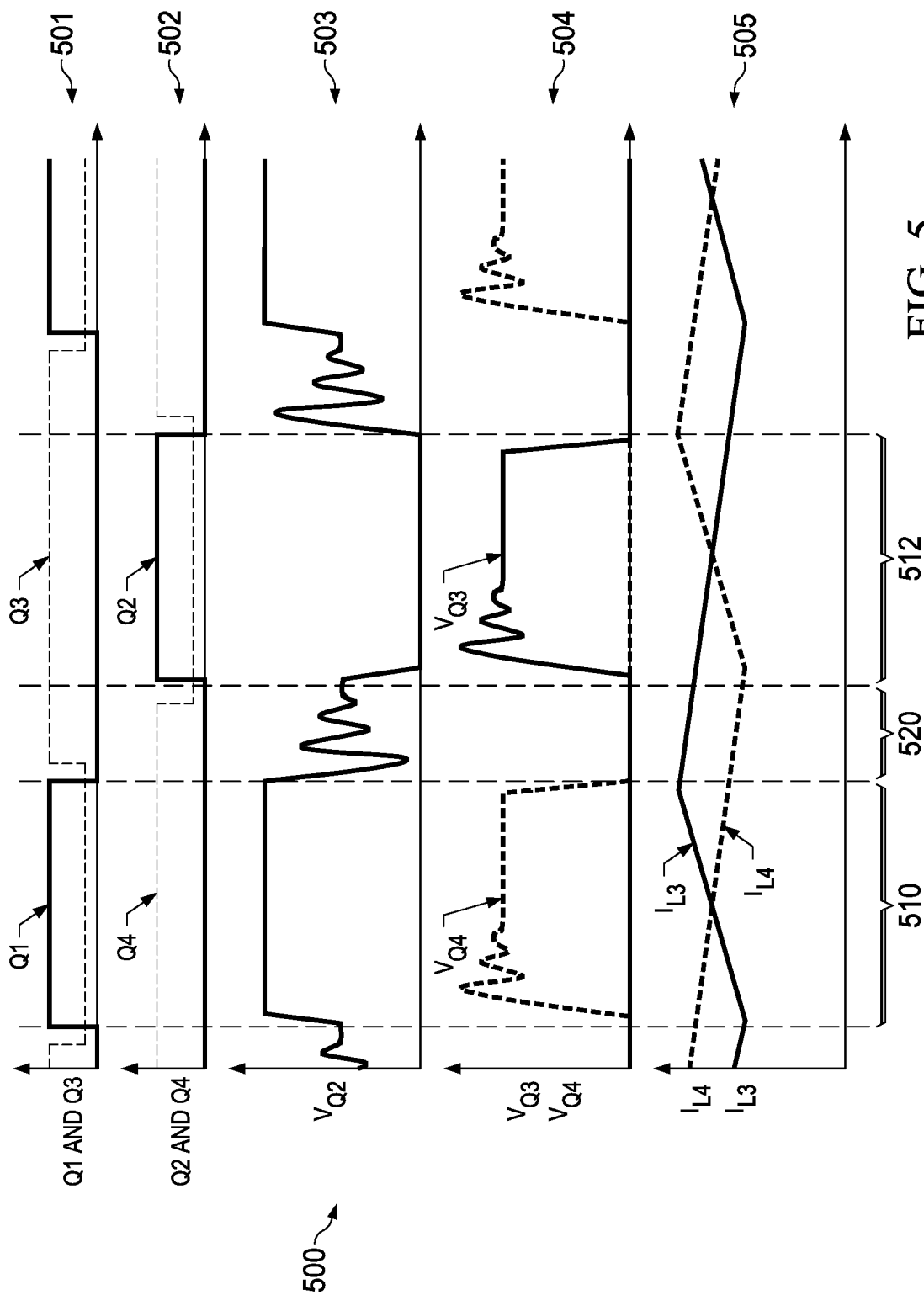


FIG. 5

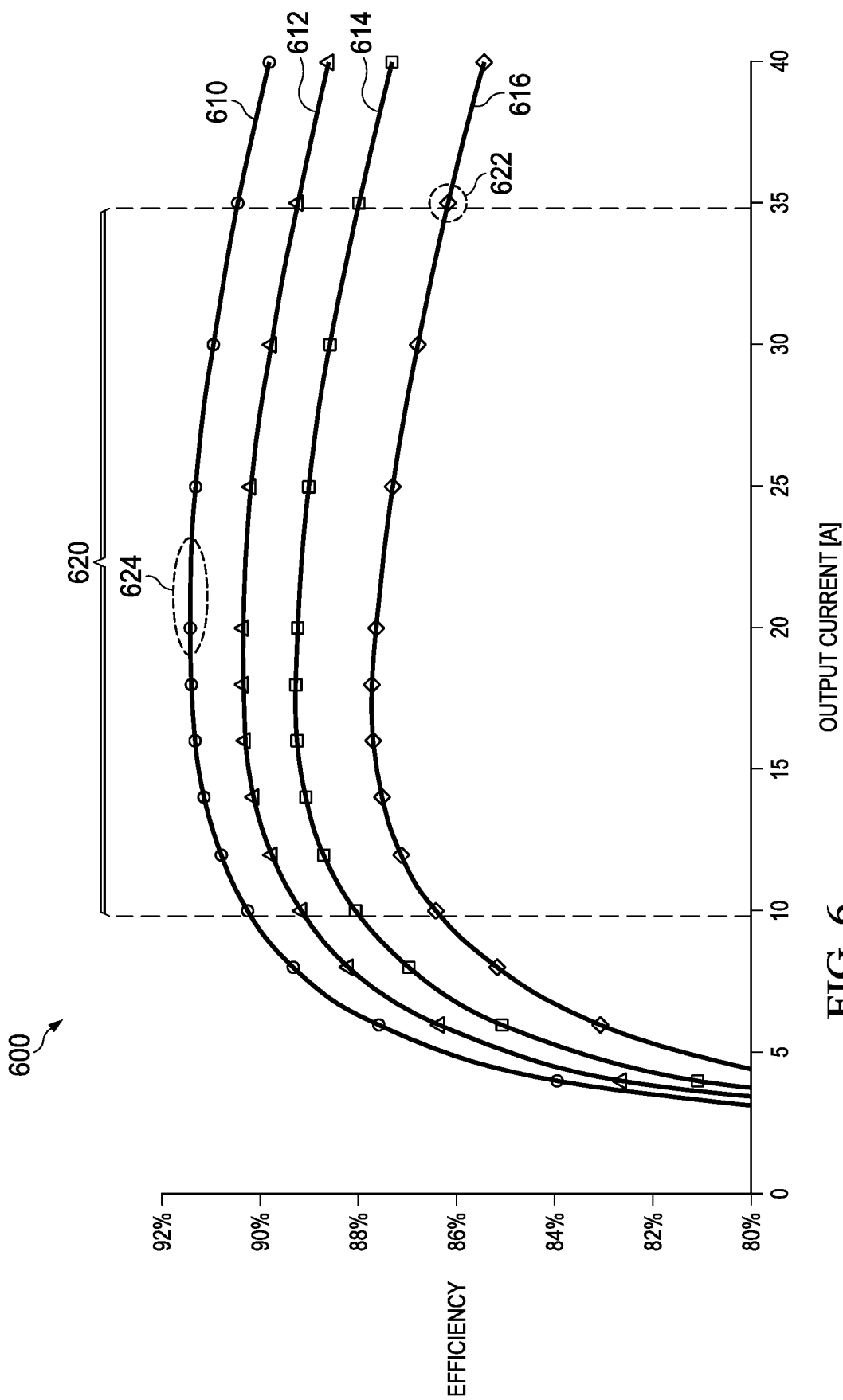


FIG. 6

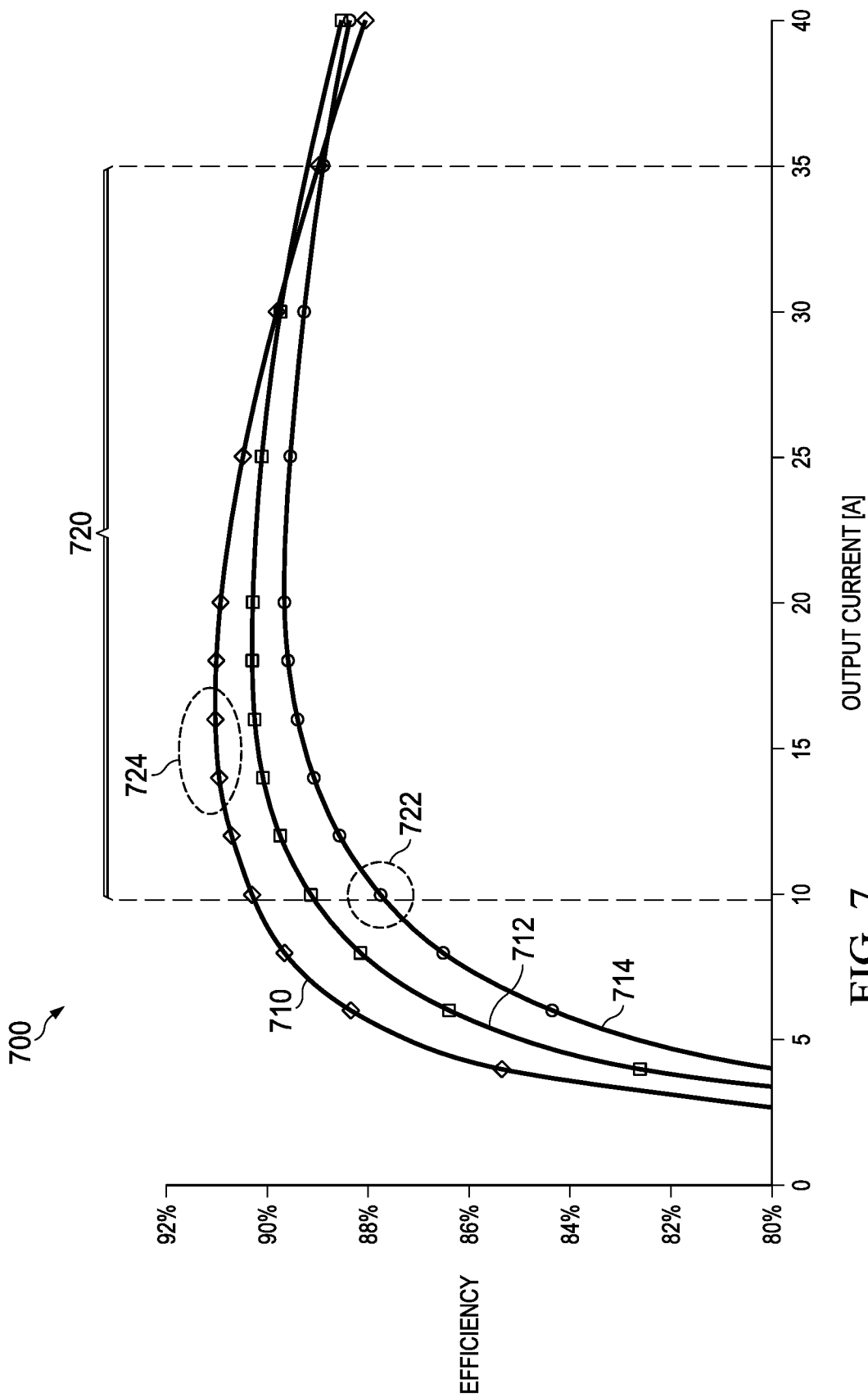


FIG. 7

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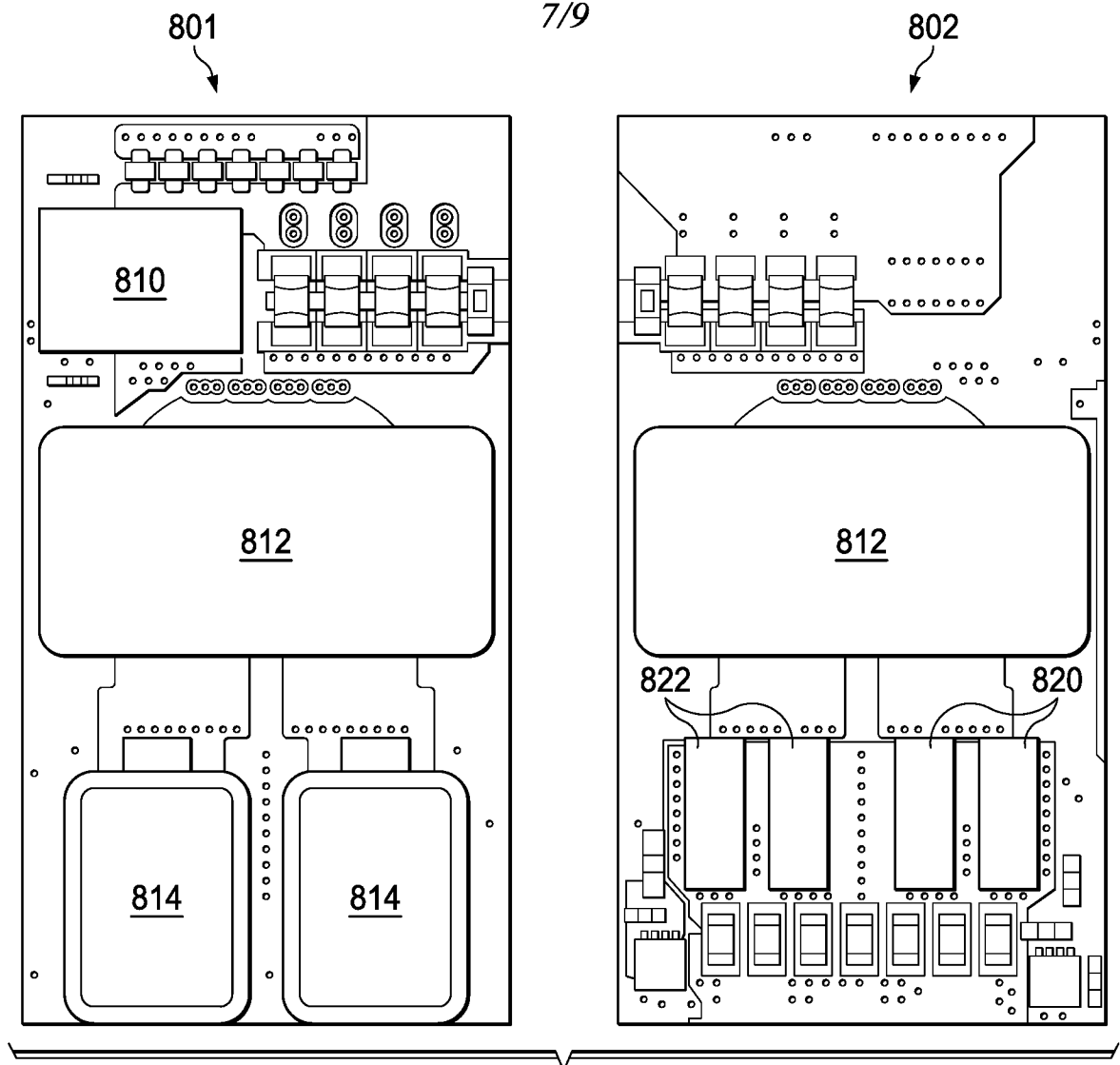


FIG. 8

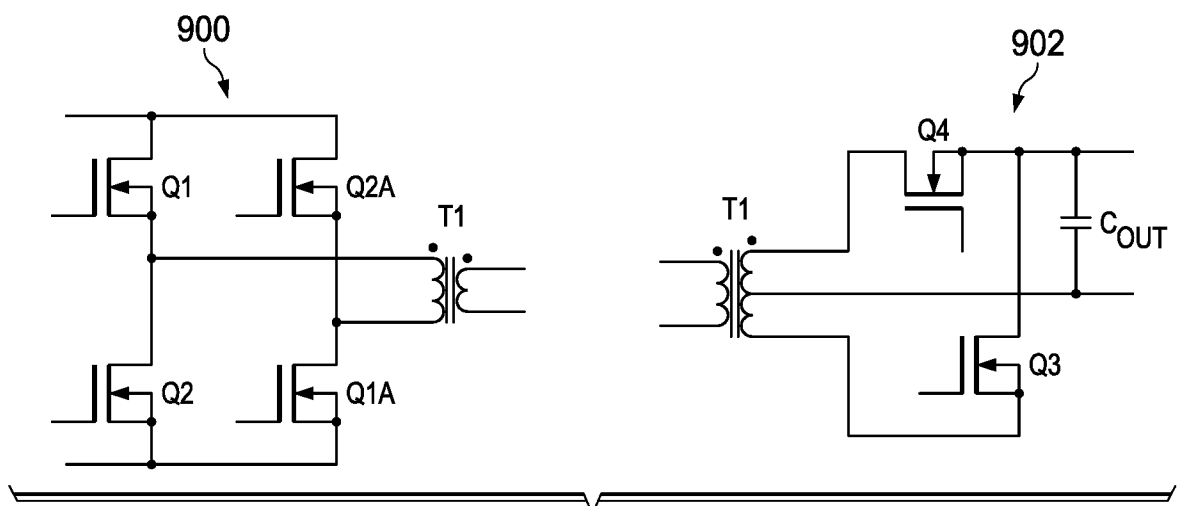


FIG. 9

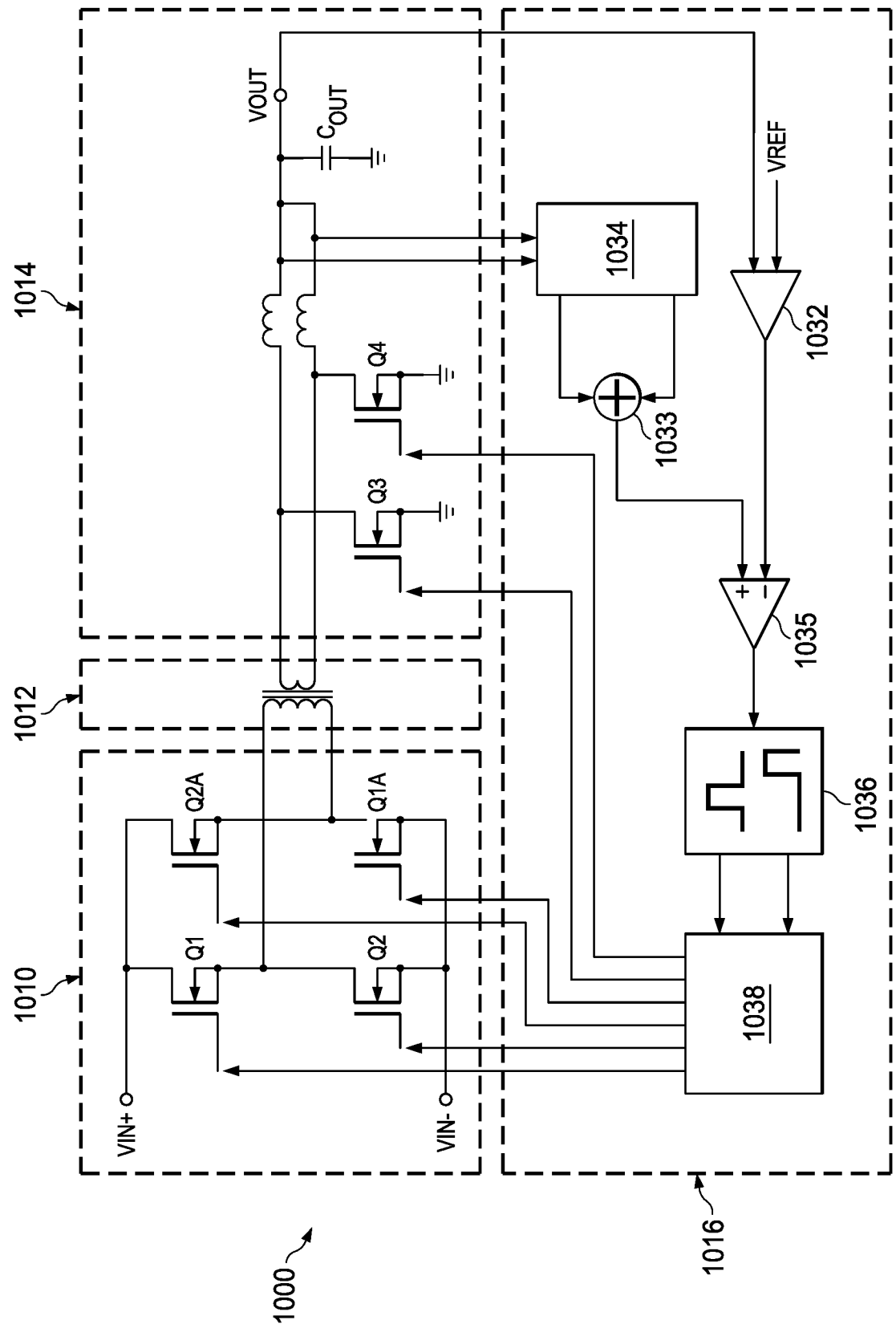


FIG. 10

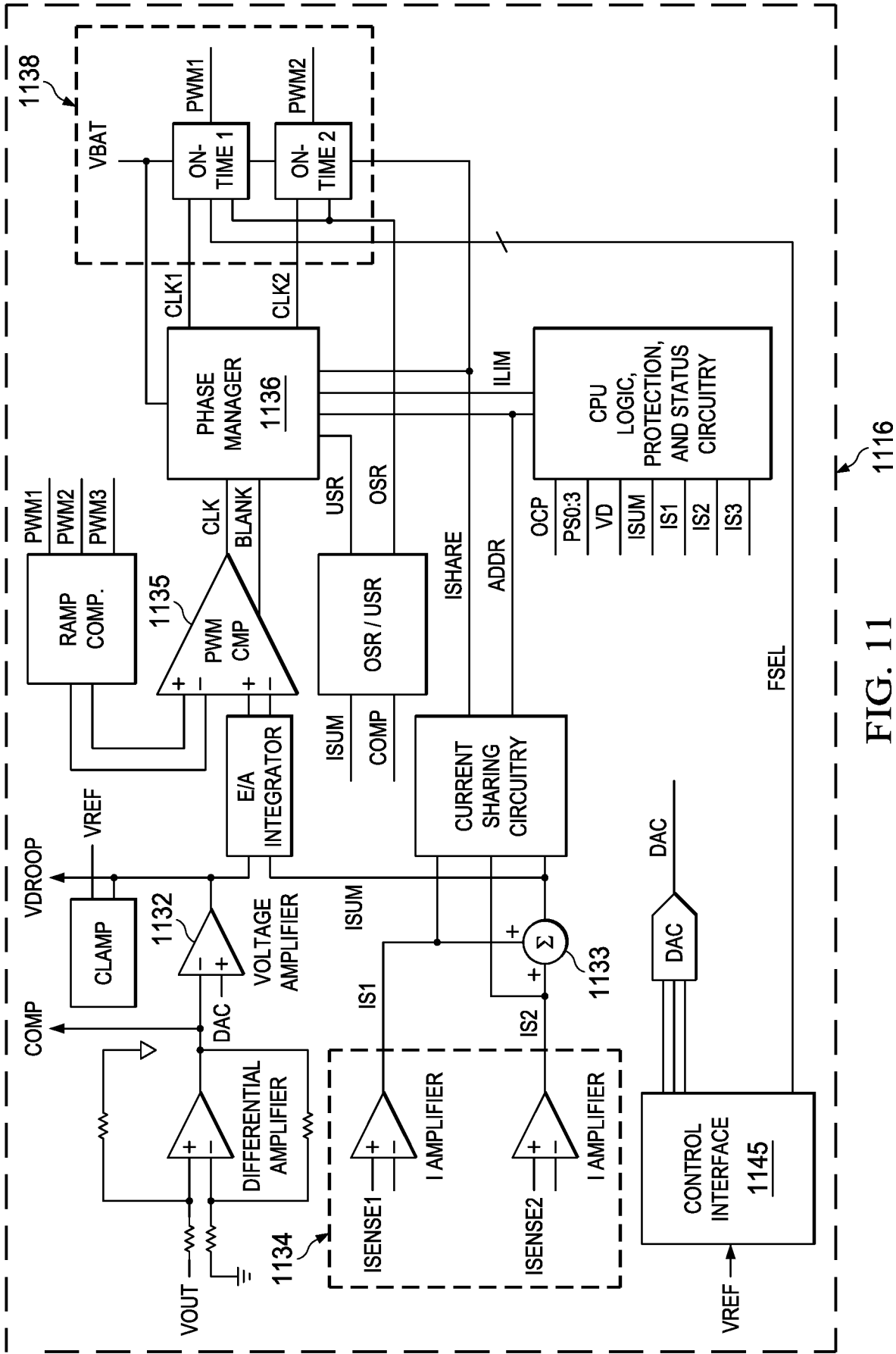


FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/043919

A. CLASSIFICATION OF SUBJECT MATTER		<i>H02M 1/08 (2006.01)</i> <i>H02M 3/325 (2006.01)</i> <i>H02M 3/337 (2006.01)</i> <i>H05K 1/00 (2006.01)</i>
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H02M 1/08, 3/22-3/227, H05K 1/00		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7800921 B2 (CONTINENTAL AUTOMOTIVE US, INC.) 21.09.2010	1-20
A	US 2006/0181906 A1 (UNIVERSITY OF CENTRAL FLORIDA RESEARCH FOUNDATION) 17.08.2006	1-20
A	US 7196914 B2 (VIRGINIA TECH INTELLECTUAL PROPERTIES, INC) 27.03.2007	1-20
A	EP 2388902 A1 (C.R.F. SOCIETA CONSORTILE PER AZIONI) 23.11.2011	1-20
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☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.		
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Date of the actual completion of the international search		Date of mailing of the international search report
28 October 2016 (28.10.2016)		17 November 2016 (17.11.2016)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37		Authorized officer A. Golovchenko Telephone No. 8-499-240-25-91