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(54) Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

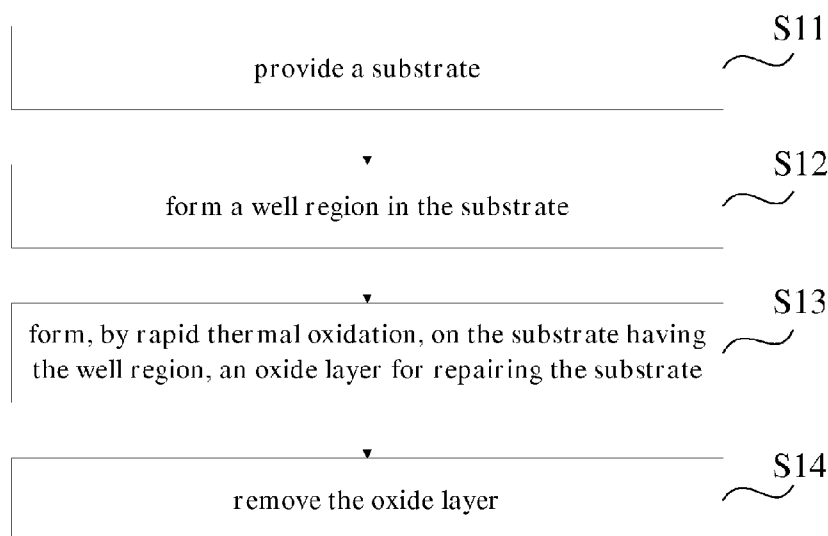


FIG. 1

(57) Abstract: A method is disclosed for manufacturing a semiconductor device. The method includes providing a substrate and forming a well region in the substrate by an ion implantation. The method also includes forming, by rapid thermal oxidation and on the substrate having the well region, an oxide layer for repairing the substrate damaged by the ion implantation. Further, the method includes removing the oxide layer and forming a gate oxide layer on the repaired substrate having the well region.

Description

Title of Invention: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

[1] FIELD OF THE INVENTION

[2] The present invention generally relates to the field of semiconductor manufacturing and, more particularly, to semiconductor devices and methods and processes for manufacturing the same .

[3] BACKGROUND

[4] With continuous progresses in Integrated Circuit (IC) manufacturing techniques and tools, the level of integration of ICs has become increasingly higher, which requires further scaling down on the sizes of the semiconductor devices. The decrease in their sizes often leads to the occurrence of the short-channel effect. The short-channel effect is an effect whereby a device with a reduced channel length has an increased possibility of punchthrough of its source and drain, causing undesired leakage current.

[5] In order to avoid the short-channel effect, a Super-Steep Retrograde Channel (SSRC) is formed by well region implantation. The process of forming the SSRC generally includes forming a P-well by implanting indium ions, and forming an N-well by implanting arsenic ions. Indium ions are relatively heavy, and the silicon substrate may be damaged by the implanted indium ions during the formation of the P-well. The damaged silicon substrate may further affect the subsequent gate oxide layer, i.e., causing weak spots on the gate oxide layer. The weak spots may accelerate the breakdown of the gate oxide layer and, therefore, reduce the reliability of the gate oxide layer.

[6] In order to improve the reliability of the gate oxide layer, some companies use an implantation dose of less than $1 \times 10^{13} \text{cm}^{-2}$ indium ions to prevent the silicon substrate from being damaged by a massive dose of indium ions. However, when the size of the semiconductor device continues to shrink, the implantation dose of indium ions has to be continuously increased to meet other performance requirements of the semiconductor device.

[7] The disclosed methods and systems are directed to solve one or more problems set forth above and other problems.

[8] BRIEF SUMMARY OF THE DISCLOSURE

[9] One aspect of the present disclosure includes a method for manufacturing a semiconductor device. The method includes providing a substrate and forming a well region in the substrate by an ion implantation. The method also includes forming, by rapid thermal oxidation and on the substrate having the well region, an oxide layer for

repairing the substrate damaged by the ion implantation. Further, the method includes removing the oxide layer and forming a gate oxide layer on the repaired substrate having the well region.

[10] Another aspect of the present disclosure includes a semiconductor device. The semiconductor device includes a substrate and a well region in the substrate formed by an ion implantation. The semiconductor device also includes a gate oxide layer on the substrate. The gate oxide layer is formed by forming, by rapid thermal oxidation and on the substrate having the well region, an oxide layer for repairing the substrate damaged by the ion implantation, removing the oxide layer, and forming a gate oxide layer on the repaired substrate having the well region.

[11] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

[12] BRIEF DESCRIPTION OF THE DRAWINGS

[13] Figure 1 illustrates an exemplary flow chart of a method for manufacturing a semiconductor device consistent with the disclosed embodiments;

[14] Figure 2 illustrates an exemplary flow chart another method for manufacturing a semiconductor device consistent with the disclosed embodiments; and

[15] Figure 3 to Figure 9 are cross-section views of a semiconductor device during a manufacturing process consistent with the disclosed embodiments.

[16] DETAILED DESCRIPTION

[17] Reference will now be made in detail to exemplary embodiments of the invention, which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[18] Figure 1 illustrates an exemplary flow chart of a method for manufacturing a semiconductor device consistent with the disclosed embodiments. As shown in Figure 1, at the beginning, a substrate is provided (S11).

[19] The substrate may include any appropriate material for making double-gate structures. For example, the substrate may include a semiconductor structure, e.g., silicon, silicon germanium (SiGe) with a monocrystalline, polycrystalline, or amorphous structure. The substrate may also include a hybrid semiconductor structure, e.g., carborundum, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide or gallium antimonide, alloy semiconductor, or a combination thereof. Further, the substrate may include a silicon-on-insulator (SOI) structure. In addition, the substrate may also include other materials, such as a multi-layered structure of epitaxial layer or buried layer. In certain embodiments, the substrate may be a silicon substrate, which may also be referred to as a silicon base.

[20] After the substrate is provided (S11), a well region is formed in the substrate (S12). It

should be noted that '*in* the substrate' and '*on* the substrate' refer to two different concepts. Specifically, the term '*in* the substrate' refers to an area ranging from the surface of the substrate to a certain depth, and the area is part of the substrate. On the other hand, the term '*on* the substrate' refers to an area above the surface of the substrate, which is not part of the substrate itself.

- [21] The well region in the substrate may be formed by various processes. For example, the processes for forming the well region in the substrate may include: forming a photoresist layer with a well region pattern on the substrate; forming a well region in the substrate by ion implantation using the photoresist layer with the well region pattern as a mask; and removing the photoresist layer with the well region pattern.
- [22] In general, an N-well may be formed by implanting pentavalent ions, such as phosphorus and arsenic ions; and a P-well may be formed by implanting trivalent ions, such as boron and indium ions. If the implanted ions are relatively heavy (e.g., indium ions), the relatively heavy ions may cause damages to the substrate. In the conventional process, after the well region is formed, rapid thermal annealing (RTA) or similar process is performed. The rapid thermal annealing can activate the implanted ions, but cannot repair the damaged surface of the silicon substrate.
- [23] As shown in Figure 1, after the well region is formed (S12), an oxide layer for repairing the substrate is formed by rapid thermal oxidation on the substrate having the well region (S13). That is, after the well region is formed in the substrate, instead of the conventional rapid thermal annealing, a rapid thermal oxidation process is performed to form an oxide layer on the substrate having the well region for repairing the substrate. The oxide layer may be formed by oxidizing the silicon substrate that is damaged during ion implantation. In certain embodiments, the oxide layer may be silicon oxide, and may have a thickness of about 100Å.
- [24] Further, the oxide layer is removed (S14). That is, the oxide layer formed in S13 is washed away, which means that the damaged portion of the silicon substrate is removed and the undamaged portion of the substrate remain. In other words, the damaged substrate is repaired. Therefore, when the subsequent gate oxide layer is formed, it is no longer affected by the damaged substrate, and the reliability of the subsequent gate oxide layer can be improved.
- [25] Figure 2 shows a flow chart of another method for manufacturing a semiconductor device with more details. As shown in Figure 2, at the beginning, a substrate is provided (S21).
- [26] The provided substrate may include a body layer and an epitaxial layer. The body layer may be N-type monocrystalline silicon; and the epitaxial layer may be lightly-doped monocrystalline silicon grown on the N-type monocrystalline silicon. The epitaxial layer may have a crystal structure same as the body layer, with a higher purity

and less crystallographic defects than the body layer. In certain other embodiments, the body layer may be germanium, indium phosphide, gallium arsenide or other semiconductor materials.

- [27] Although the substrate may include a body layer and an epitaxial layer, the body layer and the epitaxial layer are both referred as the substrate for the various manufacturing processes.
- [28] After the substrate is provided (S21), a blocking oxide layer is formed on the substrate (S22). Figure 3 shows a corresponding semiconductor device after forming the blocking oxide layer.
- [29] As shown in Figure 3, a blocking oxide layer 2 is formed on the substrate 1 by thermal oxidation. The blocking oxide layer 2 may be silicon oxide, and may have a thickness of about 150Å. Because the blocking oxide layer 2 is to serve as a blocking layer in the well region implantation, the thickness of the blocking oxide layer 2 may be relatively small.
- [30] Further, a photoresist layer with a well region pattern is formed on the substrate having the blocking oxide layer (S23). Figure 4 shows the corresponding semiconductor device after forming the photoresist layer.
- [31] As shown in Figure 4, at first, photoresist is spin-coated on the substrate 1 having the blocking oxide layer 2. Then, the photoresist is exposed by using a corresponding mask plate. Further, after the exposure and developing, a photoresist layer 3 with the well region pattern is formed on the substrate 1 having the blocking oxide layer 2.
- [32] After forming the photoresist layer 3 (S23), a well region is formed in the substrate using the photoresist layer with the well region pattern as a mask (S24). Figure 5 shows the corresponding semiconductor device after forming the well region.
- [33] As shown in Figure 5, well region 4 is formed in the substrate 1 by ion implantation using the photoresist layer 3 with the well region pattern as a mask. The well region 4 formed in the substrate may be a P-well, and the implanted ions may be indium ions. Other type of well region and/or implantation ions may also be used. Further, the dose of the implanted indium ions may be approximately $1 \times 10^{13} \text{cm}^{-2}$. Other doses higher than $1 \times 10^{13} \text{cm}^{-2}$ may also be used.
- [34] Further, the photoresist layer with the well region pattern is removed (S25). Figure 6 shows the substrate 1 with well region 4 and blocking oxide layer 2 and without the photoresist layer 3. The blocking oxide layer is also removed (S26). Figure 7 shows the substrate 1 with well region 4 and without blocking oxide layer 2.
- [35] After removing the blocking oxide layer 2 (S26), an oxide layer for repairing the substrate is formed by rapid thermal oxidation on the substrate having the well region (S27). Figure 8 shows the corresponding semiconductor device after forming the oxide layer (i.e., the repairing oxide layer).

- [36] As shown in Figure 8, an oxide layer 5 for repairing the substrate is formed on the substrate 1 having the well region 4. The oxide layer 5 may be formed by rapid thermal oxidation. That is, the oxide layer 5 may be formed by oxidizing the damaged substrate in an oxygen environment. The thickness of the formed oxide layer 5 may be controlled by controlling the time of the rapid thermal oxidation process. In certain embodiments, the thickness of the formed oxide layer 5 may be approximately 100Å, and the oxide layer 5 may be silicon oxide.
- [37] Further, the oxide layer 5 for repairing the substrate is removed (S28). That is, after the substrate 1 is repaired, the repairing oxide layer 5 is removed. The corresponding semiconductor device after removing the oxide layer 5 is similar to that shown in Figure 7 and is omitted.
- [38] After removing the oxide layer formed by rapid thermal oxidation (S28), a gate oxide layer is formed on the substrate having the well region (S29). Figure 9 shows the corresponding semiconductor device after forming the gate oxide layer.
- [39] As shown in Figure 9, a gate oxide layer 6 is formed on the substrate 1 having the well region 4 by thermal oxidation. The gate oxide layer 6 may act as a dielectric between the gate and the source/drain of the semiconductor device. The thickness of the gate oxide layer 6 may be controlled by controlling the time of the thermal oxidation process, and the thickness of the gate oxide layer 6 may range from about 20Å to hundreds of Å. In certain embodiments, the thickness of the gate oxide layer 6 may be 200Å, and the gate oxide layer 6 may be silicon oxide.
- [40] After the gate oxide layer 6 is formed on the substrate 1 having the well region 4, performance tests can be performed on the gate oxide layer 6. Based on testing results, the probability of breakdown of the gate oxide layer is considerably reduced after the repairing process; hence the reliability of the gate oxide layer is significantly improved.
- [41] By using the disclosed methods and processes, the reliability of the gate oxide layer can improve without reducing the implantation dose of ions. More specifically, by using the disclosed methods and processes, the gate oxide layer is formed on the repaired substrate, thereby avoiding the occurrence of weak spots on the gate oxide layer, and significantly improving the reliability of the gate oxide layer.
- [42] It is understood that the disclosed embodiments may be applied to any semiconductor devices. Various alternations, modifications, or equivalents to the technical solutions of the disclosed embodiments can be obvious to those skilled in the art.

Claims

- [Claim 1] A method for manufacturing a semiconductor device , comprising:
providing a substrate;
forming a well region in the substrate by an ion implantation;
forming, by rapid thermal oxidation, on the substrate having the well region, an oxide layer for repairing the substrate damaged by the ion implantation;
removing the oxide layer; and
forming a gate oxide layer on the repaired substrate having the well region.
- [Claim 2] The method according to claim 1, wherein the oxide layer for repairing the substrate has a thickness of approximately 100Å.
- [Claim 3] The method according to claim 1, wherein the well region formed in the substrate is a P-well.
- [Claim 4] The method according to claim 1, wherein the well region formed in the substrate is a P-well doped with indium ions.
- [Claim 5] The method according to claim 1, further including:
before forming the well region in the substrate, forming a blocking oxide layer on the substrate; and
after forming a well region in the substrate, removing the blocking oxide layer.
- [Claim 6] The method according to claim 1, wherein forming the well region in the substrate includes:
forming a photoresist layer with a well region pattern on the substrate;
forming the well region in the substrate using the photoresist layer with the well region pattern as a mask; and
removing the photoresist layer with the well region pattern.
- [Claim 7] The method according to claim 1, wherein the oxide layer for repairing the substrate is silicon oxide.
- [Claim 8] A semiconductor device, comprising:
a substrate;
a well region in the substrate formed by an ion implantation; and
a gate oxide layer on the substrate, wherein the gate oxide layer is formed by:
forming, by rapid thermal oxidation, on the substrate having the well region, an oxide layer for repairing the substrate damaged by the ion implantation;

removing the oxide layer; and
forming a gate oxide layer on the repaired substrate having the well region.

[Claim 9] The semiconductor device according to claim 8, wherein the oxide layer for repairing the substrate is formed by rapid thermal oxidation.

[Claim 10] The semiconductor device according to claim 8, wherein the well region in the substrate is a P-well doped with indium ions.

[Claim 11] The semiconductor device according to claim 8, wherein the oxide layer for repairing the substrate has a thickness of approximately 100Å.

[Claim 12] The semiconductor device according to claim 8, wherein the well region in the substrate is formed by:
forming a photoresist layer with a well region pattern on the substrate;
forming the well region in the substrate using the photoresist layer with the well region pattern as a mask; and
removing the photoresist layer with the well region pattern.

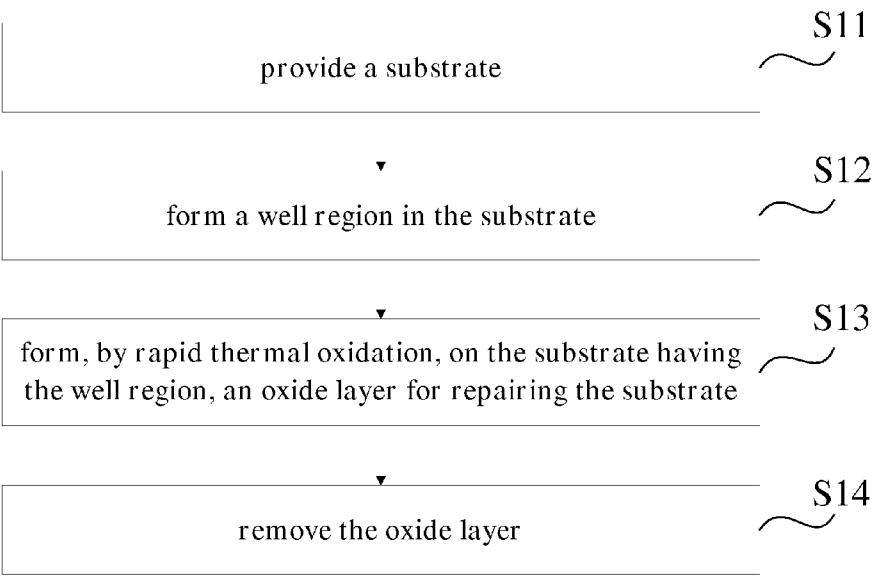


FIG. 1

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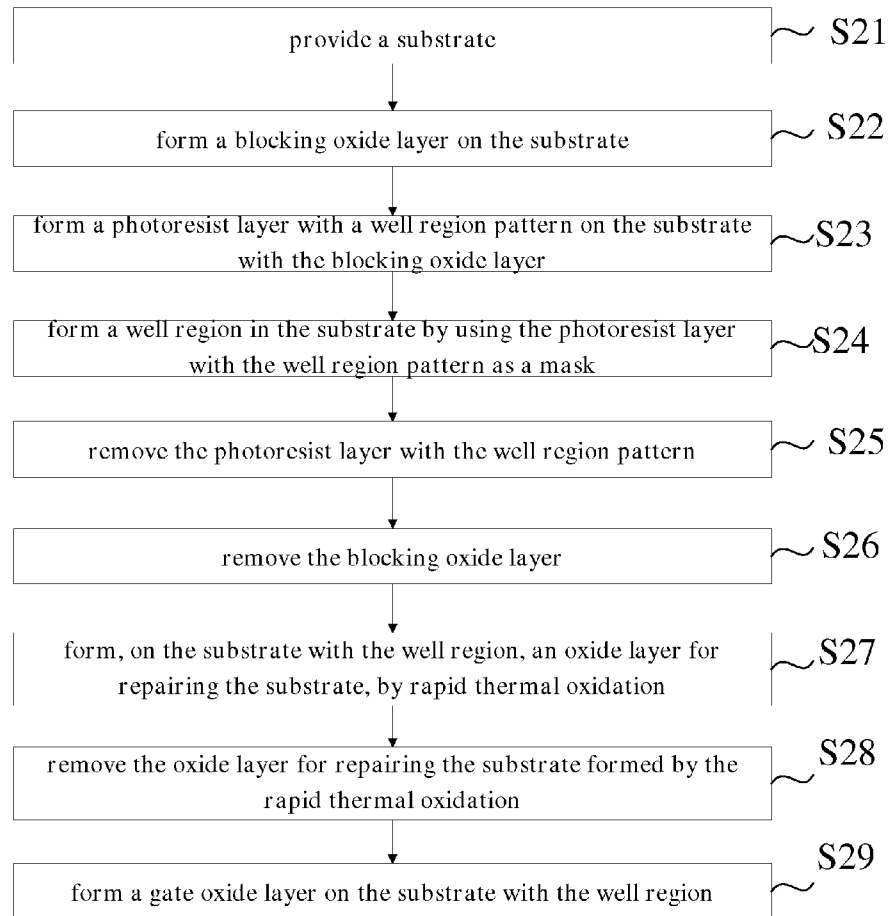


FIG. 2

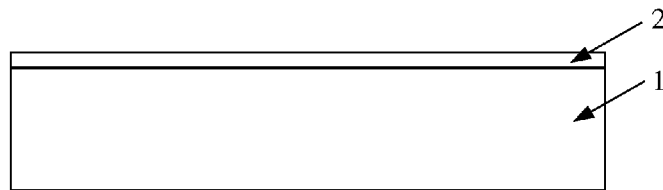


FIG. 3

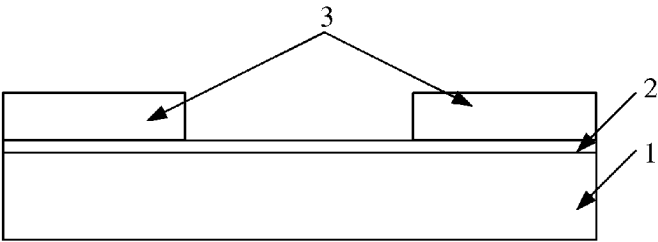


FIG. 4

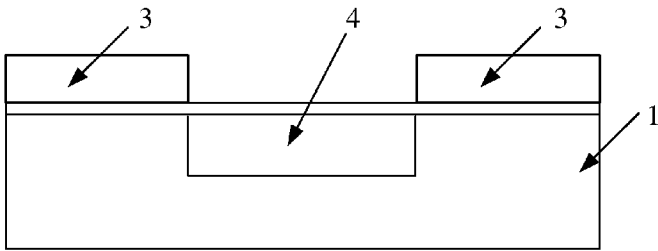


FIG. 5

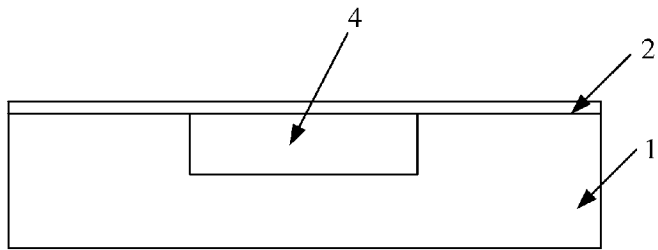


FIG. 6

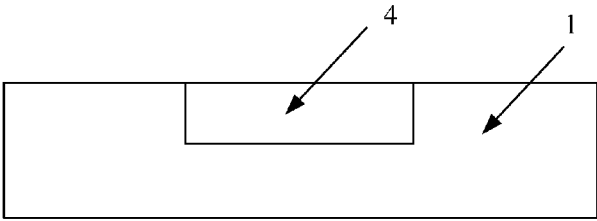


FIG. 7

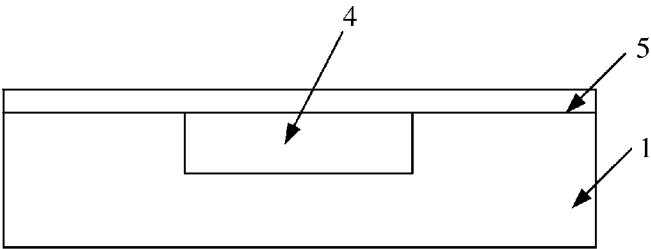


FIG. 8

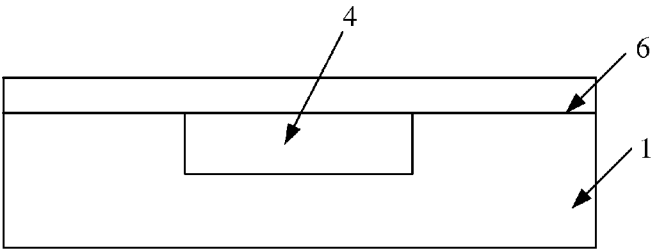


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/082400

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/02 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, EPODOC, WPI: substrate, damag+, well?, oxide, ion?, implant+, remov+, etch+, gate, insulat+, dielectric, form+, deposit+, grow+, breakdown, reliability

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US2004/0033658A1 (SAMSUNG ELECTRONICS CO.,LTD.) 19 Feb. 2004(19.02.2004) see specification: paragraphs [0015]-[0019], Figs.2A-2D	1-12
Y	US5231038A (MITSUBISHI DENKI KABUSHIKI KAISHA) 27 Jul. 1993(27.07.1993) see specification: column 7, line 59-column 8, line 64, FIGS.1A-1H	1-12
Y	JP2000-150880A (TOSHIBA KK) 30 May 2000(30.05.2000) see paragraphs [0014]-[0016], figs.1(a)-1(c)	1-12
A	US6080682A (ADVANCED MICRO DEVICES, INC.) 27 Jun. 2000(27.06.2000) see the whole document	1-12

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:	“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
“A” document defining the general state of the art which is not considered to be of particular relevance	“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
“E” earlier application or patent but published on or after the international filing date	“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
“L” document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)	“&” document member of the same patent family
“O” document referring to an oral disclosure, use, exhibition or other means	
“P” document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 09 Feb. 2012(09.02.2012)	Date of mailing of the international search report 01 Mar. 2012 (01.03.2012)
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer YANGZifang Telephone No. (86-10)62411806

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2011/082400

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
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JP2000-150880A	30.05.2000	NONE	
US6080682A	27.06.2000	NONE	